MOTOROLA

MC75365

Specifications and Applications Information

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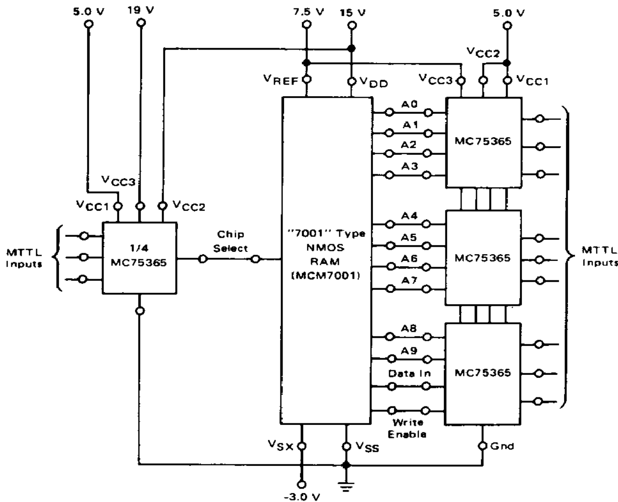
QUAD MOS CLOCK DRIVER OR HIGH-VOLTAGE, HIGH-CURRENT NAND DRIVER

The MC75365 is intended for driving the highly capacitive Address, Control and Timing inputs on a variety of MOS RAMs such as the "1103" and "7001" types. It is designed to operate from the MTTL 5.0 V power supply and the V_{SS} and V_{BB} power supplies used with the memories in most applications. Operation is recommended at $V_{CC3} \simeq V_{CC2} + 3$ V, but the part is useable over a wide latitude of supply voltages. V_{CC2} may be tied directly to V_{CC3} in many conditions.

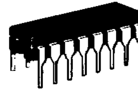
- Pin Compatible with Intel 3207 and Interchangeable with T. I. SN75365
- MTTL and MDTL Compatible, Diode-Clamped Inputs
- Two Common Enable Inputs per Gate Pair
- Low Standby Power Consumption Transient
- Capable of Driving High Capacitive Loads
- Fast Switching Operation

TYPICAL APPLICATION with "7001" Type 1 K RAM

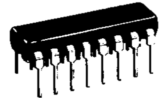


QUAD MOS CLOCK DRIVER

SILICON MONOLITHIC INTEGRATED CIRCUITS

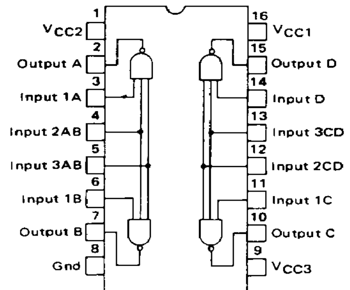


L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN CONNECTIONS



TRUTH TABLE

INPUT			OUTPUT
1	2	3	
H	H	H	L
L	I	I	H
I	L	I	H
I	I	L	H

Where:
H = High Logic State
L = Low Logic State
I = I = Irrelevant

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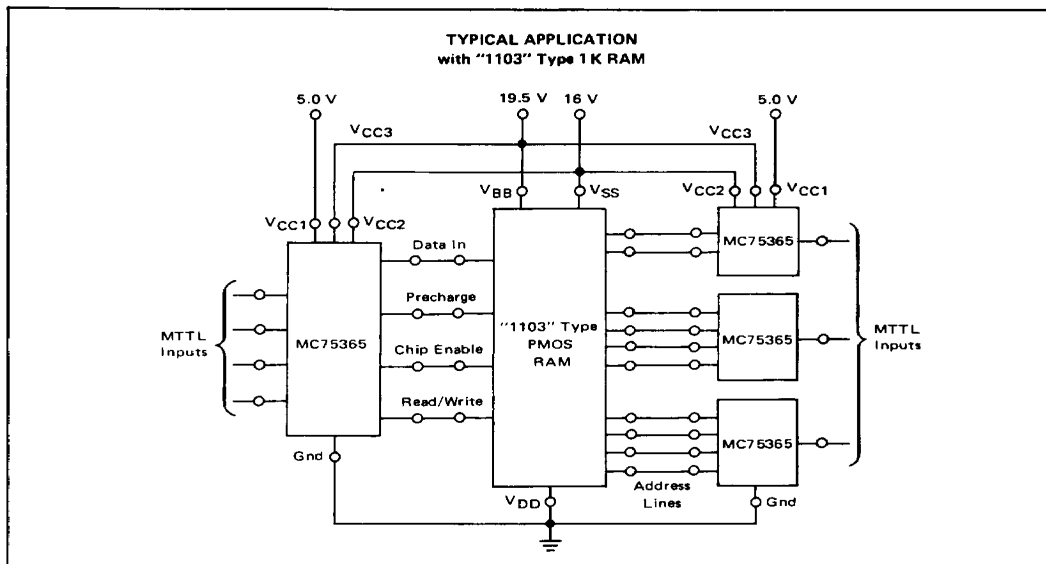

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltages	V_{CC1} V_{CC2} V_{CC3}	-0.5 to 7.0 -0.5 to 25 -0.5 to 30	V
Input Voltage	V_I	5.5	V
Input Differential Voltage (see Note 1)	V_{ID}	5.5	V
Power Dissipation (Package Limitation)			
Ceramic Package @ T_A = 25°C	P_D	1000	mW
Derate above T_A = 25°C	$1/R_{\theta JA}$	6.6	mW/°C
Plastic Package @ T_A = 25°C	P_D	830	mW
Derate above T_A = 25°C	$1/R_{\theta JA}$	6.6	mW/°C
Ceramic Package @ T_C = 25°C	P_D	3.0	Watts
Derate above T_C = 25°C	$1/R_{\theta JC}$	20	mW/°C
Plastic Package @ T_C = 25°C	P_D	1.8	Watts
Derate above T_C = 25°C	$1/R_{\theta JC}$	14	mW/°C
Operating Ambient Temperature Range	T_A	0 to 70	°C
Junction Temperature	T_J		°C
Ceramic Package		175	
Plastic Package		150	
Storage Temperature Range	T_{stg}	-65 to +150	°C

Note 1. This is the differential voltage between any two inputs to any single gate.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltages	V_{CC1} V_{CC2} V_{CC3}	4.75 4.75 V_{CC2}	5.0 20 24	5.25 24 28	V
Difference between V_{CC3} and V_{CC2}	V_{CC3}-V_{CC2}	0	4.0	10	V
Operating Temperature Range	T_A	0	–	70	°C

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ELECTRICAL CHARACTERISTICS (Unless otherwise noted T_A = 25°C, V_{CC1} = 5.0 V, V_{CC2} = 20 V, V_{CC3} = 24 V, C_L = 200 pF, R_D = 24Ω, See Figures 1 and 2.)

Characteristic	Symbol	Min	Typ*	Max	Unit
Input Voltage — High Logic State	V_{IH}	2.0	–	–	V
Input Voltage — Low Logic State	V_{IL}	–	–	0.8	V
Input Clamp Voltage (I_{IC} = -12 mA)	V_{IC}	–	–	1.5	V
Input Current — Maximum Input Voltage (V_{IH} = 5.5 V)	I_{IH1}	–	–	1.0	mA
Input Current — High Logic State	I_{IH2}				µA
(V_{IH} (1) = 2.4 V)		–	–	40	
(V_{IH} (2) or V_{IH} (3) = 2.4 V)		–	–	80	
Input Current — Low Logic State	I_{IL}				mA
(V_{IL} (1) = 0.4 V)		–	-1.0	-1.6	
(V_{IL} (2) or V_{IL} (3) = 0.4 V)		–	-2.0	-3.2	
Output Voltage — High Logic State					V
(V_{CC3} = V_{CC2} + 3.0 V, V_{IL} = 0.8 V, I_{OH} = -100 µA)	V_{OH1}	V_{CC2} -0.3	V_{CC2} -0.1	–	
(V_{CC3} = V_{CC2} + 3.0 V, V_{IL} = 0.8 V, I_{OH} = -10 mA)	V_{OH2}	V_{CC2} -1.2	V_{CC2} -0.9	–	
(V_{CC3} = V_{CC2}, V_{IL} = 0.8 V, I_{OH} = -50 µA)	V_{OH3}	V_{CC2} -1.0	V_{CC2} -0.7	–	
(V_{CC3} = V_{CC2}, V_{IL} = 0.8 V, I_{OH} = -10 mA)	V_{OH4}	V_{CC2} -2.3	V_{CC2} -1.8	–	
Output Clamp Voltage (V_{IL} = 0 V, I_{OC} = 20 mA)	V_{OC}	–	–	V_{CC2} +1.5	V
Output Voltage — Low Logic State					V
(V_{IH} = 2.0 V, I_{OL} = 10 mA)	V_{OL1}	–	0.15	0.3	
(15 V ≤ V_{CC3} ≤ 28 V, V_{IH} = 2.0 V, I_{OL} = 40 mA)	V_{OL2}	–	0.25	0.5	
Power Supply Currents — Outputs High Logic State					mA
(V_{CC1} = 5.25 V, V_{CC2} = 24 V, V_{CC3} = 28 V, V_{IL} = 0 V, I_{OH} = 0 mA)	$I_{CC1(H)}$	–	4.0	8.0	
	$I_{CC2(H)}$	–	-2.2	-3.2/+0.25	
	$I_{CC3(H)}$	–	2.2	3.5	
(V_{CC1} = 5.25 V, V_{CC2} = 24 V, V_{CC3} = 24 V V_{IL} = 0 V, I_{OH} = 0 mA)	$I_{CC2(H)}$	–	–	0.25	
	$I_{CC3(H)}$	–	–	0.5	
Power Supply Currents — Output Low Logic State					mA
(V_{CC1} = 5.25 V, V_{CC2} = 24 V, V_{CC3} = 28 V V_{IH} = 5.0 V, I_{OL} = 0 mA)	$I_{CC1(L)}$	–	31	47	
	$I_{CC2(L)}$	–	–	2.5	
	$I_{CC3(L)}$	–	16	25	
Power Supply Currents — Standby Condition					mA
(V_{CC1} = 0 V, V_{CC2} = 24 V, V_{CC3} = 24 V V_{IH} = 5.0 V, I_{OL} = 0 mA)	$I_{CC2(S)}$	–	–	0.25	
	$I_{CC3(S)}$	–	–	0.5	

*Typical Values at 25°C, V_{CC1} = 5.0 V, V_{CC2} = 20 V and V_{CC3} = 24 V

SWITCHING CHARACTERISTICS (Unless otherwise noted T_A = 25°C, V_{CC1} = 5.0 V, V_{CC2} = 20 V, V_{CC3} = 24 V, C_L = 200 pF, R_D = 24Ω, See Figures 1 and 2.)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time, Low to High State Output	t_{PLH}	10	31	48	ns
Propagation Delay Time, High to Low State Output	t_{PHL}	10	30	46	
Delay Time, Low to High State Output	t_{DLH}	–	11	20	ns
Delay Time, High to Low State Output	t_{DHL}	–	10	18	
Transition Time, Low to High State Output	t_{TLH}	–	20	33	ns
Transition Time, High to Low State Output	t_{THL}	–	20	33	

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FIGURE 1 — SWITCHING CHARACTERISTIC TEST CIRCUIT

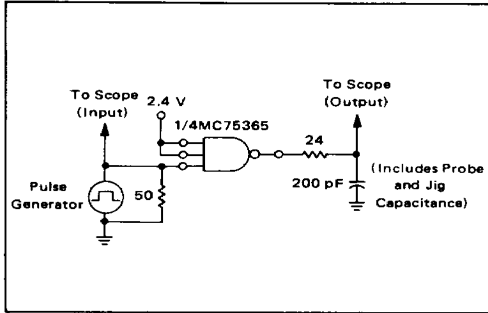
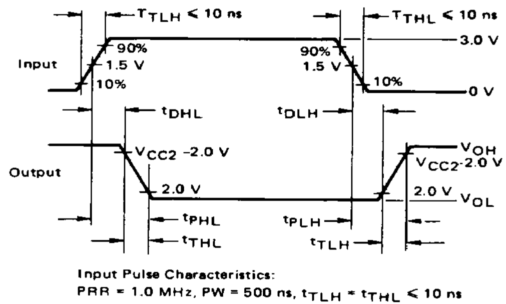


FIGURE 2 — SWITCHING CHARACTERISTICS WAVEFORMS



TYPICAL PERFORMANCE CURVES

FIGURE 3 — OUTPUT VOLTAGE — HIGH LOGIC STATE versus OUTPUT CURRENT

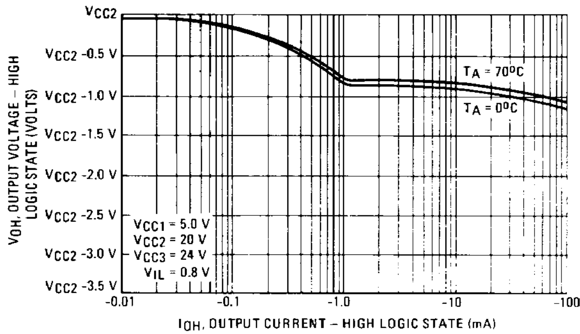


FIGURE 4 — OUTPUT VOLTAGE — HIGH LOGIC STATE versus OUTPUT CURRENT

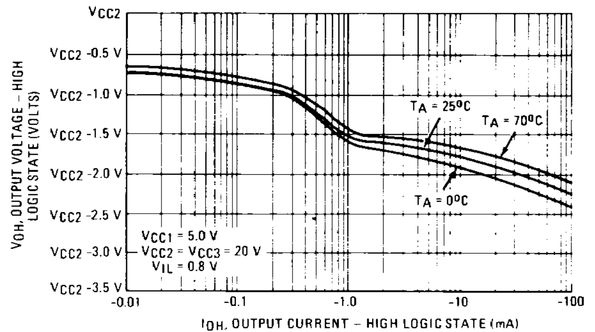


FIGURE 5 — OUTPUT VOLTAGE — LOW LOGIC STATE versus OUTPUT CURRENT

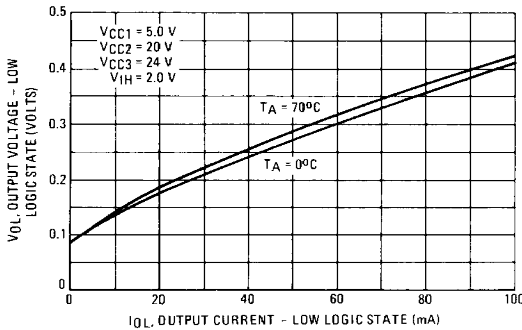
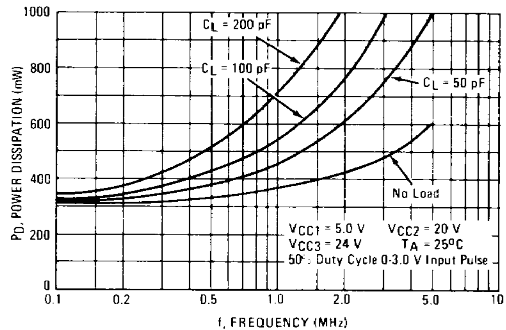


FIGURE 6 — TOTAL POWER DISSIPATION versus FREQUENCY (All Four Drivers)



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TYPICAL PERFORMANCE CURVES

FIGURE 7 — PROPAGATION DELAY TIME — LOW TO HIGH STATE OUTPUT versus AMBIENT TEMPERATURE

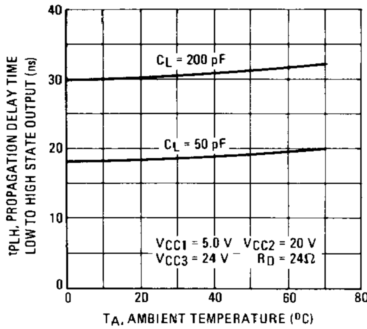


FIGURE 8 — PROPAGATION DELAY TIME — HIGH TO LOW STATE OUTPUT versus AMBIENT TEMPERATURE

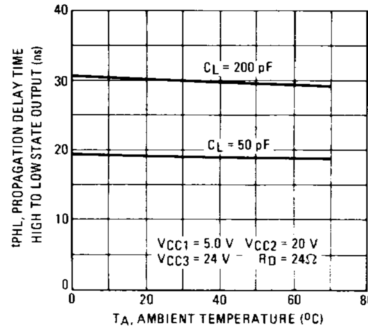


FIGURE 9 — PROPAGATION DELAY TIME — LOW TO HIGH STATE OUTPUT versus V_{CC2} SUPPLY VOLTAGE

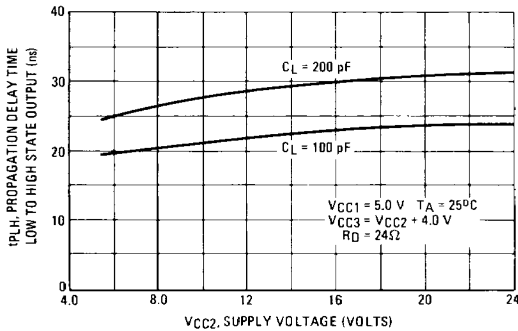


FIGURE 10 — PROPAGATION DELAY TIME — HIGH TO LOW STATE OUTPUT versus V_{CC2} SUPPLY VOLTAGE

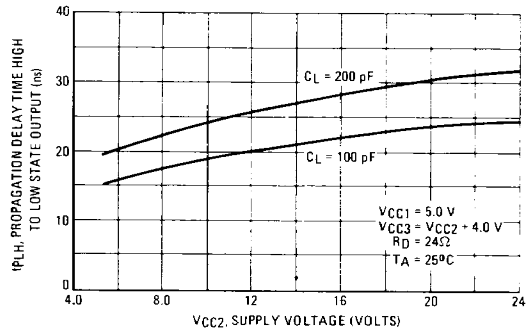


FIGURE 11 — PROPAGATION DELAY TIME — LOW TO HIGH LOGIC STATE versus LOAD CAPACITANCE

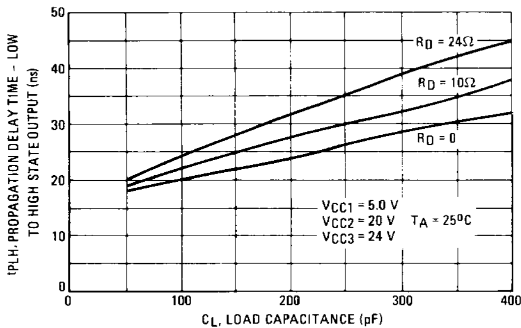
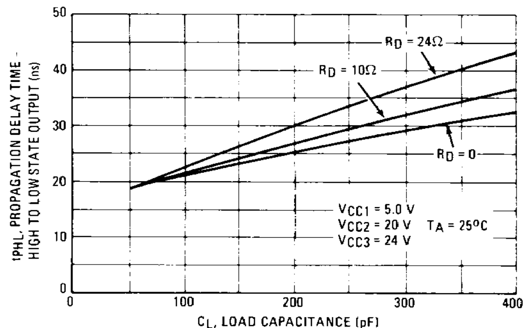


FIGURE 12 — PROPAGATION DELAY TIME — HIGH TO LOW STATE OUTPUT versus LOAD CAPACITANCE



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APPLICATIONS SUGGESTIONS

POWER CONSIDERATIONS

Circuit performance and long-term circuit reliability are affected by die temperature. Normally, both are improved by keeping the integrated circuit junction temperatures low. Electrical power dissipated in the integrated circuit is the source of heat. This heat source increases the temperature of the die relative to some reference point, normally the ambient temperature. The temperature increase depends on the amount of power dissipated in the circuit and on the net thermal resistance between the heat source and the reference point. The basic formula for converting power dissipation into junction temperature is:

$$T_J = T_A + P_D\,(R_{\theta JC} + R_{\theta CA}) \quad (1)$$

or

$$T_J = T_A + P_D\,(R_{\theta JA}) \quad (2)$$

where

T_J = junction temperature
T_A = ambient temperature
P_D = power dissipation
$R_{\theta JC}$ = thermal resistance, junction to case
$R_{\theta CA}$ = thermal resistance, case to ambient
$R_{\theta JA}$ = thermal resistance, junction to ambient.

Power Dissipation for the MC75365 MOS Clock Driver:
The power dissipation of the device (P_D) is dependent on the following system requirements: frequency of operation, capacitive loading, output voltage swing, and duty cycle. The variation of power dissipation with frequency and load capacitance for the MC75365 is illustrated in Figure 6. The power dissipation, when substituted into equation (2), should not yield a junction temperature, T_J, greater than T_J(max) at the maximum encountered ambient temperature. T_J(max) is specified for two integrated circuit packages in the maximum ratings section of this data sheet.

With these maximum junction temperature values, the maximum permissible power dissipation at a given ambient temperature may be determined. This can be done with equations (1) and (2) and the maximum thermal resistance values given in Table 1 shown on the following page.

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TABLE 1 – THERMAL CHARACTERISTICS OF "L" AND "P" PACKAGES

PACKAGE TYPE (Mounted in Socket)	$R_{\theta JA}$ (°C/W) Still Air		$R_{\theta JC}$ (°C/W) Still Air	
	MAX	TYP	MAX	TYP
"L" (Ceramic Package)	150	100	50	27
"P" (Plastic Package)	150	100	70	40

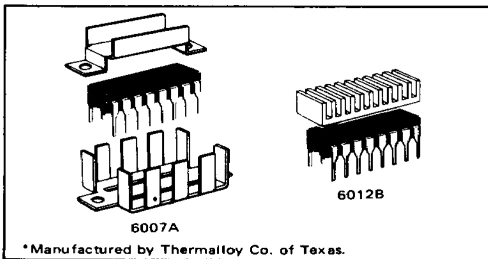
If the power dissipation determined by a given system produces a junction temperature in excess of the recommended maximum rating for a given package type, something must be done to reduce the junction temperature.

There are two methods of lowering the junction temperature without changing the system requirements. First, the ambient temperature may be reduced sufficiently to bring T_J to an acceptable value. Secondly, the $R_{\theta CA}$ term can be reduced. Lowering the $R_{\theta CA}$ term can be accomplished by increasing the surface area of the package with the addition of a heat sink or by blowing air across the package to promote improved heat dissipation.

Heat Sink Considerations:

Heat sinks come in a wide variety of sizes and shapes that will accomodate almost any IC package made. Some of these heat sinks are illustrated in Figure 13.

FIGURE 13 – THERMALLOY* HEAT SINKS



*Manufactured by Thermalloy Co. of Texas.

From Table 1, $R_{\theta JA}$(max) for the ceramic package with no heat sink and in a still air environment is 150°C/W.

For the following example the Thermalloy 6012B type heat sink, or equivalent, is chosen. With this heat sink, the $R_{\theta CA}$ for natural convection from Figure 14 is 44°C/W. From Table 1 $R_{\theta JC}$(max) = 50°C/W for the ceramic package. Therefore, the new $R_{\theta JA}$(max) with the 6012B heat sink added becomes:

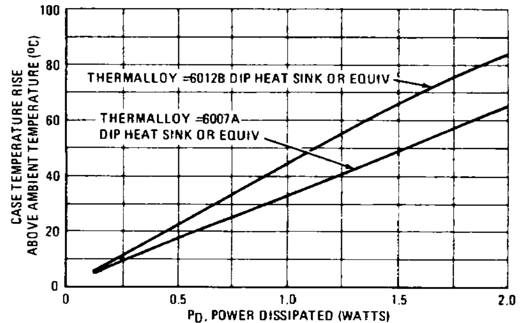
$R_{\theta JA}$(max) = 50°C/W + 44°C/W = 94°C/W.

Thus the addition of the heat sink has reduced $R_{\theta JA}$(max) from 150°C/W down to 94°C/W. With the heat sink, the maximum power dissipation by equation (2) at T_A = +70°C is:

$$P_D = \frac{175^{\circ}C - 70^{\circ}C}{+94^{\circ}C/W} = 1.11 \text{ watts.}$$

This gives approximately a 60% increase in maximum power dissipation over the power dissipation which is allowable with no heat sink.

FIGURE 14 – CASE TEMPERATURE RISE ABOVE AMBIENT versus POWER DISSIPATED USING NATURAL CONVECTION



Forced Air Considerations:

As illustrated in Figure 15, forced air can be employed to reduce the $R_{\theta JA}$ term. Note, however, that this curve is expressed in terms of typical $R_{\theta JA}$ rather than maximum $R_{\theta JA}$. Maximum $R_{\theta JA}$ can be determined in the following manner:

From Table 1 the following information is known:

(a) $R_{\theta JA}$(typ) = 100°C/W

(b) $R_{\theta JC}$(typ) = 27°C/W

Since:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad (3)$$

Then:

$$R_{\theta CA} = R_{\theta JA} - R_{\theta JC} \quad (4)$$

Therefore, in still air

$R_{\theta CA}$(typ) = 100°C/W - 27°C/W = 73°C/W

From Curve 1 of Figure 14 at 500 LFPM and equation (4),

$R_{\theta CA}$(typ) = 53°C/W - 27°C/W = 26°C/W.

Thus $R_{\theta CA}$(typ) has changed from 73°C/W (still air) to 26°C/W (500 LFPM), which is a decrease in typical $R_{\theta CA}$ by a ratio of 1:2.8. Since the typical value of $R_{\theta CA}$ was reduced by a ratio of 1:2.8, $R_{\theta CA}$(max) of 100°C/W should also decrease by a ratio of 1:2.8.

This yields an $R_{\theta CA}$(max) at 500 LFPM of 36°C/W. Therefore, from equation (3):

$R_{\theta JA}$(max) = 50°C/W + 36°C/W = 86°C/W.

Therefore the maximum allowable power dissipation at 500 LFPM and T_A = +70°C is from equation (2):

$$P_D = \frac{175^{\circ}C - 70^{\circ}C}{86^{\circ}C/W} = 1.2 \text{ watts.}$$

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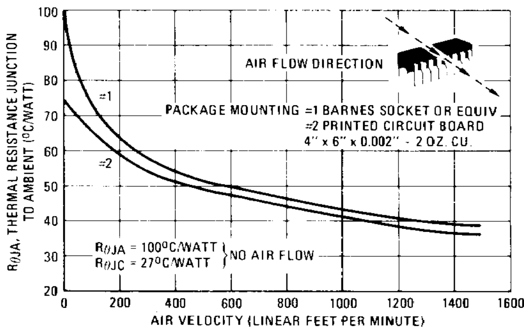
FIGURE 15 – TYPICAL THERMAL RESISTANCE ($R_{\theta JA}$) OF "L" PACKAGE versus AIR VELOCITY



Heat Sink and Forced Air Combined:

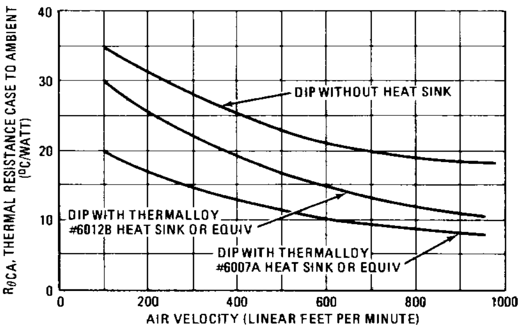
Some heat sink manufacturers provide data and curves of $R_{\theta CA}$ for still air and forced air such as illustrated in Figure 16. For example the 6012B heat sink has an $R_{\theta CA}$ = 17°C/W at 500 LFPM as noted in Figure 15. From equation (3):

Max $R_{\theta JA}$ = 50°C/W + 17°C/W = 67°C/W

From equation (2) at T_A = +70°C

$$P_D = \frac{175^{\circ}C - 70^{\circ}C}{67^{\circ}C/W}\ 1.57 \text{ watts.}$$

FIGURE 16 – THERMAL RESISTANCE $R_{\theta CA}$ versus AIR VELOCITY



Note from Table 1 and Figure 15 that if the 16-pin ceramic package is mounted directly to the PC board (2 oz. cu. underneath), that typical $R_{\theta JA}$ is considerably less than for socket mount with still air and no heat sink. The following procedure can be employed to determine the maximum power dissipation for this condition.

Given data from Table 1:

typical $R_{\theta JA}$ = 100°C/W

typical $R_{\theta JC}$ = 27°C/W

From Curve 2 of Figure 15, $R_{\theta JA}$(typ) is 75°C/W for a PC mount and no air flow. Then the typical $R_{\theta CA}$ is 75°C/W – 27°C/W = 48°C/W. From Table 1 the typical value of $R_{\theta CA}$ for socket mount is 100°C/W – 27°C/W = 73°C/W. This shows that the PC board mount results in a decrease in typical $R_{\theta CA}$ by a ratio of 1:1.5 below the typical value of $R_{\theta CA}$ in a socket mount. Therefore, the maximum value of socket mount $R_{\theta CA}$ of 100°C/W should also decrease by a ratio of 1:1.5 when the device is mounted in a PC board. The maximum $R_{\theta CA}$ becomes:

$$R_{\theta CA} = \frac{100^{\circ}C/W}{1.5} = 66^{\circ}C/W \text{ for PC board mount}$$

Therefore the maximum $R_{\theta JA}$ for a PC mount is from equation (3).

$R_{\theta JA}$ = 50°C/W + 66°C/W = 116°C/W.

With maximum $R_{\theta JA}$ known, the maximum power dissipation can be found. If T_A = 70°C then from equation (2) the maximum power dissipation may be found to be 905 mW.

In most cases, heat sink manufacturer's publish only $R_{\theta CA}$ socket mount data. Although data for PC mounting is generally not available, this should present no problem. Note in Figure 15 that an air flow greater than 250 LFPM yields a socket mount $R_{\theta JA}$ approximately 6% greater than for a PC mount. Therefore, the socket mount data can be used for a PC mount with a slightly greater safety factor. Also it should be noted that thermal resistance measurements can vary widely. These measurement variations are due to the dependency of $R_{\theta CA}$ of the type environment and measurement techniques employed. For example, $R_{\theta CA}$ would be greater for an integrated circuit mounted on a PC board with little or no ground plane versus one with a substantial ground plane. Therefore, if the maximum calculated junction temperature is on the border line of being too high for a given system application, then thermal resistance measurements should be done on the system to be absolutely certain that the maximum junction temperature is not exceeded.

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