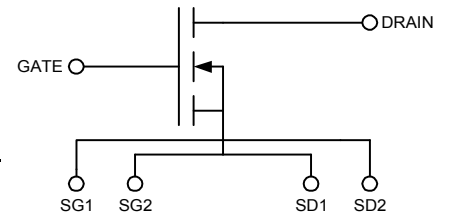


N-Channel Enhancement Mode
Low Q_g and R_g
High dv/dt
Nanosecond Switching

$V_{DSS} = 500 V$
 $I_{D25} = 4.5 A$
 $R_{DS(on)} \leq 1.5 \Omega$
 $P_{DC} = 200W$

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	$T_J = 25^\circ C$ to $150^\circ C$	500	V
V_{DGR}	$T_J = 25^\circ C$ to $150^\circ C$; $R_{GS} = 1 M\Omega$	500	V
V_{GS}	Continuous	± 20	V
V_{GSM}	Transient	± 30	V
I_{D25}	$T_c = 25^\circ C$	4.5	A
I_{DM}	$T_c = 25^\circ C$, pulse width limited by T_{JM}	27	A
I_{AR}	$T_c = 25^\circ C$	4.5	A
E_{AR}	$T_c = 25^\circ C$	-	mJ
dv/dt	$I_S \leq I_{DM}$, $di/dt \leq 100 A/\mu s$, $V_{DD} \leq V_{DSS}$, $T_J \leq 150^\circ C$, $R_G = 0.2 \Omega$	3.5	V/ns
	$I_S = 0$	>200	V/ns
P_{DC}		200	W
P_{DHS}	$T_c = 25^\circ C$ Derate $4.4 W/^\circ C$ above $25^\circ C$	80	W
P_{DAMB}	$T_c = 25^\circ C$	3.5	W
R_{thJC}		0.74	C/W
R_{thJHS}		1.50	C/W



Symbol	Test Conditions	Characteristic Values		
		$T_J = 25^\circ C$ unless otherwise specified		
		min.	typ.	max.
V_{DSS}	$V_{GS} = 0 V$, $I_D = 3 ma$	500		V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250 \mu a$	2.5	3.4	4 V
I_{GSS}	$V_{GS} = \pm 20 V_{DC}$, $V_{DS} = 0$			± 100 nA
I_{DSS}	$V_{DS} = 0.8 V_{DSS}$, $T_J = 25^\circ C$ $V_{GS} = 0$, $T_J = 125^\circ C$			25 μA
				250 μA
$R_{DS(on)}$	$V_{GS} = 15 V$, $I_D = 0.5 I_{D25}$ Pulse test, $t \leq 300 \mu s$, duty cycle $d \leq 2\%$		1.2	1.5 Ω
g_{fs}	$V_{DS} = 60 V$, $I_D = 0.5 I_{D25}$, pulse test		1.9	S
T_J		-55		+175 $^\circ C$
T_{JM}			175	$^\circ C$
T_{stg}		-55		+175 $^\circ C$
T_L	1.6mm (0.063 in) from case for 10 s		300	$^\circ C$
Weight			2	g

Features

- Isolated Substrate
 - high isolation voltage (>2500V)
 - excellent thermal transfer
 - Increased temperature and power cycling capability
- IXYS advanced low Q_g process
- Low gate charge and capacitances
 - easier to drive
 - faster switching
- Low $R_{DS(on)}$
- Very low insertion inductance (<2nH)
- No beryllium oxide (BeO) or other hazardous materials

Advantages

- Optimized for RF and high speed switching at frequencies to >100MHz
- Easy to mount—no insulators needed
- High power density

Symbol	Test Conditions	Characteristic Values		
		min.	typ.	max.
(T _J = 25°C unless otherwise specified)				
R _G				5 Ω
C _{iss}			570	pF
C _{oss}	V _{GS} = 0 V, V _{DS} = 0.8 V _{DSS(max)} , f = 1 MHz		75	pF
C _{rss}			3	pF
C _{stray}	Back Metal to any Pin		16	pF
T _{d(on)}			4	ns
T _{on}	V _{GS} = 15 V, V _{DS} = 0.8 V _{DSS} I _D = 0.5 I _{DM}		4	ns
T _{d(off)}	R _G = 0.2 Ω (External)		4	ns
T _{off}			4	ns
Q _{g(on)}			14	nC
Q _{gs}	V _{GS} = 10 V, V _{DS} = 0.5 V _{DSS} I _D = 0.5 I _{D25} , I _g = 3 ma		3.5	nC
Q _{gd}			5.5	nC

Source-Drain Diode		Characteristic Values		
(T _J = 25°C unless otherwise specified)				
Symbol	Test Conditions	min.	typ.	max.
I _S	V _{GS} = 0 V			4.5 A
I _{SM}	Repetitive; pulse width limited by T _{JM}			27 A
V _{SD}	I _F = I _S , V _{GS} = 0 V, Pulse test, t ≤ 300 μs, duty cycle ≤ 2%			1.4 V
T _{rr}			900	ns

CAUTION: Operation at or above the Maximum Ratings values may impact device reliability or cause permanent damage to the device.

Information in this document is believed to be accurate and reliable. IXYSRF reserves the right to make changes to information published in this document at any time and without notice.

For detailed device mounting and installation instructions, see the "Device Installation & Mounting Instructions" technical note on the IXYSRF web site at;

http://www.ixysrf.com/pdf/switch_mode/appnotes/7de_series_mosfet_installation_instructions.pdf

IXYS RF reserves the right to change limits, test conditions and dimensions.

IXYS RF MOSFETS are covered by one or more of the following U.S. patents:

4,835,592	4,860,072	4,881,106	4,891,686	4,931,844	5,017,508
5,034,796	5,049,961	5,063,307	5,187,117	5,237,481	5,486,715
5,381,025	5,640,045				

Fig. 1 Typical Transfer Characteristics
 $V_{DS} = 60V, PW = 20\mu S$

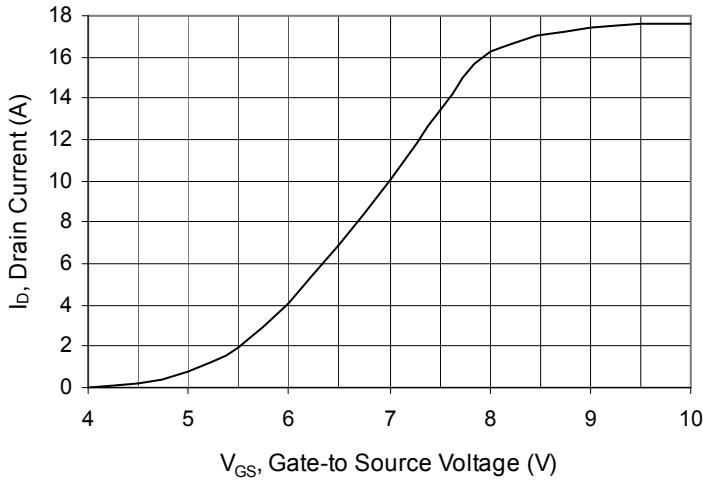


Fig. 2 Typical Output Characteristics

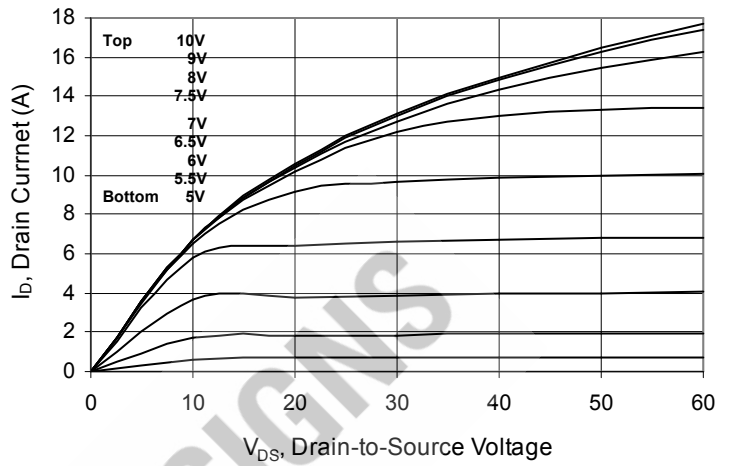


Fig. 3 Gate Charge vs. Gate-to-Source Voltage
 $V_{DS} = 250V, I_D = 2.25A$

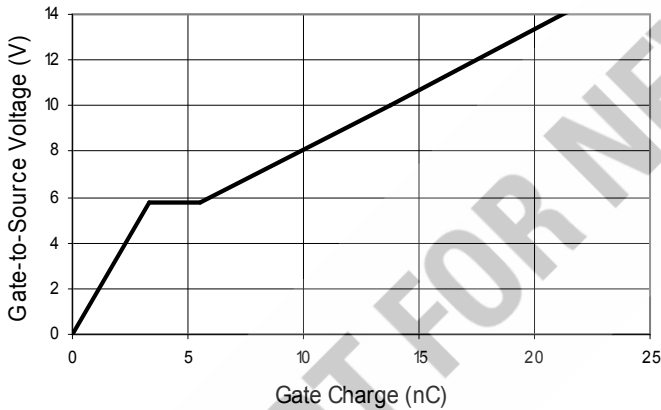


Fig. 4 V_{DS} Voltage vs. Capacitance

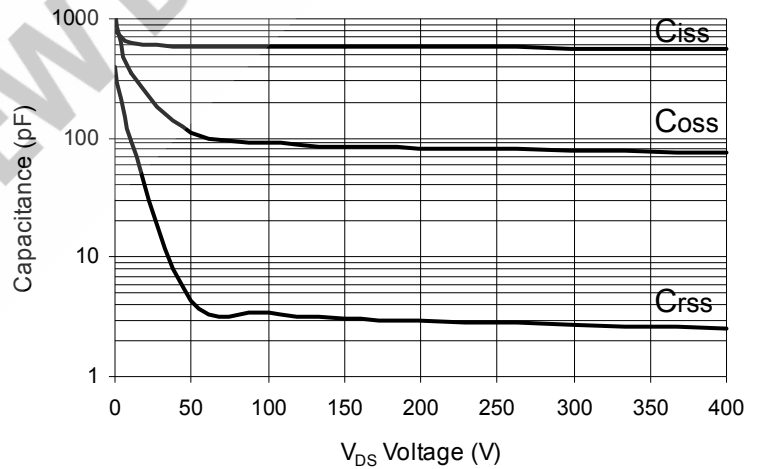
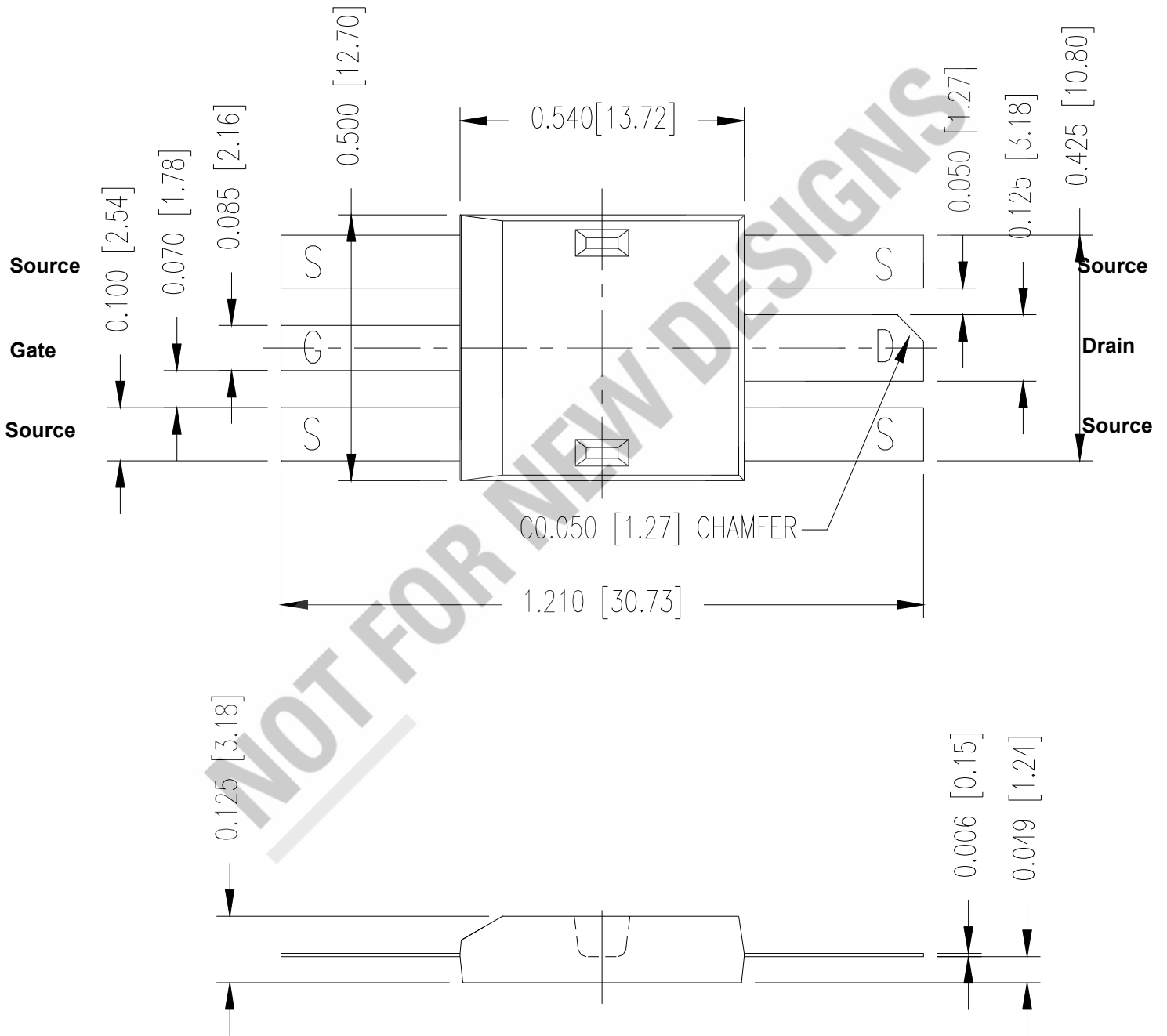


Fig. 5 Package drawing



501N04A DE-SERIES SPICE Model

The DE-SERIES SPICE Model is illustrated in Figure 6. The model is an expansion of the SPICE level 3 MOSFET model. It includes the stray inductive terms L_G , L_S and L_D . R_d is the $R_{DS(ON)}$ of the device, R_{ds} is the resistive leakage term. The output capacitance, C_{OSS} , and reverse transfer capacitance, C_{RSS} are modeled with reversed biased diodes. This provides a varactor type response necessary for a high power device model. The turn on delay and the turn off delay are adjusted via R_{on} and R_{off} .

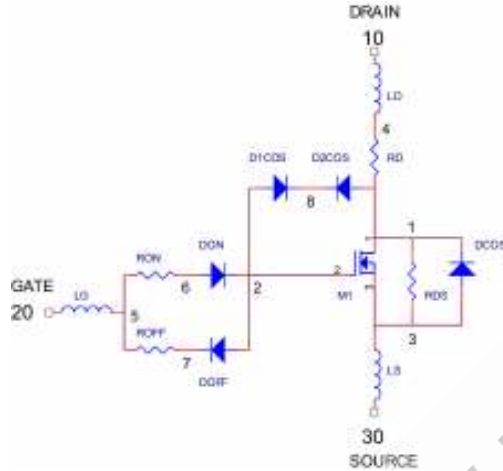


Figure 6 DE-SERIES SPICE Model

This SPICE model may be downloaded as a text file from the IXYSRF web site at
http://www.ixysrf.com/products/switch_mode.html
<http://www.ixysrf.com/spice/de150-501n04a.html>

Net List:

```
*SYM=POWMOSN
.SUBCKT 501N04A 10 20 30
*   TERMINALS: D G S
*   500 Volt 4.5 Amp 1.5 Ohm N-Channel Power MOSFET 10-30-2001
M1 1 2 3 3 DMOS L=1U W=1U
RON 5 6 9.5
DON 6 2 D1
ROF 5 7 3.5
DOF 2 7 D1
D1CRS 2 8 D2
D2CRS 1 8 D2
CGS 2 3 .6N
RD 4 1 1.5
DCOS 3 1 D3
RDS 1 3 5.0MEG
LS 3 30 .1N
LD 10 4 1N
LG 20 5 1N
.MODEL DMOS NMOS (LEVEL=3 VTO=3.0 KP=6.0)
.MODEL D1 D (IS=.5F CJO=1P BV=100 M=.5 VJ=.6 TT=1N)
.MODEL D2 D (IS=.5F CJO=175P BV=500 M=.5 VJ=.6 TT=1N RS=10M)
.MODEL D3 D (IS=.5F CJO=250P BV=500 M=.3 VJ=.4 TT=400N RS=10M)
.ENDS
```

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