OCTOBER 1976 — REVISED MARCH 1988

- **Complementary Outputs**
- **Direct Overriding Load (Data) Inputs**
- **Gated Clock Inputs**
- **Parallel-to-Serial Data Conversion**

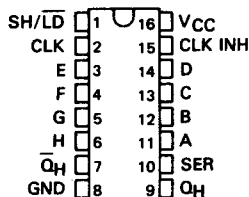| TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'165	26 MHz	210 mW
'LS165A	35 MHz	90 mW

description

The '165 and 'LS165A are 8-bit serial shift registers that shift the data in the direction of Q_A toward Q_H when clocked. Parallel-in access to each stage is made available by eight individual direct data inputs that are enabled by a low level at the shift/load input. These registers also feature gated clock inputs and complementary outputs from the eighth bit. All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design.

Clocking is accomplished through a 2-input positive-NOR gate, permitting one input to be used as a clock-inhibit function. Holding either of the clock inputs high inhibits clocking and holding either clock input low with the shift/load input high enables the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. Parallel loading is inhibited as long as the shift/load input is high. Data at the parallel inputs are loaded directly into the register while the shift/load input is low independently of the levels of the clock, clock inhibit, or serial inputs.
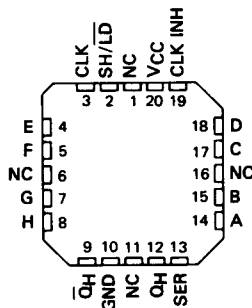
SN54165, SN54LS165A . . . J OR W PACKAGE
SN74165 . . . N PACKAGE
SN74LS165A . . . D OR N PACKAGE
(TOP VIEW)

SH/$\overline{LD}$	1	16	V_{CC}
CLK	2	15	CLK INH
E	3	14	D
F	4	13	C
G	5	12	B
H	6	11	A
$\overline{Q_H}$	7	10	SER
GND	8	9	Q_H

SN54LS165A . . . FK PACKAGE
(TOP VIEW)

FUNCTION TABLE

INPUTS					INTERNAL OUTPUTS		OUTPUT
SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A...H	$\overline{Q}_A$	$\overline{Q}_B$	Q_H
L	X	X	X	a...h	a	b	h
H	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	H	X	X	X	Q_{A0}	Q_{B0}	Q_{H0}

logic symbol[†]
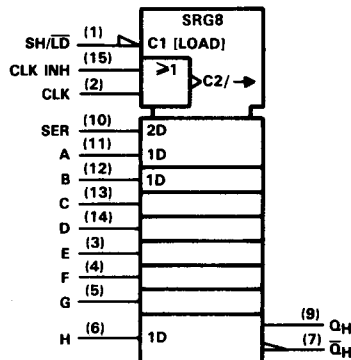
[†]This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

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schematics of inputs and outputs

'165
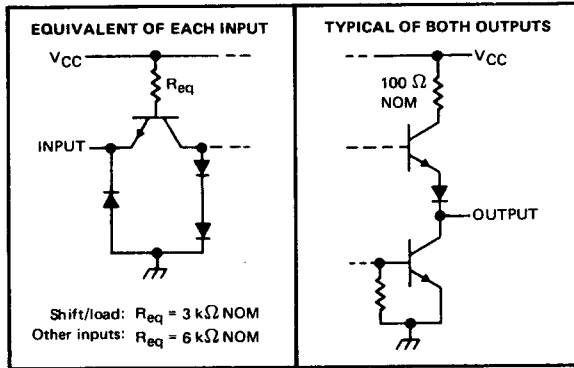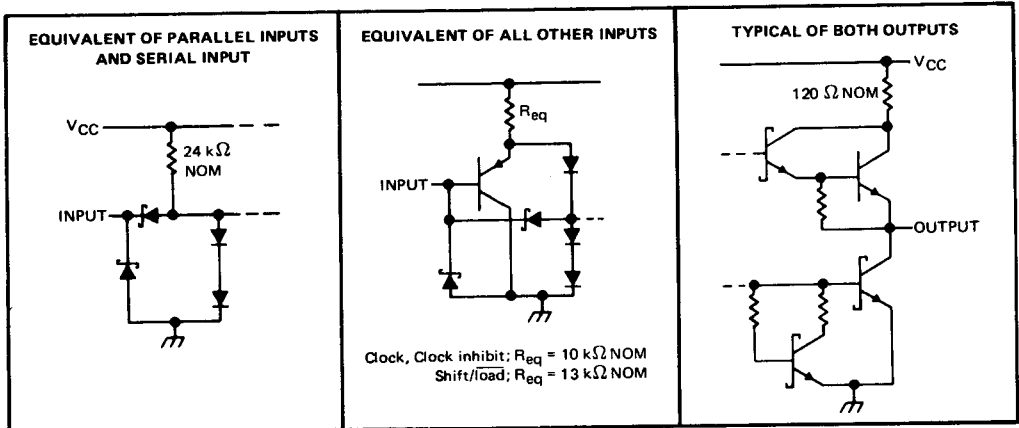
EQUIVALENT OF EACH INPUT	TYPICAL OF BOTH OUTPUTS

Shift/load: R_{eq} = 3 kΩ NOM
Other inputs: R_{eq} = 6 kΩ NOM

'LS165A

EQUIVALENT OF PARALLEL INPUTS AND SERIAL INPUT	EQUIVALENT OF ALL OTHER INPUTS	TYPICAL OF BOTH OUTPUTS

Clock, Clock inhibit; R_{eq} = 10 kΩ NOM
Shift/load; R_{eq} = 13 kΩ NOM

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logic diagram (positive logic)
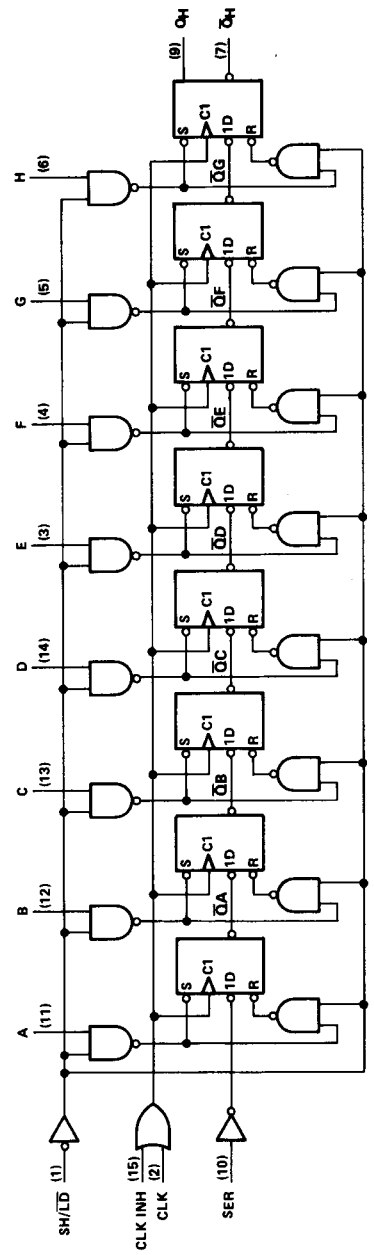
Pin numbers shown are for D, J, N, and W packages.

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typical shift, load, and inhibit sequences
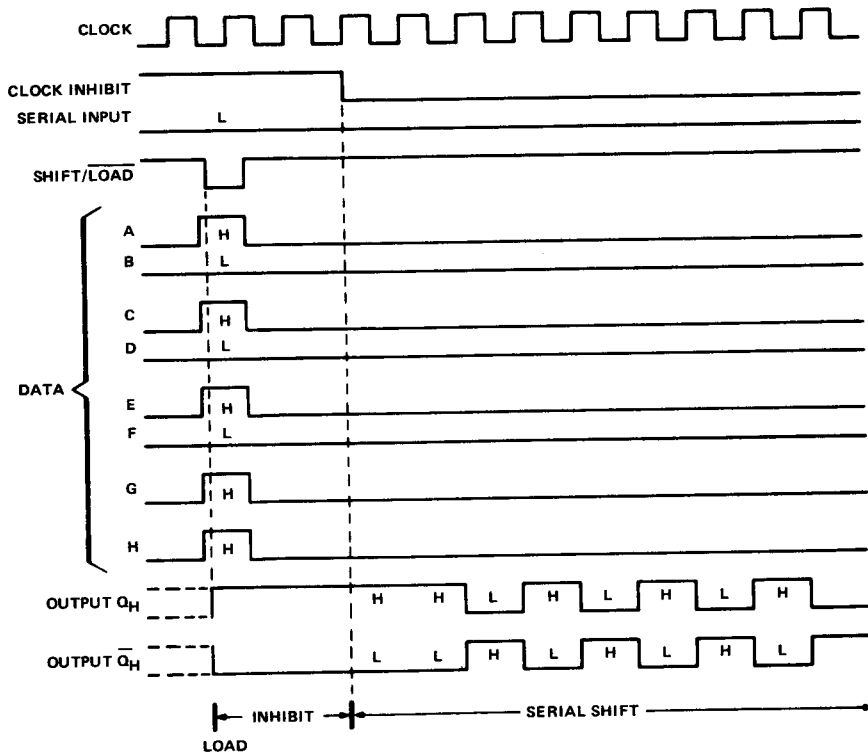
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . 7 V

Input voltage: SN54165, SN74165 . . . . 5.5 V

$\qquad$ SN54LS165A, SN74LS165A . . . . 7 V

Interemitter voltage (see Note 2) . . . . 5.5 V

Operating free-air temperature range: SN54165, SN54LS165A . . . . $-55°C$ to $125°C$

$\qquad$ SN74165, SN74LS165A . . . . $0°C$ to $70°C$

Storage temperature range . . . . $-65°C$ to $150°C$

NOTES 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
$\qquad$ 2. This is the voltage between two emitters of a multiple-emitter transistor. This rating applies for the '165 to the shift/load input in conjunction with the clock-inhibit inputs.

recommended operating conditions

	SN54165 MIN	SN54165 NOM	SN54165 MAX	SN74165 MIN	SN74165 NOM	SN74165 MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−800			−800	μA
Low-level output current, I_{OL}			16			16	mA
Clock frequency, f_{clock}	0		20	0		20	MHz
Width of clock input pulse, $t_{w(clock)}$	25			25			ns
Width of load input pulse, $t_{w(load)}$	15			15			ns
Clock-enable setup time, t_{su} (see Figure 1)	30			30			ns
Parallel input setup time, t_{su} (see Figure 1)	10			10			ns
Serial input setup time, t_{su} (see Figure 2)	20			20			ns
Shift setup time, t_{su} (see Figure 2)	45			45			ns
Hold time at any input, t_h	0			0			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS[†]	SN54165 MIN	SN54165 TYP[‡]	SN54165 MAX	SN74165 MIN	SN74165 TYP[‡]	SN74165 MAX	UNIT
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current — Shift/load	V_{CC} = MAX, V_I = 2.4 V			80			80	μA
	— Other inputs				40			40	
I_{IL}	Low-level input current — Shift/load	V_{CC} = MAX, V_I = 0.4 V			−3.2			−3.2	mA
	— Other inputs				−1.6			−1.6	
I_{OS}	Short-circuit output current §	V_{CC} = MAX	−20		−55	−18		−55	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 3		42	63		42	63	mA

NOTE 3: With the outputs open, clock inhibit and clock at 4.5 V, and a clock pulse applied to the shift/load input, I_{CC} is measured first with the parallel inputs at 4.5 V, then with the parallel inputs grounded.

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER[¶]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}				20	26		MHz
t_{PLH}	Load	Any			21	31	ns
t_{PHL}					27	40	
t_{PLH}	Clock	Any	C_L = 15 pF, R_L = 400 Ω, See figures 1 thru 3		16	24	ns
t_{PHL}					21	31	
t_{PLH}	H	Q_H			11	17	ns
t_{PHL}					24	36	
t_{PLH}	H	$\overline{Q}_H$			18	27	ns
t_{PHL}					18	27	

¶ f_{max} ≡ maximum clock frequency

t_{PLH} ≡ propagation delay time, low-to-high-level output

t_{PHL} ≡ propagation delay time, high-to-low-level output

recommended operating conditions

			SN54LS165A			SN74LS165A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency		0		25	0		25	MHz
$t_{w(clock)}$	Width of clock input pulse (See Figure 1)	clock high	15			15			ns
		clock low	25			25			
$t_{w(load)}$	Width of load input pulse	clock high	25			25			ns
		clock low	17			17			
t_{su}	Clock-enable setup time (See Figure 1)		30			30			ns
t_{su}	Parallel input setup time (See Figure 1)		10			10			ns
t_{su}	Serial input setup time (See Figure 2)		20			20			ns
t_{su}	Shift setup time (See Figure 2)		45			45			ns
t_h	Hold time at any input		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54LS165A			SN74LS165A			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX, I_{OH} = −0.4 mA		2.5	3.5		2.7	3.5		V
V_{OL}	V_{CC} = MIN V_{IH} = 2 V V_{IL} = MAX,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}	V_{CC} = MAX, V_I = 2.7 V				20			20	µA
I_{IL}	V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
I_{OS} §	V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC}	V_{CC} = MAX, See Note 3			18	30		18	30	mA

NOTE 3: With the outputs open, clock inhibit and clock at 4.5 V, and a clock pulse applied to the shift load input, I_{CC} is measured first with the parallel inputs at 4.5 V, then with the parallel inputs grounded.
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}				25	35		MHz
t_{PLH}	Load	Any			21	35	ns
t_{PHL}					26	35	
t_{PLH}	Clock	Any	R_L = 2 kΩ, C_L = 15 pF		14	25	ns
t_{PHL}			See Figures 1 thru 3		16	25	
t_{PLH}	H	Q_H			13	25	ns
t_{PHL}					24	30	
t_{PLH}	H	$\overline{Q}_H$			19	30	ns
t_{PHL}					17	25	

f_{max} = maximum clock frequency
t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output

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PARAMETER MEASUREMENT INFORMATION
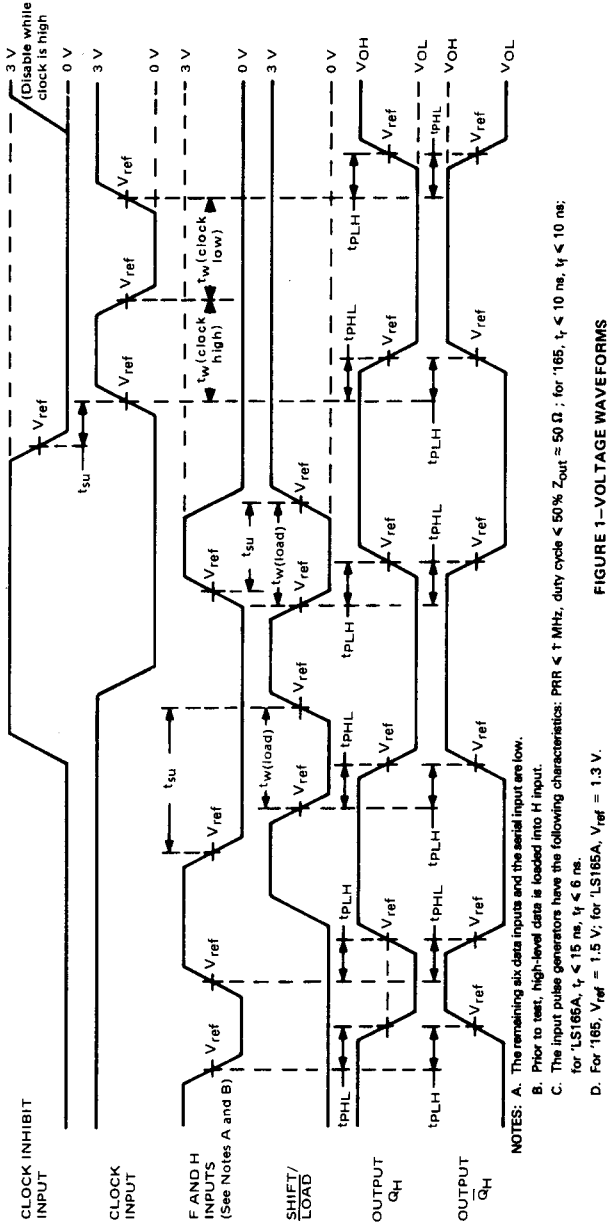
FIGURE 1—VOLTAGE WAVEFORMS

CLOCK INHIBIT INPUT

CLOCK INPUT

F AND H INPUTS (See Notes A and B)

SHIFT/LOAD

OUTPUT Q_H

OUTPUT $\bar{Q}_H$

NOTES: A. The remaining six data inputs and the serial input are low.
     B. Prior to test, high-level data is loaded into H input.
     C. The input pulse generators have the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{out} \approx 50\ \Omega$; for '165, t_r < 10 ns, t_f < 10 ns; for 'LS165A, t_r < 15 ns, t_f < 6 ns.
     D. For '165, V_{ref} = 1.5 V; for 'LS165A, V_{ref} = 1.3 V.

FIGURE 2—VOLTAGE WAVEFORMS

SHIFT/LOAD

SERIAL INPUT

CLOCK INPUT

NOTES: A. The eight data inputs and the clock-inhibit input are low. Results are monitored at output Q_H at t_{n+7}.
     B. The input pulse generators have the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{out} \approx 50\ \Omega$; for '165, t_r < 10 ns; for 'LS165A, t_r < 15 ns, t_f < 6 ns.
     C. For '165, V_{ref} = 1.5 V; for 'LS165A, V_{ref} = 1.3 V.

FIGURE 3—LOAD CIRCUIT FOR SWITCHING TESTS

TEST POINT

FROM OUTPUT UNDER TEST

V_{CC}

R_L

C_L

NOTES: A. C_L includes probe and jig capacitance.
     B. All diodes are 1N3064 or equivalent.

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