CMOS HIGH SPEED GATE ARRAY

- **High Speed Silicon Gate CMOS Technology**
- **TTL and CMOS I/O Compatible**
- **High Output Drive Compatible**
- **Gate Densities from 513 to 6,206 Gates**

■ DESCRIPTION

The SLA6000 series consists of a group of 8 CMOS gate arrays with gate counts from 513 to 6,206 gates. The series is fabricated utilizing our 2.0 micron high speed CMOS silicon gate technology to achieve propagation delays of 2ns for the internal gates and 5ns to 7ns for the I/O buffers. All I/O buffers are TTL and CMOS compatible which makes this series an ideal choice for replacing existing discrete logic as well as for new designs.

■ FEATURES

- 2.0 micron CMOS, 2 layer metalization
- High speed: tpd (2-input NAND)
  - Internal gate: 2.0ns (Typ)
  - Input buffer: T_{PLH} = 3ns, T_{PHL} = 4ns (Typ)
  - Output buffer: T_{PLH} = 6ns, T_{PHL} = 8ns (Typ), C_L = .30pF
- Output drive:
  - 6mA for a single output
  - 12mA for parallel output
- I/O level: CMOS, TTL
- Megacells compatible
- Fully migratable to S-MOS standard cell families

■ PRODUCT CONFIGURATION

Array Member	Raw Gates	Usable gates		Total # of Pads
SLA6000		Minimum	Maximum	
SLA6050	513	334	410	48
SLA6080	820	533	656	60
SLA6140	1394	906	1115	74
SLA6170	1746	1135	1396	82
SLA6270	2667	1734	2133	100
SLA6330	3312	2153	2649	110
SLA6430	4342	2822	3473	126
SLA6620	6206	4034	4964	152

Note: All arrays have 6 dedicated input pads included within total pad count.

■ ABSOLUTE MAXIMUM RATINGS

(V_{SS} = 0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	-0.3 to 7.0	V
Input voltage	V_I	-0.3 to V_{DD} +0.3	V
Output voltage	V_O	-0.3 to V_{DD} +0.3	V
Storage temperature	T_{stg}	-65 to 150	°C

■ RECOMMENDED OPERATING CONDITIONS

(V_{SS} = 0V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	—	5.25	5	5.25	V
Operating Temperature	T_{opr}	—	0	—	70	°C

■ ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V ±5%, (V_{SS} = 0V), T_a = 70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply Current	I_{DD}	Standby	—	2	—	μA
High Level Output Voltage	V_{OH}	V_{DD} = 4.75V I_{OH} = –6mA	2.4	—	—	V
Low Level Output Voltage	V_{OL}	V_{DD} = 4.75V I_{OL} = 6mA	—		0.4	V
High Level Input Voltage	V_{IH}	V_{DD} = 5.25V	2.0	—	—	V
Low Level Input Voltage	V_{IL}	V_{DD} = 4.75V	—	—	0.8	V
Input Leakage Current	I_{LI}	—	–1	—	1	μA

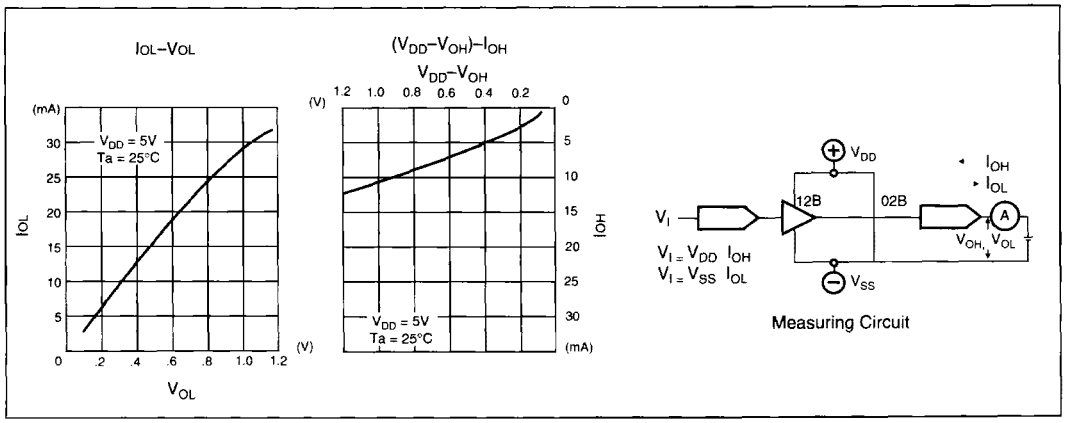
■ PACKAGE MATRIX

Package Type	No. of Pins	Device code	6050	6080	6140	6170	6270	6330	6430	6620
		No. of Pads	48	60	74	82	100	110	126	152
		Gross Gates	513	820	1394	1746	2667	3312	4342	6206
Plastic DIP	14	C14	A							
	18	C18	A*	A						
	22	C22	A							
	24	C24	A*	A*	A*					
	28	C28	A*	A*	A*	A*				
	40	C40	(A)	(A)	(A)	A*	A*			
	42	C42	A*	A*	A*	A*				
Plastic Shrink DIP	64	S64			A*	A*				
Plastic Skinny DIP	24	H24	A							
Plastic QFP	44	F44-6		A*	A*	(A)				
	52	F52-6			A*					
	60	F60-6	(A)	(A)	(A)	A*				
	60	F60-5	A*	A*	A*	(A)	A*	(A)	A*	
	80	F80-5			A*	A*	A*	A*	A*	
	100	F100-5				A*	A*	A*	A*	
Plastic SOP	24	M24-2	A	A						
	28	M28-2	A*	A*	A*					
PLCC	44	J44	A*	A*	A*					
	68	J68			A*	A*	A*	A*	A*	(A)
	84	J84				A*	A*	A*	A*	(A)
Plastic PGA	89	G89							A	
Ceramic PGA	64	P64			A*	A	A			
	72	P72					A	A		
	132	P132					A	A	A	A

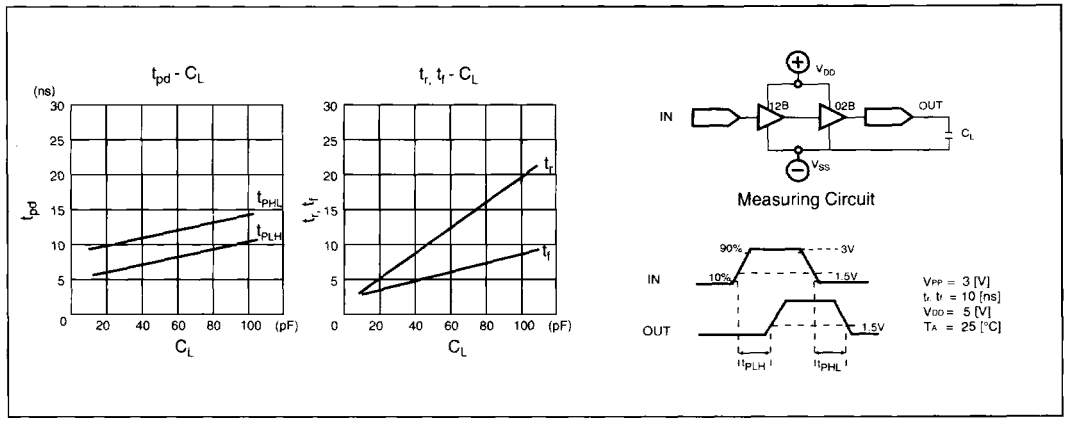
A: Available
*: Pin Pad Table Exists
(A): Lead Frame Currently Not Available
F: Currently Not Available

■ PERFORMANCE CURVES

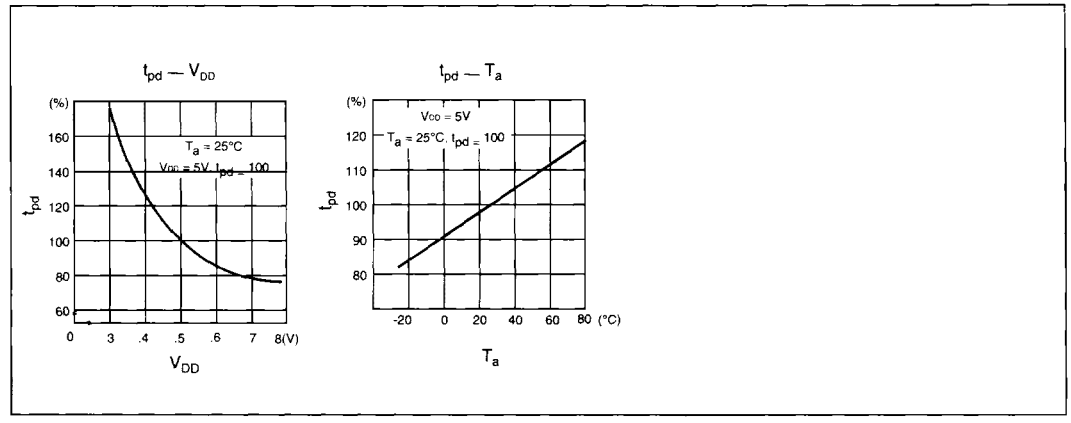
● Output Current



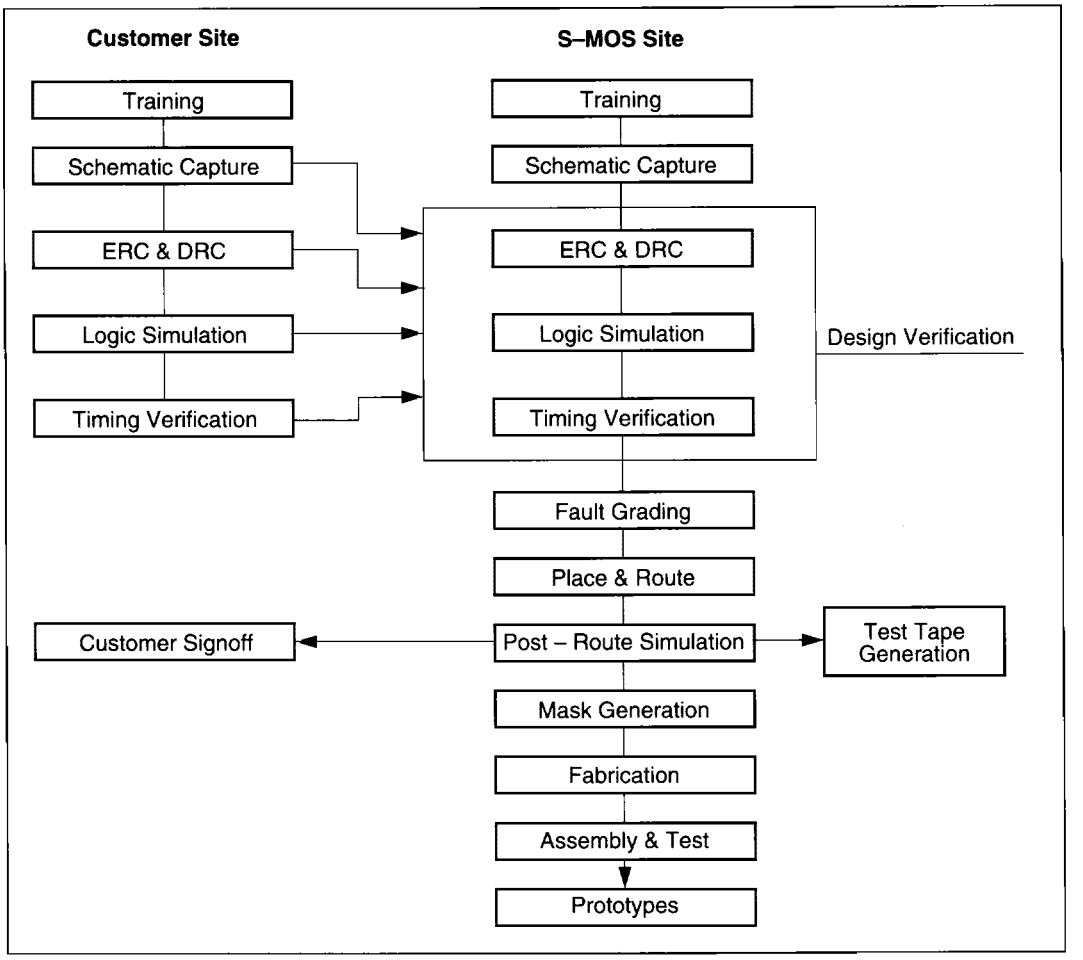
● tpd, tr, tf – CL



● Delay Time



■ **S–MOS Systems ASIC Design Flow**



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