MOTOROLA

4-Bit Decade Counter (with Synchronous Clear)

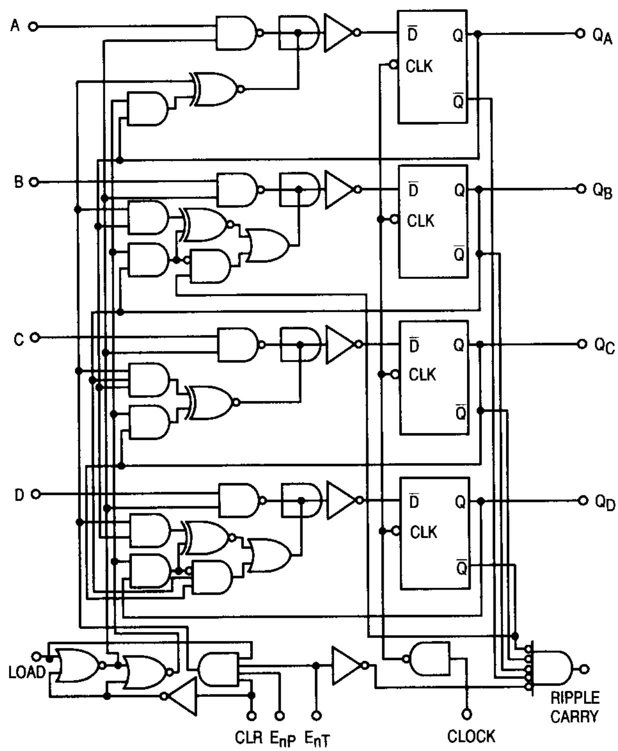
ELECTRICALLY TESTED PER:
MIL-M-38510/31511

The 'LS162A is a high-speed 4-bit synchronous counter. It is edge-triggered, synchronously presettable, and cascadable with MSI building blocks for counting, memory addressing, frequency division and other applications. The 'LS162A can count modulo 10 (BCD).

The 'LS162A has a Synchronous Reset (Clear) input that overrides all other control inputs, but is active only during the rising clock edge.

- Synchronous Counting and Loading
- Two Count Enable Inputs For High-Speed Synchronous Expansion
- Terminal Count Fully Decoded
- Typical Count Rate of 35 MHz

LOGIC DIAGRAM



Military 54LS162A

AVAILABLE AS:

1) JAN: JM38510/31511BXA
2) SMD: N/A
3) 883: 54LS162A/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

THE LETTER "M" APPEARS BEFORE THE / ON LCC.

PIN ASSIGNMENTS

FUNCT.	DIL 620-09	FLATS 650-05	LCC 756A-02	BURN-IN (COND. A)
CLR	1	1	2	V_{CC}
CLK	2	2	3	V_{CC}
A	3	3	4	V_{CC}
B	4	4	5	V_{CC}
C	5	5	7	V_{CC}
D	6	6	8	V_{CC}
E_{nP}	7	7	9	V_{CC}
GND	8	8	10	GND
Ld	9	9	12	V_{CC}
E_{nT}	10	10	13	V_{CC}
Q_D	11	11	14	V_{CC}
Q_C	12	12	15	V_{CC}
Q_B	13	13	17	V_{CC}
Q_A	14	14	18	V_{CC}
RC	15	15	19	V_{CC}
V_{CC}	16	16	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

MODE SELECT TABLE

CLR	Ld	E_{nT}	E_{nP}	Action on the Rising Clock Edge (_⌐)
L	X	X	X	Reset (Clear)
H	L	X	X	Load (D_n-Q_n)
H	H	H	H	Count (Increment)
H	H	L	X	No Change (Hold)
H	H	X	L	No Change (Hold)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

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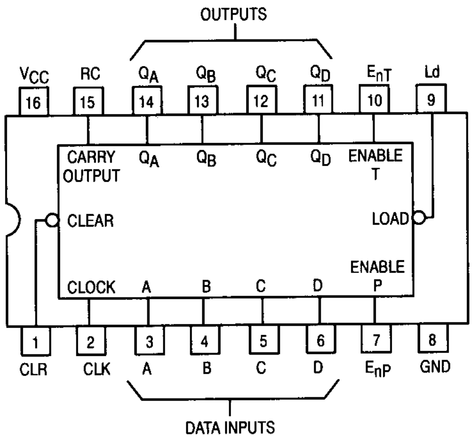
CONNECTION DIAGRAM



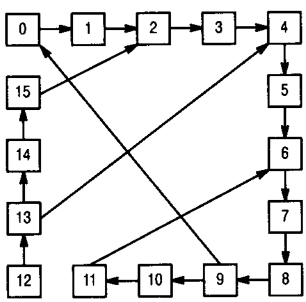
Pin Names		Loading (Note b) HIGH	LOW
Load	Parallel Enable (Active LOW)	1.0 U.L.	0.5 U.L.
A-D	Parallel Inputs (Data Inputs)	0.5 U.L.	0.25 U.L.
E_nP	Count Enable Parallel Input	0.5 U.L.	0.25 U.L.
E_nT	Count Enable Trickle Input	1.0 U.L.	0.5 U.L.
CLK	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
CLR	Master Reset (Active LOW) Input	1.0 U.L.	0.25 U.L.
Q_A-Q_D	Parallel Outputs (Note b)	10 U.L.	5(2.5) U.L.
RC	Terminal Count (Ripple Carry) Output (Note b)	10 U.L.	5(2.5) U.L.

NOTES:

a. One TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.

b. The Output LOW drive factor is 2.5 U.L. for Military (54) Temperature Ranges.

STATE DIAGRAM



LOGIC EQUATIONS

Count Enable = $E_nP \bullet E_nT \bullet Ld$

RC for LS162A = $E_nT \bullet Q_A \bullet \overline{Q_B} \bullet \overline{Q_C} \bullet Q_D$

Preset = $\overline{Ld} \bullet$ CLK + (rising clock edge)

Reset = $\overline{CR} \bullet$ CLK + (rising clock edge)

NOTE:

The LS162A can be preset to any state, but will not count beyond 9. If preset to state 10, 11, 12, 13, 14, or 15, it will return to its normal sequence within two clock pulses.

FUNCTIONAL DESCRIPTION

The 'LS162A is a 4-bit synchronous counter with a synchronous Parallel Enable (Load) feature. The counter consists of four edge-triggered D flip-flops with the appropriate data routing networks feeding the D inputs. All changes of the Q outputs occur as a result of, and synchronous with, the LOW to HIGH transition of the Clock input (CLK). As long as the set-up time requirements are met, there are no special timing or activity constraints on any of the mode control or data inputs.

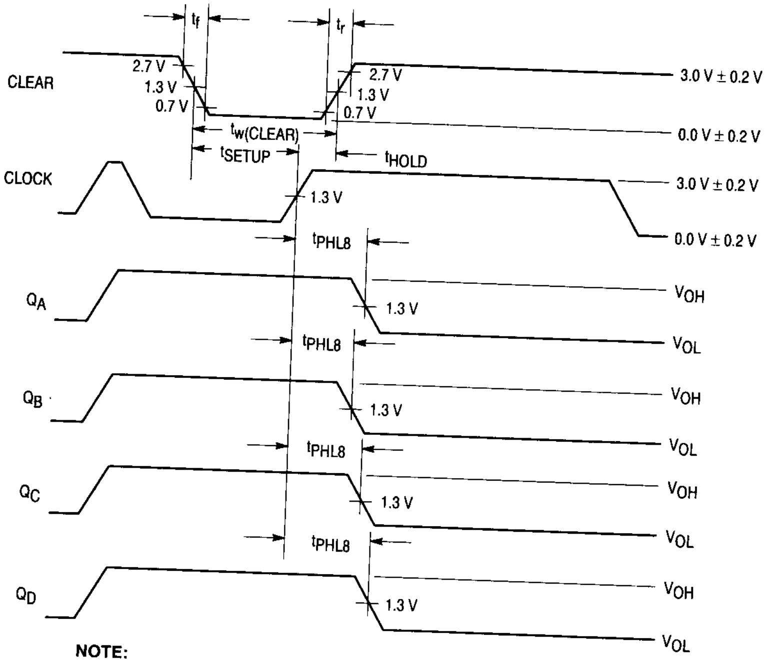
Three control inputs – Parallel Enable (Ld), Count Enable Parallel (E_nP) and Count Enable Trickle (E_nT) – select the mode of operation as shown in the table below. The Count Mode is enabled when the E_nP, E_nT, and $\overline{Ld}$ inputs are HIGH. When the $\overline{Ld}$ is LOW, the counters will synchronously load the data from the parallel inputs into the flip-flops on the LOW to HIGH transition of the clock. Either the E_nP or E_nT can be used to inhibit the count sequence. With the $\overline{Ld}$ held HIGH, a LOW on either the E_nP or E_nT inputs at least one set-up time prior to the LOW to HIGH clock transition will cause the existing output states to be retained The AND feature of the two Count Enable inputs ($E_nP \bullet E_nT$) allows synchronous cascading without external gating and without delay accumulation over any practical number of bits or digits.

The Terminal Count (RC) output is HIGH when the Counter Enable Trickle (E_nT) input is HIGH while the counter is in its maximum count state (HLLH for BCD counters, HHHH for Binary counters). Note that RC is fully decoded and will, therefore, be HIGH only for one count state.

The 'LS162A counts modulo 10 following a binary coded decimal (BCD) sequence. They generate an RC output when the E_nT input is HIGH while the counter is in the state 9 (HLLH). From this state they increment to state 0 (LLLL). If loaded with a code in excess of 9 they return to their legitimate sequence within two counts, as explained in the state diagram. States 10 through 15 do not generate an RC output.

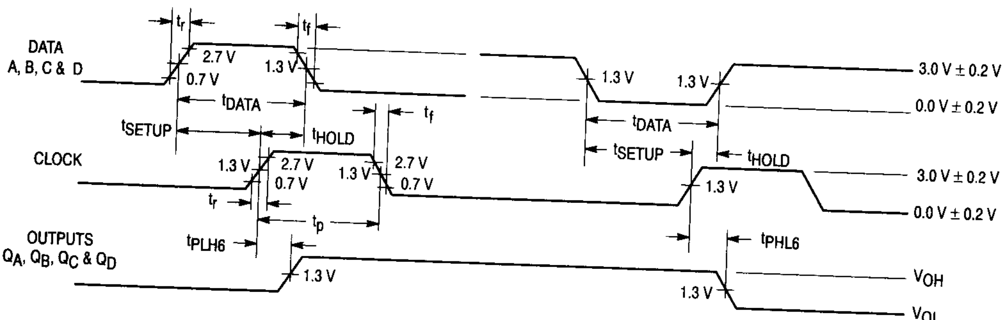
The active LOW Synchronous Reset ($\overline{CR}$) input of the 'LS162A acts as an edge-triggered control input, overriding E_nT, E_nP and $\overline{Ld}$, and resetting the four counter flip-flops on the LOW to HIGH transition of the clock. This simplifies the design from race-free logic controlled reset circuits, e.g., to reset the counter synchronously after reaching a predetermined value.

VOLTAGE WAVEFORM 1



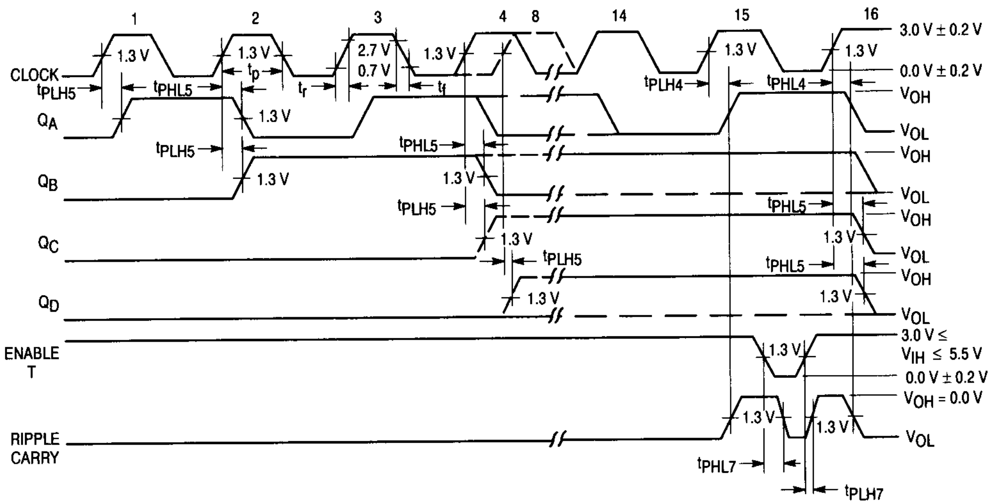
NOTE:
The Clear pulse generator has the following characteristics:
V_{gen} = 3.0 V, $t_r \le 15$ ns, $t_f \le 6.0$ ns, $t_{w(Clear)}$ = 25 ns,
t_{SETUP} = 25 ns, t_{HOLD} = 0 ns.

VOLTAGE WAVEFORM 2

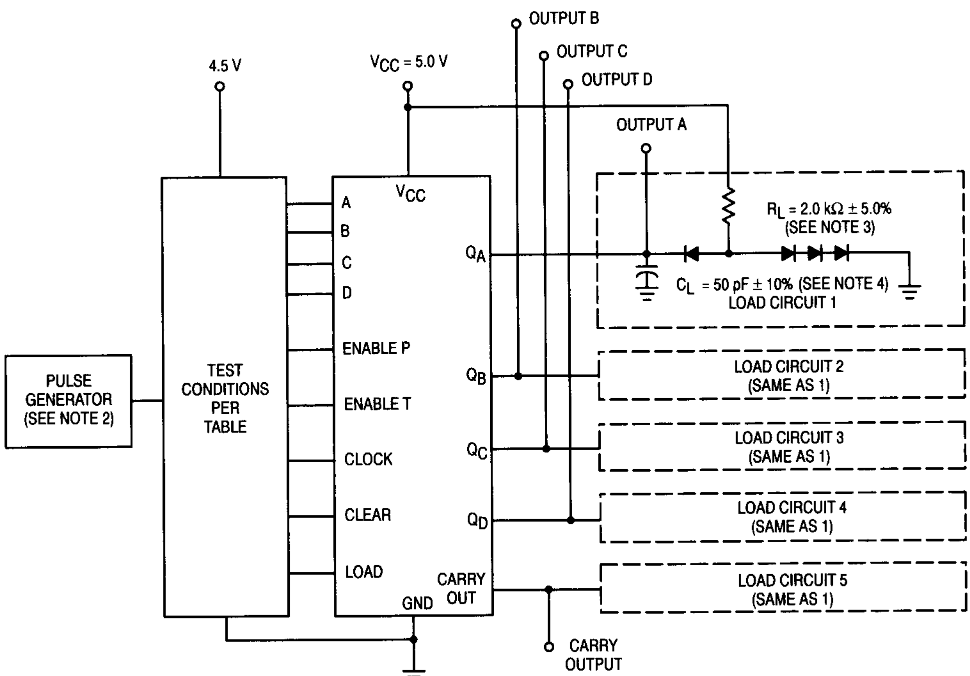


NOTE:
The data pulse generator has the following characteristics:
V_{gen} = 3.0 V, $t_r \le 15$ ns, $t_f \le 6.0$ ns, t_{DATA} = 30 ns, t_{SETUP} = 20 ns,
t_{HOLD} = 10 ns.

VOLTAGE WAVEFORM 3



TEST CIRCUIT



REFERENCE NOTES ON PAGE 5-192

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+25°C		+125°C		−55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V_{CC} = 4.5 V, I_{OH} = −0.4 mA, CR = 4.5 V, E_{nP} = open, CLK = (See Note 7), V_{IH} = 2.0 V, E_{nT} = 2.0 V, Ld = GND.
V_{OL}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V, I_{OL} = 4.0 mA, V_{IL} = 0.7 V, Ld = GND, CLK = (See Note 7), CR = 4.5 V, E_{nP} = open, E_{nT} = 0.7 V.
V_{IC}	Input Clamping Voltage		−1.5					V	V_{CC} = 4.5 V, I_{IN} = −18 mA, other inputs are open.
I_{IH}	Logical "1" Input Current		20		20		20	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, (other inputs are open).
I_{IH}	Logical "1" Input Current		40		40		40	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V (other inputs are open), (CLK, Ld & E_{nT}) are open.
I_{IHH}	Logical "1" Input Current		100		100		100	µA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V (other inputs are open).
I_{IHH}	Logical "1" Input Current		200		200		200	µA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V (other inputs are open), (CLK, Ld & $E_{nP/T}$) = GND or 5.5 V.
I_{IL1}	Logical "0" Input Current	−300	−760	−300	−760	−300	−760	µA	V_{CC} = 5.5 V, V_{IN} = 0.4 V (other inputs are open), (Ld & E_{nP}) = 4.5 V.
I_{IL2}	Logical "0" Input Current	0	−100	0	−100	0	−100	µA	V_{CC} = 5.5 V, V_{IN} = 0.4 V (other inputs are open), Ld = GND.
I_{IL3}	Logical "0" Input Current	−160	−400	−160	−400	−160	−400	µA	V_{CC} = 5.5 V, V_{IN} = 0.4 V (other inputs are open), Ld = 0.4 V.
I_{IL4}	Logical "0" Input Current	−150	−380	−150	−380	−150	−380	µA	V_{CC} = 5.5 V, V_{IN} = 0.4 V, Ld & E_{nT} = 4.5 V, other inputs are open. E_{nP} = 0.4 V.
I_{IL5}	Logical "0" Input Current	−150	−450	−150	−450	−150	−450	µA	V_{CC} = 5.5 V, CLR = 0.4 V (all other inputs are open).
I_{OS}	Output Short Circuit Current	−15	−100	−15	−100	−15	−100	mA	V_{CC} = 5.5 V, V_{IN} = 4.5 V (other inputs are open), Ld = GND, V_{OUT} = GND, CLK = (See Note 7), CR = 4.5 V, $E_{nT/P}$ = open.
I_{CCH}	Power Supply Current Off		31		31		31	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V (all inputs), Ld = 5.5 V or GND.
I_{CCL}	Power Supply Current Off		32		32		32	mA	V_{CC} = 5.5 V, V_{IN} = GND (all inputs), CLK = GND or 5.5 V.
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.7		0.7		0.7	V	V_{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V_{CC} = 5.0 V, V_{INL} = 0.4 V, and V_{INH} = 2.5 V.

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+25°C		+125°C		−55°C			
	Switching Parameters:	Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL4} t_{PHL4}	Propagation Delay /Data-Output CLK to Carry Out	3.0 —	40 35	3.0 —	56 51	3.0 —	56 51	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PLH4} t_{PLH4}	Propagation Delay /Data-Output CLK to Carry Out	3.0 —	40 35	3.0 —	56 51	3.0 —	56 51	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PHL5} t_{PHL5}	Propagation Delay /Data-Output CLK to Q_n	3.0 —	32 27	3.0 —	45 40	3.0 —	45 40	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PLH5} t_{PLH5}	Propagation Delay /Data-Output CLK to Q_n	3.0 —	29 24	3.0 —	41 36	3.0 —	41 36	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PHL6} t_{PHL6}	Propagation Delay /Data-Output CLK to Q_n	3.0 —	32 27	3.0 —	48 43	3.0 —	48 43	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PLH6} t_{PLH6}	Propagation Delay /Data-Output CLK to Q_n	3.0 —	29 24	3.0 —	42 37	3.0 —	42 37	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PHL7} t_{PHL7}	Propagation Delay /Data-Output E_{nT} to Carry Out	3.0 —	19 14	3.0 —	28 23	3.0 —	28 23	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PLH7} t_{PLH7}	Propagation Delay /Data-Output E_{nT} to Carry Out	3.0 —	19 14	3.0 —	28 23	3.0 —	28 23	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PHL8} t_{PHL8}	Propagation Delay /Data-Output CLR to Q_n	3.0 —	33 28	3.0 —	46 41	3.0 —	46 41	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
f_{MAX} f_{MAX}	Maximum Clock Frequency	22 25		22		22		MHz	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.

NOTES:
1. Voltage measurements are made with respect to ground terminal.
2. The pulse generator has the following characteristics:
   V_{GEN} = 3.0 V, t_r = 15 ns, t_f = 6.0 ns, t_p = 0.5 µs, PRR ≤ 1.0 MHz, and $Z_{OUT} \approx 50\ \Omega$.
3. All diodes are 1N3064 or equivalent.
4. C_L = 50 pF ± 10%, including scope probe and jig capacitance.
5. f_{MAX}: $t_r = t_f \leq 6.0$ ns.
6. The limits specified for C_L = 15 pF are guaranteed but not tested.
7. Apply one pulse prior to measurement as follows:


2.5 V min/5.0 V max
0.0 V

or


2.5 V min/5.0 V max
0.0 V