Three Phase Sensorless Fan Driver

FEATURES AND BENEFITS

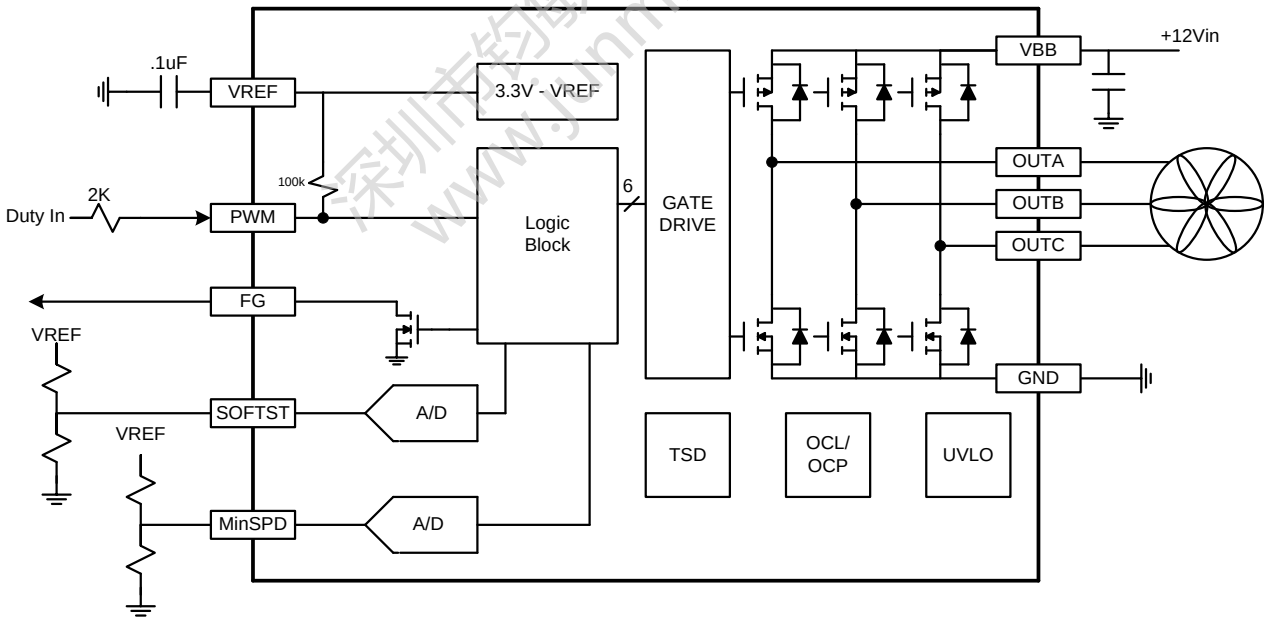
- Sinusoidal Drive For Low Audible Noise
- Minimum Speed Function
- Quiet StartUp Adjustment Feature
- High Efficiency Control Algorithm
- Sensorless Operation
- PWM Speed Input
- FG Speed Output
- Lock Detection
- Short Circuit Protection (OCP)
- Overcurrent Limit (OCL)

DESCRIPTION

The A5940 three phase motor drivers incorporate sinusoidal drive to minimize audible noise and vibration for medium power fans.

A PWM Input is provided to control motor speed.

The A5940 is available in a 3x3 10L DFN with exposed power pad, (suffix EJ), a 10L SOIC (suffix LN), and a 10 lead SOIC with exposed pad (suffix LK).



Typical Application

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Supply Voltage	V_{BB}				18	V
Input Voltage Range	V_{IN}	VSP/PWM	-.3		VBB	V
Logic Output - FG	Vo	FG (I<5mA)			18	V
Output Current	IO				I_{OCL}	A
Output Voltage	Vout	OUTA,OUTB,OUTC	-1		VBB+1	V
Junction Temperature	Tj				150	°C
Storage Temperature Range	Ts		-55		150	°C
Operating Temperature Range	Ta		-40		105	°C
Package Thermal Resistance						
EJ Package	Rja	2 sided PCB 1 in^2 Copper		60		°C/W
LN Package		Single sided PCB		130		
LK Package		2 sided PCB 1 in^2 Copper		40		

TERMINAL LIST

Pin Name	Pin Description	Num
PWM	Logic Input – Speed	1
FG	Speed Output Signal	2
VBB	Input Supply	3
OUTA	Motor Terminal	4
OUTB	Motor Terminal	5
GND	Ground	6
OUTC	Motor Terminal	7
VREF	Analog Output	8
MINSPD	Analog Input	9
SOFTST	Analog Input	10

ELECTRICAL CHARACTERISTICS VBB = 4V to 18V (unless noted otherwise)

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
VBB Supply Current	I_{BB}	PWM=LOW		8	10	mA
Total Driver Rdson (Sink + Source)	R_{DSON}	I = 1A, Tj=25C, VBB=12V		1.15	1.45	Ω
		Source Driver	650	850	1200	mΩ
		Sink Driver	200	300	450	mΩ
		I = 1A, Tj=25C, VBB=4V		1.5	1.9	Ω
VREF	V_{REF}	I_{OUT}=5mA	3.2	3.3	3.4	V
Input Pullup Resistance (PWM)	R_{PU}	PWM	70	100	130	KΩ
Logic Input Low Level	V_{IL}	PWM			.8	V
Logic Input High Level	V_{IH}		2			V
Logic Input Hysteresis	V_{HYS}		200	300	600	mv
Output Sat Voltage	V_{SAT}	I=5mA			.3	V
FG Output Leakage	I_{FG}	V=18V, FG switch OFF			1	µA
Motor Function						
PWM Duty On Threshold	DC_{ON}		8.7	9	9.3	%
PWM Duty OFF Threshold	DC_{OFF}		7.3	7.6	7.9	%
PWM Input Frequency Range	F_{PWM}		.1		100	Khz
Motor PWM Frequency	f_{PWM}		21	24.4	28.8	Khz
MIN Speed Selection		Relative to target	.5		.5	%
Input Current (MINSPD, SOFTST)	I_{IN}	VIN=0 to 5.5V	-1	0	1	µA
Protection						
VBB UVLO	VBB_{UVLO}	VBB rising		3.75	3.95	V
VBB UVLO HYS	VBB_{HYS}		150	300	450	mV
OverCurrent Limit	I_{OCL}			1.55		A
Lock Timing	t_{OFF}		4.5	5	5.5	S
Thermal Shutdown Temp.	T_{JTSD}	Temperature increasing.	150	165	180	°C
Thermal Shutdown Hysteresis	ΔT_J	Recovery = T_{JTSD} - ΔT_J		20		°C

1. Specified limits are tested at a single temperature and assured over operating temperature range by design and characterization.

Functional Description

The A5940 targets fan applications to meet the objectives of low audible noise, minimal vibration, and high efficiency. Allegro's proprietary control algorithm results in a sinusoidal current waveshape that adapts to a variety of motor characteristics to dynamically optimize efficiency across a wide range of speeds.

The speed of the fan is controlled by variable duty cycle PWM input.

The PWM input duty is measured and converted to a 9bit number. This 9 bit "demand" is applied to a pwm generator block to create the modulation profile. The modulation profile is applied to the three motor outputs, with 120 degree phase relationship, to create the sinusoidal current waveform as shown in Figure 1.

A bemf detection "window" is opened on phase A modulation profile in order to measure the rotor position so as to define the modulation timing. The control system maintains the window to a small level in order to minimize the disturbance and approximate the ideal sinusoidal current waveform as much as possible.

Protection features include lock detection with restart, motor output short circuit, supply undervoltage monitor and thermal shutdown.

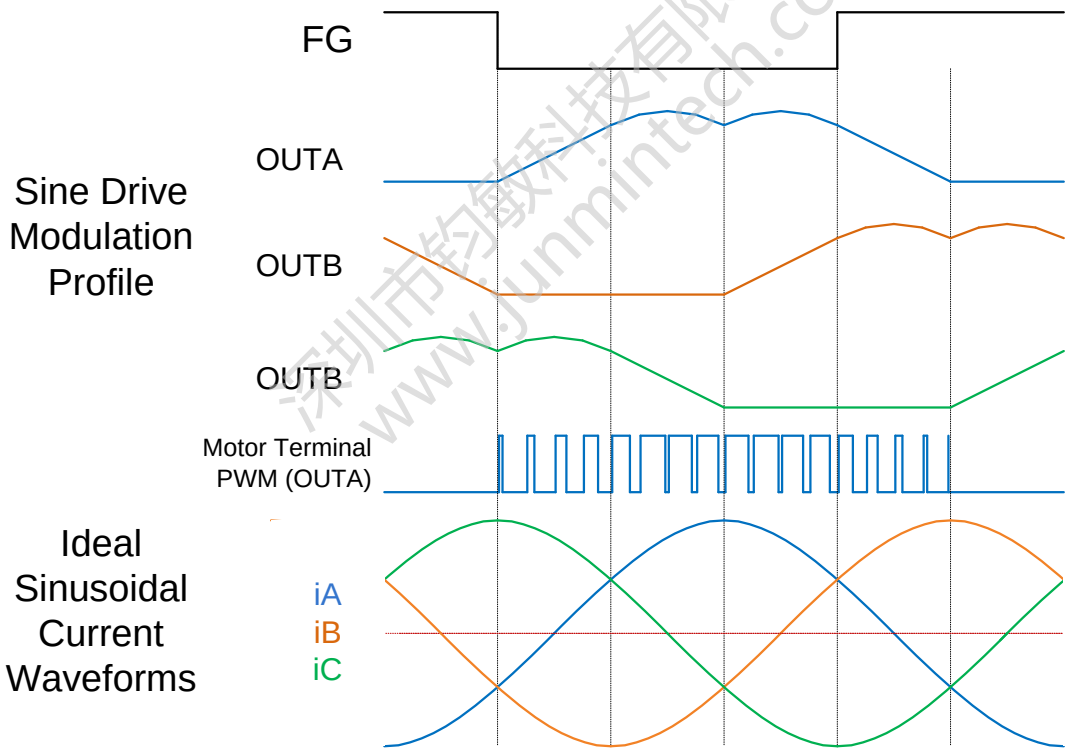


Figure 1: Sinusoidal PWM

Speed Control.

PWM – Duty Cycle Input. A duty cycle measurement circuit converts the applied duty to a demand value (9 bit resolution) to control speed of the fan.

The motor drive will be enabled if duty is larger than DC_ON The PWM input is filtered to prevent spurious noise from turning on or off unexpectedly.

There is an internal pullup (100K) that will turn motor on to maximum speed if input signal is disconnected.

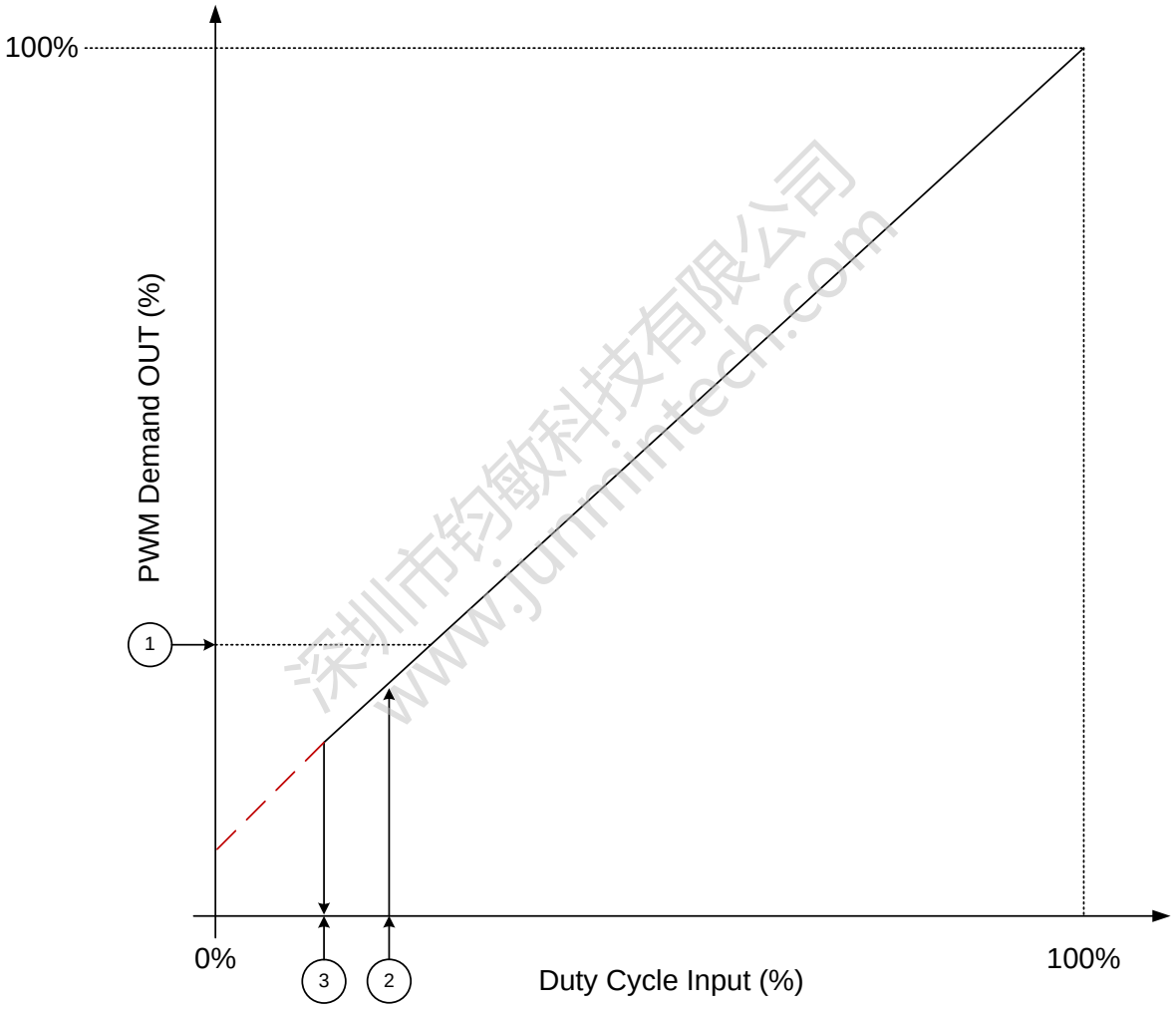


Figure 1) Speed Input Characteristic

Lock Detect. Speed is monitored to determine if rotor is locked. If a lock condition is detected, the IC will be disabled for T_{OFF} before an auto-restart is attempted.

FG. Open drain output provides speed information to the system. FG changes state one period per electrical revolution of the motor (as shown in Figure 1).

Min Speed Function. Connecting a resistor divider to VREF sets a voltage that is translated to a minimum speed clamp integer by a 4 bit A/D. Connect MINSPD to GND to turn motor off with low (< DC_{OFF}) duty applied.

A resistor divider in range 50K to 100K is recommended.

V_{MINSPD}	Code	Demand %	V_{MINSPD}	Code	Demand %
0	0	0	1.6	126	24.7
.2	51	10.0	1.8	137	26.8
.4	62	12.1	2.0	148	29
.6	73	14.3	2.2	159	31.1
.8	82	16.0	2.4	170	33.3
1	93	18.2	2.6	181	35.4
1.2	104	20.3	2.8	192	37.6
1.4	115	22.5	VREF	203	39.7

Quiet Startup Operation. The A5940 achieves quiet startup with the following sequence:

1) Slowly ramp PWM duty from zero to a chosen Open loop Demand level by stepping motor with a waveshaped sine drive modulation profile.
2) After the fixed open loop Time, the motor position is measured, an initial demand value applied, and slowly the demand is ramped to the final value which is calculated by the duty cycle measurement circuit.

StartUp Adjustment.

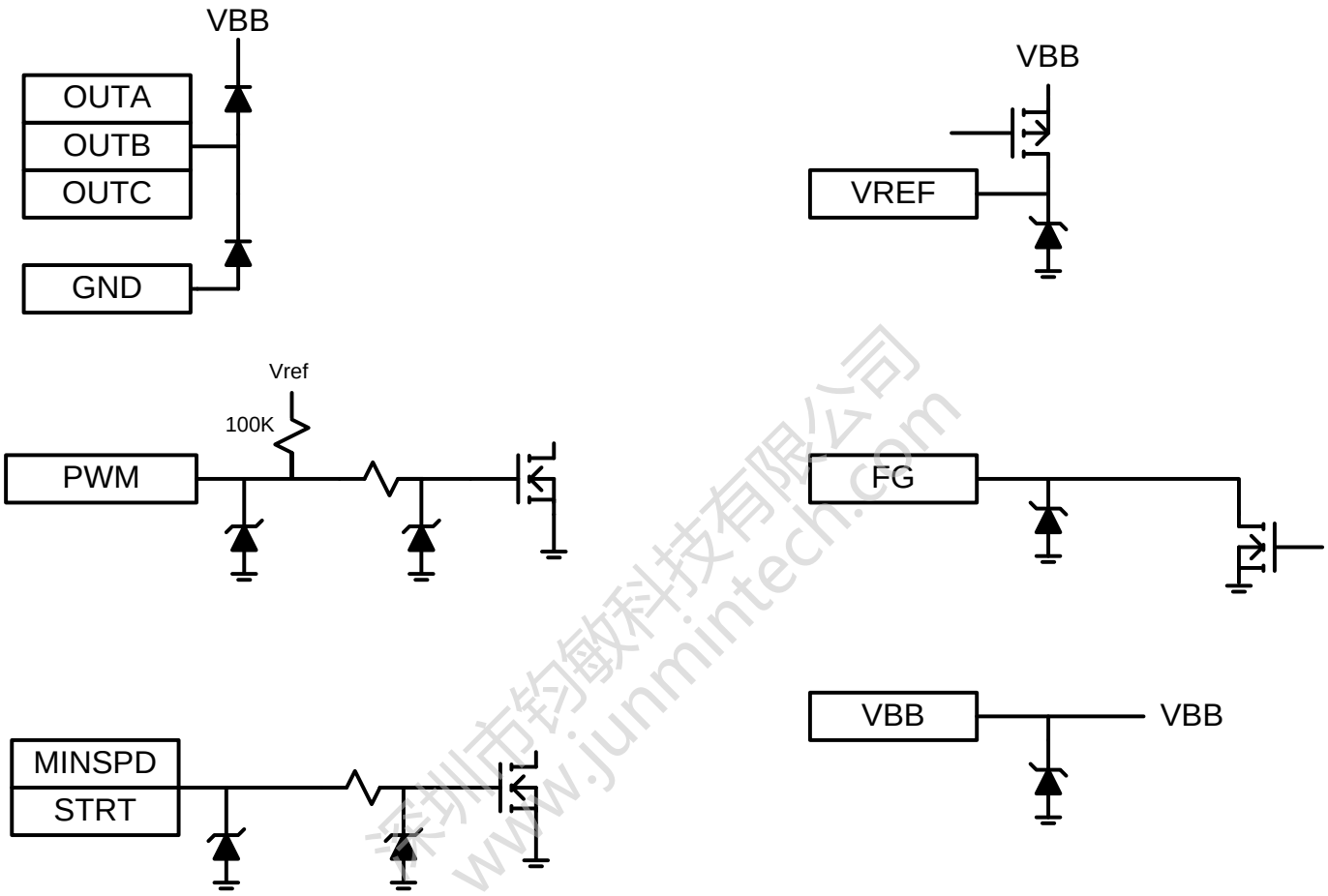
Various permutations of startup parameters are chosen via lookup table with A/D conversion.
16 choices of startup parameters are selected by applying voltage at pin SOFTST.

A resistor divider in range 50K to 100K is recommended.

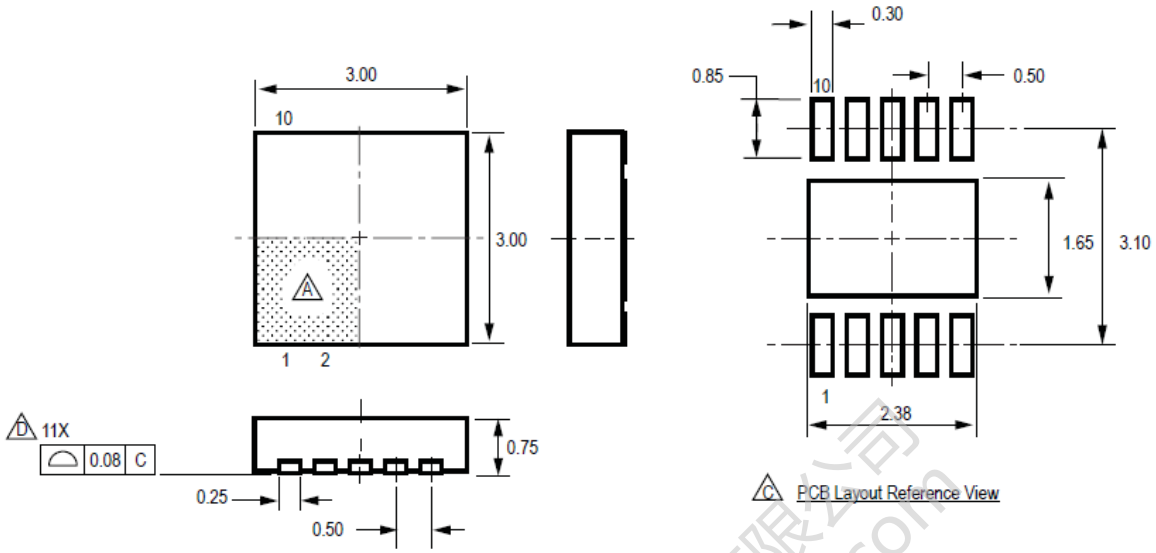
The various selections have different choices for open loop duration, open loop demand, and initial demand value of soft start after the open loop startup period.

V_{SOFTST}	Selection	Open Loop TIme (S)	Open Loop Demand (%)	Initial Soft Start Demand (%)
GND	0	1.1	22	12
.2	1	1.1	9	7
.4	2	1.1	22	12
.6	3	1.1	30	12
.8	4	1.1	41	16
1	5	1.1	54	12
1.2	6	1.1	54	25
1.4	7	1.1	64	12
1.6	8	1.1	80	25
1.8	9	1.1	98	12
2	10	1.9	30	16
2.2	11	1.9	41	25
2.4	12	1.9	61	39
2.6	13	1.9	78	39
2.8	14	1.9	99	50
VREF	15	1.9	65	25

Pin Diagrams



EJ Package 10L DFN



All dimensions nominal, not for tooling use
(reference JEDEC MO-229WEED)
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown

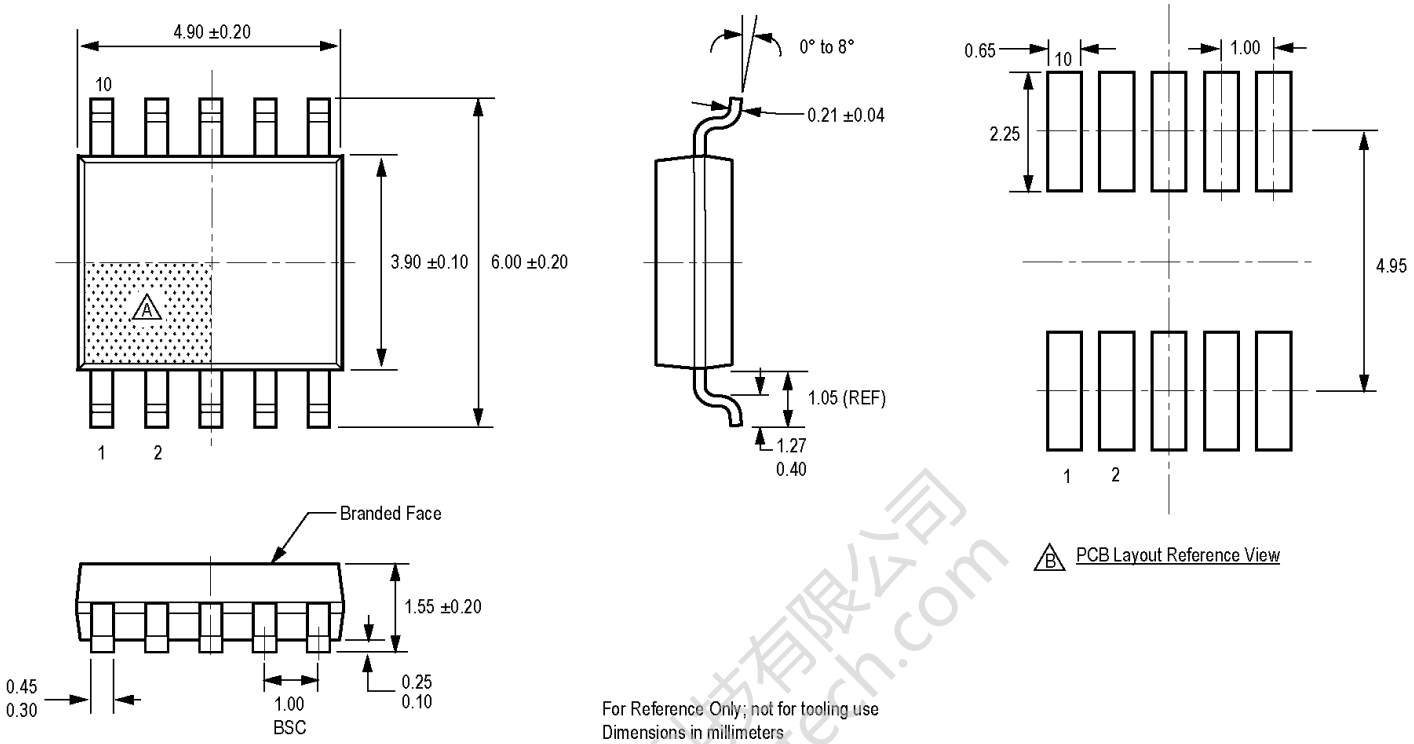
A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 SON50P300X300X80-11WEED3M); All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

LN Package 10L SSOP

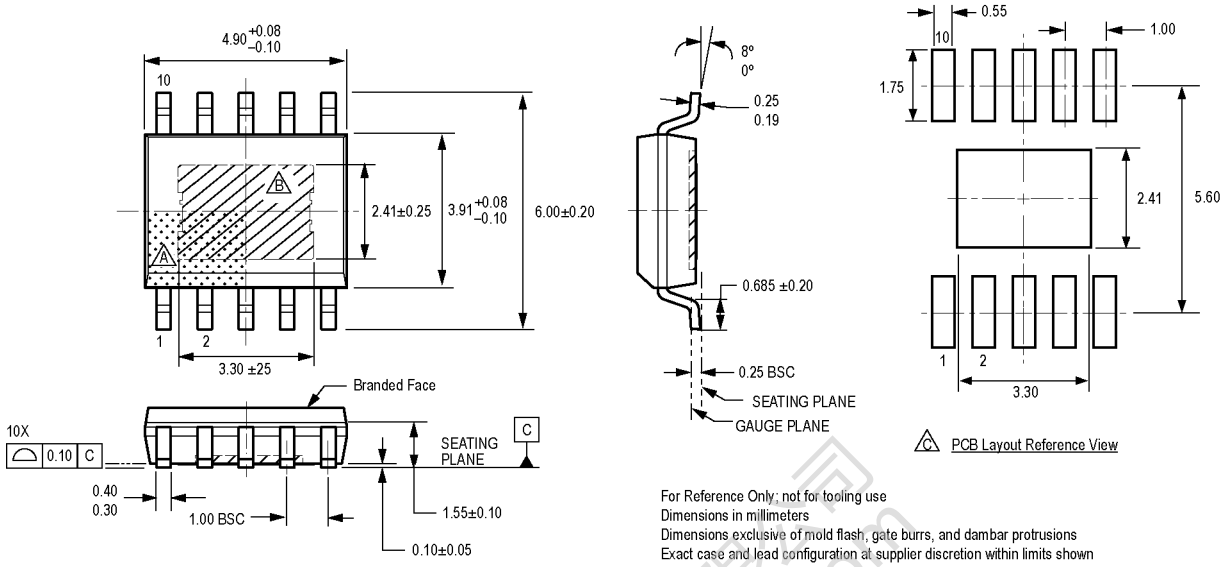


For Reference Only; not for tooling use
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Reference land pattern layout. All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias near the pin lands can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-7)

LK Package Exposed pad 10L eSOIC



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Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (bottom surface)

C Reference land pattern layout; all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)