DRAM

NEC	ISSI
uPD4504161	IS42S16128
uPD4811650	IS42G32256

NPNX	ISSI
NN514265A	IS41C16256
NN514260A	IS41C16257
NN51V4265A	IS41LV16256
NN51V4260A	IS41LV16257
NN5118165A/B	IS41C16100
NN5118160A/B	IS41C16105
NN51V18165B	IS41LV16100
NN51V18160B	IS41LV16105
NN5117405B	IS41C44002
NN5116405B	IS41C44004
NN5117400B	IS41C44052
NN5116400B	IS41C44054
NN51V17405B	IS41LV44002
NN51V17400B	IS41LV44052
NN5216165/A	IS42S16100

OKI	ISSI
MSM5416258A	IS41C16256
MSM5416260A	IS41C16257
MSM54V16258A	IS41LV16256
MSM54V16260A	IS41LV16257
MSM5118165B	IS41C16100
MSM5118160B	IS41C16105
MSM51V18165D	IS41LV16100
MSM51V16160B	IS41LV16105
MSM5117405C	IS41C44002
MSM5116405C	IS41C44004
MSM5117400C	IS41C44052
MSM5116400C	IS41C44054
MSM51V17405D	IS41LV44002
MSM51V16405D	IS41LV44004
MSM51V17400B	IS41LV44052
MSM51V16400B	IS41LV44054
MSM56V16160	IS42S16100
MSM54V25632	IS42G32256
MSM5416258	IS41C16256
MSM5416258	IS41C16256
MSM514260	IS41C16257
MSM54V32256	IS41LV32256
MSM54V25632	IS42G32256

PANASONIC	ISSI
MN4118165A	IS41C16100
MN4118160A	IS41C16105
MN41V18165A	IS41LV16100
MN41V18160A	IS41LV16105
MN4117405A	IS41C44002
MN4116405A	IS41C44004
MN4117400A	IS41C44052
MN4116400A	IS41C44054
MN4V117405A	IS41LV44002

PANASONIC	ISSI
MN4V116405A	IS41LV44004
MN4V117400A	IS41LV44052
MN4V116400A	IS41LV44054

SAMSUNG	ISSI
KM416C254D	IS41C16256
KM416C256D	IS41C16257
KM416V254D	IS41LV16256
KM416V254D	IS41LV16257
KM416C1204C	IS41C16100
KM416C1200C	IS41C16105
KM416V1204C	IS41LV16100
KM416V1200C	IS41LV16105
KM44C4104C	IS41C44002
KM44C4004C	IS41C44004
KM44C4100C	IS41C44052
KM44C4400C	IS41C44054
KM44V4104C	IS41LV44002
KM44V4004C	IS41LV44004
KM44V4100C	IS41LV44052
KM44V4400C	IS41LV44054
KM416S1120D	IS42S16100
KM4132G512	IS42G32256
KM432S2030C	IS42S32200
KM416C254D	IS41C16256
KM416V254D	IS41LV16256
KM416C256	IS41C16257
KM4132G512	IS42G32256

SIEMENS	ISSI
HYB514175B	IS41C16256
HYB514171B	IS41C16257
HYB314175B	IS41LV16256
HYB314171B	IS41LV16257
HYB5118165B	IS41C16100
HYB5118160B	IS41C16105
HYB3118165B	IS41LV16100
HYB3118160B	IS41LV16105
HYB5117405B	IS41C44002
HYB5116405B	IS41C44004
HYB5117400B	IS41C44052
HYB5116400B	IS41C44054
HYB3117405B	IS41LV44002
HYB3116405B	IS41LV44004
HYB3117400B	IS41LV44052
HYB3116400B	IS41LV44054
HYB39S16160C	IS42S16100
HYB39S16320	IS42G32256

SILICON MAGIC	ISSI
SM81C256K16C	IS41C16256
SM81L256K32	IS41LV32256
SM84L512K32	IS42G32256
SM81C256K16	IS41C16256

SILICON MAGIC	ISSI
SM81C256K16	IS41C16256
SM81L256K16	IS41LV16256
SM81C256K32	IS41LV32256
SM84L512K32	IS42G32256

TOSHIBA	ISSI
TC514265	IS41C16256
TC514V265	IS41LV16256
TC514260	IS41C16257
TC59G1631	IS42G32256
TC514265D	IS41C16256
TC514260D	IS41C16257
TC51V4265D	IS41LV16256
TC51V4260D	IS41LV16257
TC5118164C	IS41C16100
TC5118160C	IS41C16105
TC51V18164C	IS41LV16100
TC51V18160C	IS41LV16105
TC5117405C	IS41C44002
TC5116405C	IS41C44004
TC5117400C	IS41C44052
TC5116400C	IS41C44054
TC51V17405C	IS41LV44002
TC51V16405C	IS41LV44004
TC51V17400C	IS41LV44052
TC51V16400C	IS41LV44054
TC59S1616A	IS42S16100
TC59G1631	IS42G32256
TC59S6432	IS42S32200

VANGUARD	ISSI
VG2618165C	IS41C16100
VG2618160C	IS41C16105
VG26V18165C	IS41LV16100
VG26V18160C	IS41LV16105
VG2617405E	IS41C44002
VG2617400D	IS41C44052
VG26V17405E	IS41LV44002
VG26V17400D	IS41LV44052
VG3617161A	IS42S16100

IS41C4400x
IS41LV4400x SERIES

ISSI®

4M x 4 (16-MBIT) DYNAMIC RAM WITH EDO PAGE MODE

JUNE, 2001

FEATURES

- Extended Data-Out (EDO) Page Mode access cycle
- TTL compatible inputs and outputs
- Refresh Interval:
  – 2,048 cycles/32 ms
  – 4,096 cycles/64 ms
- Refresh Mode: $\overline{RAS}$-Only,
  $\overline{CAS}$-before-$\overline{RAS}$ (CBR), and Hidden
- Single power supply:
  – 5V±10% or 3.3V ± 10%
- Byte Write and Byte Read operation via two $\overline{CAS}$
- Industrial temperature range -40°C to 85°C

DESCRIPTION

The *ISSI* 4400 Series is a 4,194,304 x 4-bit high-performance CMOS Dynamic Random Access Memory. These devices offer an accelerated cycle access called EDO Page Mode. EDO Page Mode allows 2,048 or 4096 random accesses within a single row with access cycle time as short as 20 ns per 4-bit word.

These features make the 4400 Series ideally suited for high-bandwidth graphics, digital signal processing, high-performance computing systems, and peripheral applications.

The 4400 Series is packaged in a 24-pin 300-mil SOJ with JEDEC standard pinouts.

PRODUCT SERIES OVERVIEW

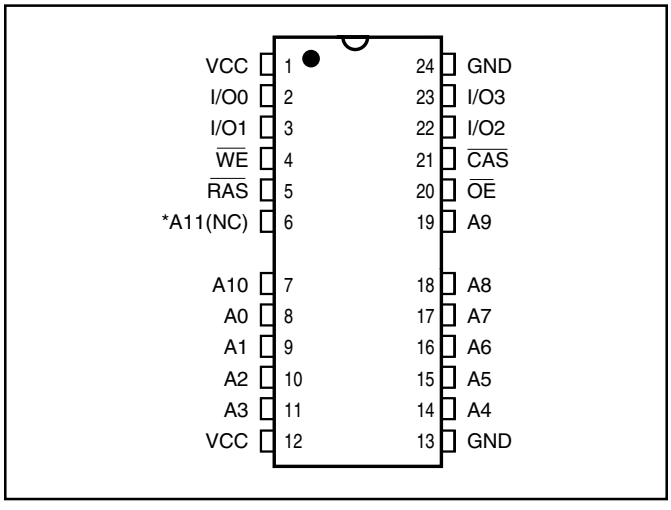
Part No.	Refresh	Voltage
IS41C44002	2K	5V ± 10%
IS41C44004	4K	5V ± 10%
IS41LV44002	2K	3.3V ± 10%
IS41LV44004	4K	3.3V ± 10%

KEY TIMING PARAMETERS

Parameter	-50	-60	Unit
RAS Access Time (t_{RAC})	50	60	ns
$\overline{CAS}$ Access Time (t_{CAC})	13	15	ns
Column Address Access Time (t_{AA})	25	30	ns
EDO Page Mode Cycle Time (t_{PC})	20	25	ns
Read/Write Cycle Time (t_{RC})	84	104	ns

PIN CONFIGURATION

24 Pin SOJ

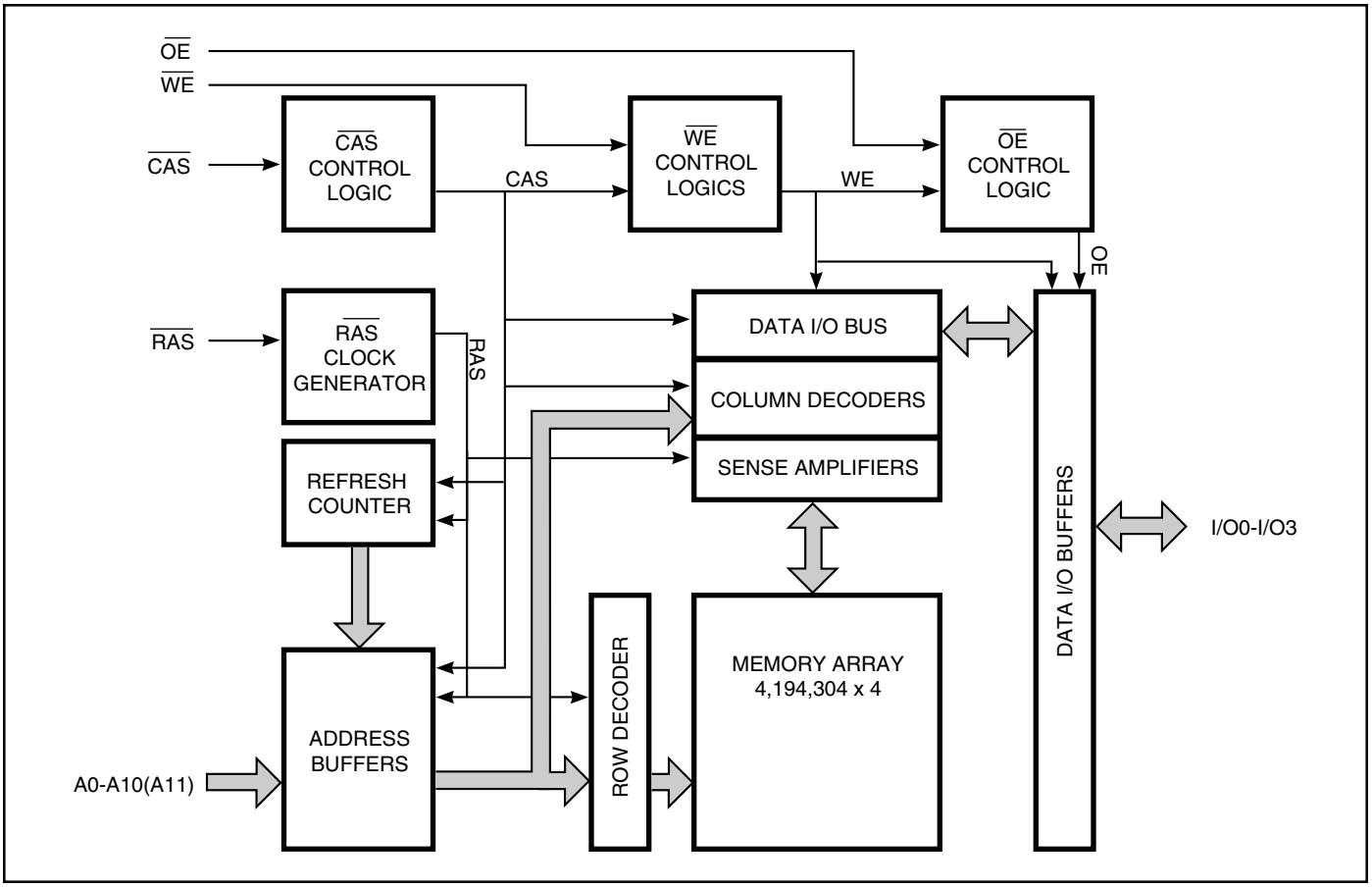


* A11 is NC for 2K Refresh devices.

PIN DESCRIPTIONS

A0-A11	Address Inputs (4K Refresh)
A0-A10	Address Inputs (2K Refresh)
I/O0-3	Data Inputs/Outputs
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
Vcc	Power
GND	Ground
NC	No Connection

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

Function		RAS	CAS	WE	OE	Address tR/tC	I/O
Standby		H	H	X	X	X	High-Z
Read		L	L	H	L	ROW/COL	DOUT
Write: Word (Early Write)		L	L	L	X	ROW/COL	DIN
Read-Write		L	L	H→L	L→H	ROW/COL	DOUT, DIN
EDO Page-Mode Read	1st Cycle:	L	H→L	H	L	ROW/COL	DOUT
	2nd Cycle:	L	H→L	H	L	NA/COL	DOUT
EDO Page-Mode Write	1st Cycle:	L	H→L	L	X	ROW/COL	DIN
	2nd Cycle:	L	H→L	L	X	NA/COL	DIN
EDO Page-Mode Read-Write	1st Cycle:	L	H→L	H→L	L→H	ROW/COL	DOUT, DIN
	2nd Cycle:	L	H→L	H→L	L→H	NA/COL	DOUT, DIN
Hidden Refresh	Read	L→H→L	L	H	L	ROW/COL	DOUT
	Write(1)	L→H→L	L	L	X	ROW/COL	DOUT
RAS-Only Refresh		L	H	X	X	ROW/NA	High-Z
CBR Refresh		H→L	L	X	X	X	High-Z

Note:
1. EARLY WRITE only.

Functional Description

The IS41C4400x and IS41LV4400x are CMOS DRAMs optimized for high-speed bandwidth, low power applications. During READ or WRITE cycles, each bit is uniquely addressed through the 11 or 12 address bits. These are entered 11 bits (A0-A10) at a time for the 2K refresh device or 12 bits (A0-A11) at a time for the 4K refresh device. The row address is latched by the Row Address Strobe ($\overline{RAS}$). The column address is latched by the Column Address Strobe ($\overline{CAS}$). $\overline{RAS}$ is used to latch the first nine bits and $\overline{CAS}$ is used the latter ten bits.

Memory Cycle

A memory cycle is initiated by bring $\overline{RAS}$ LOW and it is terminated by returning both $\overline{RAS}$ and $\overline{CAS}$ HIGH. To ensures proper device operation and data integrity any memory cycle, once initiated, must not be ended or aborted before the minimum t_{RAS} time has expired. A new cycle must not be initiated until the minimum precharge time t_{RP}, t_{CP} has elapsed.

Read Cycle

A read cycle is initiated by the falling edge of $\overline{CAS}$ or $\overline{OE}$, whichever occurs last, while holding $\overline{WE}$ HIGH. The column address must be held for a minimum time specified by t_{AR}. Data Out becomes valid only when t_{RAC}, t_{AA}, t_{CAC} and t_{OEA} are all satisfied. As a result, the access time is dependent on the timing relationships between these parameters.

Write Cycle

A write cycle is initiated by the falling edge of $\overline{CAS}$ and $\overline{WE}$, whichever occurs last. The input data must be valid at or before the falling edge of $\overline{CAS}$ or $\overline{WE}$, whichever occurs last.

Auto Refresh Cycle

To retain data, 2,048 refresh cycles are required in each 32 ms period, or 4,096 refresh cycles are required in each 64ms period. There are two ways to refresh the memory:

1. By clocking each of the 2,048 row addresses (A0 through A10) or 4096 row addresses (A0 through A11) with RAS at least once every 32 ms or 64ms respectively. Any read, write, read-modify-write or RAS-only cycle refreshes the addressed row.
2. Using a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle. $\overline{CAS}$-before-$\overline{RAS}$ refresh is activated by the falling edge of $\overline{RAS}$, while holding $\overline{CAS}$ LOW. In $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle, an internal 9-bit counter provides the row addresses and the external address inputs are ignored.

$\overline{CAS}$-before-$\overline{RAS}$ is a refresh-only mode and no data access or device selection is allowed. Thus, the output remains in the High-Z state during the cycle.

Power-On

After application of the V_{CC} supply, an initial pause of 200 µs is required followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ signal).

During power-on, it is recommended that $\overline{RAS}$ track with V_{CC} or be held at a valid V_{IH} to avoid current surges.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameters		Rating	Unit
V_T	Voltage on Any Pin Relative to GND	5V 3.3V	–1.0 to +7.0 –0.5 to +4.6	V
V_{CC}	Supply Voltage	5V 3.3V	–1.0 to +7.0 –0.5 to +4.6	V
I_{OUT}	Output Current		50	mA
P_D	Power Dissipation		1	W
T_A	Commercial Operation Temperature Industrial Operation Temperature		0 to +70 -40 to +85	°C
T_{STG}	Storage Temperature		–55 to +125	°C

Note:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages are referenced to GND.)

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	5V 3.3V	4.5 3.0	5.0 3.3	5.5 3.6	V
V_{IH}	Input High Voltage	5V 3.3V	2.4 2.0	— —	V_{CC} + 1.0 V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	5V 3.3V	–1.0 –0.3	— —	0.8 0.8	V
T_A	Commercial Ambient Temperature Industrial Ambient Temperature		0 -40	— —	70 85	°C °C

CAPACITANCE(1,2)

Symbol	Parameter	Max.	Unit
C_{IN1}	Input Capacitance: A0-A10(A11)	5	pF
C_{IN2}	Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	7	pF
C_{IO}	Data Input/Output Capacitance: I/O0-I/O3	7	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz.

ELECTRICAL CHARACTERISTICS[1]

(Recommended Operating Conditions unless otherwise noted.)

Symbol	Parameter	Test Condition	Vcc	Speed	Min.	Max.	Unit
I_{IL}	Input Leakage Current	Any input 0V ≤ V_{IN} ≤ Vcc Other inputs not under test = 0V			–5	5	µA
I_{IO}	Output Leakage Current	Output is disabled (Hi-Z) 0V ≤ V_{OUT} ≤ Vcc			–5	5	µA
V_{OH}	Output High Voltage Level	I_{OH} = –5.0 mA, Vcc = 5V I_{OH} = –2.0 mA, Vcc = 3.3V			2.4	—	V
V_{OL}	Output Low Voltage Level	I_{OL} = 4.2 mA, Vcc = 5V I_{OL} = 2 mA, Vcc = 3.3V			—	0.4	V
$I_{CC}1$	Standby Current: TTL	$\overline{RAS}$, $\overline{CAS}$ ≥ V_{IH} Commercial	5V		—	2	mA
			3.3V		—	0.5	
		Industrial	5V		—	3	
			3.3V		—	2	
$I_{CC}2$	Standby Current: CMOS	$\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2V	5V		—	1	mA
			3.3V		—	0.5	
$I_{CC}3$	Operating Current: Random Read/Write[2,3,4] Average Power Supply Current	$\overline{RAS}$, $\overline{CAS}$, Address Cycling, t_{RC} = t_{RC} (min.)		-50 -60	— —	120 110	mA
$I_{CC}4$	Operating Current: EDO Page Mode[2,3,4] Average Power Supply Current	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Cycling t_{PC} = t_{PC} (min.)		-50 -60	— —	90 80	mA
$I_{CC}5$	Refresh Current: $\overline{RAS}$-Only[2,3] Average Power Supply Current	$\overline{RAS}$ Cycling, $\overline{CAS}$ ≥ V_{IH} t_{RC} = t_{RC} (min.)		-50 -60	— —	120 110	mA
$I_{CC}6$	Refresh Current: CBR[2,3,5] Average Power Supply Current	$\overline{RAS}$, $\overline{CAS}$ Cycling t_{RC} = t_{RC} (min.)		-50 -60	— —	120 110	mA

Notes:
1. An initial pause of 200 µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-Only or CBR) before proper device operation is assured. The eight $\overline{RAS}$ cycles wake-up should be repeated any time the t_{REF} refresh requirement is exceeded.
2. Dependent on cycle rates.
3. Specified values are obtained with minimum cycle time and the output open.
4. Column-address is changed once each EDO page cycle.
5. Enables on-chip refresh and address counters.

AC CHARACTERISTICS[1,2,3,4,5,6]

(Recommended Operating Conditions unless otherwise noted.)

Symbol	Parameter	-50 Min.	-50 Max.	-60 Min.	-60 Max.	Units
t_{RC}	Random READ or WRITE Cycle Time	84	—	104	—	ns
t_{RAC}	Access Time from $\overline{RAS}$[6, 7]	—	50	—	60	ns
t_{CAC}	Access Time from $\overline{CAS}$[6, 8, 15]	—	13	—	15	ns
t_{AA}	Access Time from Column-Address[6]	—	25	—	30	ns
t_{RAS}	$\overline{RAS}$ Pulse Width	50	10K	60	10K	ns
t_{RP}	$\overline{RAS}$ Precharge Time	30	—	40	—	ns
t_{CAS}	$\overline{CAS}$ Pulse Width[23]	8	10K	10	10K	ns
t_{CP}	$\overline{CAS}$ Precharge Time[9]	9	—	9	—	ns
t_{CSH}	$\overline{CAS}$ Hold Time [21]	38	—	40	—	ns
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time[10, 20]	12	37	14	45	ns
t_{ASR}	Row-Address Setup Time	0	—	0	—	ns
t_{RAH}	Row-Address Hold Time	8	—	10	—	ns
t_{ASC}	Column-Address Setup Time[20]	0	—	0	—	ns
t_{CAH}	Column-Address Hold Time[20]	8	—	10	—	ns
t_{AR}	Column-Address Hold Time (referenced to $\overline{RAS}$)	30	—	40	—	ns
t_{RAD}	$\overline{RAS}$ to Column-Address Delay Time[11]	10	25	12	30	ns
t_{RAL}	Column-Address to $\overline{RAS}$ Lead Time	25	—	30	—	ns
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	5	—	5	—	ns
t_{RSH}	$\overline{RAS}$ Hold Time	8	—	10	—	ns
t_{RHCP}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	30	—	35	—	ns
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z[15, 24]	0	—	0	—	ns
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time[21]	5	—	5	—	ns
t_{OD}	Output Disable Time[19, 24]	3	15	3	15	ns
t_{OE}	Output Enable Time[15, 16]	—	12	—	15	ns
t_{OED}	Output Enable Data Delay (Write)	12	—	15	—	ns
t_{OEHC}	$\overline{OE}$ HIGH Hold Time from $\overline{CAS}$ HIGH	5	—	5	—	ns
t_{OEP}	$\overline{OE}$ HIGH Pulse Width	10	—	10	—	ns
t_{OES}	$\overline{OE}$ LOW to $\overline{CAS}$ HIGH Setup Time	5	—	5	—	ns
t_{RCS}	Read Command Setup Time[17, 20]	0	—	0	—	ns
t_{RRH}	Read Command Hold Time (referenced to $\overline{RAS}$)[12]	0	—	0	—	ns
t_{RCH}	Read Command Hold Time (referenced to $\overline{CAS}$)[12, 17, 21]	0	—	0	—	ns
t_{WCH}	Write Command Hold Time[17]	8	—	10	—	ns
t_{WCR}	Write Command Hold Time (referenced to $\overline{RAS}$)[17]	40	—	50	—	ns
t_{WP}	Write Command Pulse Width[17]	8	—	10	—	ns
t_{WPZ}	$\overline{WE}$ Pulse Widths to Disable Outputs	7	—	7	—	ns

AC CHARACTERISTICS (Continued)[1,2,3,4,5,6]

(Recommended Operating Conditions unless otherwise noted.)

Symbol	Parameter	-50 Min.	-50 Max.	-60 Min.	-60 Max.	Units
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time[17]	13	—	15	—	ns
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time[17, 21]	8	—	10	—	ns
t_{WCS}	Write Command Setup Time[14, 17, 20]	0	—	0	—	ns
t_{DHR}	Data-in Hold Time (referenced to $\overline{RAS}$)	39	—	39	—	ns
t_{ACH}	Column-Address Setup Time to $\overline{CAS}$ Precharge during WRITE Cycle	15	—	15	—	ns
t_{OEH}	$\overline{OE}$ Hold Time from $\overline{WE}$ during READ-MODIFY-WRITE cycle[18]	8	—	10	—	ns
t_{DS}	Data-In Setup Time[15, 22]	0	—	0	—	ns
t_{DH}	Data-In Hold Time[15, 22]	8	—	10	—	ns
t_{RWC}	READ-MODIFY-WRITE Cycle Time	108	—	133	—	ns
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time during READ-MODIFY-WRITE Cycle[14]	64	—	77	—	ns
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time[14, 20]	26	—	32	—	ns
t_{AWD}	Column-Address to $\overline{WE}$ Delay Time[14]	39	—	47	—	ns
t_{PC}	EDO Page Mode READ or WRITE Cycle Time	20	—	25	—	ns
t_{RASP}	$\overline{RAS}$ Pulse Width in EDO Page Mode	50	100K	60	100K	ns
t_{CPA}	Access Time from $\overline{CAS}$ Precharge[15]	—	30	—	35	ns
t_{PRWC}	EDO Page Mode READ-WRITE Cycle Time	56	—	68	—	ns
t_{COH}	Data Output Hold after $\overline{CAS}$ LOW	5	—	5	—	ns
t_{OFF}	Output Buffer Turn-Off Delay from $\overline{CAS}$ or $\overline{RAS}$[13,15,19, 24]	0	12	0	15	ns
t_{WHZ}	Output Disable Delay from $\overline{WE}$	3	10	3	10	ns
t_{CSR}	$\overline{CAS}$ Setup Time (CBR REFRESH)[20, 25]	5	—	5	—	ns
t_{CHR}	$\overline{CAS}$ Hold Time (CBR REFRESH)[21, 25]	8	—	10	—	ns
t_{ORD}	$\overline{OE}$ Setup Time prior to $\overline{RAS}$ during HIDDEN REFRESH Cycle	0	—	0	—	ns
t_{REF}	Auto Refresh Period 2,048 Cycles	—	32	—	32	ms
	Auto Refresh Period 4,096 Cycles	—	64	—	64	
t_T	Transition Time (Rise or Fall)[2, 3]	1	50	1	50	ns

AC TEST CONDITIONS

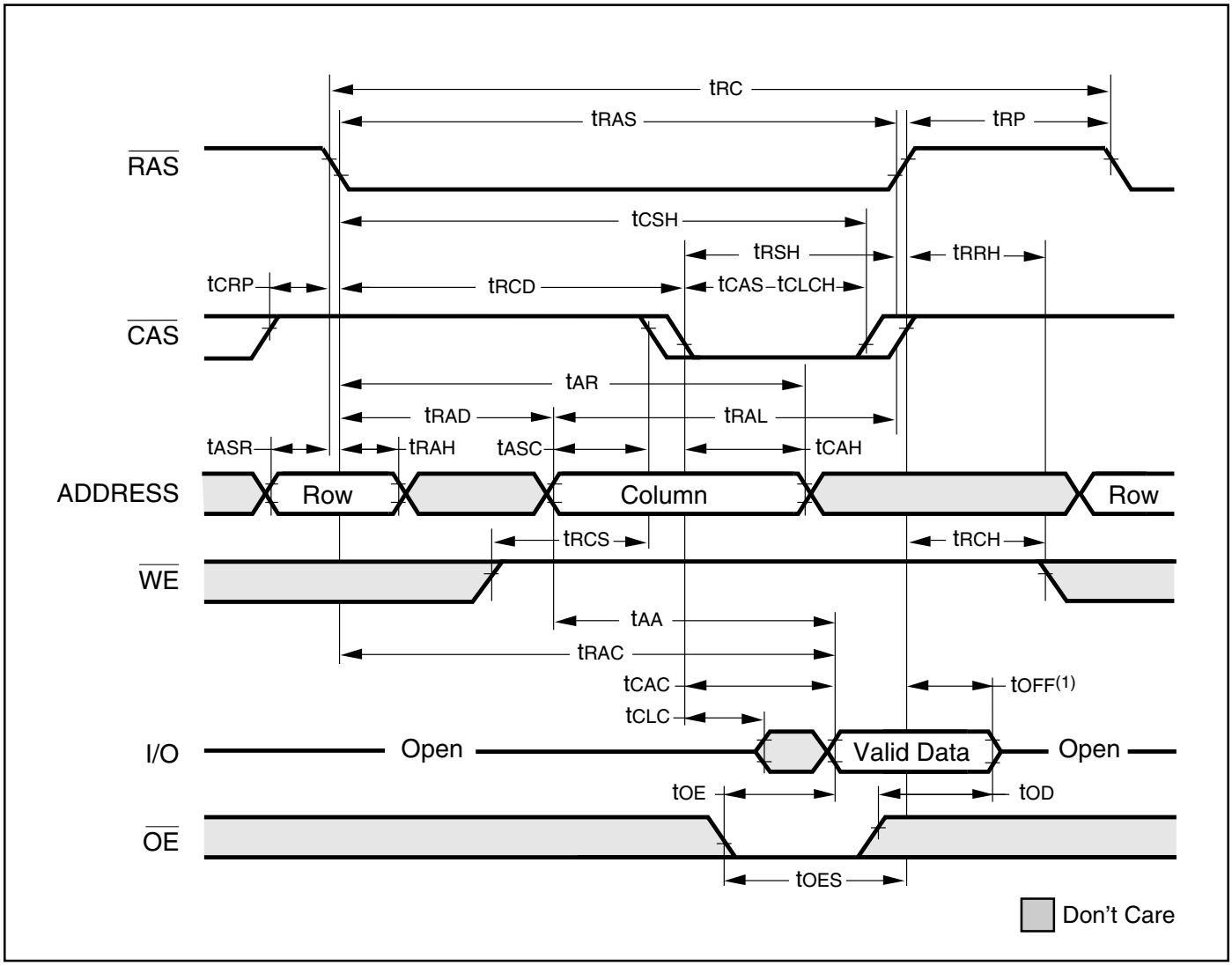
Output load: Two TTL Loads and 50 pF

Input timing reference levels: V_{IH} = 2.4V, V_{IL} = 0.8V

Output timing reference levels: V_{OH} = 2.0V, V_{OL} = 0.8V

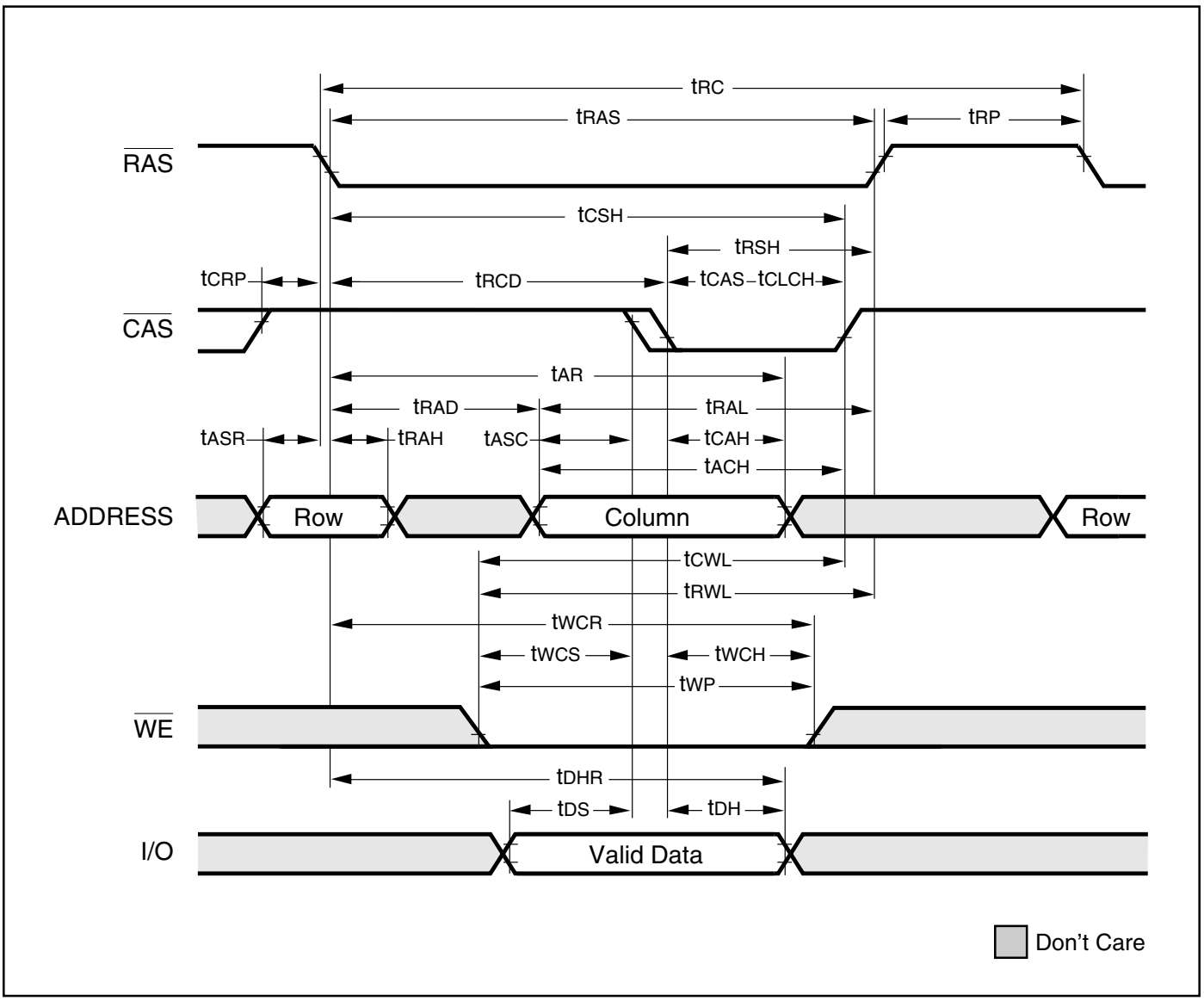
Notes:
1. An initial pause of 200 µs is required after power-up followed by eight $\overline{RAS}$ refresh cycle ($\overline{RAS}$-Only or CBR) before proper device operation is assured. The eight $\overline{RAS}$ cycles wake-up should be repeated any time the t_{REF} refresh requirement is exceeded.
2. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times, are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) and assume to be 1 ns for all inputs.
3. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. If $\overline{CAS}$ and $\overline{RAS}$ = V_{IH}, data output is High-Z.
5. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
6. Measured with a load equivalent to one TTL gate and 50 pF.
7. Assumes that t_{RCD} - t_{RCD} (MAX). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
8. Assumes that t_{RCD} • t_{RCD} (MAX).
9. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, data out will be maintained from the previous cycle. To initiate a new cycle and clear the data output buffer, $\overline{CAS}$ and $\overline{RAS}$ must be pulsed for t_{CP}.
10. Operation with the t_{RCD} (MAX) limit ensures that t_{RAC} (MAX) can be met. t_{RCD} (MAX) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (MAX) limit, access time is controlled exclusively by t_{CAC}.
11. Operation within the t_{RAD} (MAX) limit ensures that t_{RCD} (MAX) can be met. t_{RAD} (MAX) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (MAX) limit, access time is controlled exclusively by t_{AA}.
12. Either t_{RCH} or t_{RRH} must be satisfied for a READ cycle.
13. t_{OFF} (MAX) defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}.
14. t_{WCS}, t_{RWD}, t_{AWD} and t_{CWD} are restrictive operating parameters in LATE WRITE and READ-MODIFY-WRITE cycle only. If t_{WCS} • t_{WCS} (MIN), the cycle is an EARLY WRITE cycle and the data output will remain open circuit throughout the entire cycle. If t_{RWD} • t_{RWD} (MIN), t_{AWD} • t_{AWD} (MIN) and t_{CWD} • t_{CWD} (MIN), the cycle is a READ-WRITE cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of I/O (at access time and until $\overline{CAS}$ and $\overline{RAS}$ or $\overline{OE}$ go back to V_{IH}) is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW result in a LATE WRITE ($\overline{OE}$-controlled) cycle.
15. Output parameter (I/O) is referenced to corresponding $\overline{CAS}$ input.
16. During a READ cycle, if $\overline{OE}$ is LOW then taken HIGH before $\overline{CAS}$ goes HIGH, I/O goes open. If $\overline{OE}$ is tied permanently LOW, a LATE WRITE or READ-MODIFY-WRITE is not possible.
17. Write command is defined as $\overline{WE}$ going low.
18. LATE WRITE and READ-MODIFY-WRITE cycles must have both t_{OD} and t_{OEH} met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The I/Os will provide the previously written data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back to LOW after t_{OEH} is met.
19. The I/Os are in open during READ cycles once t_{OD} or t_{OFF} occur.
20. Determined by falling edge of $\overline{CAS}$.
21. Determined by rising edge of $\overline{CAS}$.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. $\overline{CAS}$ must meet minimum pulse width.
24. The 3 ns minimum is a parameter guaranteed by design.
25. Enables on-chip refresh and address counters.

READ CYCLE

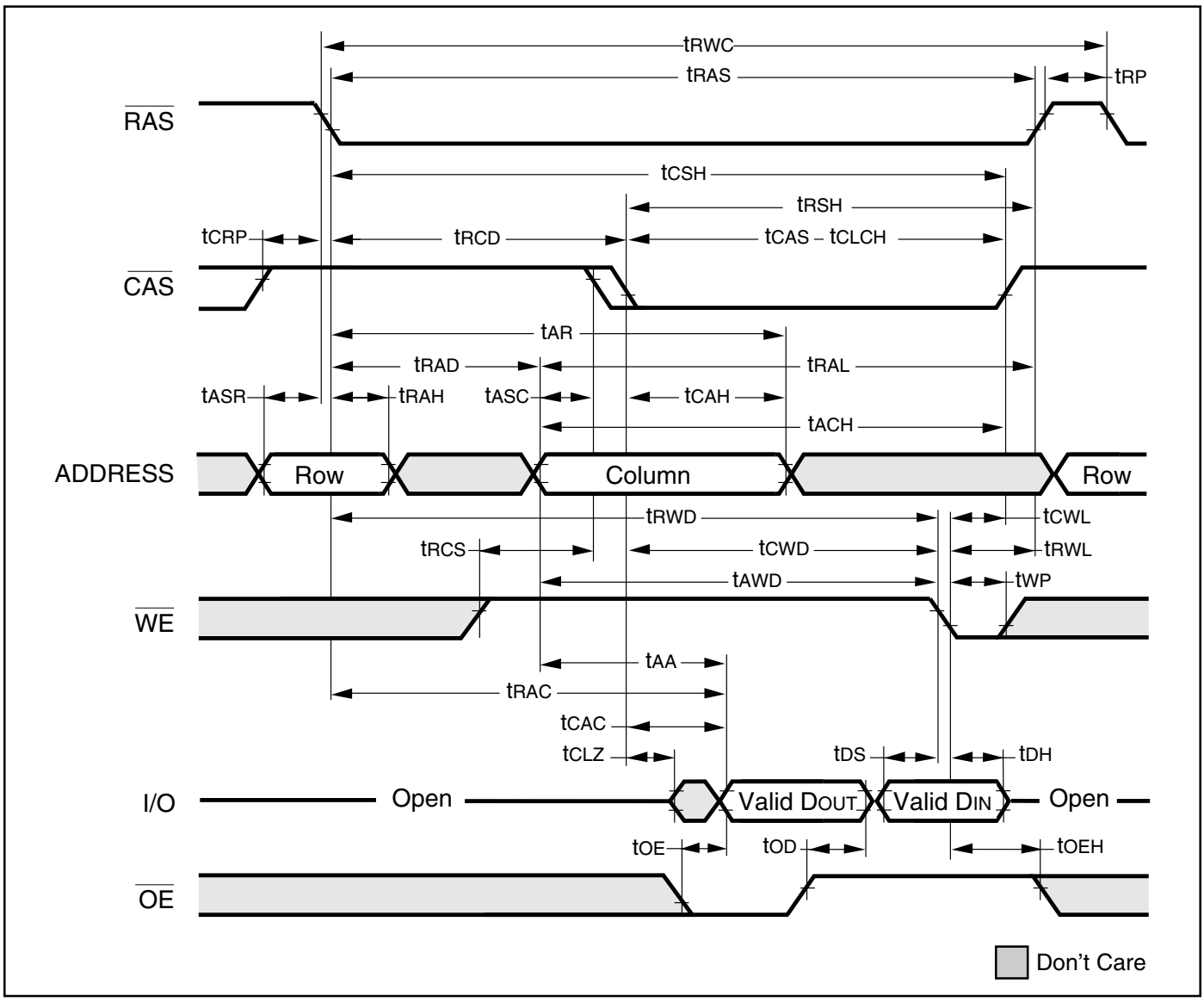


Note:
1. tOFF is referenced from rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.

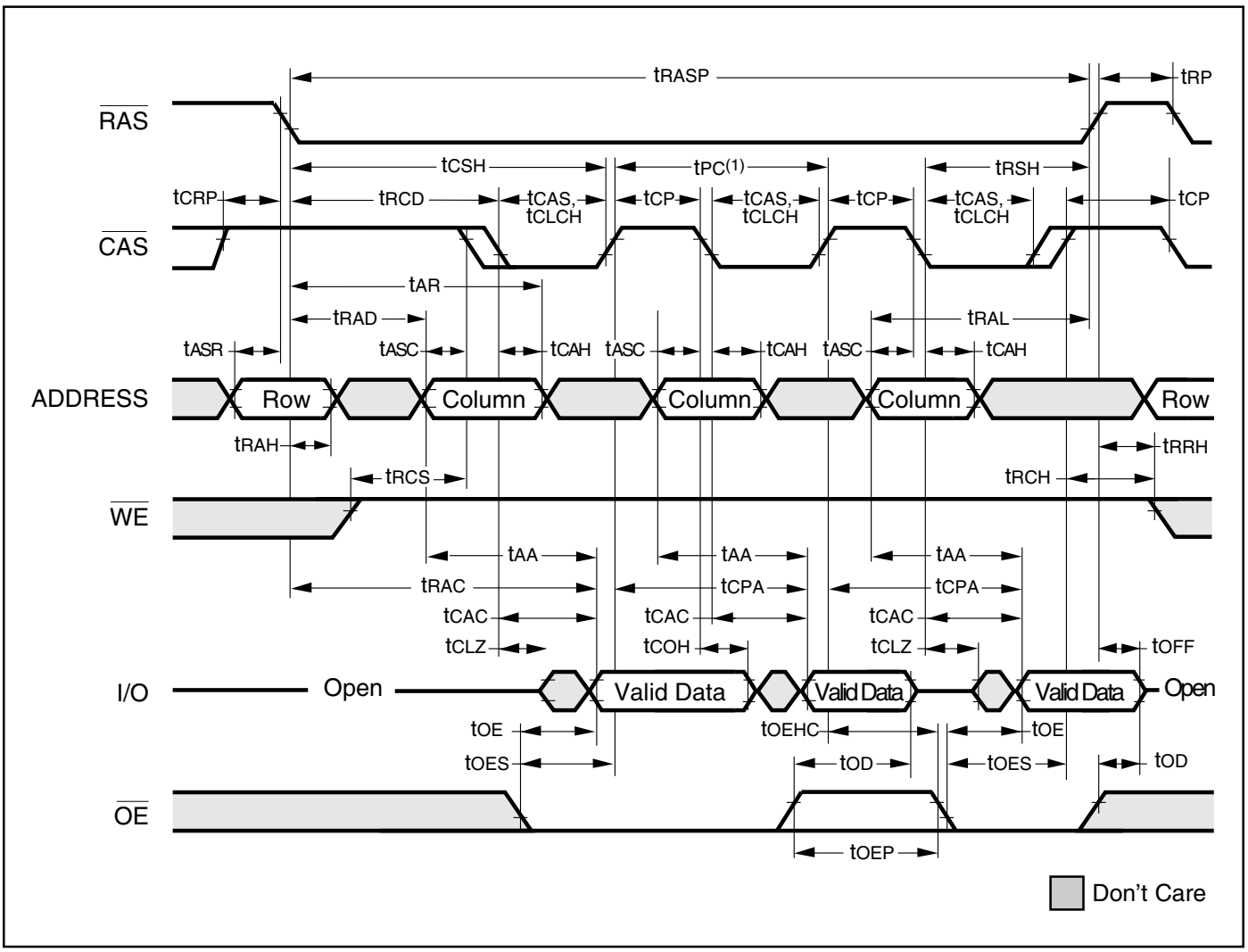
EARLY WRITE CYCLE ($\overline{OE}$ = DON'T CARE)



READ WRITE CYCLE (LATE WRITE and READ-MODIFY-WRITE Cycles)

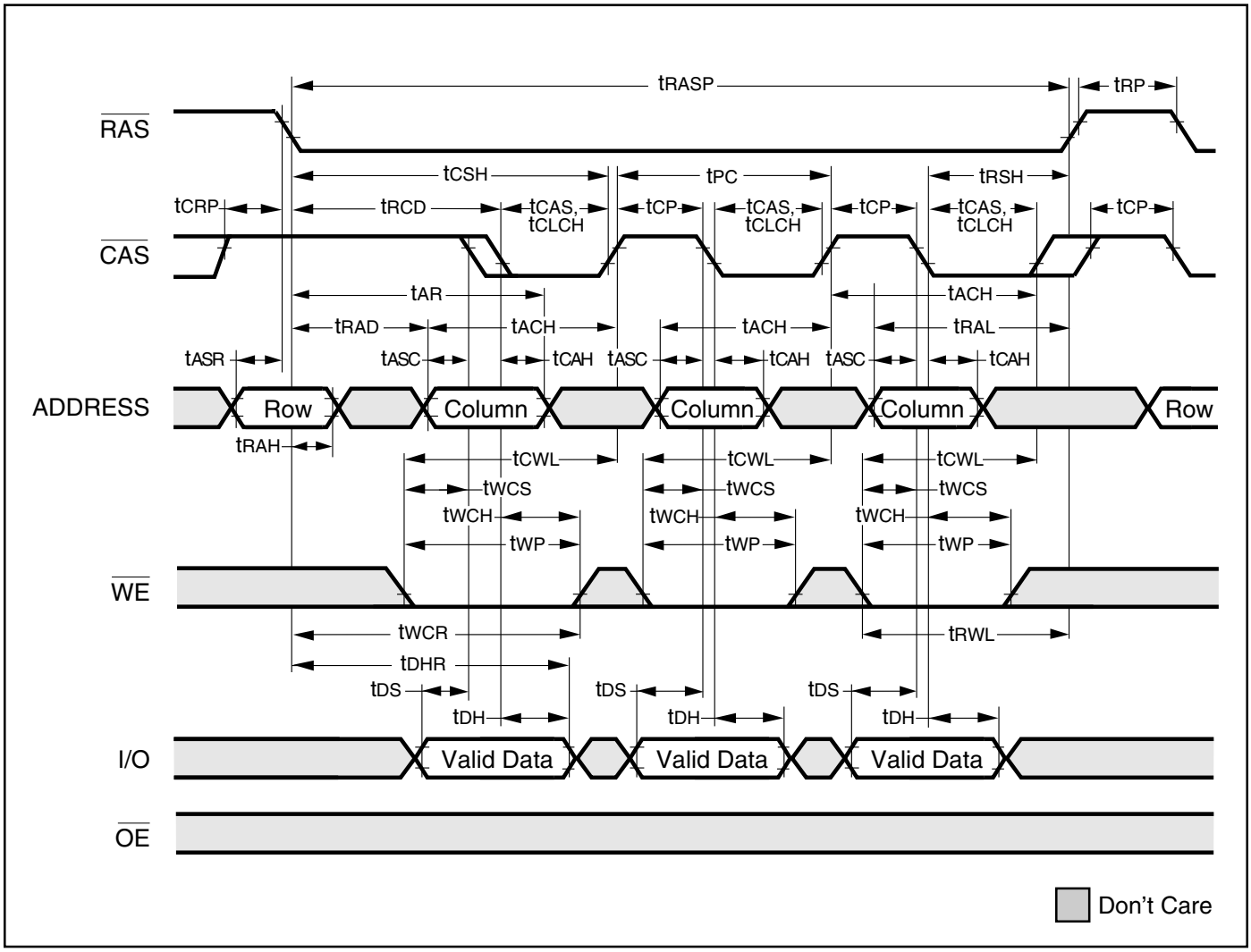


EDO-PAGE-MODE READ CYCLE

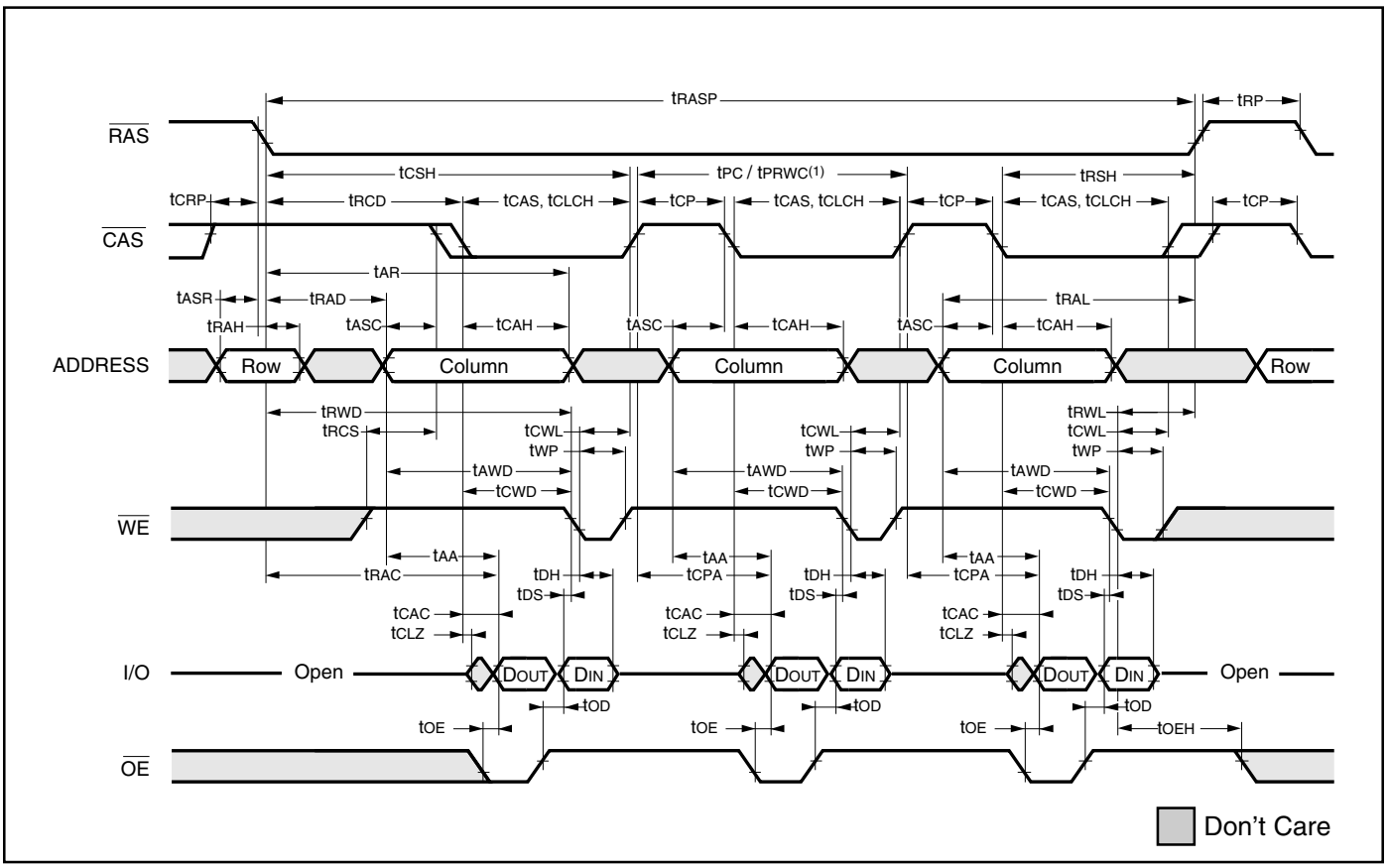


Note:
1. tPC can be measured from falling edge of $\overline{CAS}$ to falling edge of $\overline{CAS}$, or from rising edge of $\overline{CAS}$ to rising edge of $\overline{CAS}$. Both measurements must meet the tPC specifications.

EDO-PAGE-MODE EARLY-WRITE CYCLE



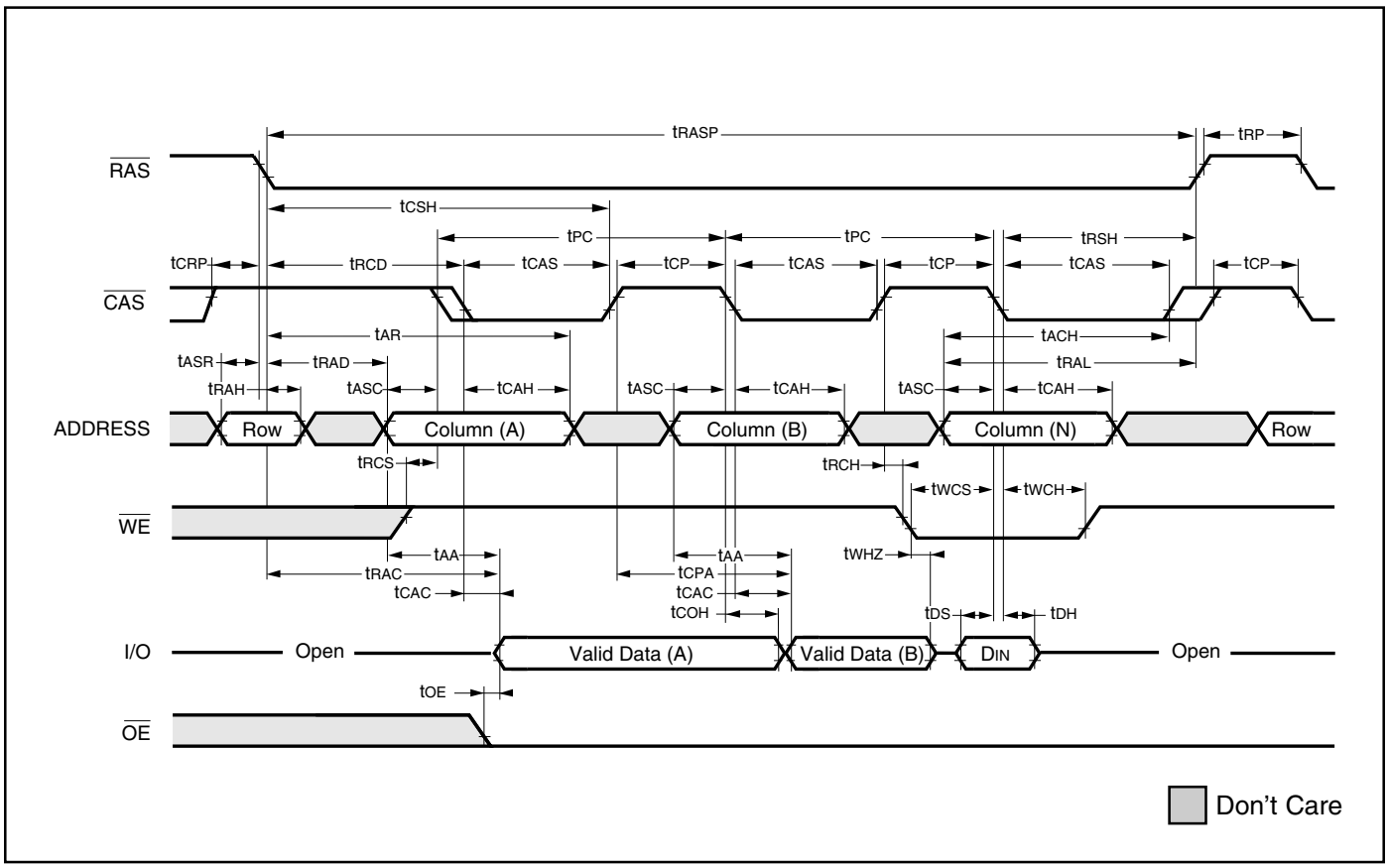
EDO-PAGE-MODE READ-WRITE CYCLE (LATE WRITE and READ-MODIFY WRITE Cycles)



Note:

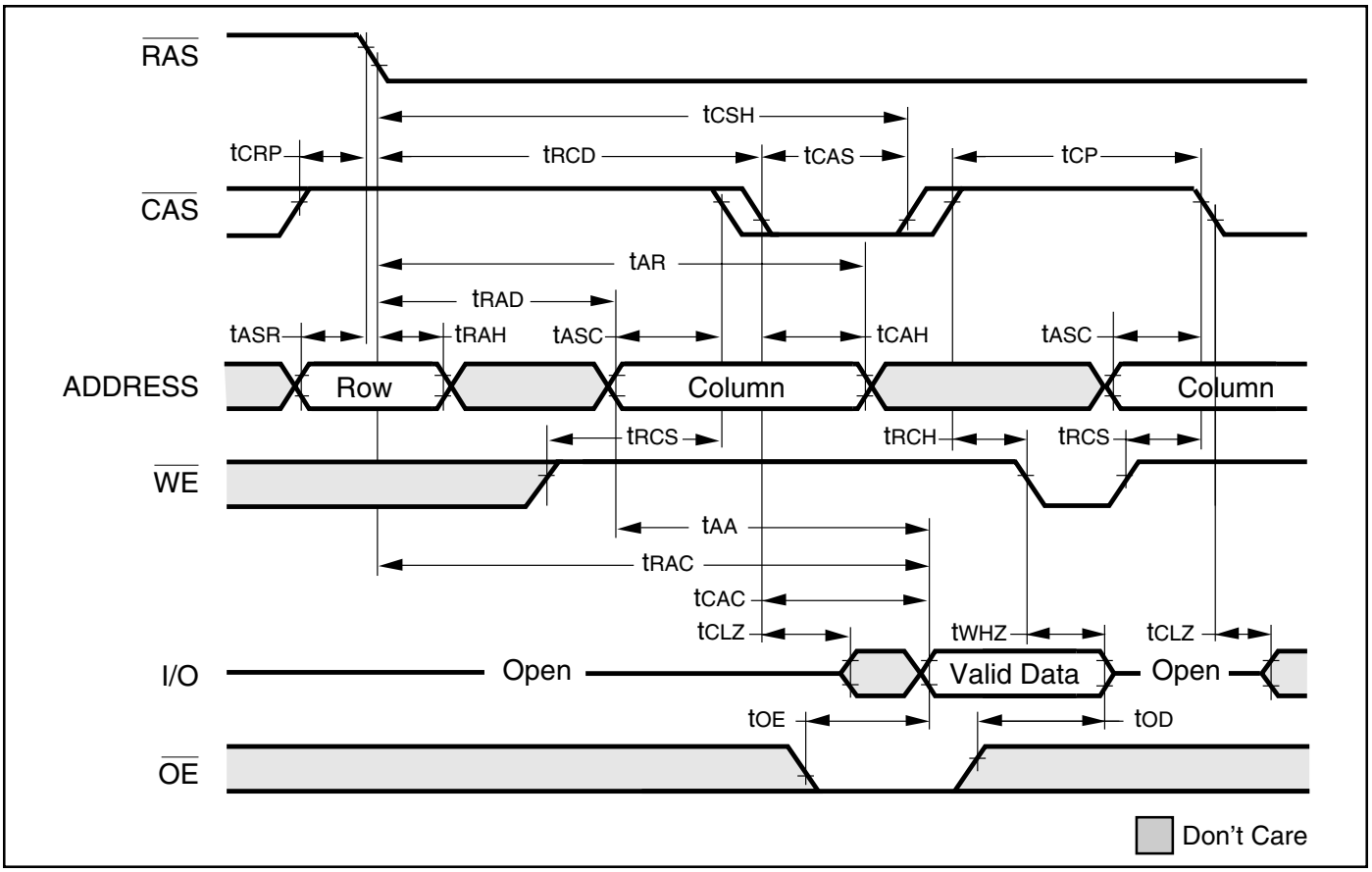
1. tPC can be measured from falling edge of $\overline{CAS}$ to falling edge of $\overline{CAS}$, or from rising edge of $\overline{CAS}$ to rising edge of $\overline{CAS}$. Both measurements must meet the tPC specifications.

EDO-PAGE-MODE READ-EARLY-WRITE CYCLE (Psuedo READ-MODIFY WRITE)

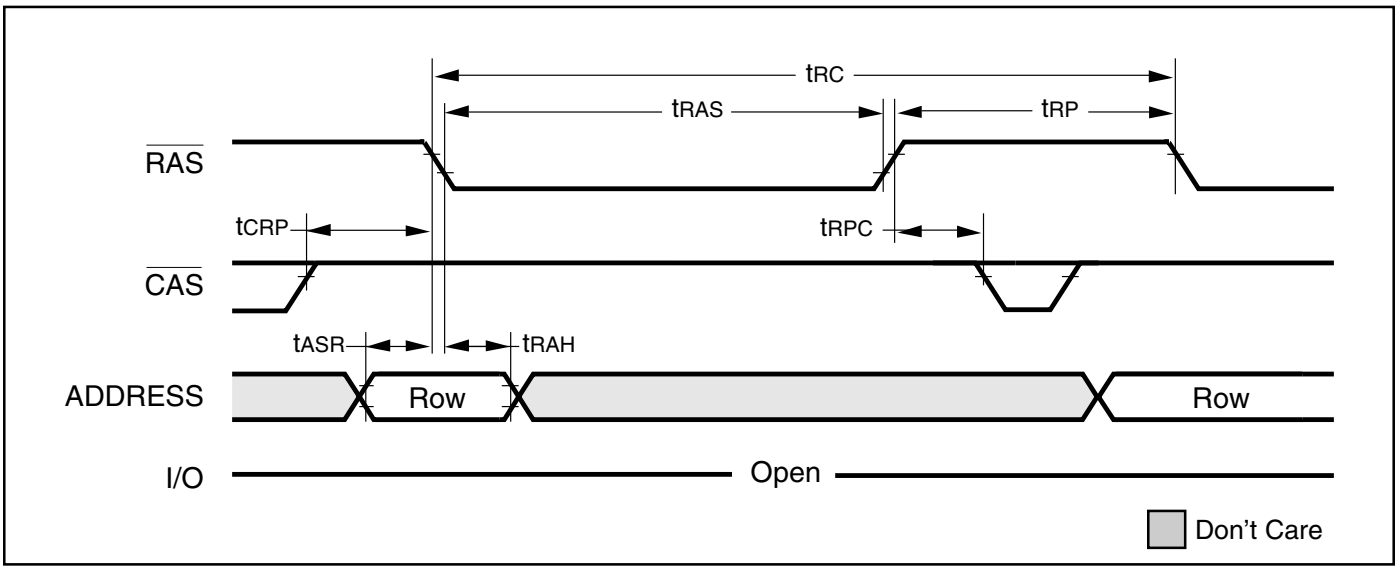


AC WAVEFORMS

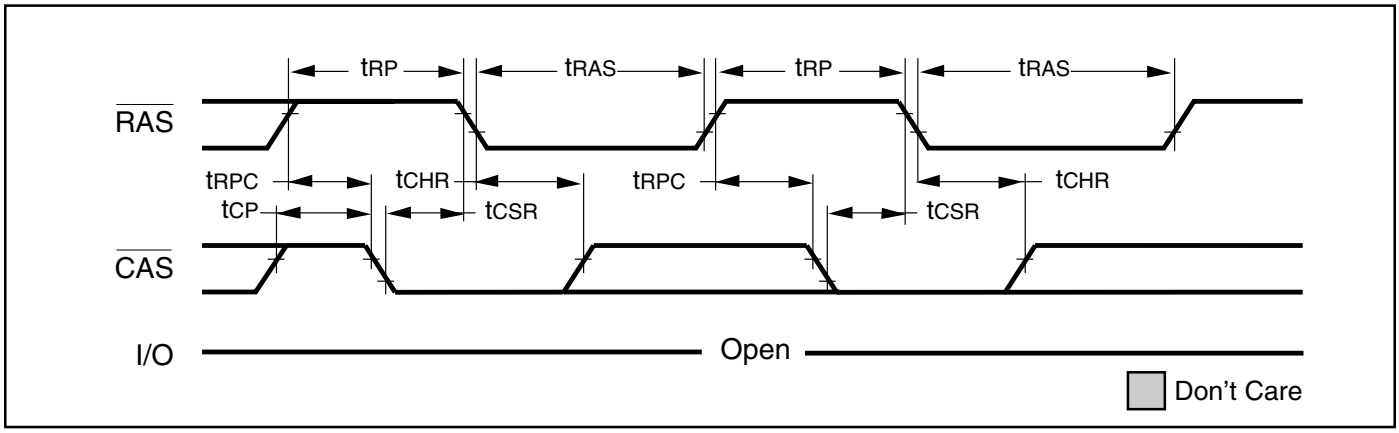
READ CYCLE (With $\overline{WE}$-Controlled Disable)



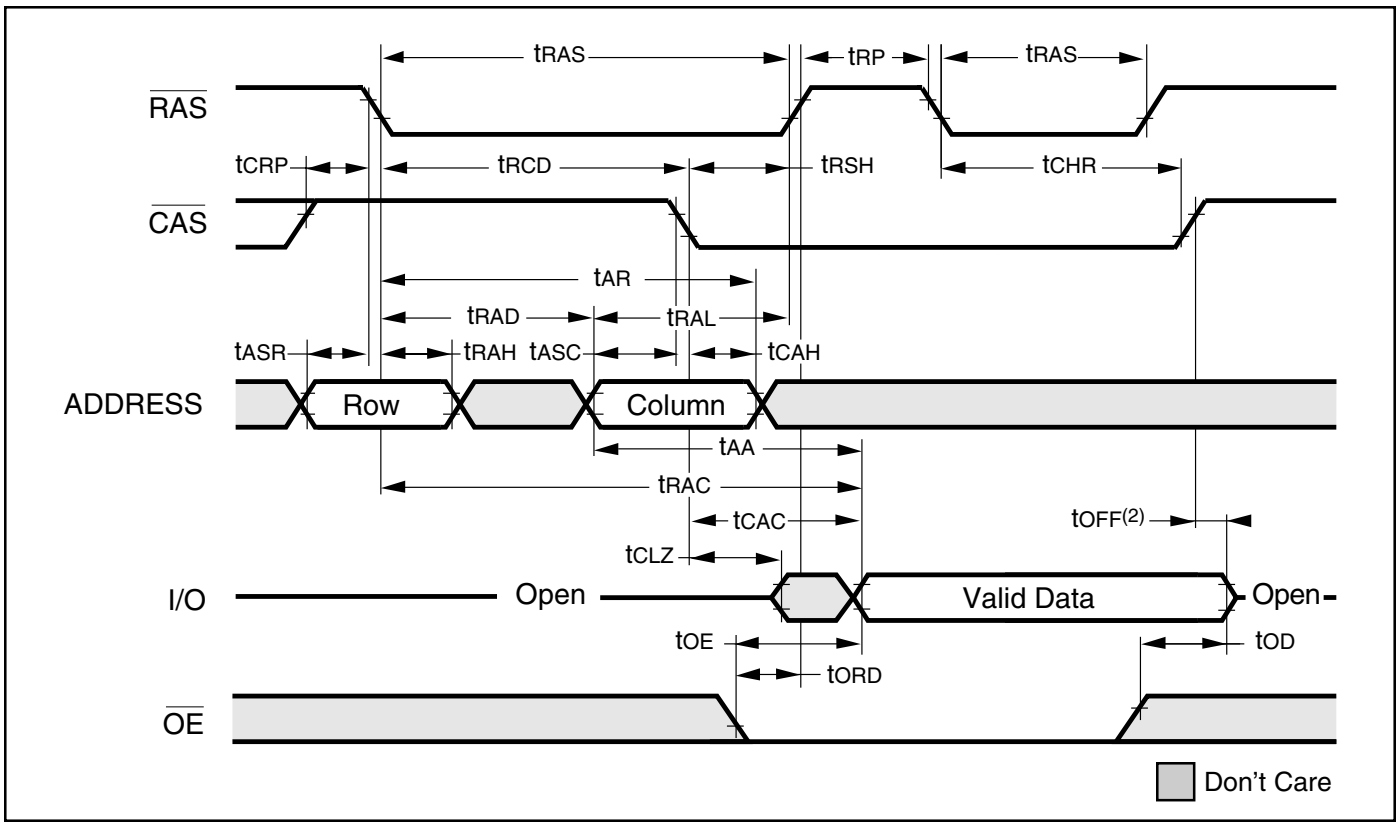
$\overline{RAS}$-ONLY REFRESH CYCLE ($\overline{OE}$, $\overline{WE}$ = DON'T CARE)



$\overline{\text{CBR}}$ REFRESH CYCLE (Addresses; $\overline{\text{WE}}$, $\overline{\text{OE}}$ = DON'T CARE)



HIDDEN REFRESH CYCLE(1) ($\overline{\text{WE}}$ = HIGH; $\overline{\text{OE}}$ = LOW)



Notes:
1. A Hidden Refresh may also be performed after a Write Cycle. In this case, $\overline{\text{WE}}$ = LOW and $\overline{\text{OE}}$ = HIGH.
2. tOFF is referenced from rising edge of $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$, whichever occurs last.

ORDERING INFORMATION

Commercial Range: 0°C to 70°C

Voltage: 5V

Speed (ns)	Order Part No.	Refresh	Package
50	IS41C44002-50J	2K	300-mil SOJ
60	IS41C44002-60J	2K	300-mil SOJ

Speed (ns)	Order Part No.	Refresh	Package
50	IS41C44004-50J	4K	300-mil SOJ
60	IS41C44004-60J	4K	300-mil SOJ

Voltage: 3.3V

Speed (ns)	Order Part No.	Refresh	Package
50	IS41LV44002-50J	2K	300-mil SOJ
60	IS41LV44002-60J	2K	300-mil SOJ

Speed (ns)	Order Part No.	Refresh	Package
50	IS41LV44004-50J	4K	300-mil SOJ
60	IS41LV44004-60J	4K	300-mil SOJ

ORDERING INFORMATION

Industrial Range: -40°C to 85°C

Voltage: 5V

Speed (ns)	Order Part No.	Refresh	Package
50	IS41C44002-50JI	2K	300-mil SOJ
60	IS41C44002-60JI	2K	300-mil SOJ

Speed (ns)	Order Part No.	Refresh	Package
50	IS41C44004-50JI	4K	300-mil SOJ
60	IS41C44004-60JI	4K	300-mil SOJ

Voltage: 3.3V

Speed (ns)	Order Part No.	Refresh	Package
50	IS41LV44002-50JI	2K	300-mil SOJ
60	IS41LV44002-60JI	2K	300-mil SOJ

Speed (ns)	Order Part No.	Refresh	Package
50	IS41LV44004-50JI	4K	300-mil SOJ
60	IS41LV44004-60JI	4K	300-mil SOJ

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