ATHEROS COMMUNICATIONS

Data Sheet

PRELIMINARY
January 2008

AR8012 Integrated 10/100 Fast Ethernet Transceiver

General Description

The Atheros AR8012 Fast Ethernet transceiver is a highly integrated physical layer device that transmits and receives high-speed data over standard category 5 (CAT 5) unshielded twisted pair cable.

The AR8012 is compliant with 100 BASE-TX and 10 BASE-T IEEE 802.3 standards. The AR8012 device uses advanced mixed-signal processing technology and integrates functions such as adaptive equalization, and timing recovery to deliver substantial power savings and operation in noisy environments.

The AR8012 device supports the Media Independent Interface (MII) for direct connection to a Fast Ethernet-capable MAC.

The AR8012 supports the Atheros Cable Diagnostic Test (CDT) feature, which uses Time Domain Reflectometry (TDR) technology to quickly and remotely identify potential cable malfunctions without deploying field support personnel or bringing down the network. The AR8012 solution detects and reports issues such as PHY malfunctions, bad/marginal cable or patch cord segments or connectors, thus significantly reducing installation time, cable debug efforts, and overall network support cost.

Manufactured in the 0.13 µm standard CMOS process, the AR8012 is packaged in a 48-pin LQFP, featuring a small body size of 7 x 7 mm.

Features

- 10/100 BASE-T IEEE 802.3 compliant
- Supports MII interface
- Low power modes with internal automatic DSP power saving scheme
- Fully integrated digital adaptive equalizers All digital baseline wander correction
- Supports external 25 MHz clock source
- Automatic speed downshift mode
- Automatic MDI/MDIX crossover
- Automatic polarity correction
- Loopback modes for diagnostics
- IEEE 802.3u compliant Auto-Negotiation
- Software programmable LED modes
- Cable Diagnostic Test (CDT)
- Requires only one 3.3V power supply
- 0.13 µm digital CMOS process
- 48-pin LQFP 7 mm x 7 mm package

AR8012 Functional Block Diagram

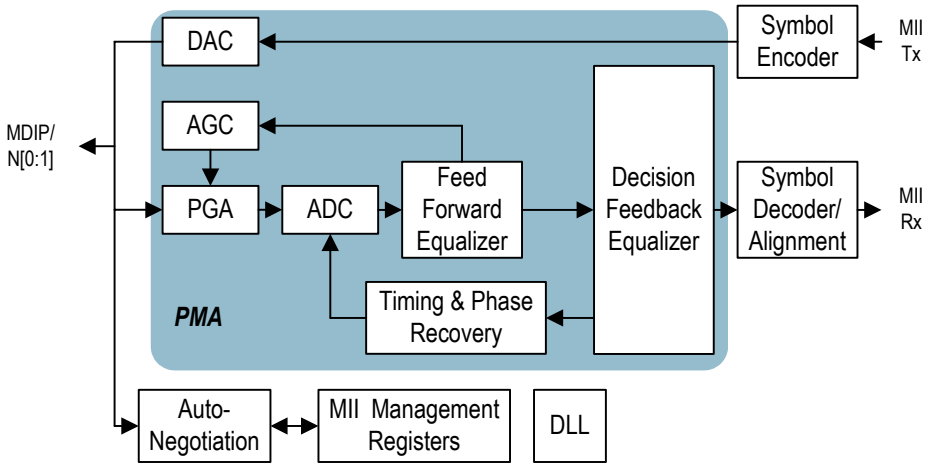

Table of Contents

1. Pin Descriptions

This section contains a package pinout for the AR8012 LQFP 48 pin and a listing of the signal descriptions (see Figure 1-1).

The following nomenclature is used for signal names:

NC	No connection to the internal die is made from this pin
_L	At the end of the signal name, indicates active low signals
P	At the end of the signal name, indicates the positive side of a differential signal
N	At the end of the signal name indicates the negative side of a differential signal

The following nomenclature is used for signal types described in Table 1-1:

D	Open drain
IA	Analog input signal
I	Digital input signal
IH	Input signals with weak internal pull-up, to prevent signals from floating when left open
IL	Input signals with weak internal pull-down, to prevent signals from floating when left open
I/O	A digital bidirectional signal
OA	An analog output signal
O	A digital output signal
P	A power or ground signal
PD	Internal pull-down for input
PU	Internal pull-up for input

Figure 1-1 shows the pinout diagram for the AR8012.

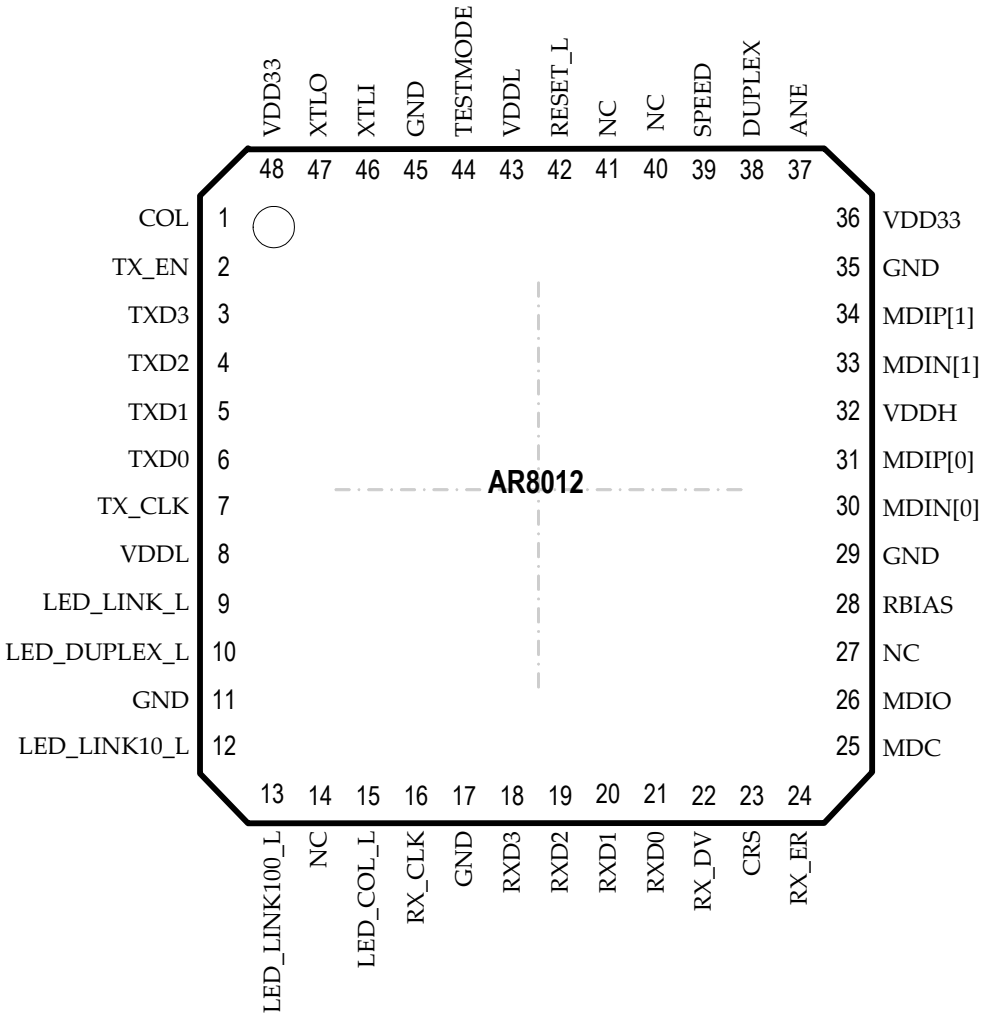

Figure 1-1. **Pinout Diagram**

Table 1-1. **Signal to Pin Relationships and Descriptions**

Symbol	Pin	Type	Description
MII			
COL	1	I/O, PD	MII collision, insert 22 Ω serial resistance
			Pull Down: LED Mode 0
			Pull Up: LED Mode 1
CRS	23	I/O, PD	MII carrier sense, insert 22 Ω serial resistance
RX_CLK	16	I/O, PD	MII receive clock, 25/2.5 MHz digital, insert 22 Ω serial resistance
RX_DV	22	I/O, PD	MII receive data valid, insert 22 Ω serial resistance
RX_ER	24	I/O, PU	MII receive error, insert 22 Ω serial resistance
RXD0	21	I/O, PD	MII receive data, insert 22 Ω serial resistance
RXD1	20	I/O, PD	MII receive data, insert 22 Ω serial resistance
RXD2	19	I/O, PD	MII receive data, insert 22 Ω serial resistance
RXD3	18	I/O, PD	MII receive data, insert 22 Ω serial resistance
TX_CLK	7	O, PD	MII transmit clock, 25/2.5 MHz digital, insert 22 Ω serial resistance
TX_EN	2	I, PD	MII transmit enable
TXD0	6	I, PD	MII transmit data
TXD1	5	I, PD	MII transmit data
TXD2	4	I, PD	MII transmit data
TXD3	3	I, PD	MII transmit data
LED			
LED_COL_L	15	I/O	Parallel LED output for collision indicator; blinking, Power-on Strapping — PHY AD 4
LED_DUPLEX_L	10	I/O	Parallel LED output for full-duplex indicator; lit Power- Strapping — PHY AD 1
LED_LINK_L	9	I/O	Parallel LED output for link indicator; lit Power-on Strapping — PHY AD 0
LED_LINK10_L	12	I/O	Parallel LED output for 10 BASE-T; LED Mode 0 - activity; blinking LED Mode 1 - link/activity; lit/blinking Power-on Strapping — PHY AD 2
LED_LINK100_L	13	I/O	Parallel LED output for 100 BASE-TX; LED Mode 0 - activity; blinking LED Mode 1 - link/activity; lit/blinking Power-on Strapping — PHY AD 3
MDI			
MDIP[0], MDIN[0]	31, 30	IA, OA, D	Media-dependent interface 0, 100 Ω transmission line
MDIP[1], MDIN[1]	34, 33	IA, OA, D	Media-dependent interface 1, 100 Ω transmission line

Table 1-1. **Signal to Pin Relationships and Descriptions (continued)**

Symbol	Pin	Type	Description	
Management Interface and Interrupt				
MDC	25	I, PU	Management data clock reference, 6.25 MHz digital	
MDIO	26	I/O, PU	Management data, 6.25 Mbps digital	
System Signal Group/Reference				
ANE	37	IH	Auto-negotiation enable	
DUPLEX	38	IH	Full-duplex enable	
RBIAS	28	OA	External 2.4 K 1% to GND to set bias current	
RESET_L	42	IH	System reset, active low, connect 5.1 K to 3.3V and 0.1 uF to ground, or to external system reset input with at least 400 ns low duration	
SPEED	39	IH	0	10BASE-T
			1	100BASE-TX
XTLI	46	IA	Crystal oscillator input side pin; 27 pF to GND	
XTLO	47	OA	Crystal oscillator output side pin; 27 pF to GND	
Tested				
TESTMODE	44	I, PU	Test mode control, static digital 0 - Test mode 1 - Normal operation (Default)	

Symbol	Pin	Description
Power		
GND	11, 17, 29, 35, 45	GND pin
VDD33	36, 48	3.3V supply voltage
VDDH	32	2.5V regulator output
VDDL	8, 43	1.5V regulator output

2. Functional Description

The Atheros AR8012 is a highly integrated analog front end (AFE) and digital signal transceiver (see Figure 2-1), providing high performance with substantial cost reduction. AFE consists of automatic gain control (AGC), ADC, DAC, drivers, and clock generation. The AR8012 provides physical layer functions to transmit and receive high-speed data over standard category 5 (CAT5) unshielded twisted pair cable.

See also the "AR8012 Functional Block Diagram" on page 1.

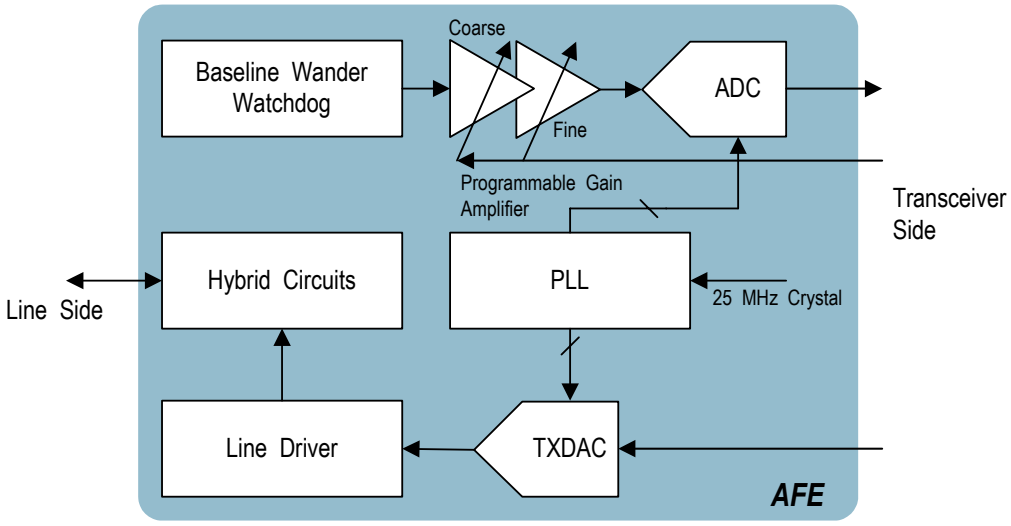

Figure 2-1. **Analog Front End**

The AR8012 10/100 PHY is fully 802.3u compliant, and supports the media-independent interface (MII) to connect to a Fast Ethernet-capable MAC.

The AR8012 transceiver combines feed-forward equalizer, feedback equalizer, and timing recovery, to enhance signal performance in noisy environments.

2.1 Transmit Functions

The AR8012 transmit channel includes 4B/5B mapper and scrambler and MLT3 encoder. Table 2-1 describes the transmit function encoder modes.

Table 2-1. **Transmit Function Encoder Modes**

Encoder Mode	Description
100BASE-TX	In 100BASE-TX mode, 4-bit data from the MII is 4B/5B serialized, scrambled, and encoded to a three-level MLT3 sequence transmitted by the PMA.
10BASE-T	In 10BASE-T mode, the AR8012 transmits and receives Manchester-encoded data.

2.2 Receive Functions

The AR8012 receive channel includes digital gain control, feed forward adaptive equalizer, decision feedback equalizer, slicer, 5B/4B de-mapper and de-scrambler, PCS receive functional block, and timing recovery logic.

2.2.1 Decoder Modes

Table 2-2 describes the receive function decoder modes.

Table 2-2. **Receive Function Decoder Modes**

Decoder Mode	Description
100BASE-TX	In 100BASE-TX mode, the receive data stream is recovered and descrambled to align to the symbol boundaries. The aligned data is then parallelized and 5B/4B decoded to 4-bit data. This output runs to the MII receive data pins after data stream delimiters have been translated.
10BASE-T	In 10BASE-T mode, the recovered 10BASE-T signal is decoded from Manchester then aligned.

2.2.2 Analog to Digital Converter

The AR8012 device employs an advanced high speed ADC on each receive channel with high resolution, which results in better SNR and lower error rates.

2.2.3 Baseline Wander Canceller

Baseline wander results from Ethernet links that AC-couple to the transceivers and from AC coupling that cannot maintain voltage levels for longer than a short time. As a result, transmitted pulses are distorted, resulting in erroneous sampled values for affected pulses. The AR8012 device uses an advanced baseline wander cancellation circuit that continuously monitors and compensates for this effect, minimizing the impact of DC baseline shift on the overall error rate.

2.2.4 Digital Adaptive Equalizer

The digital adaptive equalizer removes inter-symbol interference at the receiver. The digital adaptive equalizer takes unequalized signals from ADC output and uses a combination of feedforward equalizer (FFE) and decision feedback equalizer (DFE) for the best-optimized signal-to-noise (SNR) ratio.

2.2.5 Auto-Negotiation

The AR8012 device supports 10/100 BASE-T Copper auto-negotiation in accordance with IEEE 802.3 clauses 28 and 40. Auto-negotiation provides a mechanism for transferring information between a pair of link partners to choose the best possible mode of operation in terms of speed, duplex modes, and master/slave preference. Auto-negotiation is initiated upon any of the following scenarios:

- Power-up reset
- Hardware reset
- Software reset
- Auto-negotiation restart
- Transition from power-down to power-up
- The link goes down

If auto-negotiation is disabled, a 10BASE-T or 100BASE-TX can be manually selected using the IEEE MII registers.

2.2.6 Smartspeed Function

The Atheros Smartspeed function is an enhanced feature of auto-negotiation that allows the AR8012 device to fall back in speed based on cabling conditions as well as operate over CAT3 cabling (in 10BASE-T mode) or two-pair CAT5 cabling (in 100BASE-TX mode).

By default, the Smartspeed feature is enabled. Refer to the register "Extended PHY-Specific Control" on page 28, which describes how to set the parameters. Set these register bits to control the Smartspeed feature:

- Bit [5]: 1 = Enables Smartspeed (default)
- Bits [4:2]: Sets the number of link attempts before adjusting
- Bit [1]: Timer to determine the stable link condition

2.2.7 Automatic MDI/MDIX Crossover

During auto-negotiation, the AR8012 device automatically determines and sets the required MDI configuration, eliminating the need for external crossover cable. If the remote device also implements automatic MDI crossover, the crossover algorithm as described in IEEE 802.3 clause 40.4.4 ensures that only one device performs the required crossover.

2.2.8 Polarity Correction

If cabling has been incorrectly wired, the AR8012 automatically corrects polarity errors on the receive pairs.

2.3 Loopback Modes

2.3.1 Digital Loopback

Digital loopback provides the ability to loop transmitted data back to the receiver using digital circuitry in the AR8012 device. The registers "100BASE-TX Test Mode Select" and "Test Configuration for 10 Base-T" on page 33 are used to determine at which point the signal loops back (for different modes, respectively).

Figure 2-2 shows a block diagram of digital loopback.

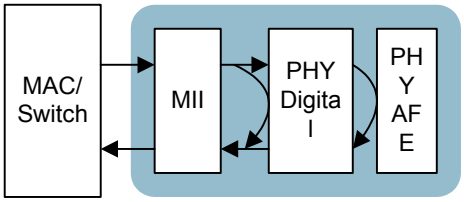

Figure 2-2. **Digital Loopback**

2.3.2 External Cable Loopback

External cable loopback loops MII Tx to MII Rx through a complete digital and analog path and an external cable, thus testing all the digital data paths and all the analog circuits. Figure 2-3 shows a block diagram of external cable loopback.

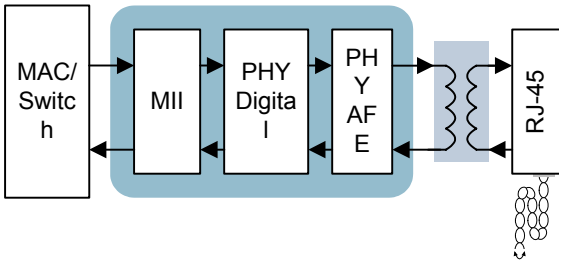

Figure 2-3. **External Cable Loopback**

2.3.3 Cable Diagnostic Test

The Cable Diagnostic Test (CDT) feature in the AR8012 device uses Time Domain Reflectometry (TDR) to identify remote and local PHY malfunctions, bad/marginal cable or patch cord segments, or connectors. Some of the possible problems that can be diagnosed include opens, shorts, cable impedance mismatch, bad connectors, and termination mismatch. The CDT can be performed when there is no link partner or when the link partner is auto-negotiating.

2.3.4 LED Interface

The LED interface can either be controlled by the PHY or controlled manually, independent of the state of the PHY. Five status LEDs are available. These can be used to indicate operation speed, duplex mode, and link status. The LEDs can be programmed to different status functions from their default value. They can also be controlled directly from the MII register interface.

2.3.5 Power Supplies

The AR8012 device requires only one power supply: 3.3V.

2.3.6 Low Power Modes

The AR8012 device supports the software power-down low power mode. The standard IEEE power-down mode is entered by setting the POWER_DOWN bit (bit [11]) of the register "Control" on page 18 equal to one.

In this mode, the AR8012 device ignores all MAC interface signals except the MDC/MDIO. It does not respond to any activity on the CAT 5 cable. The F1 device cannot wake up on its own. It can only wake up by setting the POWER_DOWN bit (bit [11]) of the register "Control" on page 18" to 0.

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3-1 summarizes the absolute maximum ratings and Table 3-2 lists the recommended operating conditions for the AR8012. Absolute maximum ratings are those values beyond which damage to the device can occur. Functional operation under these conditions, or at any other condition beyond those indicated in the operational sections of this document, is not recommended.

Table 3-1. **Absolute Maximum Ratings**

Symbol	Parameter	Max Rating	Unit
VDD33	3.3V supply voltage	3.8	V
T_{store}	Storage temperature	–65 to 150	°C
ESD	Electrostatic discharge tolerance	2000	V

3.2 Recommended Operating Conditions

Table 3-2. **Recommended Operating Conditions**

Symbol	Parameter		Min	Typ	Max	Unit
VDD33	3.3V supply voltage		3.0	3.3	3.6	V
T_A	Ambient Temperature		0		70	°C
T_J	Junction Temperature		0		125	°C
θ_{JA}	Junction to Ambient Temperature	2-layer PCB	—	110	—	°C/W
		4-layer PCB	—	70	—	°C/W
θ_{JC}	Junction to Case Temperature	2-layer PCB	—	33.1	—	°C/W
		4-layer PCB	—	32.7	—	°C/W
θ_{JT}	Junction to Top Center Temperature	2-layer PCB	—	14	—	°C/W
		4-layer PCB	—	10	—	°C/W

3.3 MII DC Characteristics

Table 3-3 shows the MII DC characteristics.

Table 3-3. **MII DC Characteristics**

Symbol	Parameter	Min	Max	Unit
V_{OH}	Output high voltage	2.0	3.0	V
V_{OL}	Output low voltage	GND	0.4	V
V_{IH}	Input high voltage	1.7	—	V
V_{IL}	Input low voltage	—	0.7	V
I_{IH}	Input high current	—	15	µA
I_{IL}	Input low current	–15	—	µA

Figure 3-1 shows the MII AC timing diagram.

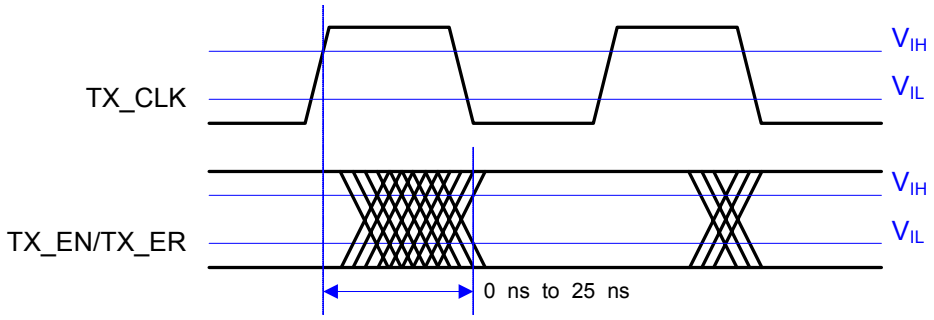

Figure 3-1. **MII AC Tx Timing Diagram**

Figure 3-2 shows the MII AC timing diagram.

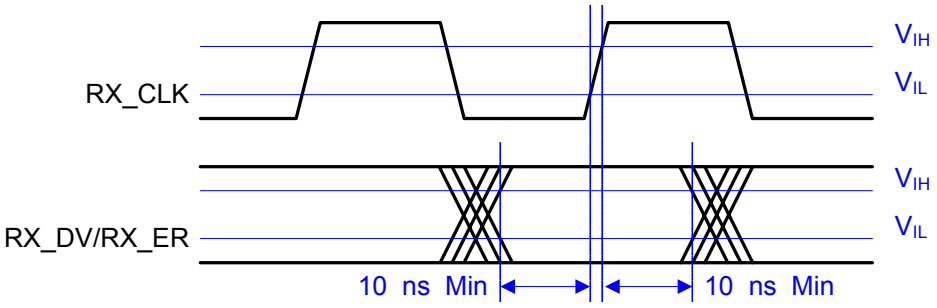

Figure 3-2. **MII AC Rx Timing Diagram**

3.4 MDIO Characteristics

Table 3-4 shows the MDIO DC characteristics.

Table 3-4. **MDIO DC Characteristics**

Symbol	Parameter	Min	Max	Unit
V_{OH}	Output high voltage	2.4	—	V
V_{OL}	Output low voltage	—	0.4	V

Table 3-4. **MDIO DC Characteristics**

I_{IH}	Input high current	—	–0.4	mA
I_{IL}	Input low current	0.4	—	mA

Figure 3-3 shows the MDIO AC timing diagram.

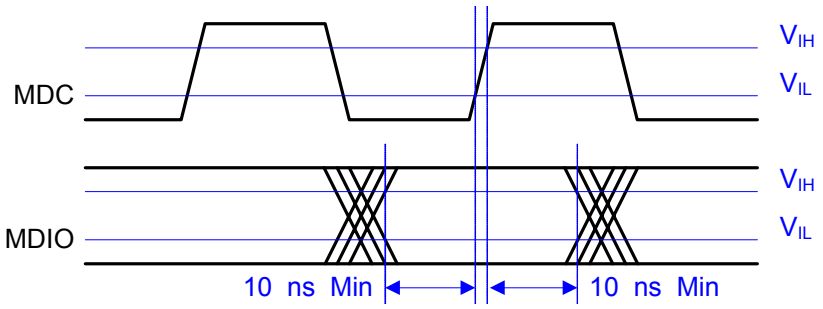

Figure 3-3. **MDIO AC Timing Diagram**

3.5 Power-On Strapping

Table 3-5 shows the pin-to-PHY core configuration signal power-on strapping.

Table 3-5. **Power-On Strapping[1]**

PHY Pin Name	Pin	Default	PHY Core Configuration Signal	Description
LED_LINK_L	9	0	PHYADDRESS[0]	PHY address
LED_DUPLEX_L	10	0	PHYADDRESS[1]	
LED_LINK10_L	12	0	PHYADDRESS[2]	
LED_LINK100_L	13	0	PHYADDRESS[3]	
LED_COL_L	15	0	PHYADDRESS[4]	
COL	1	0	LED_MODE	if COL = 0
				LED_LINK10_L becomes a 10BASE-T Activity LED; Blinking when transmitting or receiving data.
				LED_LINK100_L becomes a 100BASE-TX Activity LED; Blinking when transmitting or receiving data.
				if COL=1
				LED_LINK10_L becomes a 10BASE-T Link/Activity LED; Lit when a valid Link is present — blinking when transmitting or receiving data.
				LED_LINK100_L becomes a 100BASE-TX Link/ Activity LED; Lit when a valid Link is present — blinking when transmitting or receiving data

[1]Default values: 0 = Pull-down, 1 = Pull-up with 10 K resistor.

3.6 Typical Power Consumption Parameters

The following conditions apply to the typical characteristics unless otherwise specified:

V_{DD33} = 3.3V, T_{amb} = 25 °C

Table 3-6 shows the typical power drain as a function of the AR8012's operating mode.

Table 3-6. **Total System Power**

Mode	Current	Power
100BASE-TX	117 mA	387 mW
10BASE-T	120 mA	396 mW

4. Register Descriptions

Table 4-1 shows the reset types used in this document.

Table 4-1. **Reset Types**

Type	Description
LH	Register field with latching high function. If status is high, then the register is set to one and remains set until a read operation is performed through the management interface or a reset occurs.
LL	Register field with latching low function. If status is low, then the register is cleared to a zero and remains cleared until a read operation is performed through the management interface or a reset occurs.

Table 4-1. **Reset Types (continued)**

Type	Description
Retain	Value written to a register field takes effect without a software reset.
SC	Self-Clear. Writing a one to this register causes the desired function to execute immediately, and the register field clears to zero when the function is complete.
Update	The value written to the register field does not take effect until a software reset is executed. The value can still be read after it is written.

4.1 Register Summary

Table 4-2 summarizes the registers for the AR8012.

Table 4-2. **Register Summary**

Offset	Register	Page
0x00	Control	page 18
0x01	Status	page 19
0x02	PHY Identifier [18:3]	page 20
0x03	PHY Identifier [19:24]	page 20
0x04	Auto-Negotiation Advertisement	page 20
0x05	Link partner ability	page 22
0x06	Auto-Negotiation Expansion	page 23
0x10	Function Control	page 24
0x11	PHY-Specific Status	page 25
0x12	Interrupt Enable	page 26
0x13	Interrupt Status	page 27
0x14	Extended PHY-Specific Control	page 28
0x15	Receive Error Counter	page 28
0x16	Virtual Cable Tester Control	page 29
0x18	LED Control	page 29
0x19	Manual LED Override	page 30
0x1C	Virtual Cable Tester Status	page 31
0x1D	Debug Port1 (Address Offset)	page 31
0x1E	Debug Port2 (Data Port)	page 31

4.1.1 Control

Offset: 0x00
Mode: Read/Write
Hardware Reset: 0
Software Reset: See field descriptions

Bit	Name	SW Reset	Description	
15	RESET	SC	PHY software reset	
			0	Normal operation
			1	PHY reset Writing a 1 to this bit causes immediate PHY reset. Once the operation is done, this bit clears to 0 automatically.
14	LOOPBACK	0	When loopback is active, the transmitter data on TXD loops back to RXD internally. The link breaks when loopback is enabled.	
			0	Disable loopback
			1	Enable loopback
13	SPEED_SELECTION (LSB)	Update	After completing auto-negotiation, this bit reflects the speed status	
			0	10 Base-T
			1	100 Base-T
12	AUTO_ NEGOTIATION	Update	Upon hardware reset, this bit depends on ANEN_PAD; all other configurations are 0:	
			0	Disable the auto-negotiation process
			1	Enable the auto-negotiation process
11	POWER_DOWN	0	When the port switches from power-down to normal operation, software reset and restart auto-negotiation perform even when RESET (bit [15]) and RESTART_AUTO_NEGOTIATION (bit [9]) are not set.	
			0	Normal operation
			1	Power-down
10	ISOLATE	0	0	Normal Operation
			1	Isolate
9	RESTART_AUTO_ NEGOTIATION	SC	Auto-negotiation automatically restarts after hardware or software reset regardless of whether or not this bit is set	
			0	Normal operation
			1	Restart auto-negotiation process
8	DUPLEX MODE	Update	After completing auto-negotiation, this bit reflects duplex status	
			0	Half-duplex
			1	Full-duplex
7	COLLISION TEST	0	Setting this bit to 1 causes the COL pin to assert whenever the TX_EN pin is asserted. This bit takes effect only when in 10M loopback mode.	
			0	Disable COL signal test
			1	Enable COL signal test
6	SPEED SELECTION (MSB)	Update	See description in bit ["13"]	
5:0	RES	00000	Reserved. Always set to 00000.	

4.1.2 Status

Offset: 0x01
Mode: Read-Only
Hardware Reset: See field descriptions
Software Reset: See field descriptions

Bit	Name	HW Reset	SW Reset	Description	
15	100BASE-T4	0	0	100BASE-T4: this protocol is not available	
				0	PHY not able to perform 100 BASE-T4
14	100BASE-X FULL-DUPLEX	1	1	Capable of 100-Tx full duplex operation	
13	100BASE-X HALF-DUPLEX	1	1	Capable of 100-Tx half duplex operation	
12	10 MBPS FULL-DUPLEX	1	1	Capable of 10 Base-T full duplex operation	
11	10 MBS HALF-DUPLEX	1	1	Capable of 10 Base-T half duplex operation	
10	100BASE-T2 FULL-DUPLEX	0	0	Not able to perform 100 Base-T2	
9	100BASE-T2 HALF-DUPLEX	0	0	Not able to perform 100 Base-T2	
8	EXTENDED STATUS	1	1	Extended status information	
7	RESERVED	0	0	Always 0	
6	MF PREAMBLE SUPPRESSION	1	1	PHY accepts management frames with preamble suppressed	
5	AUTO-NEGOTIATION COMPLETE	0	0	0	Auto negotiation process not complete
				1	Auto negotiation process complete
4	REMOTE FAULT	0	0	This bit clears after read “SC”.	
				0	Remote fault condition detected.
				1	Remote fault condition not detected
3	AUTO-NEGOTIATION ABILITY	1	1	PHY able to perform auto negotiation	
2	LINK STATUS	0	0	Indicates whether the link was lost since the last read. For the current link status, read LINK_REAL_TIME (bit [10]) of the register “PHY-Specific Status” on page 25. Latching low function.	
				0	Link is down
				1	Link is up
1	JABBER DETECT	0	0	This bit clears after read “SC”.	
				0	Jabber condition not detected
				1	Jabber condition detected
0	EXTENDED CAPABILITY	1	1	Extended register capabilities	

4.1.3 PHY Identifier [18:3]

Offset: 0x02
Mode: Read-Only
Hardware Reset: 0x004D
Software Reset: 0x004D

Bit	Name	Description
15:0	Unique Identifier Bit	Organizationally unique identifier bits [18:3]

4.1.4 PHY Identifier [19:24]

Offset: 0x03
Mode: Read-Only
Hardware Reset: 0xD021
Software Reset: 0xD021

Bit	Name	Description
15:0	OUI LSB Model Revision	Organizationally unique identifier bits [19:24]

4.1.5 Auto-Negotiation Advertisement

Offset: 0x04
Mode: Read/Write
Hardware Reset: 0x0DE1
Software Reset: See field descriptions

Bit	Name	SW Reset	Description	
15	NEXT_PAGE	Update	Should be set to 0 if no additional next pages are needed	
			0	Not advertised
			1	Advertise
14	ACK	0	Must be set to 0	
13	REMOTE FAULT	Update	0	Do not set remote fault bit
			1	Set remote fault bit
12	RES	0	Reserved	
11	ASYMMETRIC PAUSE	Update	0	No asymmetric pause
			1	Asymmetric pause
10	PAUSE	Update	A write to this register bit does not take effect until one of the following also occurs: ■ Software reset asserts (see RESET (bit [15] of the register "Control" on page 18) ■ Restart auto-negotiation asserts (see AUTO_NEGOTIATION (bit [9] of the "Control" register) ■ Power-down transitions from power-down to normal operation (see POWER_DOWN (bit [11] of the "Control" register) ■ The link goes down	
			0	MAC PAUSE not implemented
			1	MAC PAUSE implemented
9	100BASE-T4	0	Not able to perform 100 Base-T4	

Bit	Name	SW Reset	Description
8	100BASE-TX FULL DUPLEX	Update	A write to this register bit does not take effect until one of the following also occurs: ■ Software reset asserts (see RESET (bit [15] of the register "Control" on page 18) ■ Restart auto-negotiation asserts (see AUTO_NEGOTIATION (bit [9] of the "Control" register) ■ Power-down transitions from power-down to normal operation (see POWER_DOWN (bit [11] of the "Control" register) ■ The link goes down 0 Not advertised 1 Advertised
7	100BASE-TX HALF DUPLEX	Update	A write to this register bit does not take effect until one of the following also occurs: ■ Software reset asserts (see RESET (bit [15] of the register "Control" on page 18) ■ Restart auto-negotiation asserts (see AUTO_NEGOTIATION (bit [9] of the "Control" register) ■ Power-down transitions from power-down to normal operation (see POWER_DOWN (bit [11] of the "Control" register) ■ The link goes down 0 Not advertised 1 Advertised
6	10BASE-TX FULL DUPLEX	Update	A write to this register bit does not take effect until one of the following also occurs: ■ Software reset asserts (see RESET (bit [15] of the register "Control" on page 18) ■ Restart auto-negotiation asserts (see AUTO_NEGOTIATION (bit [9] of the "Control" register) ■ Power-down transitions from power-down to normal operation (see POWER_DOWN (bit [11] of the "Control" register) ■ The link goes down 0 Not advertised 1 Advertised
5	10BASE-TX HALF DUPLEX	Update	A write to this register bit does not take effect until one of the following also occurs: ■ Software reset asserts (see RESET (bit [15] of the register "Control" on page 18) ■ Restart auto-negotiation asserts (see AUTO_NEGOTIATION (bit [9] of the "Control" register) ■ Power-down transitions from power-down to normal operation (see POWER_DOWN (bit [11] of the "Control" register) ■ The link goes down 0 Not advertised 1 Advertised
4:0	SELECTOR FIELD	00001	Selector field mode 00001 802.3

4.1.6 Link Partner Ability (Base Page)

Offset: 0x05
Mode: Read-Only
Hardware Reset: 0
Software Reset: 0

Bit	Name	Description	
15	NEXT PAGE	Received code word bit [15]	
		0	Link partner not capable of next page
		1	Link partner capable of next page
14	ACK	Acknowledge; received code word bit [14]	
		0	Link partner does not have next page ability
		1	Link partner received link code word
13	REMOTE FAULT	Received code word bit [13]	
		0	Link partner has not detected remote fault
		1	Link partner detected remote fault
12	TECHNOLOGY ABILITY FIELD	This bit clears when the link goes down and loads when a base page is received. Received code word bit [12].	
11	ASYMMETRIC PAUSE	Received code word bit [11]	
		0	Link partner does not request asymmetric pause
		1	Link partner requests asymmetric pause
10	PAUSE	Received code word bit [10]	
		0	Link partner is not capable of pause operation
		1	Link partner is capable of pause operation
9	100BASE-T4	Received code word bit [9]	
		0	Link partner is not 100BASE-T4 capable
		1	Link partner is 100BASE-T4 capable
8	100BASE-TX FULL DUPLEX	Received code word bit [8]	
		0	Link partner is not 100BASE-TX full-duplex capable
		1	Link partner is 100BASE-TX full-duplex capable
7	100BASE-TX HALF DUPLEX	Received code word bit [7]	
		0	Link partner is not 100BASE-TX half-duplex capable
		1	Link partner is 100BASE-TX half-duplex capable
6	10BASE-TX FULL DUPLEX	Received code word bit [6]	
		0	Link partner is not 10BASE-T full-duplex capable
		1	Link partner is 10BASE-T full-duplex capable
5	10BASE-TX HALF DUPLEX	Received code word bit [5]	
		0	Link partner is not 10BASE-T half-duplex capable
		1	Link partner is 10BASE-T half-duplex capable
4:0	SELECTOR FIELD	Received code word bit [4:0]	

4.1.7 Auto-Negotiation Expansion

Offset: 0x06
Mode: Read-Only
Hardware Reset: 0x0004
Software Reset: Decided by the PHY inner state

Bit	Name	Description	
15:5	RES	Reserved. Must be set to 0.	
4	PARALLEL DETECTION FAULT	Software resets this bit to 0; clear after read	
		0	No fault has been detected
		1	A fault has been detected
3	LINK PARTNER NEXT PAGE ABLE	Software resets this bit to 0; clear after read	
		0	Link partner is not next page capable
		1	Link partner is next page capable
2	LOCAL NEXT PAGE ABLE	The software reset value is determined by bit [15] of the "Auto-Negotiation Advertisement" register.	
		0	Local device is not next page capable
		1	Local device is next page able
1	PAGE RECEIVED	On software reset, this bit value is reserved; LH; cleared after a read.	
		0	No new page has been received
		1	A new page has been received
0	LINK PARTNER AUTO-NEGOTIATION ABLE	Software reset to 0.	
		0	Link partner is not auto-negotiation capable
		1	Link partner is auto-negotiation capable

4.1.8 Function Control

Offset: 0x10
Mode: Read/Write
Hardware Reset: 0x0062
Software Reset: See field descriptions

Bit	Name	SW Reset	Description	
11	ASSERT_CRS_ON_TRANSMIT	Retain	This bit has no effect in full-duplex	
			0	Never assert on transmit
			1	Assert on transmit
9:8	ENERGY_DETECT	Retain	0x = Off	
			10	Sense only on Receive (Energy Detect)
			11	Sense and periodically transmit NLP
6:5	MDI_CROSSOVER_MODE	Update	Changes to these bits are disruptive to the normal operation; therefore any changes to this register must be followed by a software reset to take effect.	
			00	Manual MDI configuration
			01	Manual MDIX configuration
			10	Reserved
			11	Enable automatic crossover for all modes
4:3	RES	0	Reserved	
2	SQE_TEST	Retain	SQE Test is automatically disabled in full-duplex mode regardless of the state of this bit	
			0	SQE test disabled
			1	SQE test enabled
1	POLARITY_REVERSAL	Retain	If polarity is disabled, then the polarity is forced to be normal in 10BASE-T	
			0	Polarity reversal enabled
			1	Polarity reversal disabled
0	DISABLE_JABBER	Retain	0	Enable jabber function
			1	Disable jabber function

4.1.9 PHY-Specific Status

Offset: 0x11
Mode: Read-Only
Hardware Reset: 0x0010
Software Reset: 0

Bit	Name	Description	
15:14	SPEED	Valid only after resolved bit [11] of this register = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled.	
		00	10 Mbps
		01	100 Mbps
		10	Reserved
		11	Reserved
13	DUPLEX	Valid only after resolved bit [11] of this register = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled.	
		0	Half-duplex
		1	Full-duplex
12	PAGE_RECEIVED (real-time)	0	Page not received
		1	Page received
11	SPEED_DUPLEX_ RESOLVED	When Auto-Negotiation is not enabled, this bit = 1 for force speed	
		0	Not resolved
		1	Resolved
10	LINK (real-time)	0	Link down
		1	Link up
9:7	RES	Reserved. Always set to 0.	
6	MDI_CROSSOVER_ STATUS	Valid only after resolved bit [11] of this register = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. This bit is 0 or 1 depending on what is written to bits [6:5] of the register "Function Control" on page 24 in manual configuration mode. "Function Control" bits [6:5] are updated with software reset.	
		0	MDI
		1	MDIX
5	SMARTSPEED_ DOWNGRADE	0	Smartspeed downgrade does not occur
		1	Smartspeed downgrade occurs
4	ENERGY_DETECT_ STATUS	0	Active
		1	Sleep
3	TRANSMIT_PAUSE _ENABLED	Valid only after resolved bit [11] of this register = 1. The resolved bit is set when auto-negotiation is completed or disabled. A reflection of the MAC pause resolution.	
		0	Transmit pause disabled
		1	Transmit pause enabled
2	RECEIVE_ PAUSE_ENABLED	A reflection of the MAC pause resolution. This status bit is valid only after resolved bit [11] of this register = 1. The resolved bit is set when auto-negotiation is completed or disabled.	
		0	Receive pause disabled
		1	Receive pause enabled
1	POLARITY (real-time)	0	Normal
		1	Reversed
0	JABBER (real-time)	0	No jabber
		1	Jabber

4.1.10 Interrupt Enable

Offset: 0x12
Mode: Read/Write
Hardware Reset: 0
Software Reset: See field descriptions

Bit	Name	SW Reset	Description	
15	Auto-Negotiation Error Interrupt Enable	Retain	0	Interrupt disable
			1	Interrupt enable
14	Speed Changed Interrupt Enable	Retain	0	Interrupt disable
			1	Interrupt enable
13	Duplex Changed Interrupt Enable	Retain	0	Interrupt disable
			1	Interrupt enable
12	Page Received Interrupt Enable	Retain	0	Interrupt disable
			1	Interrupt enable
11	Auto-Negotiation Completed Interrupt Enable	Retain	0	Interrupt disable
			1	Interrupt enable
10	Link Status Changed Interrupt Enable	Retain	0	Interrupt disable
			1	Interrupt enable
9	Symbol Error Interrupt Enable	Retain	0	Interrupt disable
			1	Interrupt enable
8	False Carrier Interrupt Enable	Retain	0	Interrupt disable
			1	Interrupt enable
7	FIFO Over/ Underflow Interrupt Enable	Retain	0	Interrupt disable
			1	Interrupt enable
6	MDI Crossover Changed Interrupt Enable	Retain	0	Interrupt disable
			1	Interrupt enable
5	Smartspeed Interrupt Enable	Retain	0	Interrupt disable
			1	Interrupt enable
4	Energy Detect Interrupt Enable	Retain	0	Interrupt disable
			1	Interrupt enable
3:2	RES	0	Reserved. Always set to 00.	
1	Polarity Changed Interrupt Enable	Retain	0	Interrupt disable
			1	Interrupt enable
0	Jabber Interrupt Enable	0	0	Interrupt disable
			1	Interrupt enable

4.1.11 Interrupt Status

Offset: 0x13
Mode: Read-Only
Hardware Reset: 0

Note: All bits clear on read.

Bit	Name	Description	
15	AUTO _NEGOTIATION_ ERROR	An error is said to occur if MASTER/SLAVE does not resolve, parallel detect fault, no common HCD, or link does not come up after negotiation is completed.	
		0	No Auto-Negotiation Error
		1	Auto-Negotiation Error
14	SPEED_CHANGED	0	Speed not changed
		1	Speed changed
13	DUPLEX_ CHANGED	0	Duplex not changed
		1	Duplex changed
12	PAGE_RECEIVED	0	Page not received
		1	Page received
11	AUTO_ NEGOTIATION_ COMPLETED	0	Auto-Negotiation not completed
		1	Auto-Negotiation completed
10	LINK_STATUS _CHANGED	0	Link status not changed
		1	Link status changed
9	SYMBOL_ERROR	0	No symbol error
		1	Symbol error
8	FALSE_CARRIER	0	No false carrier
		1	False carrier
7	FIFO_OVER/ _UNDERFLOW	0	No FIFO Error
		1	Over/Underflow Error
6	MDI_CROSSOVER _CHANGED	0	Crossover not changed
		1	Crossover changed
5	SMARTSPEED _INTERRUPT	0	No Smartspeed interrupt detected
		1	Smartspeed interrupt detected
4	ENERGY_DETECT _CHANGED	0	No energy detect state change detected
		1	Energy detect state changed
3:2	RES	Reserved. Always set to 00.	
1	POLARITY_ CHANGED	0	Polarity not changed
		1	Polarity changed
0	JABBER	0	No jabber
		1	Jabber

4.1.12 Extended PHY-Specific Control

Offset: 0x14
Mode: Read/Write
Hardware Reset: 0x02C
Software Reset: See field descriptions

Bit	Name	SW Reset	Description	
15:8	RES	0	Reserved. Must be set to 00000000.	
7	CFG_PAD_EN	0	0	(Default) Auto-negotiation arbitration FSM does not bypass the LINK_STATUS_CHECK state
			1	Auto-negotiation arbitration FSM bypasses the LINK_STATUS_CHECK state when the 10 baset/100 baset ready signal is asserted
6	MR_LTDIS	Update	0	The NLP receive link integrity test FSM does not stay at the NLP_TEST_PASS state
			1	The NLP receive link integrity test FSM stays at the NLP_TEST_PASS state
5	SMARTSPEED_EN	Update	The default value is one; if this bit is set to one and cable inhibits completion of the training phase, then after a few failed attempts, the device automatically adjusts the highest ability to the next lower speed: from 100 to 10.	
4:2	SMARTSPEED_RETRY_LIMIT	Update	The default value is three; if set to three, then the device attempts five times before adjusting; the number of attempts can be changed through setting these bits.	
			000	2 retries
			001	3 retries
			010	4 retries
			011	5 retries (default)
			100	6 retries
			101	7 retries
			110	8 retries
			111	9 retries
1	BYPASS_SMARTSPEED_TIMER	Update	0	The stable link condition is determined 2.5 seconds after the link is established (default)
			1	The stable link condition is determined as soon as the link is established
0	RES	Update	Reserved. Must be set to 0.	

4.1.13 Receive Error Counter

Offset: 0x15
Mode: Read/Write
Hardware Reset: 0
Software Reset: 0

Bit	Name	Description
15:0	RO_MODE_ RECEIVE_ERROR_ COUNT	The counter pegs at 0xFFFF and does not roll over. (Only for 100Base-T)

4.1.14 Virtual Cable Tester Control

Offset: 0x16
Mode: Read/Write
Hardware Reset: 0
Software Reset: 0

Bit	Name	Description	
15:10	RES	Reserved	
9:8	MDI_PAIR_ SELECT	Cable defect tester (CDT) control registers Use the cable defect tester control registers to select which MDI pair is shown in the register "Virtual Cable Tester Status" on page 31.	
		00	MDI[0] pair
		01	MDI[1] pair
		10	Reserved
		11	Reserved
7:1	RES	Reserved	
0	ENABLE_TEST	When set, hardware automatically disable this bit when CDT is done	
		0	Disable CDT Test
		1	Enable CDT Test

4.1.15 LED Control

Offset: 0x18
Mode: Read/Write
Hardware Reset: 0x4100
Software Reset: No default on software reset

Bit	Name	Description			
15	DISABLE_LED	0	Enable		
		1	Disable		
14:12	LED_ON_TIME	000	5 ms	100	84 ms
		001	10 ms	101	168 ms
		010	21 ms	111:110	42 ms
		011	42 ms		
11	RES	Reserved			
10:8	LED_OFF_TIME	000	21 ms	100	330 ms
		001	42 ms	101	671 ms
		010	84 ms	111:110	168 ms
		011	168 ms		
7:5	RES	Reserved			
4:3	LED_LINK_ CONTROL	00	Direct LED mode		
		11	Master/slave LED mode		
		01, 10	Combined LED modes		
2	LED_DUPLEX_ CONTROL	0	Duplex		
		1	Duplex/Collision		
1	LED_RX_CONTROL	0	Receive activity		
		1	Receive activity and link		
0	LED_TX_CONTROL	0	Transmit activity		
		1	Transmit activity and link		

4.1.16 Manual LED Override

Offset: 0x19
Mode: Read/Write
Hardware Reset: 0
Software Reset: 0

Bit	Name	Description	
15:12	RES	Reserved	
11:10	LED_DUPLEX	■ LED OFF: LED pin output is high ■ LED ON: LED pin output is low	
		00	Normal
		01	Blink
		10	LED Off
		11	LED On
9:8	LED_LINK10	■ LED OFF: LED pin output is high ■ LED ON: LED pin output is low	
		00	Normal
		01	Blink
		10	LED Off
		11	LED On
7:6	LED_LINK100	■ LED OFF: LED pin output is high ■ LED ON: LED pin output is low	
		00	Normal
		01	Blink
		10	LED Off
		11	LED On
5:4	RES	Reserved	
3:2	LED_RX	■ LED OFF: LED pin output is high ■ LED ON: LED pin output is low	
		00	Normal
		01	Blink
		10	LED Off
		11	LED On
1:0	LED_TX	■ LED OFF: LED pin output is high ■ LED ON: LED pin output is low	
		00	Normal
		01	Blink
		10	LED Off
		11	LED On

4.1.17 Virtual Cable Tester Status

Offset: 0x1C
Mode: Read-Only
Hardware Reset: 0
Software Reset: 0

Bit	Name	Description	
15:10	RES	Reserved	
9:8	STATUS	The content of this register applies to the cable pair selected in the register "Virtual Cable Tester Control" on page 29.	
		00	Valid test, normal cable (no short or open in cable)
		01	Valid test, short in cable
		10	Valid test, open in cable
		11	Link up state and cable untested
7:0	DELTA_TIME	Delta time to indicate distance	

4.1.18 Debug Port1 (Address Offset)

Offset: 0x1D
Mode: Read/Write
Hardware Reset: 0
Software Reset: 0

Bit	Name	Description
15:6	RES	Reserved
5:0	ADDRESS_OFFSET	Address index to access the debug registers

4.1.19 Debug Port2 (Data Port)

Offset: 0x1E
Mode: Read/Write
Hardware Reset: 0x024E
Software Reset: Decided by the "Analog Test Control" register.

Bit	Name	Description
15:0	DATA	Data contents of the debug registers as addressed by the "Debug Port1 (Address Offset)" register

4.2 Debug Register Descriptions

Table 4-3 summarizes the debug registers for the AR8012.

Table 4-3. **Debug Register Summary**

Offset	Register	Page
0x10	100BASE-Tx Test Mode Select	page 33
0x12	Test Configuration for 10BASE-T	page 33

4.2.20 100BASE-TX Test Mode Select

Offset: 0x10
Mode: Read/Write
Hardware Reset: 0
Software Reset: 0

Bit	Name	Description
15:6	RES	Reserved. Always set to 0.
5	TM100_ENA	Enable dig100 loopback test mode
4	PMD_LPBK_2	PMA loopback, test MLT-3 encoder and MLT-3 decoder
3	PMD_LPBK_1	PMD loopback, test scrambler and descrambler
2	PMA_LPBK_2	PMA loopback, test carrier detect and link monitor
1	PMA_LPBK_1	PMA loopback, test FEF generator and FEF detector
0	PCS_LPBK	PCS loopback, test PCS_TX and PCS_RX

4.2.21 Test Configuration for 10 Base-T

Offset: 0x12
Mode: Read/Write
Hardware Reset: 0
Software Reset: 0

Bit	Name		Description
15:3	RES	Reserved. Always set to 0.	
2	LOOPBACK_MODE_ SELECT	0	LPBK1 Shallow in loopback mode
		1	LPBK2 Deep in loopback mode
1:0	TEST_MODE	00	Normal
		01	Packet with all ones; 10 MHz sine wave
		10	Pseudo random
		11	Normal link pulse only

5. Package Dimensions

The AR8012 is packaged in a LQFP 48. The body size is 7 mm by 7 mm. The package drawings and dimensions are provided in Figure 5-1 and Table 5-1.

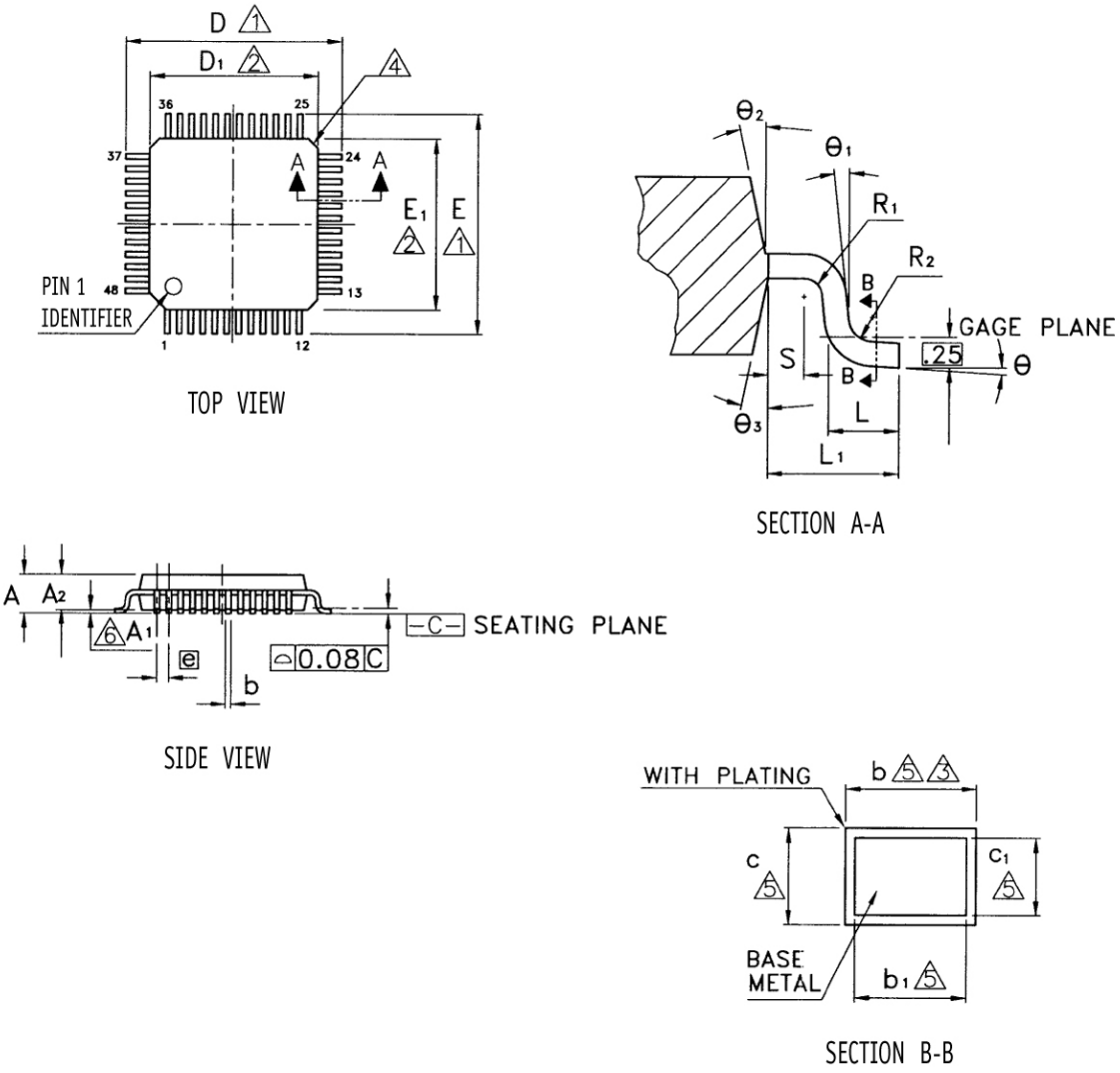

Figure 5-1. **Package Views**

Table 5-1. **Package Dimensions**

Dimension Label	Min	Nom	Max	Unit	Min	Nom	Max	Unit
A	—	—	1.60	mm	—	—	0.063	inches
A1	0.05	—	0.15	mm	0.002	—	0.006	inches
A2	1.35	1.40	1.45	mm	0.053	0.055	0.057	inches
b	0.17	0.22	0.27	mm	0.007	0.009	0.011	inches
b1	0.17	0.20	0.23	mm	0.007	0.008	0.009	inches
c	0.09	—	0.20	mm	0.004	—	0.008	inches
c1	0.09	—	0.16	mm	0.004	—	0.006	inches
D	9.00 BASIC			mm	0.354 BASIC			inches
D1	7.00 BASIC			mm	0.276 BASIC			inches
E	9.00 BASIC			mm	0.354 BASIC			inches
E1	7.00 BASIC			mm	0.354 BASIC			inches
e	0.50 BASIC			mm	0.020 BASIC			inches
L	0.45	0.60	0.75	mm	0.018	0.024	0.030	inches
L1	1.00 REF				0.039 REF			
R1	0.08	—	—	mm	0.003	—	—	inches
R2	0.08	—	0.20	mm	0.003	—	0.008	inches
S	0.20	—	—	mm	0.008	—	—	inches
θ	0	3.5	7		0	3.5	7	°
θ1	0	—	—		0	—	—	°
θ2	12° TYP				12° TYP			
θ3	12° TYP				12° TYP			

Notes:
1. To be determined at seating plane C.
2. Dimensions D1 and E1 do not include mold protrusion.
3. Dimension b does not include dambar protrusion. Dambar can not be located on the lower radius of the foot.
4. Exact shape of each corner is optional.
5. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
6. A1 is defined as the distance from the seating plane to the lowest point of the package body.
7. Controlling dimension: millimeter.
8. Reference document: JEDEC MS-026, BBC.

6. Ordering Information

The order number AR8012-BG1A specifies a current version of the AR8012.

Document Number: 981-00072-001 MKG-0607 Rev. 1

Atheros Communications, Incorporated
5480 Great America Parkway
Santa Clara, CA 95054
t: 408/773-5200
f: 408/773-9940
www.atheros.com