UCC2960, UCC3960
PRIMARY-SIDE STARTUP CONTROLLER

SLUS430A – APRIL 1999 – REVISED DECEMBER 2000

- **Operates With Secondary-Side PWM Control**
- **Receives Isolated PWM Command Through a Pulse-Edge-Transformer**
- **Initial Free-Running Soft-Start Up with Duty-Cycle Clamping**
- **Up to 400-kHz Synchronizable Switching Frequency**
- **High-Current FET Drive (1.5-A Sink, 0.75-A Source)**
- **Overcurrent Protection**
- **Undervoltage Lockout with 2-V Hysteresis**
- **Low-Current Startup**

typical operating circuit

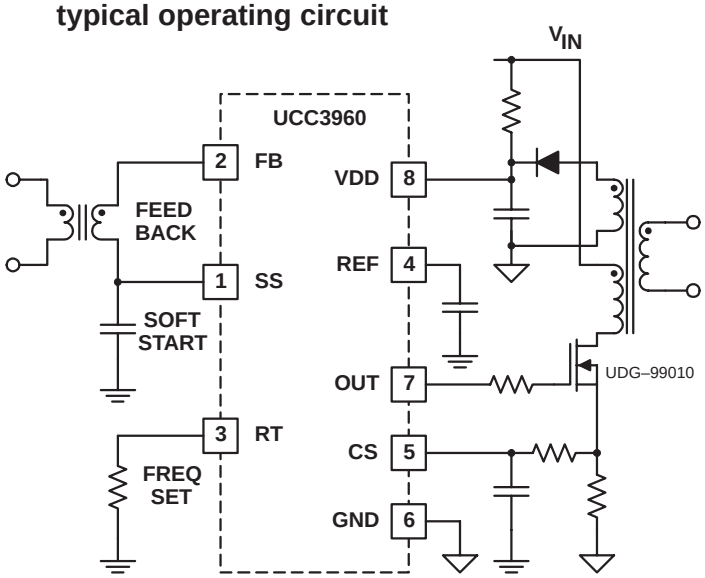


Figure 1

description

The UCC3960 primary-side startup controller is a unique solution that provides all the primary-side functions required for a single-ended, isolated offline, switch-mode power converter that uses secondary-side PWM control. It is usable with a wide range of secondary circuits and is especially well suitable for systems where sophisticated handling of overload conditions is required.

Secondary-side control assumes that output voltage and current measurements are interfaced directly to an output ground-referenced PWM stage that develops the power switch command for the supply. This digital PWM command can then be transmitted to the primary-side power switch through a simple and low-cost isolating pulse transformer. With secondary-side control, it is much easier to monitor and control the system load with tightly coupled analog control loops. Load-oriented features such as output current sharing and synchronous rectification are implemented more easily.

The UCC3960 provides all the circuitry required on the primary side of a secondary–side controlled power supply. It features a free running 60-kHz to 360-kHz oscillator that is synchronizable to the secondary-side PWM signal and also has the ability to accept start/stop PWM commands from the isolating pulse edge transformer. The use of an extremely small and low-cost pulse transformer allows for higher converter bandwidth. This also eliminates the loop-gain variations due to initial accuracy and aging of an opto-coupler feedback element or the size penalty of a gate transformer. It also includes an undervoltage lockout circuit with 2-V hysteresis, a low current startup with active low during UVLO, a soft-start capability, a 5-V reference and a high current power output.

In a non-typical use, the UCC3960 can accommodate an analog feedback signal through an opto-isolator where it can operate in voltage-mode control mode with primary-side peak current limiting.

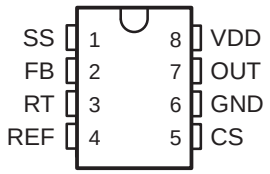
The UCC3960 and the UCC2960 are available in the 8-pin SOIC (D) and PDIP (P) packages. A 14-pin package version is available as UCC2961 and UCC3961 that includes additional protection features such as multimode overcurrent protection, volt-second clamp, programmable overvoltage and undervoltage sense lines, and the self-bias regulator.

AVAILABLE OPTIONS

TA	PACKAGED DEVICES	
	SOIC–8 SMALL OUTLINE (D)	PDIP–8 PLASTIC DIP (P)
–40°C to 85°C	UCC2960D	UCC2960P
0°C to 70°C	UCC3960D	UCC3960P

† The SOIC (D) packages are available taped and reeled. Add an R suffix to the device type (e.g., UCC2960DR) to order quantities of 2500 devices per reel.

D OR P PACKAGE
(TOP VIEW)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†‡

Input voltage, $V_{I(VDD)}$ . . . . . 19 V
Input current, $I_{I(VDD)}$ . . . . . 25 V
Output current, I_O § . . . . . –1.5 A / 2 A
Reference current, I_{REF} . . . . . –7.5 mA
Output voltage: REF . . . . . –0.3 V to VDD+0.3 V
Input voltage: SS, RT, CS . . . . . –0.3 V to VDD+0.3 V
FB . . . . . –7.0 V to VDD+0.3 V
Operating junction temperature range, T_J . . . . . –55°C to 150°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ Unless otherwise indicated, voltages are reference to ground and currents are positive into and negative out of the specified terminals. Pulsed is defined as a less than 10% duty cycle with a maximum duration of 500 μs.

§ 4 nF load with 4-Ω series resistor.

electrical characteristics V_{DD} = 12 V, RT = 53.3 kΩ, C_{VDD} = 1 μF, C_{REF} = 0.1 mF, C_{SS} = 0.01 μF, R_{OUT} = 4 Ω, C_{OUT} = 1 nF and $T_A = T_J$ (unless otherwise stated)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Section (VDD)					
Clamp voltage	I_{VDD} = 10mA	16	17.5	19	V
Operating current	No load, C_{OUT} = 0	1.8	2.3	2.8	mA
Starting current	V_{DD} = 9V	100	150	200	μA
Undervoltage Lockout Section					
Start threshold voltage		9.5	10	10.5	V
Hysteresis voltage		1.7	2	2.3	V
Voltage Reference Section (REF)					
Reference voltage		4.75	5.0	5.25	V
Load regulation voltage	I_{REF} = 0 mA to –2.5 mA		3	5	mV
Line regulation voltage	V_{DD} = 10 V to 12 V		3	5	mV
Short-circuit current		8	10	16	mA
Soft-Start Section (SS)					
Discharge current	SD = 4.5 V Pulsed	3	5	7	μA
Charge current	SD = 4.5 V Pulsed	–5	–7	–10	μA
Low–threshold voltage		0.9	1	1.1	V
Clamp threshold voltage		4.5	5	5.5	V
ON resistance	V_{DD} = 7.5 V	2.5	3.3	5	kΩ
Current Sense Section (CS)					
Threshold voltage	Pulse–by–pulse	0.9	1	1.1	V
	Immediate	1.3	1.4	1.5	V
Input bias current	CS = 1.1 V pulsed			0.2	μA
Delay time CS to OUT		60	100	140	ns
ON resistance		600	800	1000	Ω
Oscillator Section					
Frequency		135	150	165	kHz
Frequency change with voltage	VDD = 10 V to 12 V		0.02	0.2	%/V
Minimum duty cycle			0%		
Maximum duty cycle		69%	72%	75%	
Output Section (OUT)					
Low-level output voltage	I_{OUT} = 100 mA (dc), See Note 1		0.7	1.0	V
High-level output voltage	I_{OUT} = –40 mA (dc) , See Note 2		0.56	1.0	V
Low-level output voltage during UVLO	I_{OUT} = 20 mA (dc), V_{DD} = 7.5V			1.5	V
Rise time			30	60	ns
Fall time			15	30	ns

NOTES: 1. OUT low, nominal of 0.7 V reflects the 3-Ω DMOS ON resistance plus 4-Ω R_{SERIES}.
2. OUT high (VDD – OUT) nominal of 0.56 V reflects the 10-W HVPMOS ON resistance plus 4-Ω R_{SERIES}

electrical characteristics V_{DD} = 12 V, RT = 53.3 kΩ, C_{VDD} = 1 μF, C_{REF} = 0.1 mF, C_{SS} = 0.01 μF, R_{OUT} = 4 Ω, C_{OUT} = 1 nF and $T_A = T_J$ (unless otherwise stated)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Feedback Section (FB)						
Input bias current	FB = 4.5 V,	SS = 0 V			0.4	μA
Negative compliance voltage	I_{FB} = –100 mA,	SS = 0 V	–6.8	–7.2	–7.6	V
Delay time, FB–SS to OUT, rising edge	FB–SS pulsed = 2 V,	FB = SS	40	70	100	ns
Delay time, FB–SS to OUT, falling edge	FB–SS pulsed = 2 V,	FB = SS	50	85	120	ns

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CS	5	I	Pulse-by-pulse and shutdown overcurrent sense input pin
FB	2	I	Control input for the signal from a secondary–side PWM controller
GND	6		Ground for the IC.
OUT	7	O	Drive pin for the MOSFET power switch
RT	3	I	Sets the free-running startup oscillator frequency.
REF	4	O	Output reference
SS	1	I	Primary-side soft-start function
VDD	8		Power input connection

detailed descriptions

current sense (CS)

This is the pulse-by-pulse and shutdown overcurrent sense input pin. This current-sense pin triggers a pulse-by-pulse termination anytime a 1.0-V threshold is exceeded while a signal in excess of 1.375 V on this pin initiates a complete shutdown. Since the CS pin can be noise sensitive, it is good practice to insert a small low-pass RC filter between this pin and the current sensor.

feedback (FB)

This is the control input for the signal from a secondary-side PWM controller whose pulse-width command has been differentiated by the feedback pulse edge transformer (PET) into positive *start* and negative *stop* pulses. These signals are used to turn on and off the primary power switch and must have an amplitude of at least $V_{SS} \pm 2.0$ V (4 V peak-to-peak) for at least 25 ns per pulse and no more than 200 ns per pulse. The maximum amplitude allowed on this pin is $V_{SS} \pm 7.0$ V.

output drive (OUT)

This drive pin for the N–channel MOSFET power switch sinks (1.5 A) and sources (0.75 A) fast, high-current gate drive pulses. During shutdown, this pin is self–biased to an active low state. A minimum of 4 W should be added in series with the output to ensure that the on-chip driver safe operating area is not exceeded. (Data from the IRF820/830/840 family of MOSFETs, commonly available in the TO–220 package, is used to derive this value. The gate charge needed to provide full enhancement was used to establish an equivalent capacitance of up to 4000 pF.)

detailed descriptions (continued)

ground (GND)

This pin is the reference point for grounding all analog functions and must be kept as clean as possible from all switching noise. It should be closely bypassed to VDD.

timing resistor (RT)

A resistor from this pin to GND establishes a current,

$$I_{SET} = \frac{2\ V}{RT} \quad (1)$$

which is mirrored internally for several functions. It establishes the free–running startup switching frequency with an internal capacitor according to the relationship,

$$fs = \frac{8.0 \times 10^9}{RT} \quad (2)$$

The startup oscillator has a rise and fall time set to limit the duty-cycle of the power switch to a maximum of 72%, a limit that is maintained even after the feedback signal takes command. The range of RT is 22.2 kΩ to 133 kΩ, giving a free-run frequency range range of 60 kHz to 360 kHz, respectively. Variations in the free-running oscillator frequency overtemperature are very small. The typical temperature coefficient is –40 Hz per degree Celsius, measured at 150 kHz.

voltage reference (REF)

This 5-V output is usable with external loads of up to 10 mA. The voltage is also the source for all internal analog threshold settings and should be bypassed with a minimum of 0.1-µF capacitance to GND.

soft-start (SS)

The pin implements the primary-side soft-start function. This is the connection point for an external capacitor that determines the rate of increase in commanded pulse width for the power switch at startup. It also serves as the ac ground return for the feedback pulse transformer to provide a tracking bias for the FB input.

power (VDD)

The power input connection for all the control circuitry conducts all the gate charge current for the power FET. It should be closely bypassed with at least 1.0-µF to GND. This pin is internally shunt regulated to clamp at 17.5 V to protect the internal components. So if a voltage source above this value is possible, external current limiting must be provided.

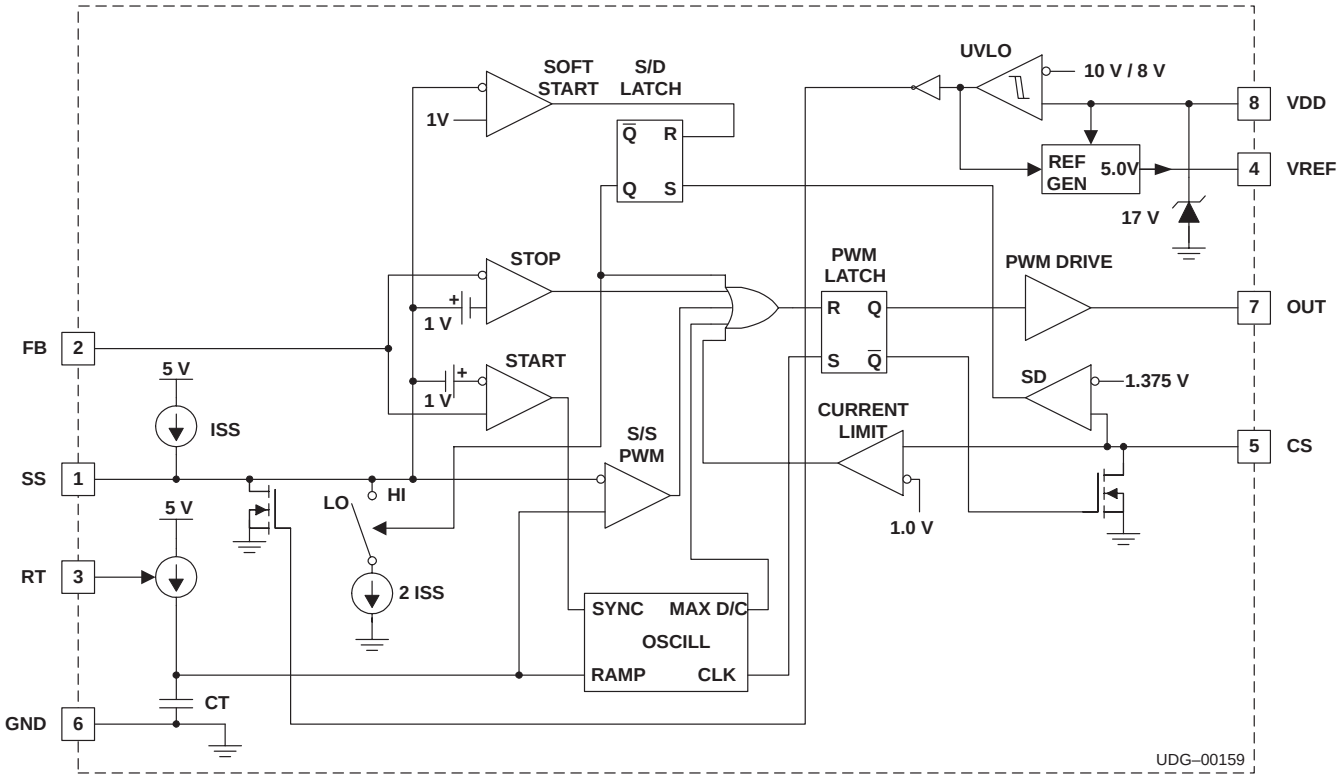


Figure 1. UCC3960 Block Diagram

DETAILED DESCRIPTION

startup oscillator

The RT pin is connected to an internal 2.0 V nominal, unity-gain closed-loop amplifier that is referenced to a voltage divider off the 5.0-V reference. When a 22.2-kΩ resistor is connected from the RT pin to GND an approximate I_{RT} = 90 mA internal current is realized that charges the internal oscillator capacitor, approximately 58 pF. I_{RT} = 90 mA produces a maximum free running oscillator frequency of 360 kHz at a 70% duty cycle. When a 133.3-kΩ resistor is connected from the RT pin to GND an approximate I_{RT} = 15 mA internal current is realized, which produces a minimum free running oscillator frequency of 60 kHz at approximately 72% duty cycle. This maximum duty cycle is setup by on-chip MOSFET current mirrors that are not programmable.

Any frequency between these two limits (6:1 maximum to minimum frequency) is obtainable by linearly scaling the RT resistance between the minimum 22.2-kΩ and maximum 133.3-kΩ values. The secondary-side PWM frequency should be fixed at (1 / 0.9) or 1.11 times the user programmed primary-side free running oscillator frequency for proper primary-side synchronization. Therefore, in all cases the recommended secondary-side synchronization frequency shall be 1.11 times higher than the selected primary-side free running startup frequency. Taking into consideration the two extreme limits for primary-side free running startup frequency, the secondary-side operating frequency should be set between 400 kHz and 67 kHz.

DETAILED DESCRIPTION

soft-start

The soft-start section contains all the circuitry required to produce a user programmable slowly increasing PWM duty cycle, starting from 0% to a maximum of 72%. The soft-start cycle is triggered either by the initial primary-side startup procedure or after any one of three user-programmable fault conditions and one fixed fault condition. The PWM duty cycle increases according to the charge rate of an user-selectable external soft-start capacitor, connected from the SS pin to GND. The SS capacitor is charged by a nominal 7-μA internal current source.

Should the CS pin rise in voltage above 1.375 V, a soft-start cycle is triggered. The soft-start cycle disables the output driver OUT and holds it in the low state until the capacitor connected from the SS pin to GND is discharged below 1.0 V by an internal 5-μA current sink. After this discharge period, the PMW output OUT is enabled and the duty cycle is allowed to slowly increase as before.

synchronization

The SS pin and the FB pin accepts the secondary-side of a small signal synchronization transformer. A series blocking capacitor inserted in the primary-side of the synchronization transformer is intended to differentiate the square-wave gate drive output of the secondary-side PWM controller while preventing the transformer from saturation. The soft-start capacitor also provides an ac GND at the SS pin or the synchronization transformer secondary. The small signal synchronization transformer provides galvanic isolation between primary and secondary side and must have adequate voltage breakdown rating between the primary and secondary windings.

Two comparators, with an approximate 1.0-V offset each, are connected to the FB pin to provide plus and minus differential voltage comparison with a 2.0-V deadband between the FB and SS pins. The 2.0-V deadband prevents inductive backswing of the small-signal transformer from giving false secondary-side pulse-edge detection.

Enough energy must be coupled into the comparator differential inputs to ensure reliable comparator switching. This requires sufficient voltage overdrive above the 1.0-V comparator threshold and a specified transformer circuit time constant to provide a minimum synchronization pulse width.

On receiving the first recognizable negative going voltage pulse (turnoff command) generated from the falling edge of the differentiated square-wave gate drive signal on the secondary-side, the PWM latch is reset and a synchronization latch is set. After this event, all primary-side PMW driver output is slaved to the secondary-side driver output in both frequency and duty cycle. The triggering of a soft-start cycle by a fault condition resets the synchronization latch to again allow the internal startup oscillator to control the PWM latch.

PWM

The PWM section consists of a reset dominant SR latch with necessary logical gating on the set input to allow control from the free running startup oscillator until feedback from the secondary-side PWM gate drive output is detected. After the occurrence of detectable feedback from the secondary-side gate driver, the control of the primary-side PWM latch is handed off to the secondary-side PWM controller. A nine-input OR gate on the PWM latch reset dominant input allows the numerous fault conditions to reset the PWM latch and control from either the startup oscillator or feedback from the secondary-side PWM output driver.

DETAILED DESCRIPTION

UVLO and REF

The under voltage lockout (UVLO) circuit enables normal operation after VDD exceeds the 10.0-V turnon threshold and permits operation until VDD falls below the 8-V turnoff threshold. While activated, the UVLO circuit holds the PWM gate driver output (OUT) and the internal-reference buffer amplifier output REF low. To insure proper soft-start, internal N-channel MOSFET switches discharge external capacitor connected to the SS pin during undervoltage conditions.

The 5-V internal reference is connected to the REF pin and must be bypassed using a good quality, high-frequency capacitor. This 5-V reference is not available externally while the chip is disabled by the under voltage lockout circuit.

current sense

The current sense (CS) circuit monitors the voltage across a ground referenced current sense resistor, connected between the source of the external power MOSFET and GND. The signal amplitude at the CS pin is compared to two thresholds, (1.0 V and 1.375 V respectively), by two independent voltage comparators.

A voltage level greater than 1.0 V, but less than 1.375 V, sets the reset dominant shutdown latch and resets the PWM latch. The SD latch is reset when the startup oscillator arrives at its 4.0-V threshold.

During the OFF period of the PWM latch, any capacitance connected to the CS pin is discharged to GND potential by an internal 800-Ω device.

VDD clamp

To insure that the absolute maximum voltage ratings of internal devices are not violated, an internal shunt voltage regulator is provided to clamp the VDD pin at a nominal 17.5-V maximum voltage. Similarly to other shunt or Zener-like voltage regulator circuits, the current through the internal VDD clamp must be limited below the maximum current level indicated in the datasheet. In addition to limiting the current through the clamp circuit, the maximum power dissipation capability of the particular package used in the application has to be considered.

OUT driver

An internal output driver (OUT) is provided to drive the gate of an external N–channel power MOSFET. The output driver consists of a nominal 4.0-Ω ON-resistance P-channel MOSFET for turnon, and a nominal 2.0-Ω ON-resistance D–channel MOSFET used during the turn–off of the external MOSFET transistor. An external series gate resistance is specified to maintain an acceptable SOA (Safe Operating Area) for the DMOS device of the internal output driver. As discussed in the UVLO section before, the under voltage lockout (UVLO) circuit holds the PWM gate driver output low while UVLO conditions exists.

APPLICATION INFORMATION

The evaluation circuit of the UCC3960 as the primary-side startup circuit and UC38C45 as the secondary-side controller is shown in Figure 2.

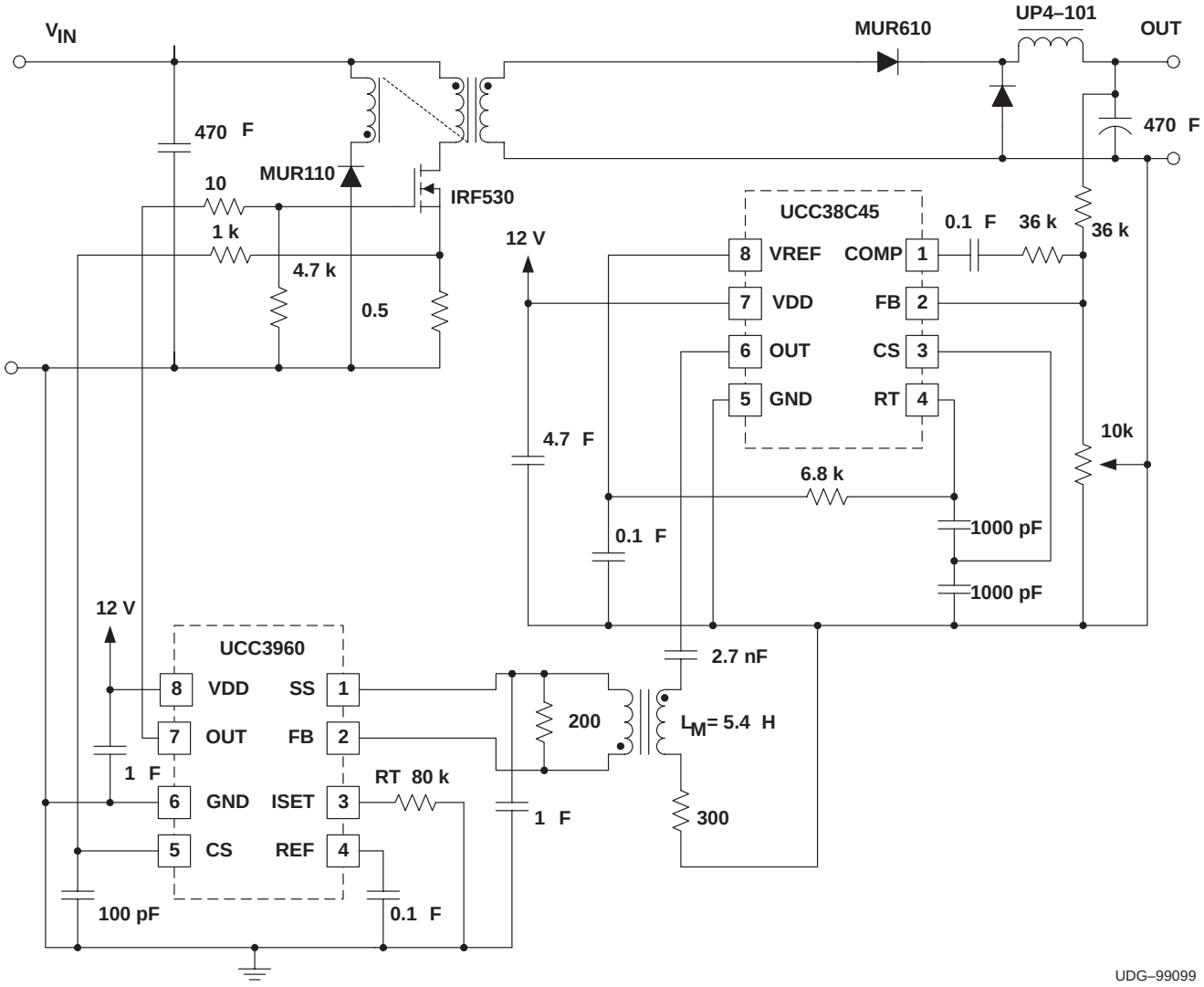


Figure 2. Evaluation Circuit UCC3960

APPLICATION INFORMATION

pulse-edge transmission circuit

The UCC3960 uses a pulse-edge-transmission (PET) circuit to transmit isolated gate-pulse information from the secondary-side controller. It is important for the PET circuitry to have proper frequency response and adequately high damping (low Q-factor) in order to precent excessive overshoot. The circuit is shown in Figure 3.

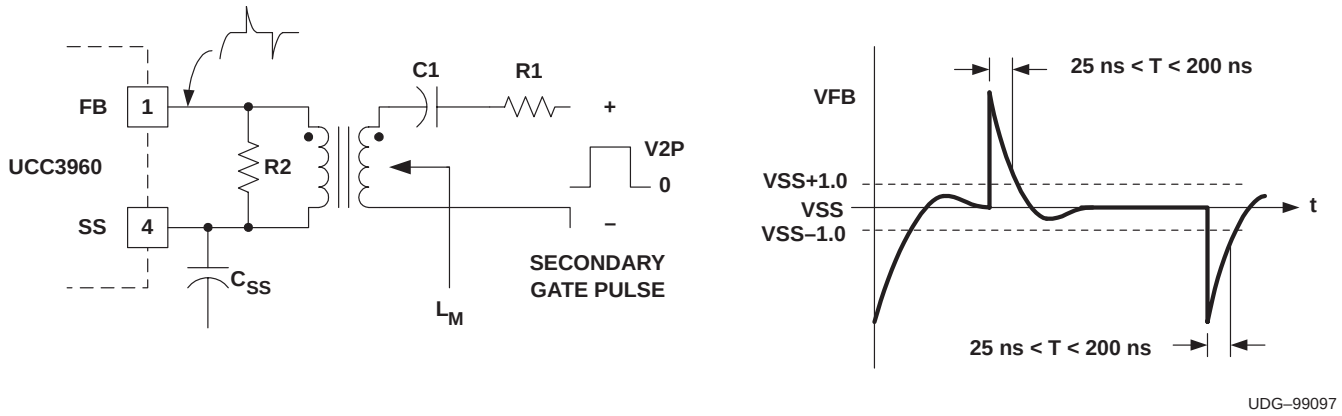


Figure 3. Pulse Edge Transmission (PET) Circuit

The pulse width measured at the FB pin must be less than 25 ns when measured at 1 V above the soft-start voltage and 200 ns when measured at 1 V below the soft-start voltage. The feedback (FB) voltage must not be overdriven by more than 5 V above or 5 V below the soft-start voltage. In order to prevent false triggering, the feedback voltage must not ring below the soft-start voltage by more than ±0.9 V. This can be met if the PET circuit has a resonant frequency of 880 kHz and a Q of 0.25. The following values meet those specifications for a 12-V segondary gate pulse signal, over the full range of UCC3960 operating frequencies.

T1 1:1 turns ratio, LM = 5.4-µH, Ferronics 11–622J, N1 = N2 = 4 turns

R1 300 Ω

C1 2700 pF

R2 200 Ω

Pulse-edge-transmission (PET) circuits in standard surface-mount packages are available from Pulse Engineering (Part #PA0128, Part #PA0115) and from Cooper Electronic Technologies (Coiltronix), (Part #CTX01–15157).

PARAMETER MEASUREMENT INFORMATION

NORMAL OPERATING WAVEFORMS

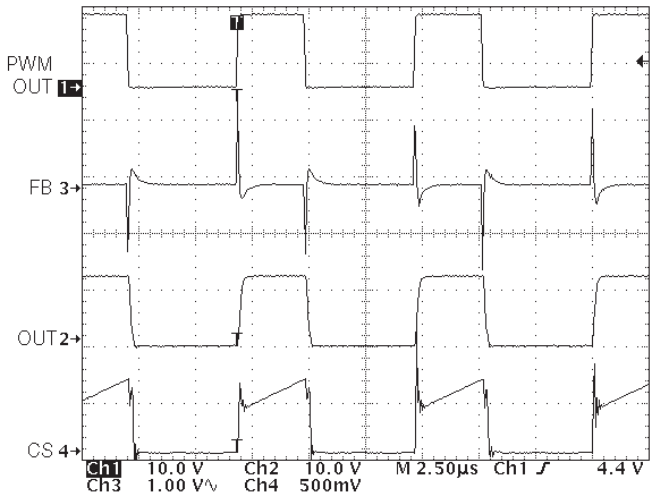


Figure 4

OPERATING WAVEFORMS DURING OVERLOAD

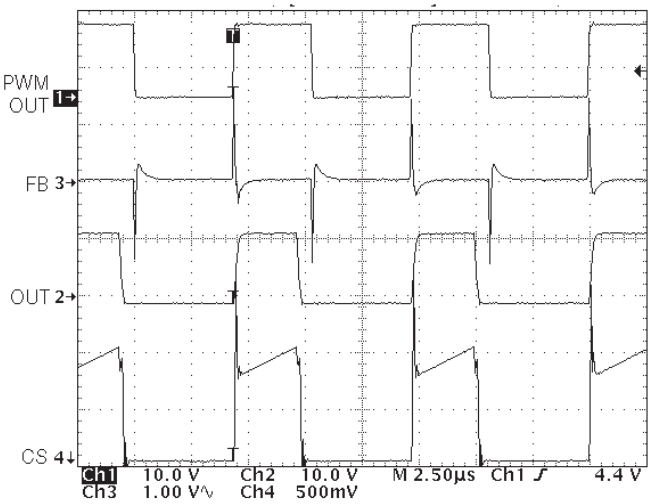


Figure 5

OPERATING WAVEFORMS DURING NO LOAD

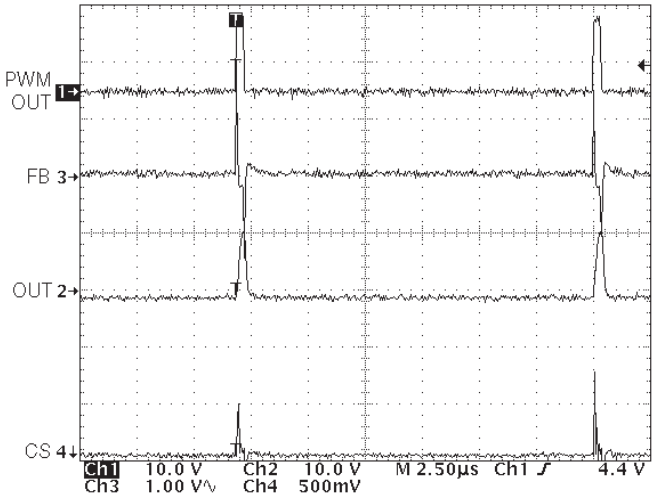


Figure 6

ADDITIONAL REFERENCES

1. Dennis, Mark and Michael Madigan, *50-W Forward Converter with Synchronous Rectification and Secondary-Side Control*, SEM–1300, Topic 4, Texas Instruments Literature Number SLUP002.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC2960D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UCC2960	Samples
UCC3960D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC3960	Samples
UCC3960P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	UCC3960P	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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