Am25LS160A/161A/162A/163A
Am54LS/74LS160A/161A/162A/163A
Synchronous Four-Bit Counters

DISTINCTIVE CHARACTERISTICS

- Synchronous presettable counters
- Decade ('LS160A and 'LS162A) and binary ('LS161A and 'LS163A) counters
- Asynchronous ('LS160A and 'LS161A) and synchronous ('LS162A and 'LS163A) clear inputs
- Am25LS devices offer the following improvements over Am54/74LS
  - Higher speed
  - 50mV lower V_{OL}
  - Twice the fan-out over military range
  - 440μA source current
- 100% product assurance screening to MIL-STD-883 requirements

FUNCTIONAL DESCRIPTION

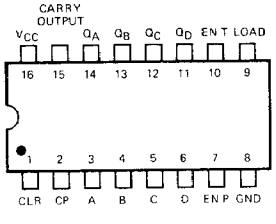
The Am25LS160A, Am25LS161A, Am25LS162A and Am25LS163A synchronous, presettable counters have internal look-ahead carry and ripple carry output for high-speed counting applications. The Am25LS160A and Am25LS162A are decade counters and the Am25LS161A and Am25LS163A are 4-bit binary counters. Counting or loading occurs on the positive transition of the clock pulse. A LOW level on the load input causes the data on the A, B, C and D inputs to be shifted to the appropriate Q outputs on the next positive clock transition. The load need meet only the set-up and hold time requirements with respect to the clock.

The Am25LS160A and the Am25LS161A feature an asynchronous clear. A LOW level at the clear input sets the Q outputs LOW regardless of the other inputs. The Am25LS 162A and Am25LS163A have a synchronous clear. A LOW level at the clear input sets the Q outputs LOW after the next positive clock transition regardless of the enable inputs.

Both count-enable inputs P and T must be HIGH to count. Count enable T is included in the ripple carry output gate for cascading connection. The enable P or T inputs need meet only the set-up and hold time requirements with respect to the clock.

The Am54LS/74LS160A series are standard performance versions of the Am25LS160A series counters. See appropriate electrical characteristic tables for detailed Am25LS improvements.

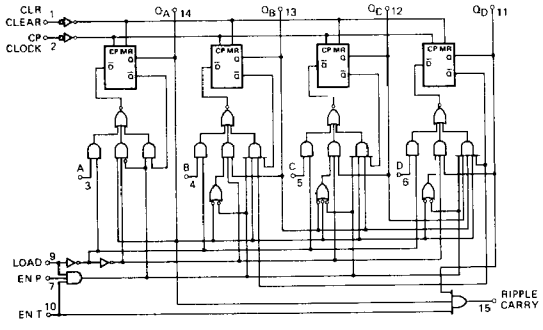
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

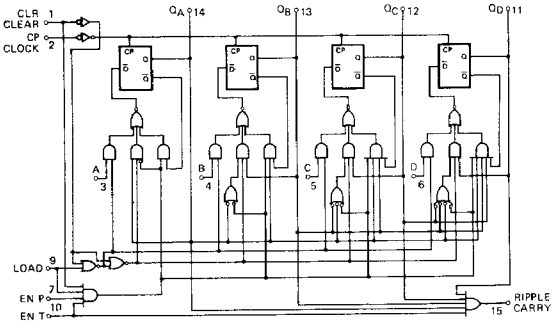
LOGIC DIAGRAMS

Am25LS160A Synchronous Decade Counter



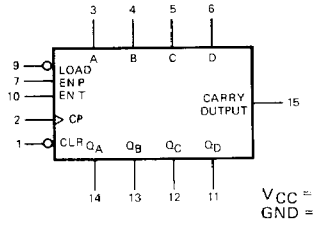
Am25LS162A synchronous decade counters are similar; however, the clear is synchronous as shown for the Am25LS163A binary counters.

Am25LS163A Synchronous Binary Counter



Am25LS161A synchronous binary counters are similar; however, the clear is asynchronous as shown for the Am25LS160A decade counters.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

Am54LS/74LS160A, 161A, 162A and 163A

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ (MIN. = 4.75V MAX. = 5.25V)

MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ (MIN. = 4.50V MAX. = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −400μA V_{IN} = V_{IH} or V_{IL}	MIL	2.5	3.4		Volts
			COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN. V_{IN} = V_{IH} or V_{IL}	All, I_{OL} = 4mA		0.25	0.4	Volts
			74LS only, I_{OL} = 8mA		0.35	0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V	A, B, C, D, EN P			−0.4	mA
			Load, EN T, CP			−0.8	
			Clear '160A, '161A			−0.4	
			Clear '162A, '163A			−0.8	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V	A, B, C, D, EN P			20	μA
			Load, CP, EN T			40	
			Clear '160A, '161A			20	
			Clear '162A, '163A			40	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 7.0V	A, B, C, D, EN P			0.1	mA
			Load, CP, EN T			0.2	
			Clear '160A, '161A			0.1	
			Clear '162A, '163A			0.2	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.		−15		−100	mA
I_{CCH}	Power Supply Current All Outputs HIGH	V_{CC} = MAX. (Note 4)			18	31	mA
I_{CCL}	Power Supply Current All Outputs LOW	V_{CC} = MAX. (Note 5)			19	32	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. I_{CCH} is measured with the load input HIGH, then again with the load input LOW, with all other inputs HIGH and all outputs open.
5. I_{CCL} is measured with the clock input HIGH, then again with the clock input LOW, with all other inputs LOW and all outputs open.

SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description		Am25LS Min.	Am25LS Typ.	Am25LS Max.	Am54LS/74LS Min.	Am54LS/74LS Typ.	Am54LS/74LS Max.	Units	Test Conditions
t_{PLH}	Clock to Carry Output			20	30		20	35	ns	C_L = 15pF, R_L = 2.0kΩ
t_{PHL}				18	28		18	35		
t_{PLH}	Clock to Q Output with Load Input HIGH			10	18		13	24	ns	
t_{PHL}				12	20		18	27		
t_{PLH}	Enable T to Carry Output			8	14		9	14	ns	
t_{PHL}				8	14		9	14		
t_{PLH}	Clock to Q Output with Load Input LOW			10	18		13	24	ns	
t_{PHL}				12	20		18	27		
t_{PHL}	Clear to Q Output (Note 1)			18	28		20	28	ns	
t_{pw}	Pulse Width	Clock	25			25			ns	
		Clear	20			20				
t_s	Set-up Time	Data – A, B, C, D	20			20			ns	
		Enable P	20			20				
		Load, Enable T	20			20				
		Clear (Note 2)	20			20				
t_h	Hold Time – Any Input		3			3			ns	
f_{max} (Note 3)	Maximum Clock Frequency		35	50		25	32		MHz	

Notes: 1. Measured from clear input on 'LS160A and 'LS161A. Measured from clock input on 'LS162A and 'LS163A.
2. Applies to 'LS162A and 'LS163A only.
3. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

Am25LS ONLY SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description		Am25LS COM'L T_A = 0°C to +70°C, V_{CC} = 5.0V ±5% Min.	Am25LS COM'L Max.	Am25LS MIL T_A = −55°C to +125°C, V_{CC} = 5.0V ±10% Min.	Am25LS MIL Max.	Units	Test Conditions
t_{PLH}	Clock to Carry Output			43		50	ns	C_L = 50pF, R_L = 2.0kΩ
t_{PHL}				40		47		
t_{PLH}	Clock to Q Output with Load Input HIGH			28		32	ns	
t_{PHL}				30		35		
t_{PLH}	Enable T to Carry Output			18		21	ns	
t_{PHL}				18		21		
t_{PLH}	Clock to Q Output with Load Input LOW			28		32	ns	
t_{PHL}				30		35		
t_{PHL}	Clear to Q Output (Note 1)			41		47	ns	
t_{pw}	Pulse Width	Clock	37		42		ns	
		Clear	30		35			
t_s	Set-up Time	Data – A, B, C, D	30		35		ns	
		Enable P	30		35			
		Load, Enable T	30		35			
		Clear (Note 2)	30		35			
t_h	Hold Time – Any Input		8		9		ns	
f_{max} (Note3)	Maximum Clock Frequency		26		23		MHz	

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

3

DEFINITION OF FUNCTIONAL TERMS

CP Clock pulse. Enters data or counts on the positive-going edge.

CLR Clear. On the Am25LS160A and Am25LS161A, the clear is asynchronous. A LOW on the clear sets all four flip-flops LOW. On the Am25LS162A and Am25LS163A the clear is synchronous. A LOW on the clear sets all four flip-flops LOW after the next positive-going clock edge.

Load Load. When the load is LOW, data on the A, B, C and D inputs is transferred to the output on the positive-going clock edge. When the load is HIGH, the counter is enabled.

EN P Enable P. Parallel count enable. Must be HIGH to count.

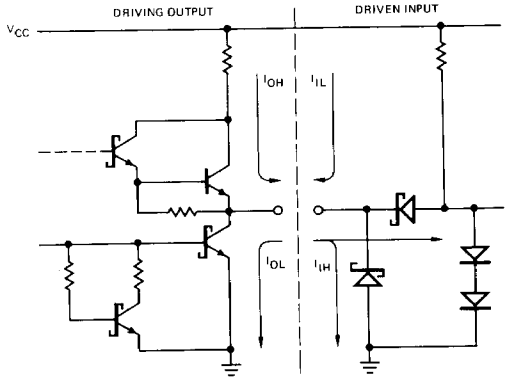
EN T Enable T. Serial trickle count enable. Must be HIGH to count.

A, B, C, D The four counter parallel inputs.

Q_A, Q_B, Q_C, Q_D The four counter outputs.

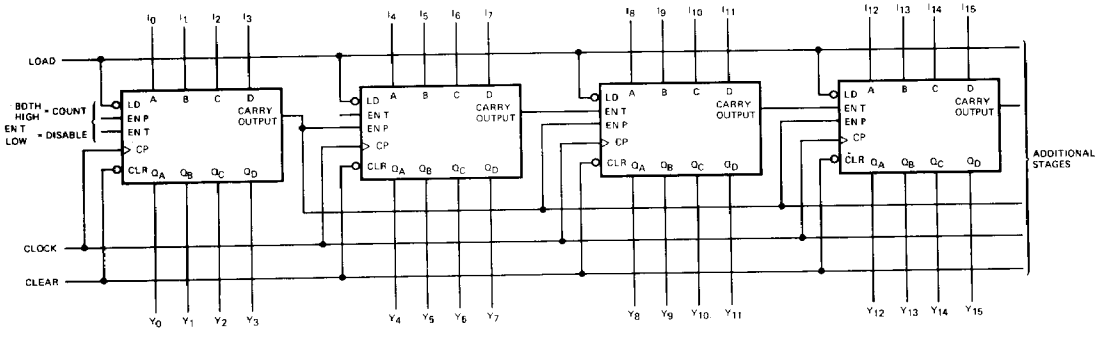
Carry Output Carry look-ahead circuitry for cascading. Will be HIGH when the four-bit counter is maximum (1001 for BCD and 1111 for binary).

Am25LS • Am54LS/74LS LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



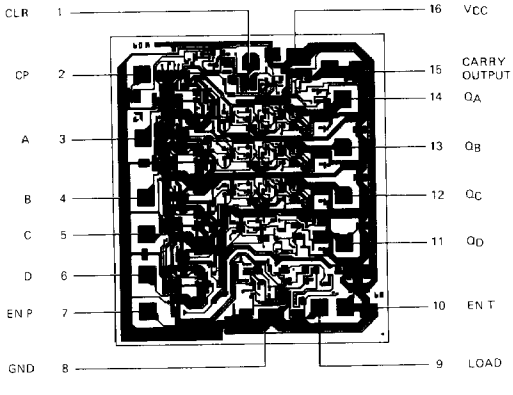
Note: Actual current flow direction shown.

APPLICATIONS



High-speed, look-ahead carry counter for BCD (Am25LS160A or Am25LS162A) or binary (Am25LS161A or Am25LS163A). Can count modulo N, N_1-to-N_2, or N_1-to-N maximum.

Metallization and Pad Layout



DIE SIZE 0.072" X 0.082"

IMAGE UNAVAILABLE