

MM54HC354/MM74HC354/ MM54HC356/MM74HC356 8-Channel TRI-STATE® Multiplexers with Latches

General Description

The MM54HC354/MM74HC354 and MM54HC356/MM74HC356 utilize advanced silicon-gate CMOS technology. They exhibit the high noise immunity and low power dissipation of standard CMOS integrated circuits, along with the ability to drive 15 LS-TTL loads. Due to the large output drive capability and the TRI-STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system.

These data selectors/multiplexers contain full on-chip binary decoding to select one of eight data sources. The data select address is stored in transparent latches that are enabled by a low level address on pin 11, \overline{SC} . Data on the 8 input lines is stored in a parallel input/output register which in the MM54HC354/MM74HC354 is composed of 8 transparent latches enabled by a low level on pin 9, \overline{DC} , and in the MM54HC356/MM74HC356 is composed of 8 edge-triggered flip-flops, clocked by a low to high transition on pin 9, CLK. Both true (Y) and complementary (W) TRI-STATE outputs are available on both devices.

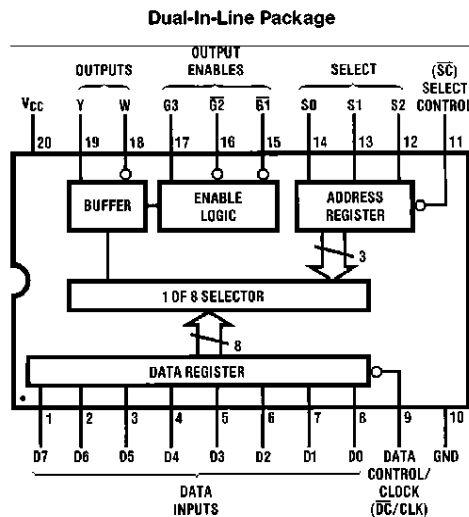
The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS-TTL logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Transparent latches on data select inputs
- Choice of data registers:
 - Transparent (*354)
 - Edge-triggered (*356)
- TRI-STATE complementary outputs with fanout of 15 LS-TTL loads
- Typical propagation delay:
 - Data to output (*354): 32 ns
 - Clock to output (*346): 35 ns
- Wide power supply range: 2V–6V
- Low quiescent supply current: 80 μ A maximum
- Low input current: 1 μ A maximum

MM54HC354/MM74HC354/MM54HC356/MM74HC356
8-Channel TRI-STATE Multiplexers with Latches

Connection Diagram



TL/F/5208-1

Top View

Order Number MM54HC354/356 or MM74HC354/356

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Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|--|--------------------------|
| Supply Voltage (V_{CC}) | -0.5V to +7.0V |
| DC Input Voltage (V_{IN}) | -1.5V to $V_{CC} + 1.5V$ |
| DC Output Voltage (V_{OUT}) | -0.5V to $V_{CC} + 0.5V$ |
| Clamp Diode Current (I_{CD}) | ± 20 mA |
| DC Output Current, per pin (I_{OUT}) | ± 35 mA |
| DC V_{CC} or GND Current, per pin (I_{CC}) | ± 70 mA |
| Storage Temperature Range (T_{STG}) | -65°C to +150°C |
| Power Dissipation (P_D) (Note 3) | 600 mW |
| S.O. Package only | 500 mW |
| Lead Temp. (T_L) (Soldering 10 seconds) | 260°C |

Operating Conditions

| | Min | Max | Units |
|--|-----|----------|-------|
| Supply Voltage (V_{CC}) | 2 | 6 | V |
| DC Input or Output Voltage (V_{IN} , V_{OUT}) | 0 | V_{CC} | V |
| Operating Temp. Range (T_A) | | | |
| MM74HC | -40 | +85 | °C |
| MM54HC | -55 | +125 | °C |
| Input Rise or Fall Times (t_r , t_f) | | | |
| $V_{CC} = 2.0V$ | | 1000 | ns |
| $V_{CC} = 4.5V$ | | 500 | ns |
| $V_{CC} = 6.0V$ | | 400 | ns |

DC Electrical Characteristics (Note 4)

| Symbol | Parameter | Conditions | V_{CC} | $T_A = 25^\circ C$ | | | 74HC | | 54HC | | Units |
|----------|--|---|----------|--------------------|-------------------|-----------|-----------------------------|---------|------------------------------|--|-------|
| | | | | | | | $T_A = -40$ to $85^\circ C$ | | $T_A = -55$ to $125^\circ C$ | | |
| | | | | Typ | Guaranteed Limits | | | | | | |
| V_{IH} | Minimum High Level Input Voltage | | 2.0V | | 1.5 | 1.5 | 1.5 | 1.5 | V | | |
| | | | 4.5V | | 3.15 | 3.15 | 3.15 | 3.15 | V | | |
| | | | 6.0V | | 4.2 | 4.2 | 4.2 | 4.2 | V | | |
| V_{IL} | Maximum Low Level Input Voltage** | | 2.0V | | 0.5 | 0.5 | 0.5 | 0.5 | V | | |
| | | | 4.5V | | 1.35 | 1.35 | 1.35 | 1.35 | V | | |
| | | | 6.0V | | 1.8 | 1.8 | 1.8 | 1.8 | V | | |
| V_{OH} | Minimum High Level Output Voltage | $V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 20 \mu A$ | 2.0V | 2.0 | 1.9 | 1.9 | 1.9 | 1.9 | V | | |
| | | | 4.5V | 4.5 | 4.4 | 4.4 | 4.4 | 4.4 | V | | |
| | | | 6.0V | 6.0 | 5.9 | 5.9 | 5.9 | 5.9 | V | | |
| | | $V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 6.0$ mA $ I_{OUT} \leq 7.8$ mA | 4.5V | 4.2 | 3.98 | 3.84 | 3.7 | 3.7 | V | | |
| | | | 6.0V | 5.7 | 5.48 | 5.34 | 5.2 | 5.2 | V | | |
| | | | | | | | | | | | |
| V_{OL} | Maximum Low Level Output Voltage | $V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} < 20 \mu A$ | 2.0V | 0 | 0.1 | 0.1 | 0.1 | 0.1 | V | | |
| | | | 4.5V | 0 | 0.1 | 0.1 | 0.1 | 0.1 | V | | |
| | | | 6.0V | 0 | 0.1 | 0.1 | 0.1 | 0.1 | V | | |
| | | $V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 6.0$ mA $ I_{OUT} \leq 7.8$ mA | 4.5V | 0.2 | 0.26 | 0.33 | 0.4 | 0.4 | V | | |
| | | | 6.0V | 0.2 | 0.26 | 0.33 | 0.4 | 0.4 | V | | |
| | | | | | | | | | | | |
| I_{IN} | Maximum Input Current | $V_{IN} = V_{CC}$ or GND | 6.0V | | ± 0.1 | ± 1.0 | ± 1.0 | μA | | | |
| I_{OZ} | Maximum TRI-STATE Output Leakage Current | $V_{OUT} = V_{CC}$ or GND $\bar{G}1 = V_{IH}$ | 6.0V | | ± 0.5 | ± 5.0 | ± 10 | μA | | | |
| I_{CC} | Maximum Quiescent Supply Current | $V_{IN} = V_{CC}$ or GND $I_{OUT} = 0 \mu A$ | 6.0V | | 8.0 | 80 | 160 | μA | | | |

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: -12 mW/°C from 65°C to 85°C; ceramic "J" package: -12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V $\pm 10\%$ the worst case output voltages (V_{OH} and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at $V_{CC} = 5.5V$ and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN} , I_{CC} , and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

** V_{IL} limits are currently tested at 20% of V_{CC} . The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC}=5V, T_A=25^{\circ}C, t_r=t_f=6\text{ ns}$

MM54HC354/MM74HC354

| Symbol | Parameter | Conditions | Typ | Guaranteed Limit | Units |
|--------------------|--|--|-----|------------------|-------|
| t_{PHL}, t_{PLH} | Maximum Propagation Delay D0–D7 to either Output | $C_L = 45\text{ pF}$ | 32 | 46 | ns |
| t_{PHL}, t_{PLH} | Maximum Propagation Delay DC to either Output | $C_L = 45\text{ pF}$ | 38 | 53 | ns |
| t_{PHL}, t_{PLH} | Maximum Propagation Delay S0–S2 to either Output | $C_L = 45\text{ pF}$ | 40 | 56 | ns |
| t_{PHL}, t_{PLH} | Maximum Propagation Delay \overline{SC} to either Output | $C_L = 45\text{ pF}$ | 42 | 58 | ns |
| t_{PZH}, t_{PZL} | Maximum Output Enable Time | $R_L = 1\text{ k}\Omega$ $C_L = 45\text{ pF}$ | 17 | 24 | ns |
| t_{PHZ}, t_{PLZ} | Maximum Output Disable Time | $R_L = 1\text{ k}\Omega$ $C_L = 5\text{ pF}$ | 23 | 32 | ns |
| t_S | Minimum Setup Time D0–D7 to \overline{DC} , S0–S2 to \overline{SC} | | 3 | 10 | ns |
| t_H | Minimum Hold Time D0–D7 to \overline{DC} , S0–S2 to \overline{SC} | | 0 | 5 | ns |
| t_W | Minimum Pulse Width, \overline{SC} or \overline{DC} | | 10 | 15 | ns |

MM54HC356/MM74HC356

| Symbol | Parameter | Conditions | Typ | Guaranteed Limit | Units |
|--------------------|--|--|-----|------------------|-------|
| t_{PHL}, t_{PLH} | Maximum Propagation Delay CLK to either Output | $C_L = 45\text{ pF}$ | 35 | 50 | ns |
| t_{PHL}, t_{PLH} | Maximum Propagation Delay S0–S2 to either Output | $C_L = 45\text{ pF}$ | 40 | 56 | ns |
| t_{PHL}, t_{PLH} | Maximum Propagation Delay \overline{SC} to either Output | $C_L = 45\text{ pF}$ | 42 | 58 | ns |
| t_{PZH}, t_{PZL} | Maximum Output Enable Time | $R_L = 1\text{ k}\Omega$ $C_L = 45\text{ pF}$ | 17 | 24 | ns |
| t_{PHZ}, t_{PLZ} | Maximum Output Disable Time | $R_L = 1\text{ k}\Omega$ $C_L = 5\text{ pF}$ | 23 | 32 | ns |
| t_S | Minimum Setup Time D0–D7 to CLK, S0–S2 to \overline{SC} | | 3 | 10 | ns |
| t_H | Minimum Hold Time D0–D7 to CLK, S0–S2 to \overline{SC} | | 0 | 5 | ns |
| t_W | Minimum Pulse Width, \overline{SC} or CLK | | 10 | 15 | ns |

AC Electrical Characteristics MM54HC354/MM74HC354 (Continued)

$V_{CC}=2.0-6.0V$, $C_L=50\text{ pF}$, $t_r=t_f=6\text{ ns}$ (unless otherwise specified)

| Symbol | Parameter | Conditions | V_{CC} | $T_A = 25^\circ\text{C}$ | | 74HC $T_A = -40\text{ to }85^\circ\text{C}$ | | 54HC $T_A = -55\text{ to }125^\circ\text{C}$ | | Units |
|-----------------------|--|---|----------|--------------------------|-------------------|--|--|---|----|-------|
| | | | | Typ | Guaranteed Limits | | | | | |
| t_{PHL} , t_{PLH} | Maximum Propagation Delay D0–D7 to either Output | $C_L = 50\text{ pF}$ $C_L = 150\text{ pF}$ | 2.0V | 90 | 235 | 294 | | 352 | | ns |
| | | | 2.0V | 100 | 275 | 344 | | 412 | | ns |
| | | $C_L = 50\text{ pF}$ $C_L = 150\text{ pF}$ | 4.5V | 35 | 47 | 59 | | 70 | | ns |
| | | | 4.5V | 40 | 55 | 68 | | 83 | | ns |
| t_{PHL} , t_{PLH} | Maximum Propagation Delay \overline{DC} to either Output | $C_L = 50\text{ pF}$ $C_L = 150\text{ pF}$ | 2.0V | 115 | 270 | 337 | | 405 | | ns |
| | | | 2.0V | 125 | 310 | 387 | | 465 | | ns |
| | | $C_L = 50\text{ pF}$ $C_L = 150\text{ pF}$ | 4.5V | 40 | 54 | 68 | | 82 | | ns |
| | | | 4.5V | 46 | 62 | 78 | | 93 | | ns |
| t_{PHL} , t_{PLH} | Maximum Propagation Delay S0–S2 to either Output | $C_L = 50\text{ pF}$ $C_L = 150\text{ pF}$ | 2.0V | 120 | 285 | 356 | | 427 | | ns |
| | | | 2.0V | 130 | 325 | 406 | | 488 | | ns |
| | | $C_L = 50\text{ pF}$ $C_L = 150\text{ pF}$ | 4.5V | 42 | 57 | 71 | | 86 | | ns |
| | | | 4.5V | 50 | 65 | 81 | | 97 | | ns |
| t_{PHL} , t_{PLH} | Maximum Propagation Delay \overline{SC} to either Output | $C_L = 50\text{ pF}$ $C_L = 150\text{ pF}$ | 2.0V | 120 | 300 | 375 | | 450 | | ns |
| | | | 2.0V | 110 | 340 | 425 | | 510 | | ns |
| | | $C_L = 50\text{ pF}$ $C_L = 150\text{ pF}$ | 4.5V | 45 | 60 | 75 | | 90 | | ns |
| | | | 4.5V | 52 | 68 | 85 | | 102 | | ns |
| t_{PHZ} , t_{PLZ} | Maximum Output Enable Time | $R_L = 1\text{ k}\Omega$ $C_L = 50\text{ pF}$ $C_L = 150\text{ pF}$ | 2.0V | 50 | 125 | 156 | | 188 | | ns |
| | | | 2.0V | 60 | 165 | 206 | | 248 | | ns |
| | | $C_L = 50\text{ pF}$ $C_L = 150\text{ pF}$ | 4.5V | 18 | 25 | 31 | | 38 | | ns |
| | | | 4.5V | 25 | 33 | 41 | | 49 | | ns |
| t_{PHZ} , t_{PLZ} | Maximum Output Disable Time | $R_L = 1\text{ k}\Omega$ $C_L = 50\text{ pF}$ | 2.0V | 68 | 165 | 206 | | 248 | | ns |
| | | | 4.5V | 24 | 33 | 41 | | 49 | | ns |
| | | $C_L = 50\text{ pF}$ $C_L = 150\text{ pF}$ | 6.0V | 20 | 28 | 35 | | 42 | | ns |
| | | | 6.0V | 21 | 28 | 35 | | 42 | | ns |
| t_s | Minimum Setup Time D0–D7 to \overline{DC} , S0–S2 to \overline{SC} | | 2.0V | 6 | 50 | 60 | | 75 | | ns |
| | | | 4.5V | 3 | 10 | 13 | | 15 | | ns |
| | | | 6.0V | 3 | 10 | 13 | | 15 | | ns |
| t_H | Minimum Hold Time D0–D7 to \overline{DC} , S0–S2 to \overline{SC} | | 2.0V | 0 | 5 | 5 | | 5 | | ns |
| | | | 4.5V | 0 | 5 | 5 | | 5 | | ns |
| | | | 6.0V | 0 | 5 | 5 | | 5 | | ns |
| t_W | Minimum Pulse Width \overline{SC} or \overline{DC} | | 2.0V | 30 | 80 | 100 | | 120 | | ns |
| | | | 4.5V | 10 | 16 | 20 | | 24 | | ns |
| | | | 6.0V | 10 | 15 | 18 | | 20 | | ns |
| t_{TLH} , t_{THL} | Maximum Output Rise and Fall Time | $C_L = 50\text{ pF}$ | 2.0V | 25 | 60 | 75 | | 90 | | ns |
| | | | 4.5V | 7 | 12 | 15 | | 18 | | ns |
| | | | 6.0V | 6 | 10 | 13 | | 15 | | ns |
| C_{PD} | Power Dissipation Capacitance (Note 5) | (per package) Active TRI-STATE | | 150 | | | | | pF | |
| C_{IN} | Maximum Input Capacitance | | | 5 | 10 | 10 | | 10 | | pF |
| C_{OUT} | Maximum Output Capacitance | | | 15 | 20 | 20 | | 20 | | pF |

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

AC Electrical Characteristics MM54HC356/MM74HC356 (Continued)

$V_{CC}=2.0-6.0V$, $C_L=50\text{ pF}$, $t_r=t_f=6\text{ ns}$ (unless otherwise specified)

| Symbol | Parameter | Conditions | V_{CC} | $T_A=25^\circ\text{C}$ | | 74HC | 54HC | Units |
|-----------------------|---|------------------------|----------|------------------------|-------------------|--------------------------------------|---------------------------------------|-------|
| | | | | | | $T_A=-40\text{ to }85^\circ\text{C}$ | $T_A=-55\text{ to }125^\circ\text{C}$ | |
| | | | | Typ | Guaranteed Limits | | | |
| t_{PHL} , t_{PLH} | Maximum Propagation Delay CLK to either Output | $C_L=50\text{ pF}$ | 2.0V | 100 | 225 | 318 | 338 | ns |
| | | | 2.0V | 110 | 295 | 369 | 442 | ns |
| | | $C_L=150\text{ pF}$ | 4.5V | 36 | 51 | 63 | 76 | ns |
| | | | 4.5V | 42 | 59 | 73 | 90 | ns |
| t_{PHL} , t_{PLH} | Maximum Propagation Delay S0-S2 to either Output | $C_L=50\text{ pF}$ | 2.0V | 120 | 285 | 356 | 427 | ns |
| | | | 2.0V | 130 | 325 | 406 | 488 | ns |
| | | $C_L=150\text{ pF}$ | 4.5V | 42 | 57 | 71 | 86 | ns |
| | | | 4.5V | 50 | 65 | 81 | 97 | ns |
| t_{PHL} , t_{PLH} | Maximum Propagation Delay SC to either Output | $C_L=50\text{ pF}$ | 2.0V | 120 | 300 | 375 | 450 | ns |
| | | | 2.0V | 110 | 340 | 425 | 510 | ns |
| | | $C_L=150\text{ pF}$ | 4.5V | 45 | 60 | 75 | 90 | ns |
| | | | 4.5V | 52 | 68 | 85 | 102 | ns |
| t_{PZH} , t_{PZL} | Maximum Output Enable Time | $R_L=1\text{ k}\Omega$ | 2.0V | 50 | 125 | 156 | 188 | ns |
| | | | 2.0V | 60 | 165 | 206 | 248 | ns |
| | | $C_L=50\text{ pF}$ | 4.5V | 18 | 25 | 31 | 38 | ns |
| | | | 4.5V | 25 | 33 | 41 | 49 | ns |
| t_{PHZ} , t_{PLZ} | Maximum Output Disable Time | $R_L=1\text{ k}\Omega$ | 2.0V | 68 | 165 | 206 | 248 | ns |
| | | | 4.5V | 24 | 33 | 41 | 49 | ns |
| | | $C_L=50\text{ pF}$ | 6.0V | 20 | 28 | 35 | 42 | ns |
| | | | 6.0V | 21 | 28 | 35 | 42 | ns |
| t_S | Minimum Setup Time D0-D7 to CLK, S0-S2 to \overline{SC} | 2.0V | 6 | 50 | 60 | 75 | ns | |
| | | 4.5V | 3 | 10 | 13 | 15 | ns | |
| | | 6.0V | 3 | 10 | 13 | 15 | ns | |
| t_H | Minimum Hold Time D0-D7 to CLK, S0-S2 to \overline{SC} | 2.0V | 0 | 5 | 5 | 5 | ns | |
| | | 4.5V | 0 | 5 | 5 | 5 | ns | |
| | | 6.0V | 0 | 5 | 5 | 5 | ns | |
| t_W | Minimum Pulse Width SC to CLK | 2.0V | 30 | 80 | 100 | 120 | ns | |
| | | 4.5V | 10 | 16 | 20 | 24 | ns | |
| | | 6.0V | 10 | 15 | 18 | 20 | ns | |
| t_r , t_f | Maximum Clock Input Rise and Fall Time | 2.0V | | 1000 | 1000 | 1000 | ns | |
| | | 4.5V | | 500 | 500 | 500 | ns | |
| | | 6.0V | | 400 | 400 | 400 | ns | |
| t_{TLH} , t_{THL} | Maximum Output Rise and Fall Time | $C_L=50\text{ pF}$ | 2.0V | 25 | 60 | 75 | 90 | ns |
| | | 4.5V | 7 | 12 | 15 | 18 | ns | |
| | | 6.0V | 6 | 10 | 13 | 15 | ns | |
| C_{PD} | Power Dissipation Capacitance (Note 5) | (per package) Active | | 150 | | | | pF |
| | | TRI-STATE | | 50 | | | | pF |
| C_{IN} | Maximum Input Capacitance | | | 5 | 10 | 10 | 10 | pF |
| C_{OUT} | Maximum Output Capacitance | | | 15 | 20 | 20 | 20 | pF |

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}V_{CC}f+I_{CC}$.

Function Table

| Inputs | | | | | | | | | | Outputs | |
|---------|----|----|---------------------|--------------|-----------------|-----------------|----|---|-------------------|---------|--|
| Select† | | | Data Control 'HC354 | Clock 'HC356 | Output Enables | | | W | Y | | |
| S1 | S2 | S0 | \overline{DC} | CLK | $\overline{G1}$ | $\overline{G2}$ | G3 | | | | |
| X | X | X | X | X | X | H | X | X | Z | Z | |
| X | X | X | X | X | X | X | H | X | Z | Z | |
| X | X | X | X | X | X | X | X | L | Z | Z | |
| L | L | L | L | L | ↑ | L | L | H | $\overline{D0}$ | D0 | |
| L | L | L | L | H | H or L | L | L | H | $\overline{D0_n}$ | D0_n | |
| L | L | H | L | L | ↑ | L | L | H | $\overline{D1}$ | D1 | |
| L | L | H | H | H | H or L | L | L | H | $\overline{D1_n}$ | D1_n | |
| L | H | L | L | L | ↑ | L | L | H | $\overline{D2}$ | D2 | |
| L | H | L | H | H | H or L | L | L | H | $\overline{D2_n}$ | D2_n | |
| L | H | H | L | L | ↑ | L | L | H | $\overline{D3}$ | D3 | |
| L | H | H | H | H | H or L | L | L | H | $\overline{D3_n}$ | D3_n | |
| H | L | L | L | L | ↑ | L | L | H | $\overline{D4}$ | D4 | |
| H | L | L | H | H | H or L | L | L | H | $\overline{D4_n}$ | D4_n | |
| H | L | H | L | L | ↑ | L | L | H | $\overline{D5}$ | D5 | |
| H | L | H | H | H | H or L | L | L | H | $\overline{D5_n}$ | D5_n | |
| H | H | L | L | L | ↑ | L | L | H | $\overline{D6}$ | D6 | |
| H | H | L | H | H | H or L | L | L | H | $\overline{D6_n}$ | D6_n | |
| H | H | H | L | L | ↑ | L | L | H | $\overline{D7}$ | D7 | |
| H | H | H | H | H | H or L | L | L | H | $\overline{D7_n}$ | D7_n | |

H = high level (steady state)

L = low level (steady state)

X = irrelevant (any input, including transitions)

Z = high-impedance state (off state)

↑ = transition from low to high level

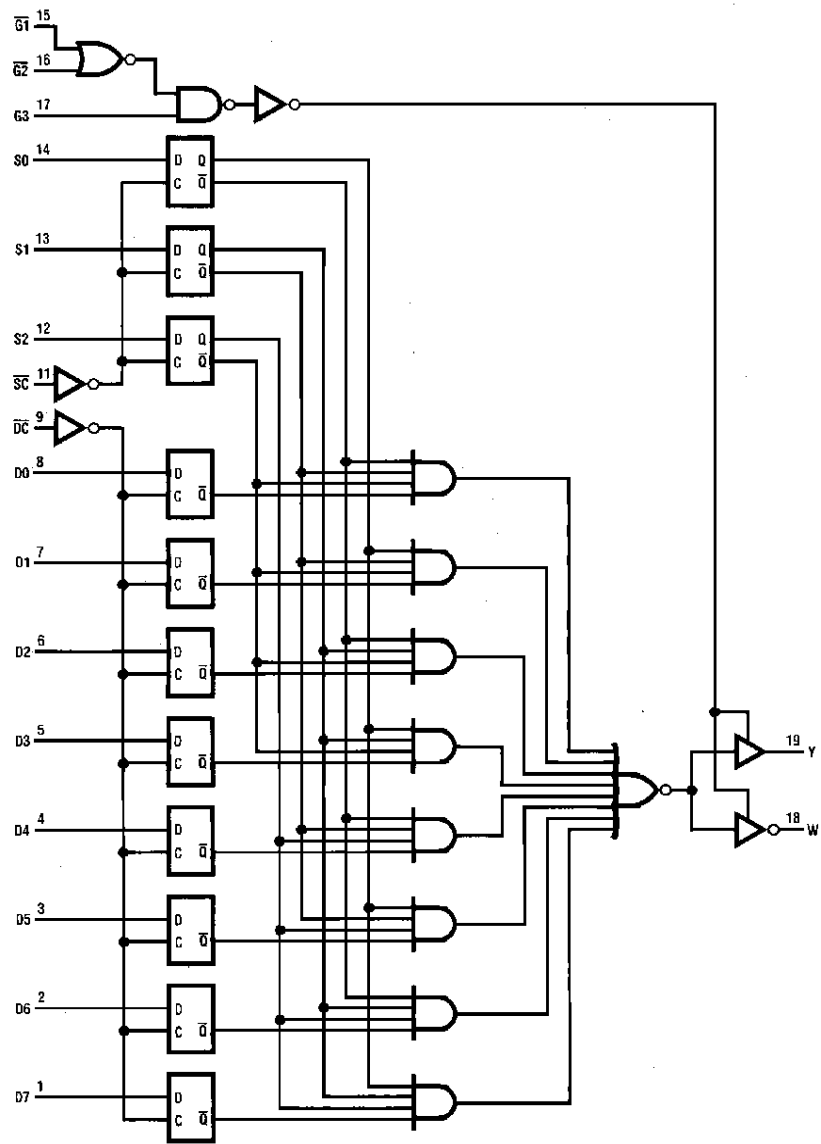
D0...D7 = the level steady-state inputs at inputs D0 through D7, respectively, at the time of the low-to-high clock transition in the case of 'HC356

D0_n...D7_n = the level of steady state inputs at inputs D0 through D7, respectively, before the most recent low-to-high transition of data control or clock.

†This column shows the input address set-up with \overline{SC} low.

Logic Diagram

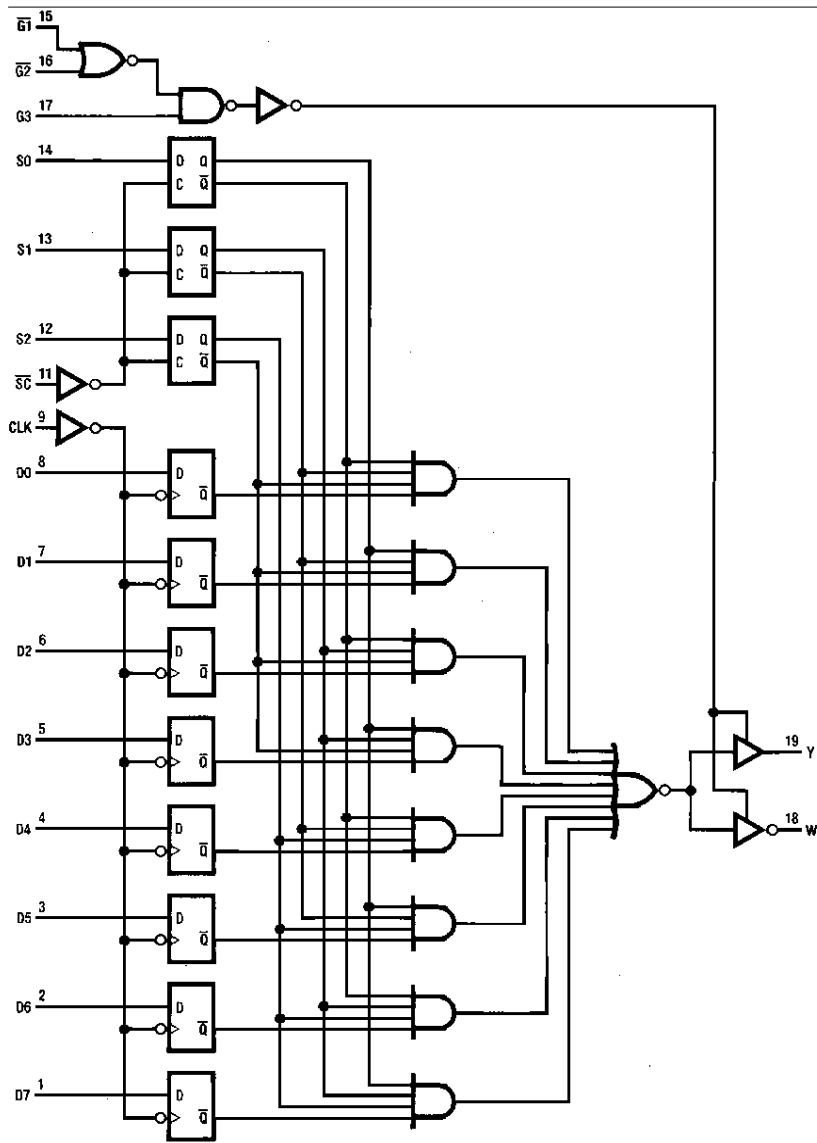
'HC354



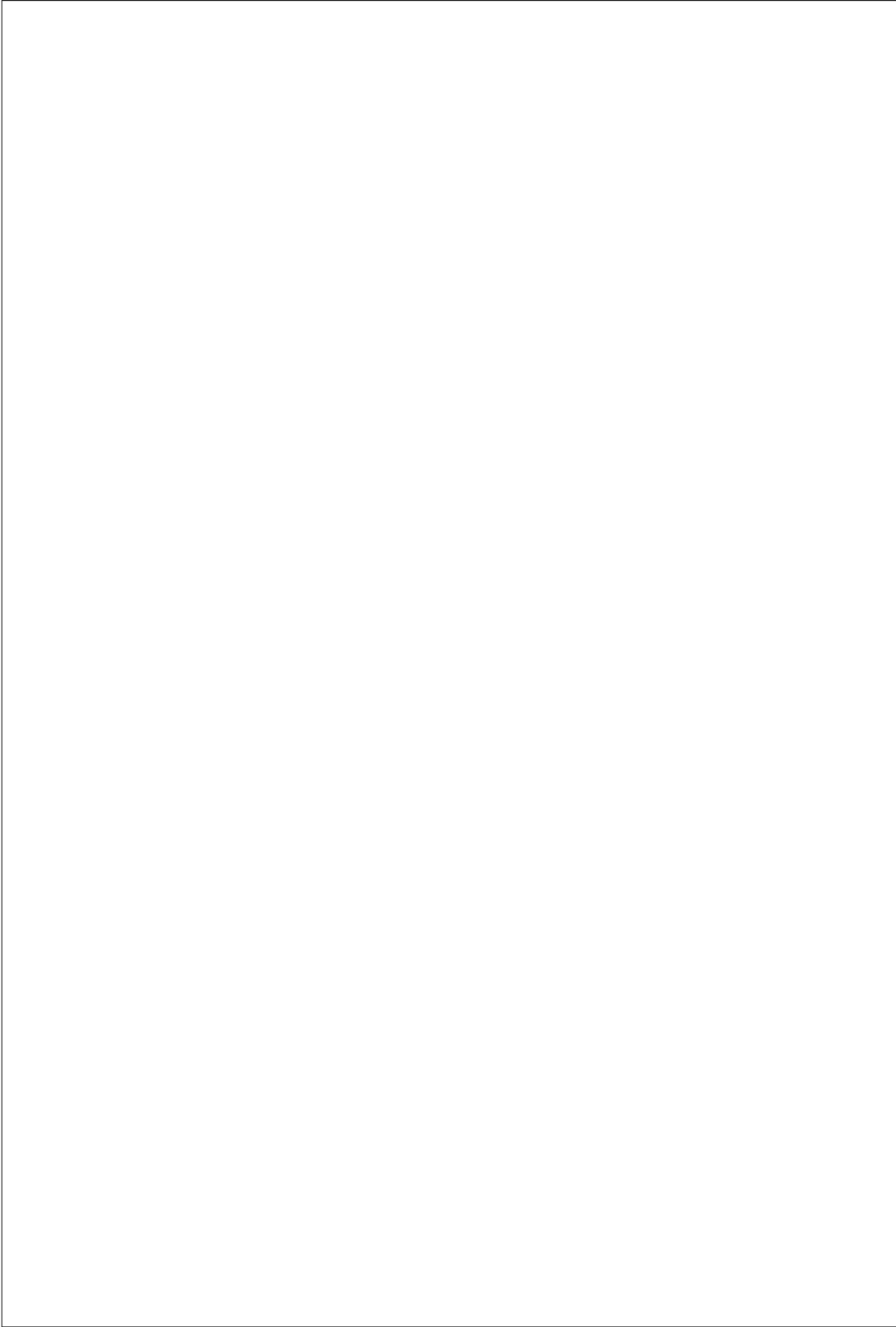
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Logic Diagram

'HC356

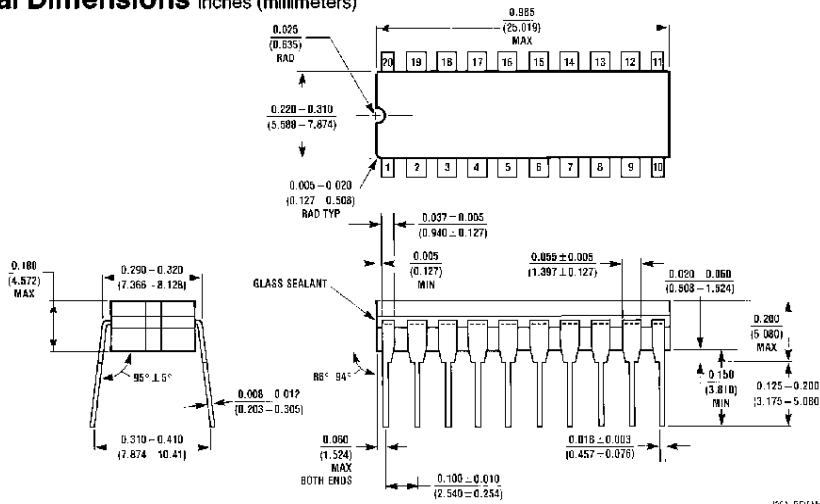


TL/F/5208-3

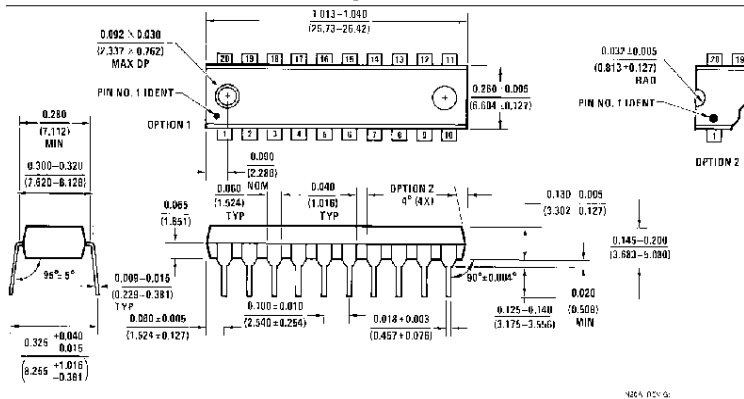


**MM54HC354/MM74HC354/MM54HC356/MM74HC356
8-Channel TRI-STATE Multiplexers with Latches**

Physical Dimensions inches (millimeters)



Ceramic Dual-In-Line Package (J)
Order Number MM54HC354J, MM54HC356J, MM74HC354J or MM74HC356J
NS Package Number J20A



Molded Dual-In-Line Package (N)
Order Number MM74HC354N or MM74HC356N
NS Package Number N20A

LIFE SUPPORT POLICY

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