M66240P/FP

4-CH 16-BIT PWM GENERATOR

DESCRIPTION

The M66240 is a programmable channel PWM generator produced using the silicon gate CMOS process.

The M66240 can connect directly to the MPU data bus and consists of a 16-bit prescaler and a PWM counter. The pulse output includes three kinds of modes, allowing the independent control of each channel. Combining the A-D function and the timer function of the one-chip microcomputer provides a software servo system.

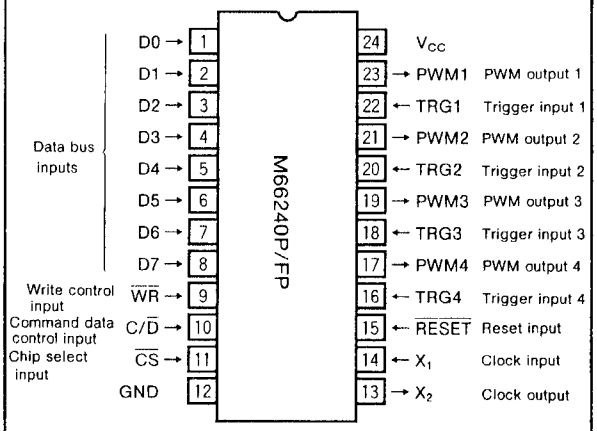
FEATURES

- 4-channel independent control possible
- Three pulse output modes incorporated.
- PWM repetitive frequency : 50kHz (max.)
  (Mode 0, 8-bit resolution, fxin/255 at prescaler setting= 0)
- Output polarity selection possible
- External triggering possible
- The output after reset is in the high impedance state.
- Change of mode setting becomes effective after the current cycle.
- The RESET incorporates a negative-going noise eliminator and the TRG1-4 incorporates a positive-going noise eliminator.
- High output current : $I_O = \pm 24mA$

APPLICATION

Control of DC motors and stepping motors, heater phase controllers, software servos for office automation equipment, and industrial equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 24P4D
24P2W-A

FUNCTION

Four separate 16-bit prescalers and 16-bit PWM counters can be separately programmed by the control instruction from the MPU.

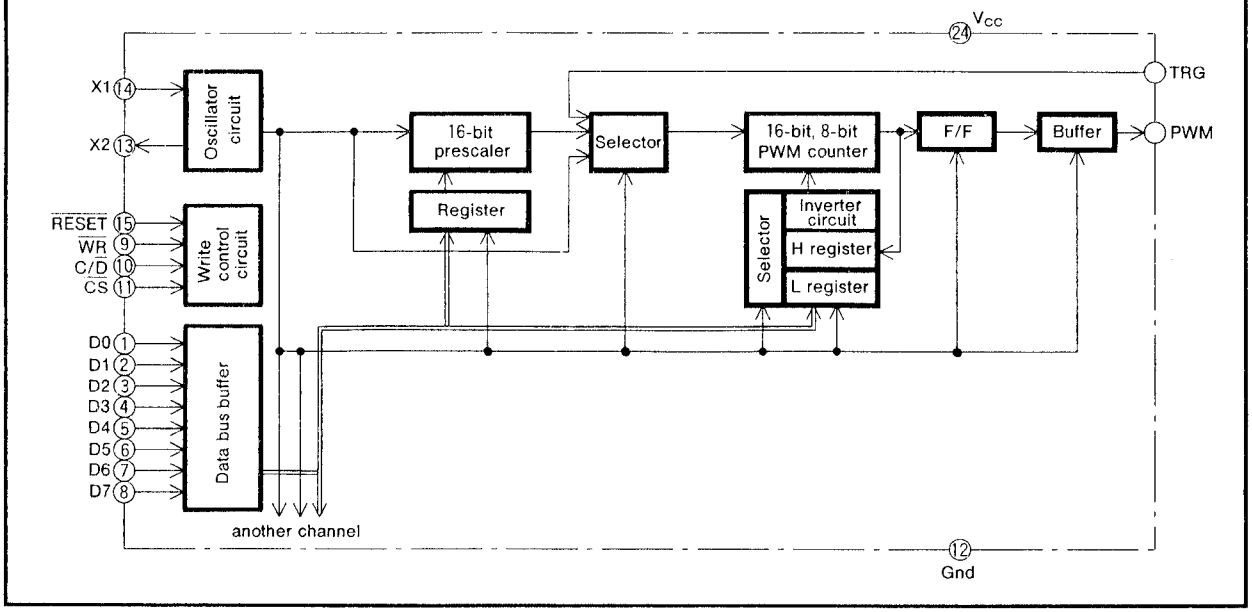
The output is made in one of three modes (Mode 0, Mode 1, and Mode 2).

In Mode 0, setting only the value of H width repeatedly outputs the set pulse width.

In Mode 1, setting only the value of H width outputs one shot of the pulse width set by trigger input.

In Mode 2, setting both H width and L width repeatedly outputs the set pulse width.

BLOCK DIAGRAM



PIN DESCRIPTIONS

Pin name	Description	I/O	Function
$\overline{RESET}$	Reset input	Input	Clears the command register and the flip-flop at "L"
D0~D7	Data bus input	Input	Inputs the data from MPU over the 8-bit data bus.
$\overline{WR}$	Write input	Input	Writes the data bus data to the control register or data register when the state changes from "L" to "H".
C/$\overline{D}$	Command/data input	Input	Data at the data bus is regarded as a command at high level and as data at low level.
$\overline{CS}$	Chip select input	Input	Communication with MPU is enabled at low-level. Any control from MPU is ignored at high level.
X_1	Clock input	Input	I/O to the built-in clock generator circuit. Providing a crystal resonator between X_1 and X_2 sets the frequency. To make external clock input, connect the clock source to X_1 pin and leave X_2 pin open.
X_2	Clock output	Output	
TRG1~ TRG4	Trigger input	Input	This is used when external trigger is selected in mode setting. Set to low level when not in use.
PWM1~ PWM4	PWM output	Output	PWM output pins. Outputs become the high-impedance state after reset or after disable is specified by command 3. D0 of command 1 allows the selection of output polarity.

OPERATION

Commands

The information on data bus inputs D0 through D7 is loaded as command when command data control input C/$\overline{D}$=1 and as data when C/$\overline{D}$=0.

There are three kinds of commands. (See Figure 1.)

Command 1 selects the output mode and external trigger input of each channel and sets the output polarity of H width. Command 2 specifies, on a byte basis, to which 16-bit register of the prescaler and PWM counter of each channel data is to be written.

The second and subsequent bytes of command 2 write prescaler value and PWM value. Depending on the location specified by command 2, the data of the second and subsequent bytes must be written in the order shown in Figure 2.

Command 3 is used to start or stop the prescaler and PWM counter operation.

Data input

At initialization, all 16 bits of the prescaler value must be written.

In mode 0 or 1, the PWM value must be written to all 16 bits of H register (In mode 0 at 8-bit resolution, only the lower byte of the H register is used.); in mode 2, the value must be written to all 16 bits of H and L registers.

To change the values of all 16 bits in the prescaler or the PWM counter during operation, values should be written to the upper byte first and then to the lower byte. To change the values of the lower byte only, the values of only the lower byte should be written.

To change the values of the upper byte, the values of all 16 bits should be written. To change the values of H register in Mode 2, the H register value should be written followed by the L register value.

When values are written to the lower byte (lower byte of L register in Mode 2), the write cycle of data register is completed.

If the data register value is changed during a PWM signal output operation (exactly, after the end of the write operation), the PWM output is updated starting with the cycle next to the current output cycle.

To change the mode (i.e., to execute command 1), disable the output first (i.e., execute command 3).

Figure 3 shows the flow chart of the basic operation. (The order of the prescaler's and PWM counter's data setting is not fixed.)

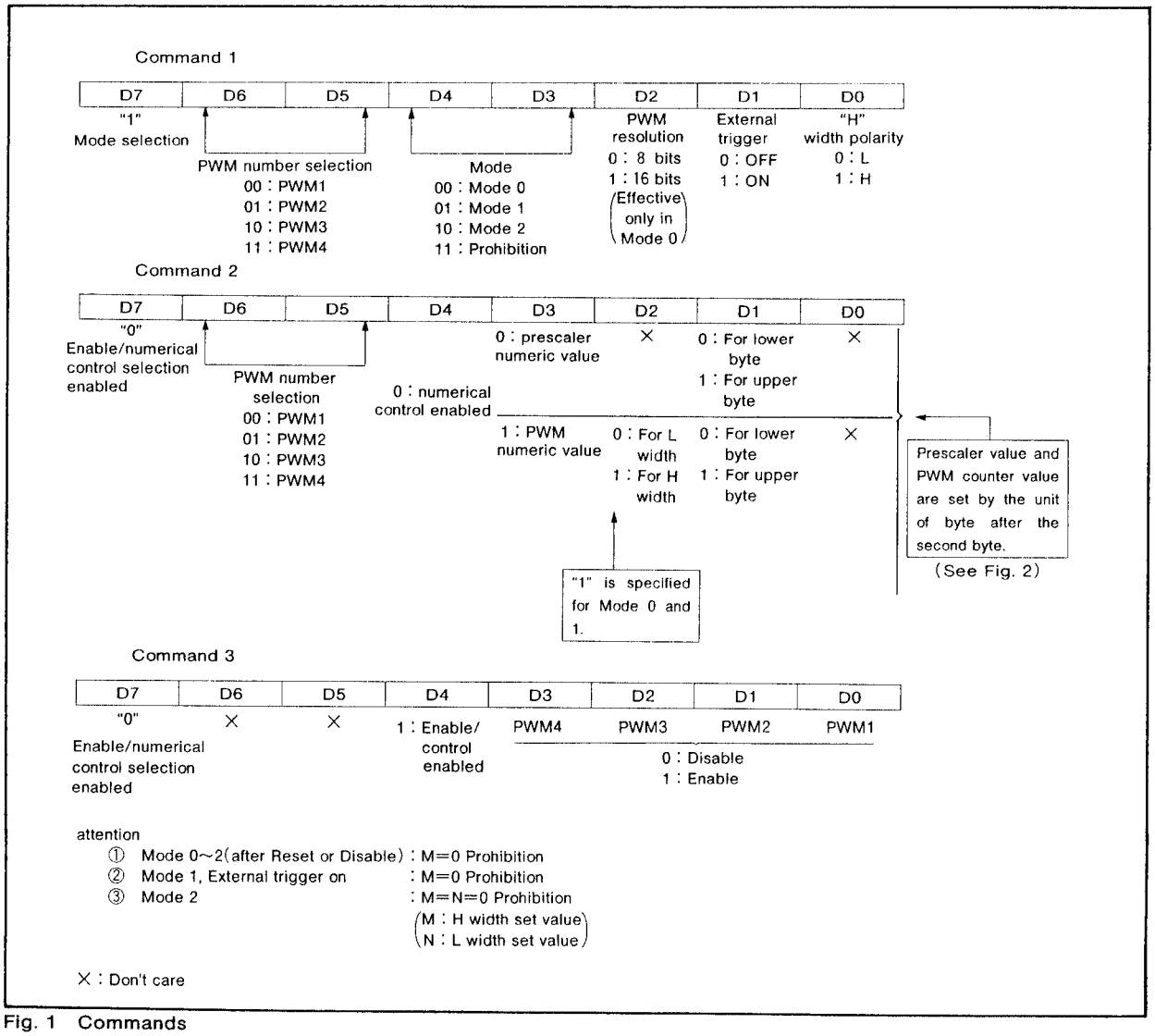


Fig. 1 Commands

First byte (command 2)			Second byte	Third byte	Fourth byte	Fifth byte	Remark
D3	D2	D1					
1	1	1	Upper byte for PWM H register	Lower byte for PWM H register	—	—	When Mode0 or 1
1	1	0	Lower byte for PWM H register	—	—	—	
1	1	1	Upper byte for PWM H register	Lower byte for PWM H register	Upper byte for PWM L register	Lower byte for PWM L register	When Mode 2
1	1	0	Lower byte for PWM H register	Upper byte for PWM L register	Lower byte for PWM L register		
1	0	1	Upper byte for PWM L register	Lower byte for PWM L register	—	—	
1	0	0	Lower byte for PWM L register	—	—	—	
0	×	1	Upper byte for prescaler register	Lower byte for prescaler register	—	—	
0	×	0	Lower byte for prescaler register	—	—	—	

Fig. 2 Data-setting sequence for registers

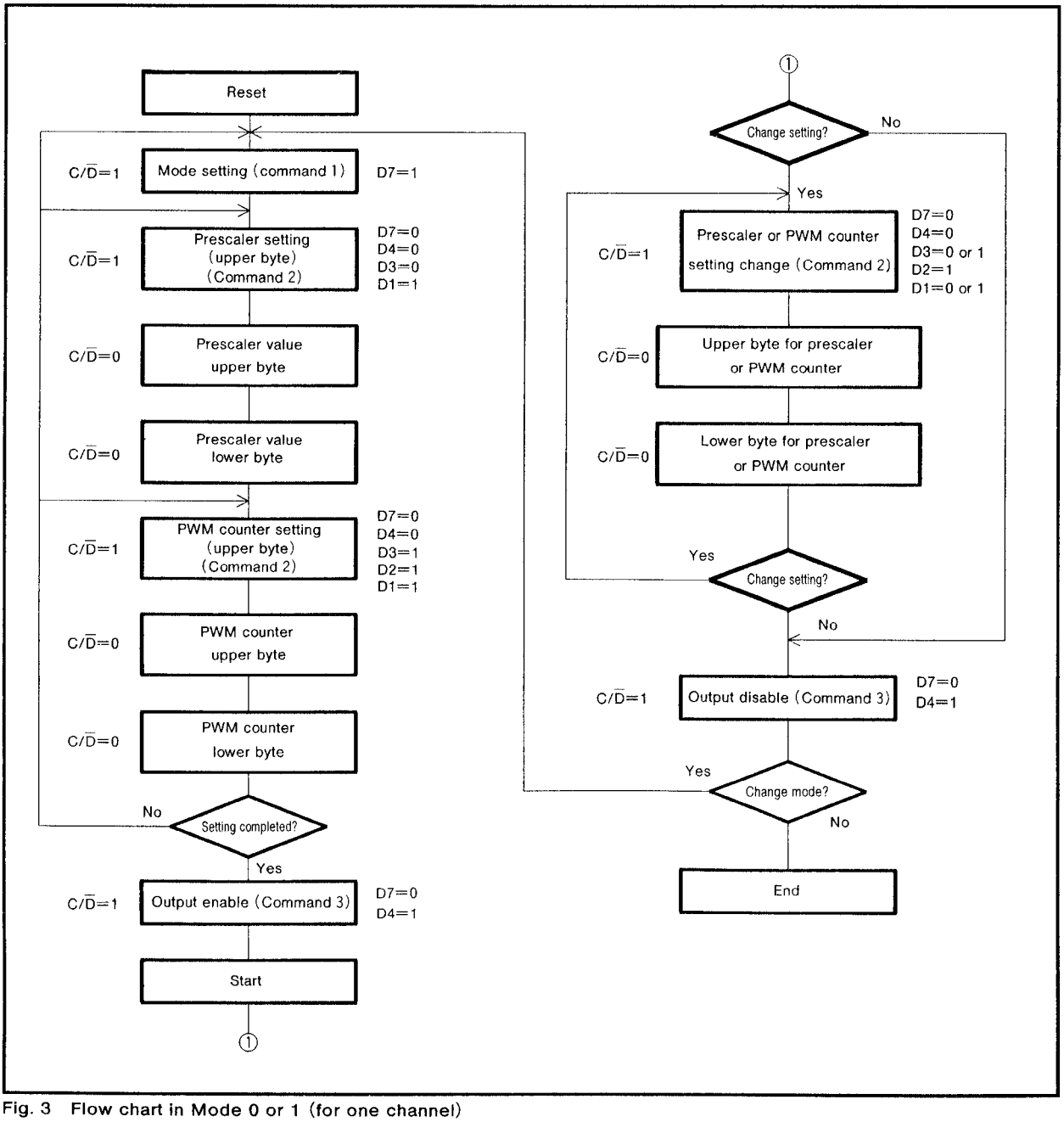


Fig. 3 Flow chart in Mode 0 or 1 (for one channel)

PWM waveform output

The M66240 has a built-in 16-bit prescaler and a PWM counter. The duty cycle of output pulse can be freely specified by changing the values of the prescaler and the PWM counter. The output is made in one of three modes (Mode 0, Mode 1, and Mode 2). The description of these modes is given below.

(1) Mode 0

This mode is selected by writing "0" to D4 and D3 in command 1.

Figure 9 shows the block diagram (for one channel) in this mode.

The 16-bit PWM counter can be used as an 8-bit PWM counter only in this mode (command 1 : D2=0). The setting with PWM resolution=8 bits must be written to the lower 8 bytes of H register. In this mode, the H output pulse width is determined by the prescaler register value L and PWM register value M. The PWM output cycle time is determined by the prescaler register value L, irrespective of the PWM register value M. (See Fig. 4)

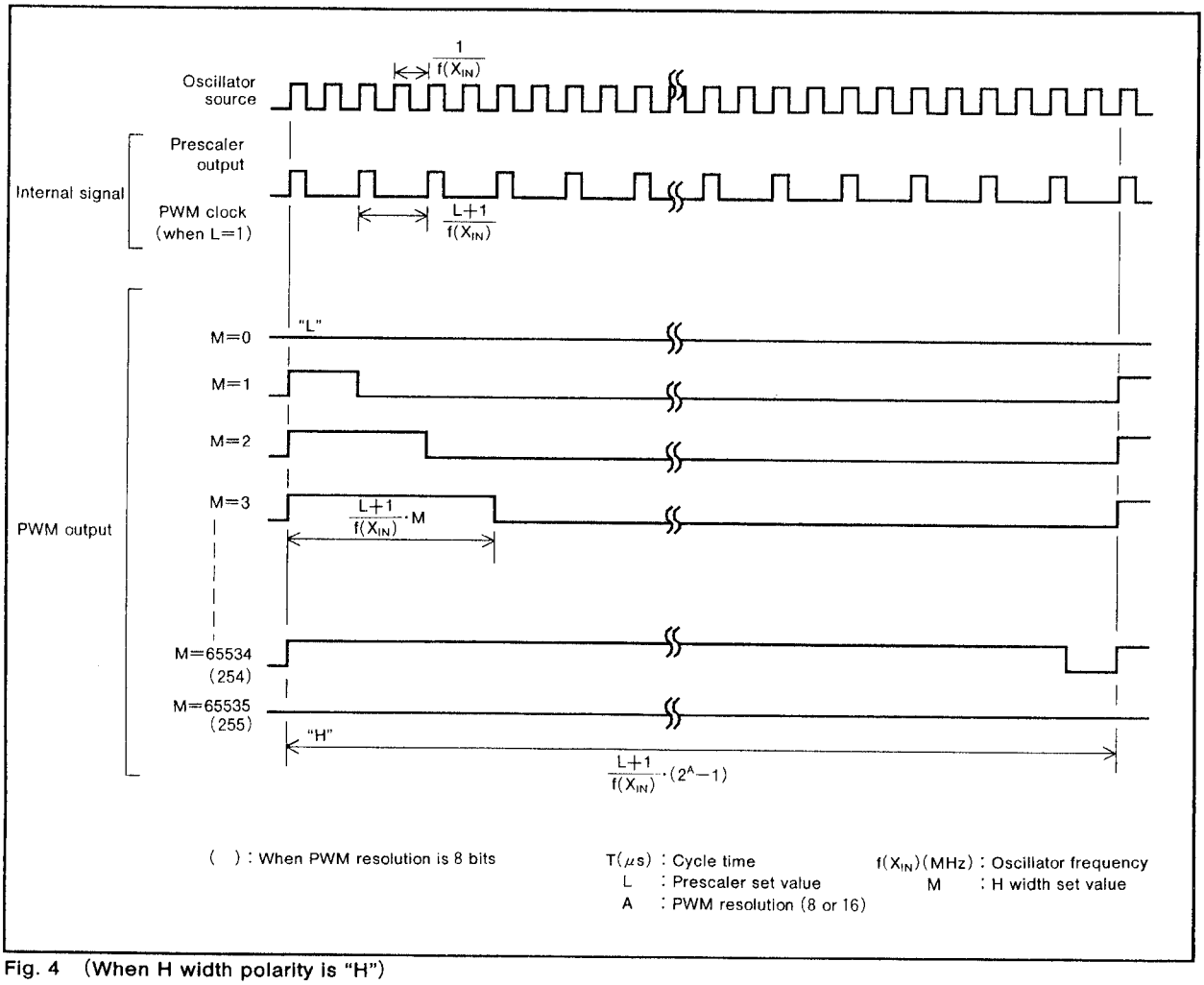


Fig. 4 (When H width polarity is "H")

(2) Mode 1

This mode is selected by setting D4=0 and D3=1 in command 1.

Figure 10 shows the block diagram in this mode (for one channel).

This mode outputs, on the trigger signal, one shot of the pulse determined by value M of PWM register. The type of this output operation is determined by whether the external trigger signal or the internal trigger signal is used. Operation varies according to the choice of external and internal trigger signals.

① External trigger selected (D1=1 in command 1): This mode outputs, when a trigger pulse is applied to trigger input TRG, one shot of output pulse. Therefore, cycle time T becomes cycle time f_{IN} of the trigger pulse to be applied to trigger input TRG.

The output pulse width is determined by the prescaler register value L and PWM register value M. (See Fig. 5)

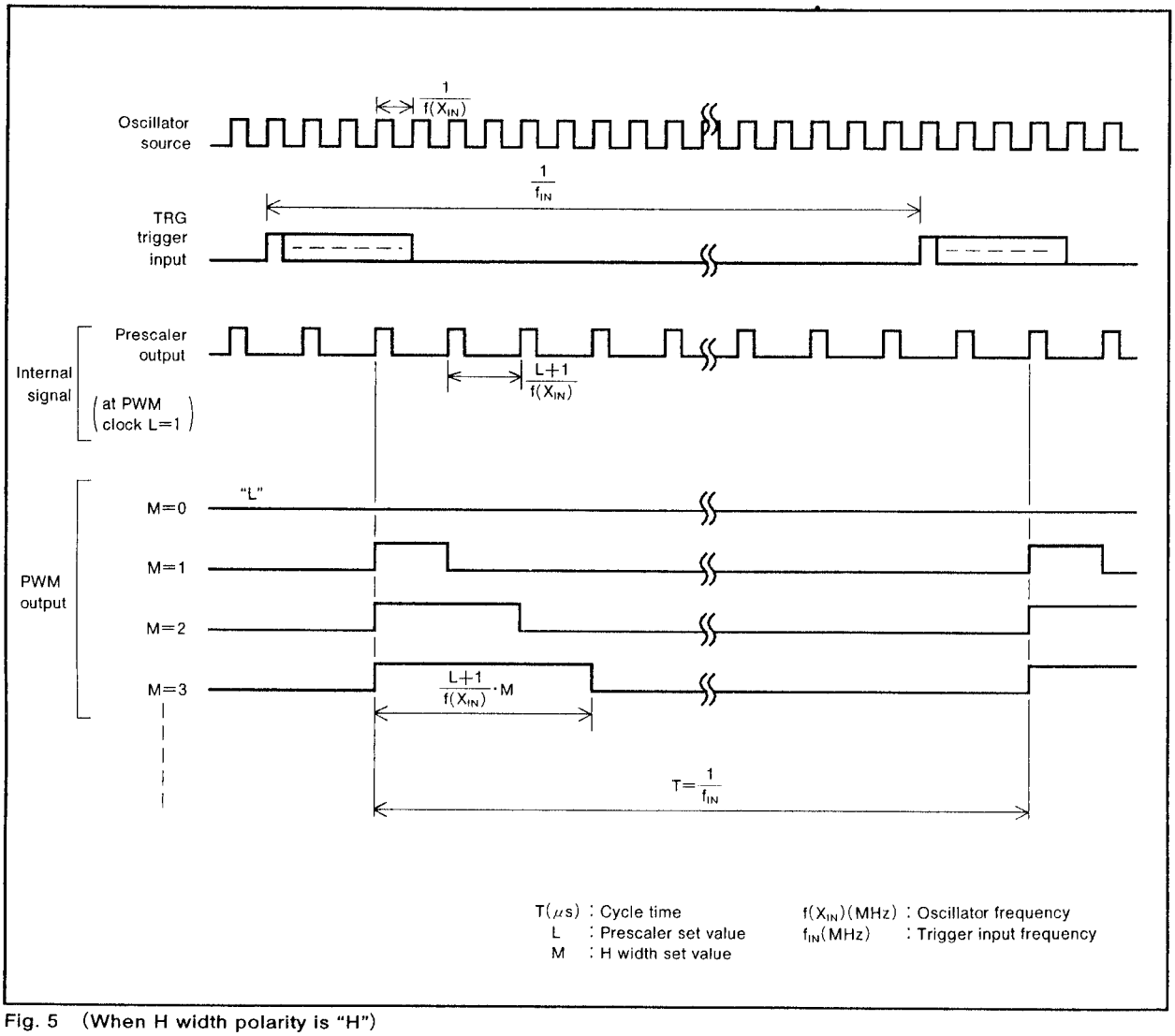


Fig. 5 (When H width polarity is "H")

② Internal trigger selected (D1=0 in command 1) :
In this mode, the trigger signal is generated by the prescaler. Therefore, the cycle time T of output pulse is determined by the prescaler register value L. In this case, the oscillator source becomes the PWM counter clock and the output pulse width is determined by the PWM register value M. (See Fig. 6)

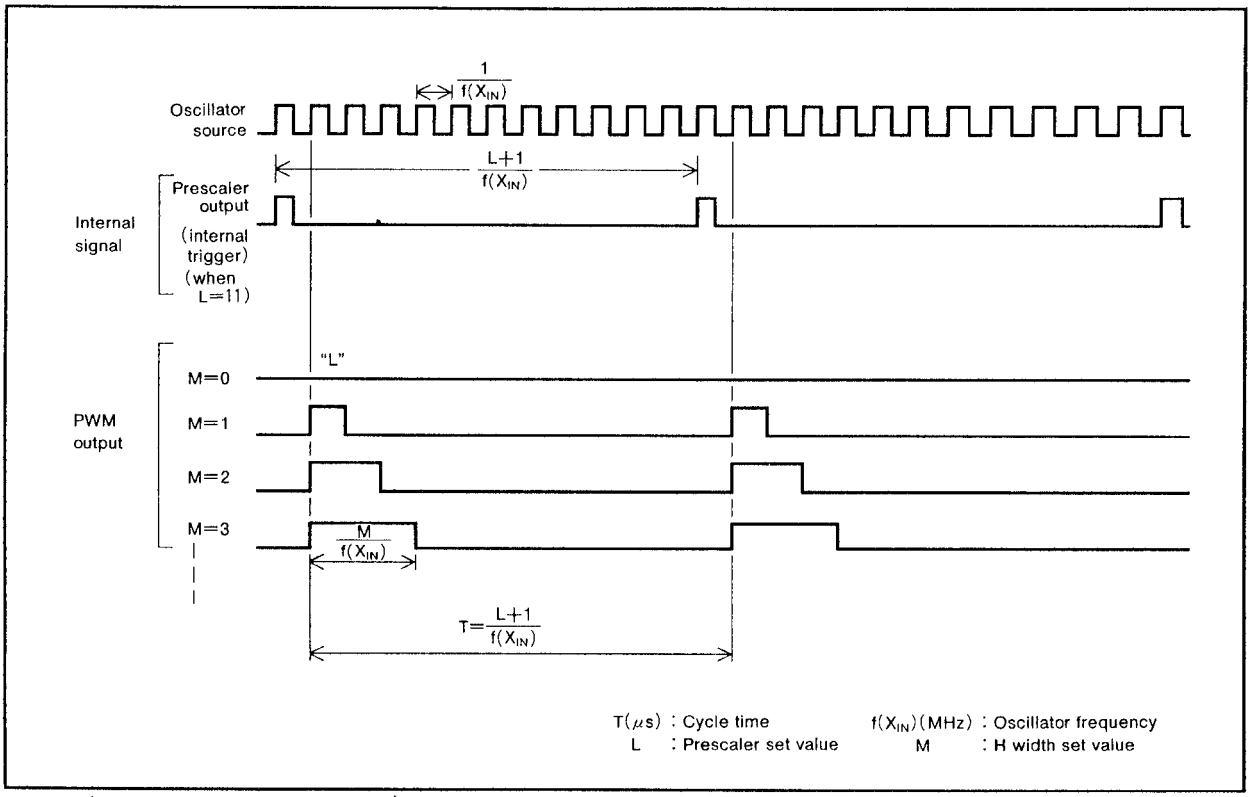


Fig. 6 (When H width polarity is "H")

In Mode 1, the retrigger state is caused when the cycle time of trigger pulse gets smaller than value M of PWM register.

(3) Mode 2

This mode is selected by writing D4=1 and D3=0 in command 1. Fig. 11 shows the block diagram of this mode (for one channel).

The high-level pulse value M is set to the H register of PWM in Modes 0 and 1, but, in this mode, the high-level pulse value M is set to the H register of PWM and the low-level pulse value N is set to the L register of PWM. Therefore, the pulse width and cycle time T of PWM output are determined by value L of the prescaler register and values M and N of H and L registers of PWM (see Fig. 7).

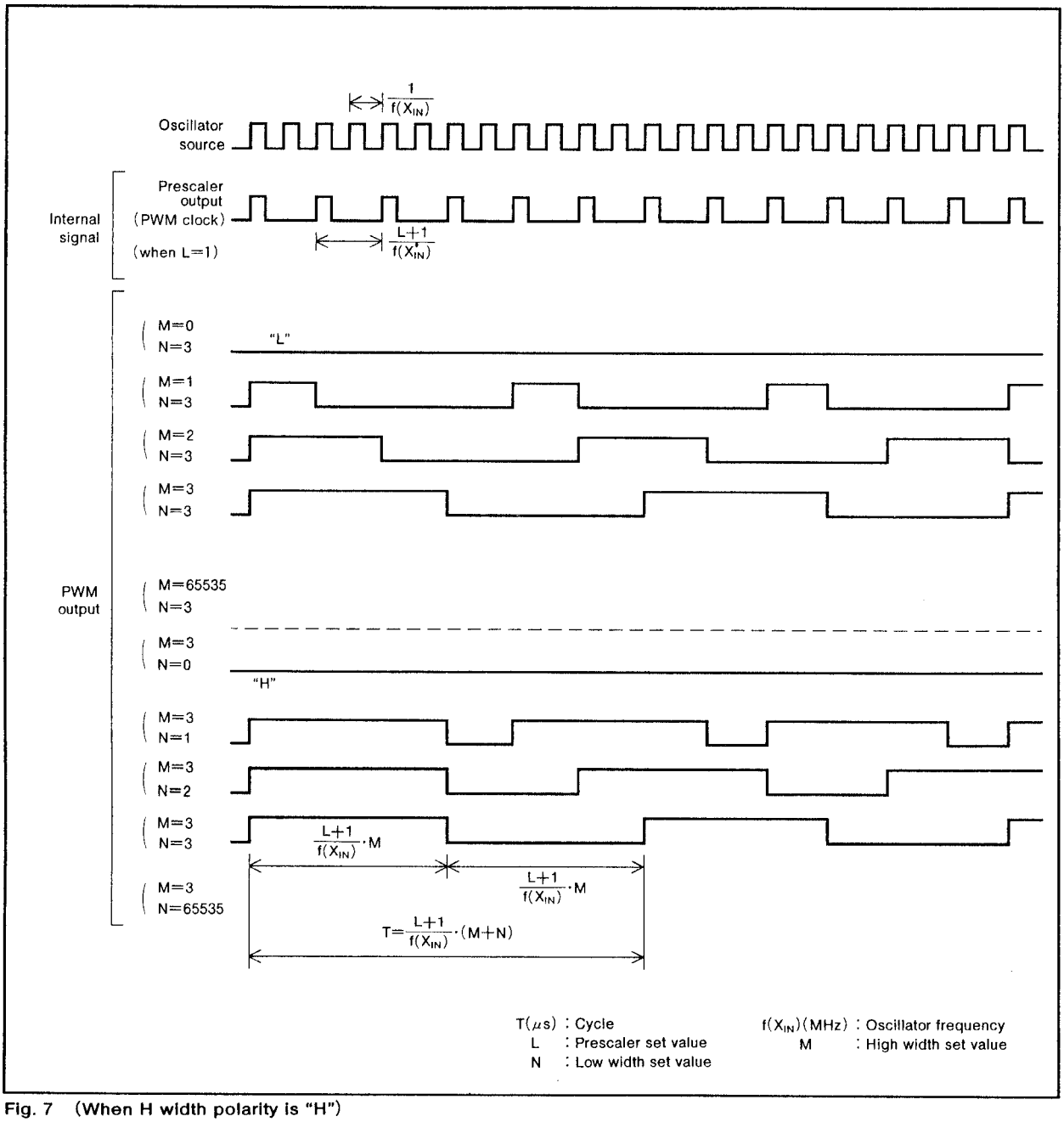


Fig. 7 (When H width polarity is "H")

Initial state

When external trigger ON is selected in D1 in the case of Command 1, starting the operation of the internal circuit by writing enable by Command 3 does not output a pulse to PWM output, which is held in the high impedance state.
The pulse can be output to PWM output by entering H level in TRG input for Mode 0 or Mode 2 or H pulse in TRG input in Mode 1 (see Fig. 8).
Putting TRG input to L level during PWM output in Mode 0 or Mode 2 makes PWM output keep its state. Putting TRG input back to H level starts the operation from that point.

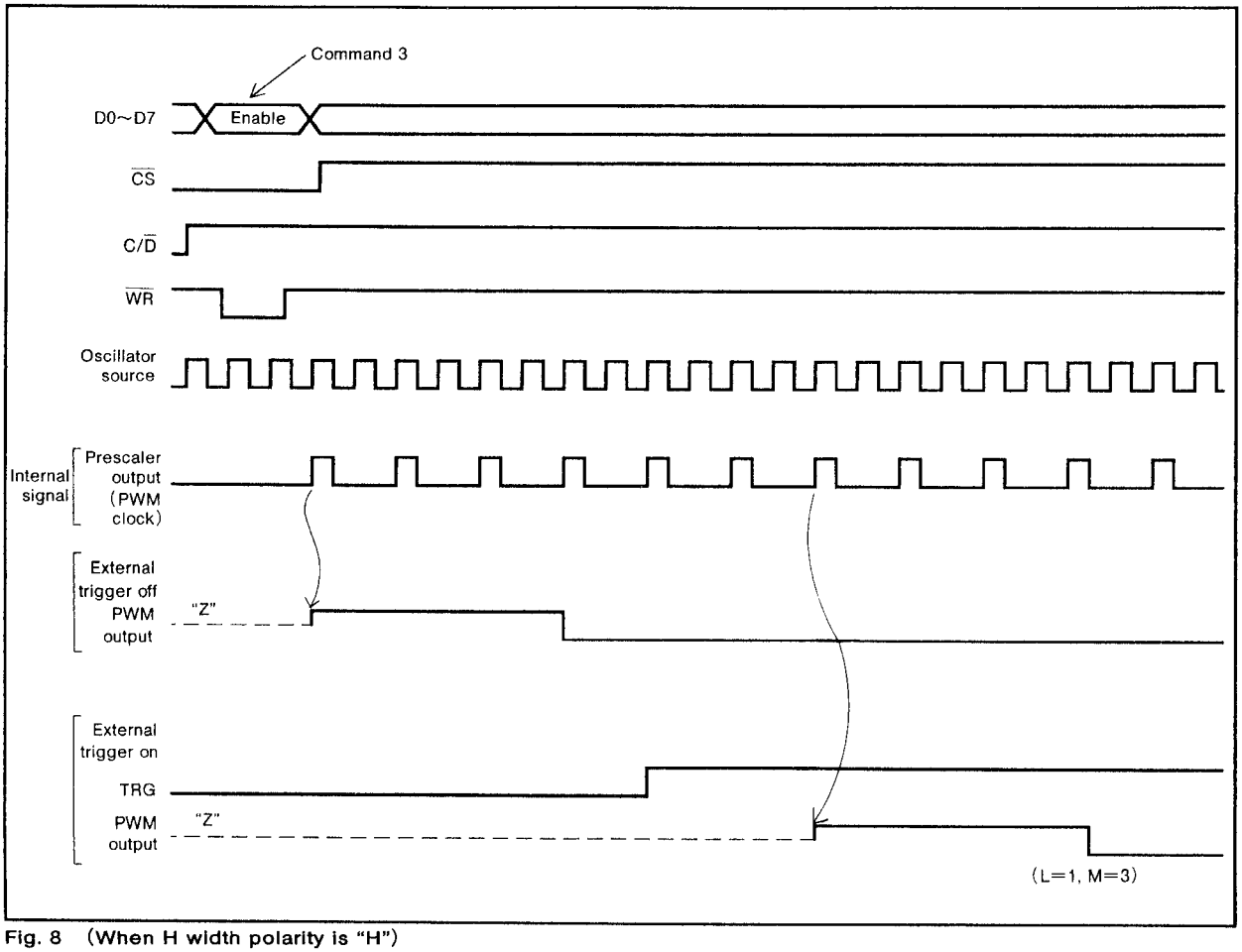


Fig. 8 (When H width polarity is "H")

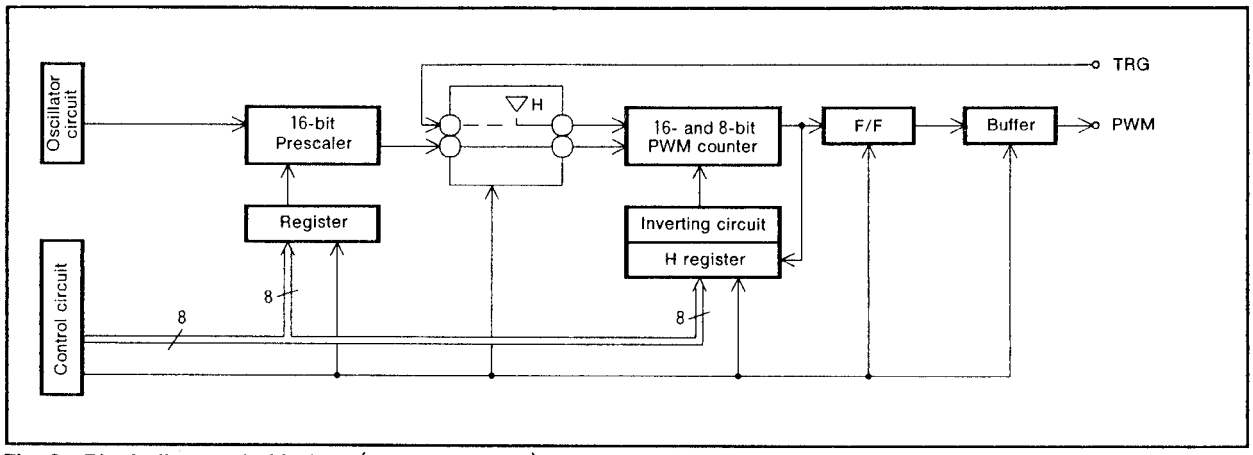


Fig. 9 Block diagram in Mode 0 (for one channel)

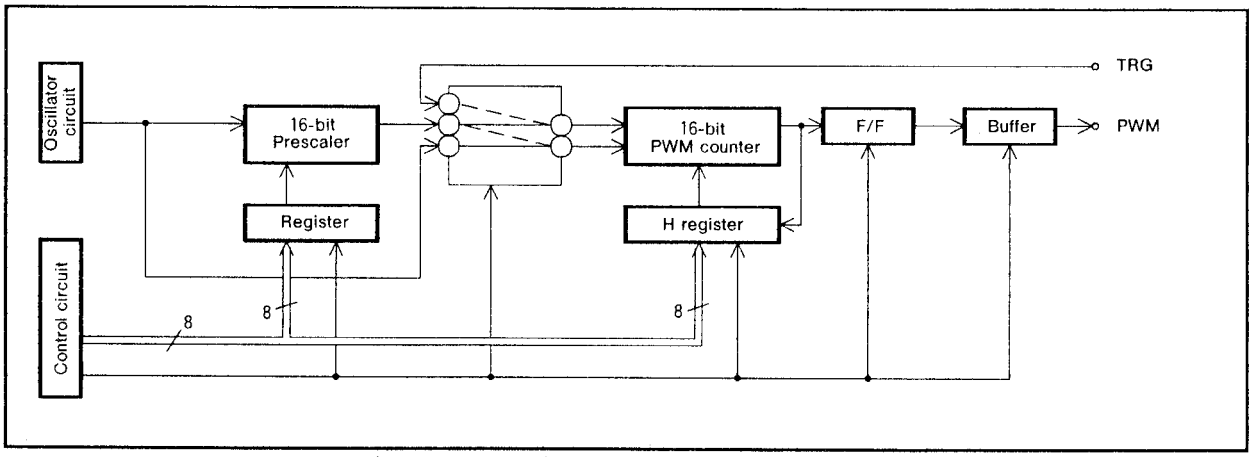


Fig. 10 Block diagram in Mode 1 (for one channel)

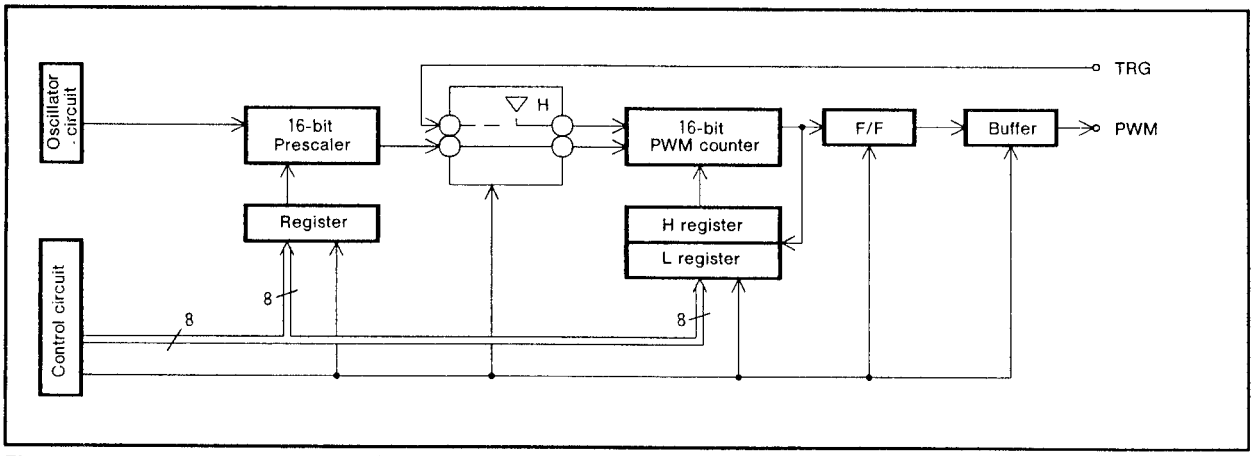


Fig. 11 Block diagram in Mode 2 (for one channel)

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power voltage		−0.5～+7.0	V
V_I	Input voltage		−0.5～V_{CC}+0.5	V
V_O	Output voltage		−0.5～V_{CC}+0.5	V
I_{IK}	Input protect diode current	V_I<0V	−20	mA
		V_I>V_{CC}	+20	
I_{OK}	Output parasitic diode current	V_O<0V	−20	mA
		V_O>V_{CC}	+20	
I_O	Output current		±50	mA
I_{CC}	Power/GND current	V_{CC} GND	±200	mA
P_d	Power dissipation		500	mW
T_{stg}	Storage temperature		−65～150	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V_{CC}	Power voltage	4.5	5.0	5.5	V
GND	Power voltage		0		V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
T_{opr}	Ambient operating temperature	−40		85	℃

ELECTRICAL CHARACTERISTICS (T_a=−40～85℃, V_{CC}=5V±10%)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_T+	Positive going threshold voltage	V_O=0.1, V_{CC}−0.1V, I_O=20μA $\overline{RESET}$, TRG1～4			2.4	V
V_T−	Negative going threshold voltage	V_O=0.1, V_{CC}−0.1V, I_O=20μA $\overline{RESET}$, TRG1～4	0.6			V
V_H	Hysteresis width	V_O=0.1, V_{CC}−0.1V, I_O=20μA $\overline{RESET}$, TRG1～4	0.2			V
V_{IH}	"H" Input voltage	V_O=0.1, V_{CC}−0.1V, I_O=20μA D_0～D_7, CS, $\overline{WR}$, C/$\overline{D}$	2.0			V
V_{IL}	"L" input voltage	V_O=0.1, V_{CC}−0.1V, I_O=20μA D_0～D_7, CS, $\overline{WR}$, C/$\overline{D}$			0.8	V
V_{IH}	"H" input voltage	V_O=0.1, V_{CC}−0.1V, I_O=20μA X1	V_{CC}×0.8			V
V_{IL}	"L" input voltage	V_O=0.1, V_{CC}−0.1V, I_O=20μA X1			V_{CC}×0.2	V
V_{OH}	"H" output voltage	V_I=V_{IH}, V_{IL} I_{OH}=−24mA PWM1～PWM4	V_{CC}−0.8			V
V_{OL}	"L" output voltage	V_I=V_{IH}, V_{IL} I_{OL}=24mA PWM1～PWM4			0.55	V
I_{IH}	"H" input current	V_I=V_{CC}			1.0	μA
I_{IL}	"L" input current	V_I=GND			−1.0	μA
I_{OZH}	Off-state "H" output current	V_O=V_{CC}			5.0	μA
I_{OZL}	Off-state "L" output current	V_O=GND			−5.0	μA
I_{CC}	Quiescent current consumption	V_I=V_{CC}, GND I_O=0μA			100	μA
ΔI_{CC}	Max. quiescent current consumption	V_I=2.4V, 0.4V (Note 1)			2.9	mA

Note 1 : Set only one input to this value; fix other inputs to V_{CC} or GND.

SWITCHING CHARACTERISTICS (T_a=−40~85℃, V_{CC}= 5 V±10%)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{PZL(\overline{W}-PWM)}$	Output enable time after write (Mode 0, 2, external trigger OFF)	C_L=50pF		$\frac{L+2}{f}+44$	$\frac{L+2}{f}+110$	ns
$t_{PZH(\overline{W}-PWM)}$	Output enable time after write (Mode 0, 2, external trigger OFF)			$\frac{L+2}{f}+43$	$\frac{L+2}{f}+110$	ns
$t_{PZL(\overline{W}-PWM)}$	Output enable time after write (Mode 1, external trigger OFF)			$\frac{L+3}{f}+34$	$\frac{L+3}{f}+110$	ns
$t_{PZH(\overline{W}-PWM)}$	Output enable time after write (Mode 1, external trigger OFF)			$\frac{L+3}{f}+33$	$\frac{L+3}{f}+110$	ns
$t_{PZL(T-PWM)}$	Output enable time after trigger (Mode 0, 2, external trigger ON)			$\frac{2(L+1)}{f}+44$	$\frac{2(L+1)}{f}+110$	ns
$t_{PZH(T-PWM)}$	Output enable time after trigger (Mode 0, 2, external trigger ON)			$\frac{2(L+1)}{f}+38$	$\frac{2(L+1)}{f}+110$	ns
$t_{PZL(T-PWM)}$	Output enable time after trigger (Mode 1, external trigger ON)			$\frac{2(L+1)}{f}+41$	$\frac{2(L+1)}{f}+110$	ns
$t_{PZH(T-PWM)}$	Output enable time after trigger (Mode 1, external trigger ON)			$\frac{2(L+1)}{f}+39$	$\frac{2(L+1)}{f}+110$	ns
$t_{PLH(X1-PWM)}$	Output propagation time after clock (all modes)			41	110	ns
$t_{PHL(X1-PWM)}$	Output propagation time after clock (all modes)			44	110	ns
$t_{PLH(T-PWM)}$	Output propagation time after trigger (Mode 1, external trigger ON)			$\frac{2(L+1)}{f}+40$	$\frac{2(L+1)}{f}+110$	ns
$t_{PHL(T-PWM)}$	Output propagation time after trigger (Mode 1, external trigger ON)			$\frac{2(L+1)}{f}+42$	$\frac{2(L+1)}{f}+110$	ns
$t_{PLZ(\overline{R}-PWM)}$	Output disable time after reset			58	150	ns
$t_{PHZ(\overline{R}-PWM)}$	Output disable time after reset			60	150	ns
$t_{PLZ(\overline{W}-PWM)}$	Output disable time after write			32	150	ns
$t_{PHZ(\overline{W}-PWM)}$	Output disable time after write			30	150	ns

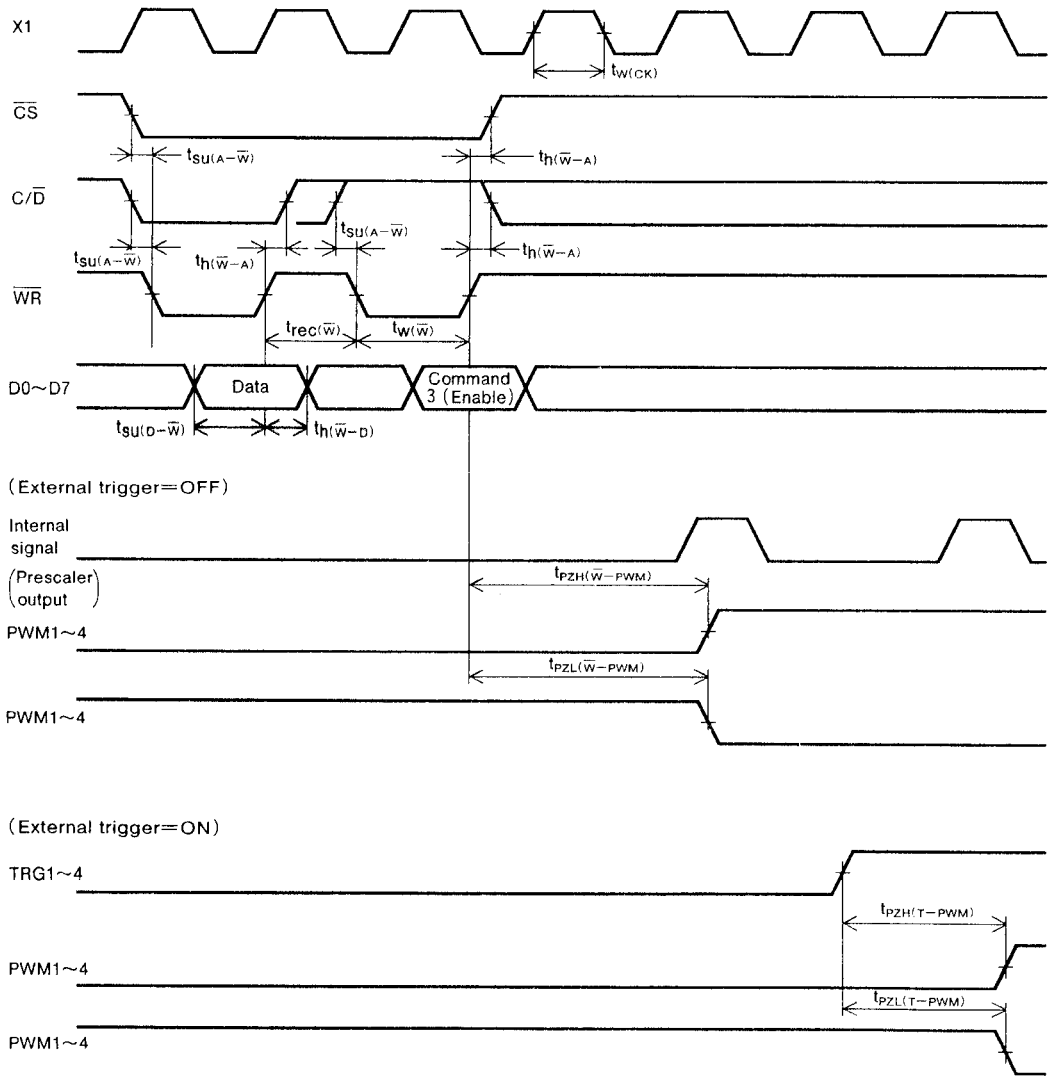
f(MHz) : Clock input frequency
L : Prescaler setting

TIMING CONDITIONS (T_a=−40~85℃, V_{CC}= 5 V±10%)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{C(X1)}$	Clock cycle		78.5			ns
$t_{WH(X1)}$	Clock "H" pulse width		35	9		ns
$t_{WL(X1)}$	Clock "L" pulse width		35	12		ns
$t_{r(X1)}$	Clock rise time				20	ns
$t_{f(X1)}$	Clock fall time				20	ns
$t_{SU(A-\overline{W})}$	Address setup time before write (CS, C/D)		0	−11		ns
$t_{h(\overline{W}-A)}$	Address hold time after write (CS, C/D)		0	−11		ns
$t_{SU(D-\overline{W})}$	Data setup time before write		100	55		ns
$t_{h(\overline{W}-D)}$	Data hold time after write		0	−28		ns
$t_{w(\overline{W})}$	Write pulse width		100	12		ns
$t_{rec(\overline{W})}$	Write recovery time		100	12		ns
$t_{w(T)}$	Trigger pulse width		100	23		ns
$t_{w(\overline{R})}$	Reset pulse width		100	30		ns
$t_{rec(\overline{R}-\overline{W})}$	Recovery time before write		100			ns

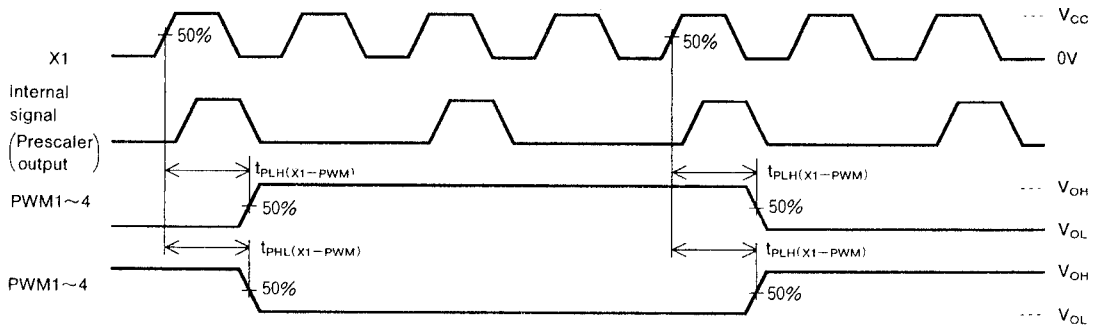
TIMING CHART

(1) MCU interface

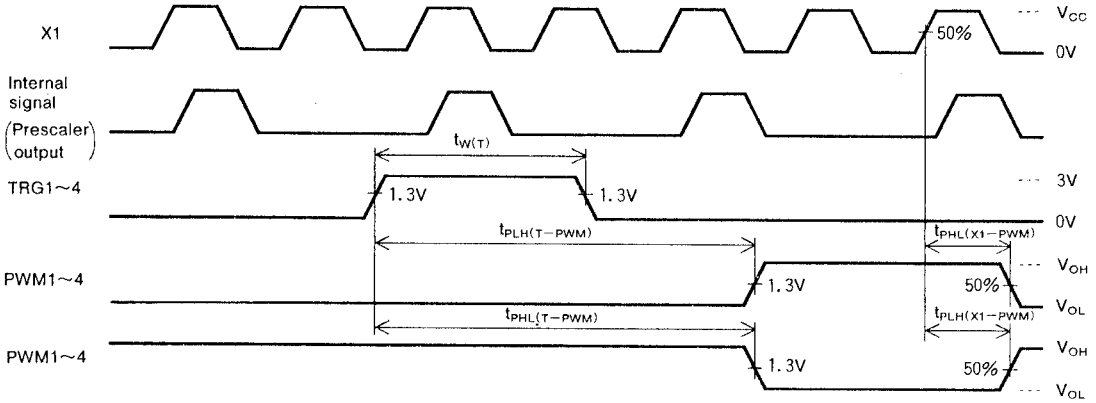


(2) In operation

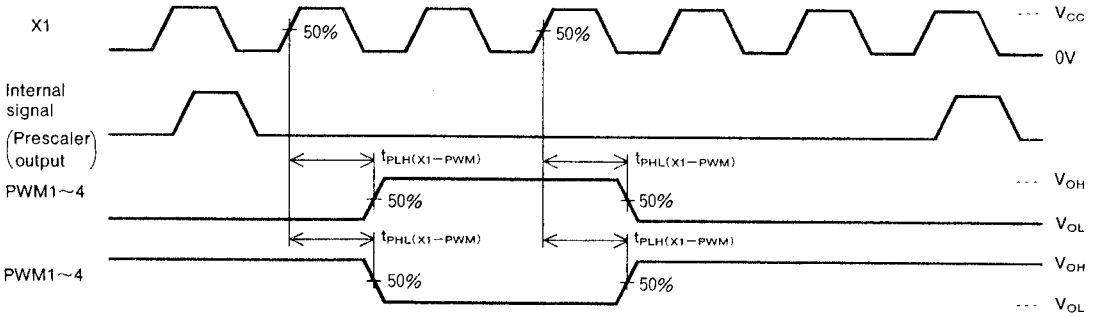
Mode 0, 2 (external trigger ON, OFF)



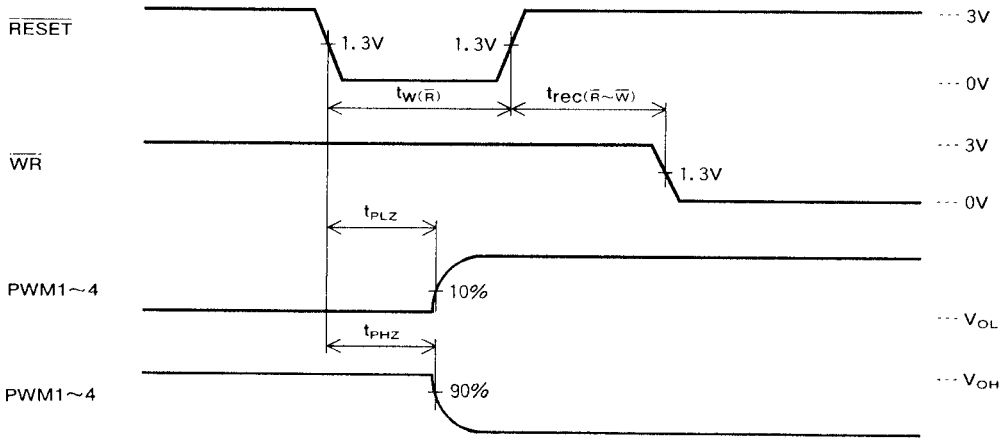
Mode 1 (external trigger ON)



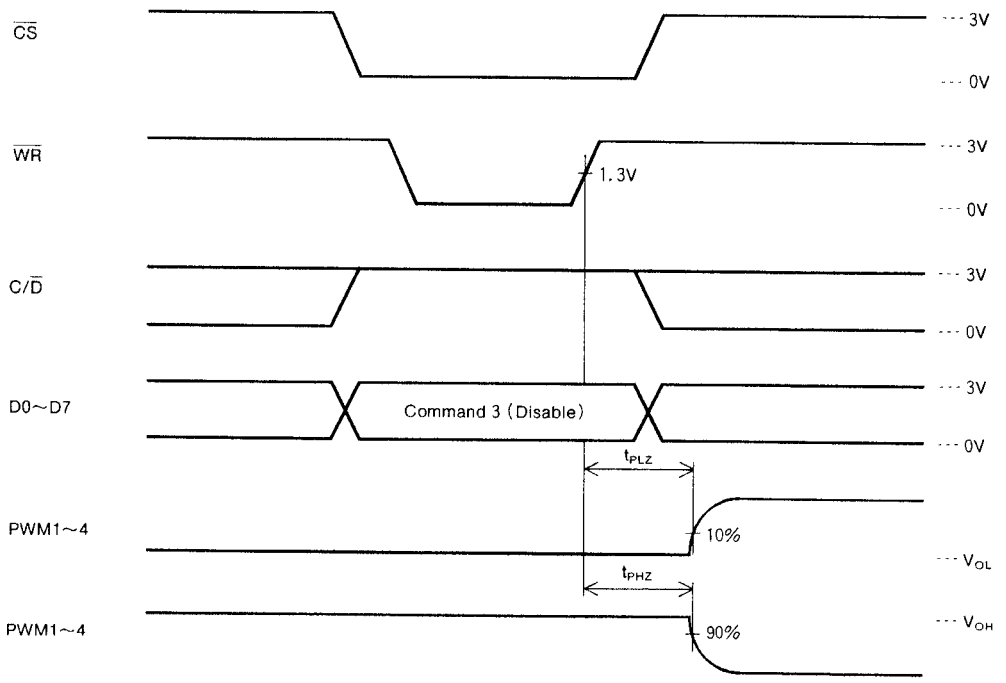
Mode 1 (external trigger OFF)



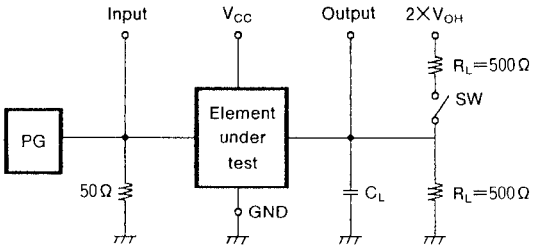
(3) At reset



(4) At disable



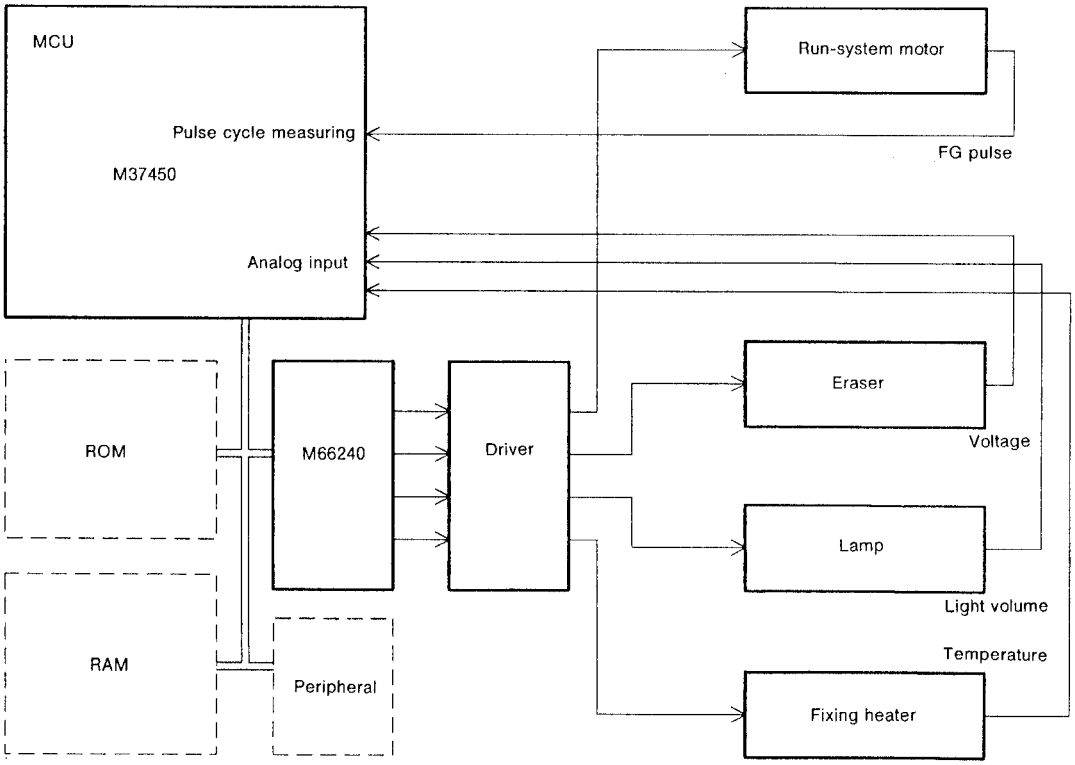
Measuring circuit



Parameter	SW
t_{TCH}, t_{THL} t_{PLH}, t_{PHL}	Open
t_{PLZ}	Closed
t_{PHZ}	Open
t_{PZL}	Closed
t_{PZH}	Open

(1) Characteristics of pulse generater (PG)(10%~90%)
t_r=3ns, t_f=3ns
(2) C_L includes stray probe and wiring capacitance.

APPLICATION EXAMPLE



Note) M37450 : ROM 4KB~16KB
RAM 128B~384B
Timer Multifunctional 16-bit type with pulse cycle measuring mode×3
A-D 8-bits, 8 channels
PWM 20kHz cycle, 1 channel
UART Clock sync and async, 1 channel