Preliminary Product Information

IMP50E10 EPAC™ (Electrically Programmable Analog Circuit)

Introduction

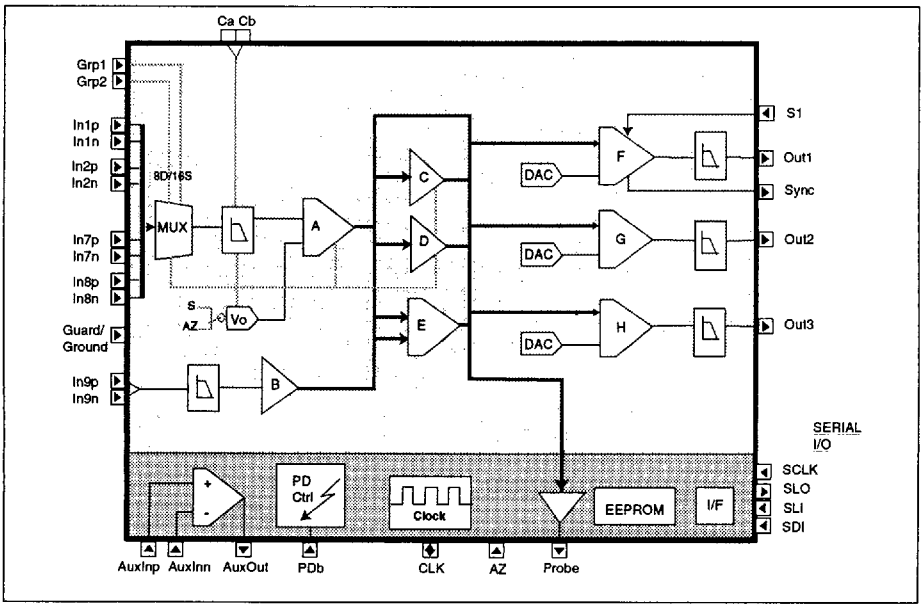
The IMP50E10 offers unequaled flexibility in an analog IC by using optimized analog switches and on-chip EEPROM to store user-programmable circuit configurations. Programming is made easy using Analog Magic™, the software design environment for the EPAC family. The IMP50E10 is optimized for use in multi-channel analog signal conditioning applications. Strong advantages are realized when multiple input signal amplitudes and offsets are necessary, because the IMP50E10 can simultaneously switch between up to four different gain and offset settings. Users can also take advantage of the low power, switched capacitor CMOS technology used in the IMP50E10 for battery powered circuits.

Applications

Signal Conditioning
Process Control
Data Logging
DSP Front End
Test Equipment

Key Features

- User-Programmable Functions Include: Programmable Gain Amplifiers, Comparators, Multiplexer, DACs, Track-and-Hold, Filtering, Power Consumption, and Interconnect
- Unconditionally Stable Regardless of Circuit Configuration
- Fast Prototypes: Go From Start to Finish in One Hour
- Single Supply 5V Operation
- Group Switching Allows Programmable Gains and Offsets to Vary Depending on Input Channel Selection
- "What-You-See-Is-What-You-Get" (WYSIWYG) Design Environment
- Sleep Mode Current < 40µA
- Offset Auto-Zero to Within 25µV
- 125kHz Throughput (Nyquist rate)
- No External Components Required
- MagicProbe™ for Easy In-System Debugging



Block Diagram

IMP50E10 EPAC (Electrically Programmable Analog Circuit)

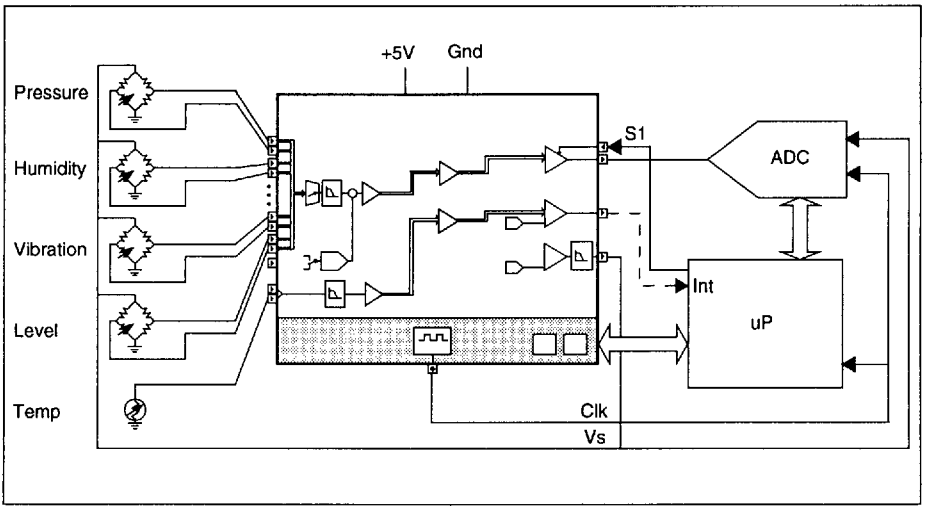
General Description

The IMP50E10 is a member of IMP's EPAC product line. An EPAC device allows circuit and system-level designers to develop highly integrated analog or analog-digital systems without the time and risk associated with traditional analog ASIC and custom-IC approaches. An EPAC device is essentially the analog counterpart to a field-programmable digital circuit (FPLD, FPGA, etc.). The IMP50E10 allows permanent storage of configuration data in on-chip EEPROM. Additionally, the configuration can be changed in real time by writing to the chip's configuration registers on-the-fly. With Analog Magic, the Windows™-based EPAC Design-System, the user can configure and program an EPAC device in minutes. Once programmed, an EPAC device configures itself automatically upon power-up or with a user command. Programming is achieved through a simple 3-wire serial interface. The configuration can be modified anytime.

The IMP50E10 consists of several flexible, functional modules, each of which offers a variety of features and characteristics, such as programmable gain, hysteresis, speed, etc. Most importantly, all functions can be realized without any external components and without any transistor-level design.

Modules can be interconnected in various ways without any impact on performance or stability. Interconnect is made possible via optimized analog switches. Routing of signals is semi-automatic and fully supported by Analog Magic. Thus, it is very easy to select modules, set their functions and parameters, and connect them to other blocks. As a result, the user can quickly implement and change a certain analog function and immediately test it in the system.

A complete EPAC Development System is available including Analog Magic, the IMP50E10 device-specific data-file, sample parts, and all hardware needed to program the parts directly from the user's PC.



Application Example of a Data Acquisition System (showing only the used modules inside the chip)

IMP50E10 EPAC (Electrically Programmable Analog Circuit)

IMP50E10 Feature Highlights

The IMP50E10 is optimized for use in multi-channel analog signal conditioning applications where channel dependent gain and offset settings are advantageous. Two high-impedance input amplifier modules and three core amplifier modules are available to amplify analog signals, offering gain settings from 0.5 to 10 in eight steps. Input signals containing substantial DC offsets can be shifted by means of an offset nullor module in 25µV, 100µV, 1mV, and 20mV steps, up to a maximum voltage of ±2.54V. The IMP50E10 operates off a single +5V supply and needs no external components.

Programmable output modules can be used as amplifiers, voltage references, track-and-hold amplifiers, and comparators (with and without hysteresis). All output modules have a 5-bit DAC, which can be used to either generate a reference voltage or to program the thresholds when in comparator mode.

The IMP50E10 accepts up to 9 fully-differential or 17 single-ended input signals. Input signals between V_{SS} and V_{DD} (true rail-to-rail swing) are acceptable. An integrated single-pole continuous-time filter can be switched into the signal path to limit the signal bandwidth to 15kHz, removing the need for an external anti-alias filter. An optional external capacitor can be added to achieve lower corner frequencies.

Even though all analog modules feature local offset cancellation and low-frequency noise suppression, an overall Auto-Zero loop is available which cancels offsets along a path from the multiplexer to any one of the three output modules, achieving overall offsets as low as ±25µV. A dedicated pin is available to re-trigger the preprogrammed Auto-Zero sequence.

One uncommitted amplifier is available which can be used with user-provided (i.e., external) feedback components.

The IMP50E10 features a variety of power-down options (e.g., per module or for the entire chip) as well as a low-power mode where modules operate at about 12% of the normal power consumption and at 1/8 speed and bandwidth. This is especially useful for battery-operated or remotely operated systems. A dedicated power-down pin is available to put the chip into a user-programmable power-down mode.

All on-chip modules can be connected to other modules in a variety of ways. Unused modules can be turned off. Thus, one IMP50E10 can serve a large number of analog applications by simply programming the desired functions and characteristics. Configuration data can be stored permanently in an on-chip EEPROM, with automatic configuration upon power-up. A security bit can be set which disables reading back of the EEPROM contents.

With MagicProbe, an interactive real-time debugging mode, the user can easily probe internal signals, while the IC is in the system.

Analog Magic also supports documentation of the final design, including a text report and a print out of the schematic. The final configuration data is made available for use in a microprocessor-based environment where on-the-fly reconfiguration is advantageous. Furthermore, the complete bit-map for the IMP50E10 is available for real-time microprocessor control of selected modules.

IMP50E10 EPAC (Electrically Programmable Analog Circuit)

General Electrical Characteristics

Unless otherwise specified, $4.5V < V_{DD} < 5.5V$, $T_A = 0–70^{\circ}C$

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Power Supply Voltage		4.5	5	5.5	V
Quiescent Supply Current	Sleep mode		40	70	µA
	Low power, all modules active		3.8	5	mA
	Turbo power, all modules active		18	20	mA
Programming Time	to EEPROM, f_{clock} = 800Hz, full configuration		340		ms
	to Configuration Register, f_{clock} = 1.5 MHz, full configuration		200		µs
EEPROM Download Time	To Configuration Register		1		ms
Channel Scan Rate	< 4 channels, modules A & F, no filters, normal power			8	µs per channel
	> 4 channels, modules A & F, no filters, normal power			26	µs per channel
Write Cycles	to EEPROM	10,000			
Data Retention	$T_A = 70°C$	10			Years
System Clock	Master mode		500		kHz
Internal Sampling Rate	Normal power		250		kHz
	Low power		31		kHz
System Bandwidth	Using internal anti-alias filter	13.5	15	17	kHz
	Normal power, no filter (limited by Nyquist rate)	115	125	132	kHz
	low-power mode, filter on or off (Nyquist rate reduced)	13	15	16	kHz
Input Signal Range		$V_{SS} - 0.2$		$V_{DD} + 0.2$	V
Common-Mode Range		0		5	V
Output Signal Range	R_L = 10 kΩ	$V_{SS} + 0.05$		$V_{DD} - 0.05$	V

General Electrical Characteristics (Cont.)

Unless otherwise specified, $4.5V < V_{DD} < 5.5V$, $T_A = 0–70^{\circ}C$

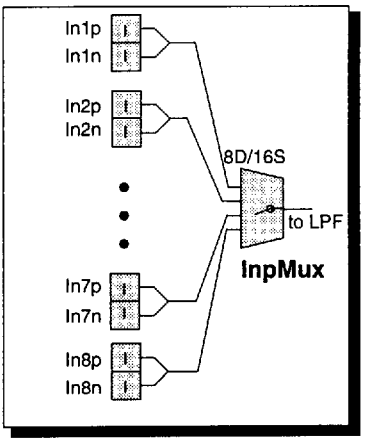
PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Minimum Gain	All modules in series		1		V/V
Maximum Gain	All modules in series		20,000		V/V
Gain Error	Modules A, C, & F in series, gains = 10,4,2		±2		%
Gain Drift	T_A = 0–70°C,Modules A, C, & F in series, gains = 10, 4, 2		30		ppm/°C
Input Offset Voltage	Modules A, C, & F in series, gains = 10, 4, 2, no auto-zero, V_{CM} = 2.5V		±4		mV
	With auto-zero		100		µV
Input Offset Drift	Modules A, C, & F in series, gains = 10, 4, 2, with auto-zero		60		µV/°C
Input Noise Voltage Density	Modules A & F in series, gains = 10,2, f = 5kHz		0.4		$\mu V/\sqrt{Hz}$
Total Harmonic Distortion	2nd, 3rd order harmonics, modules A & F in series, 0.5<Vin<4.5, gain = 1, f = 1kHz		-68		dB

Input Modules

Input Multiplexer Module

Key features:

- 8 fully differential or 16 single-ended inputs
- Channels are selectable through serial I/O
- Channels are evenly divided into 4 groups
- Groups are selectable through the serial interface or through the Grp select pins
- Guard/Ground pin available to increase CMRR or serve as external ground reference for auto-zero
- Built-in zero-reference for auto-zero



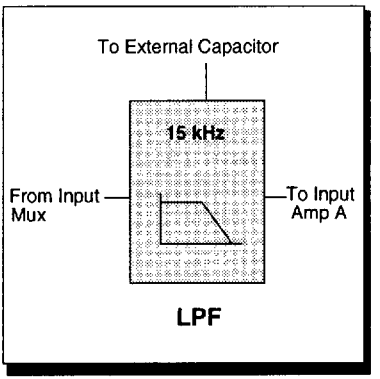
Performance Characteristics of the Input Multiplexer

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Number of Channels	Differential mode Single-ended mode		8 16		
Power Supply Current			0		µA
On Resistance				100	Ω
Off Resistance		10			MΩ
Crosstalk			-70		dB
Input Voltage Range		V_{SS} – 0.2		V_{DD} + 0.2	V

Low Pass Filter (LPF) Module

Key features:

- Select the internal capacitor (f_c = 15 kHz) or provide an external one for $f_c \leq 845$ kHz
- Filters both differential and single-ended signals
- Zero DC power consumption (passive filter)
- Single-pole RC filter architecture with 6dB per octave roll-off
- Utilizing group switching, the internal or external capacitor option can be programmed differently depending upon which group is used



Performance Characteristics of the LPF Module

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Power Supply Current			0		µA
Settling Time	5 time constants (99.3%)		53		µs
Cutoff Frequency	$C_{internal}$ = ON	13	15	17	kHz
	$C_{internal}$ = OFF		845		kHz
Low Pass Resistor			144		kΩ

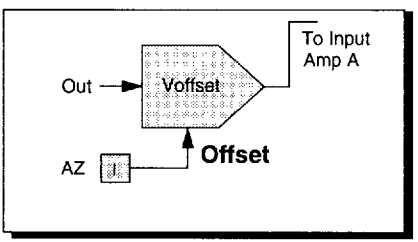
Calculating $C_{external}$ for a desired cutoff frequency:

$0.1 \le f_c \le 15$ kHz; $C_{internal}$ = ON; $C_{external} = \frac{1}{892E3 \times f_c} - 75$ pF

$0.1 \le f_c \le 845$ KkHz; $C_{internal}$ = OFF; $C_{external} = \frac{1}{892E3 \times f_c}$

Offset Module

Key features:



- 10 bit DAC (7 magnitude + 1 sign + 2 step-size)
- 4 step sizes (25µV/100µV/1mV/20mV)
- ±127 steps, true bipolar operation with no missing codes
- Utilizes group switching so that offsets can be programmed to different voltages depending upon which group is used
- Auto-zero capability between the multiplexer and any Output Module (F, G, or H)

Performance Characteristics of the Offset Module

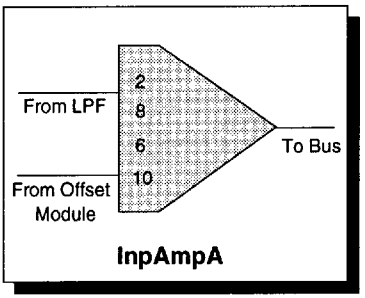
PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Power Supply Current	Normal power		380	400	µA
	Low power		50		µA
Voltage Range	LSB, range 1 Full scale, range 1		25 ±3.175		µV mV
	LSB, range 2 Full scale, range 2		100 ±12.7		µV mV
	LSB, range 3 Full scale, range 3		1.0 ±127		mV mV
	LSB, range 4 Full scale, range 4		20 ±2.54		mV V
Voltage Range Error	All ranges		3		%
Voltage Drift	Fine range		100		ppm/°C

IMP50E10 EPAC (Electrically Programmable Analog Circuit)

Input Amplifier Module A

Key features:

- Accepts single-ended and differential input signals
- Local auto-zero and 1/f noise cancellation
- Gain choices available: 0.5, 1, 2, 3, 4, 6, 8, 10
- Utilizes group switching so that up to four different gain settings can be programmed, with the amplification level depending upon which group is selected

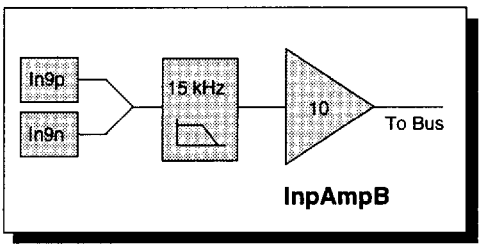


Performance Characteristics of Input Amplifier Module A

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Power Supply Current	Normal power Low power		380 50	400 60	µA µA
Gain Error	Gain = 1 . . . 10		0.2		%
Gain Drift			tbd		
Input Offset Voltage	V_{CM} = 2.5V, gain = 4		±1		mV
Input Offset Drift	V_{CM} = 2.5V		10		µV/°C
Input Impedance	Differential mode, normal power, gain = 4, V_{CM} = 2.5V		20		MΩ
	Differential mode, low power, V_{CM} = 2.5V		20		MΩ
	Common mode, normal power, V_{CM} = 2.5V		2		MΩ
	Common mode, low power, V_{CM} = 2.5V		16		MΩ
PSRR	@ 60Hz		60		dB
CMRR	@ 0Hz, gain=4		55		dB
Propagation Delay	Normal power		4		µs

Input Amplifier Module B

All electrical specifications and features are identical to those of Input Amplifier Module A, with the exception that there is no group switching capability. Also, the filter can be programmed to be either on or off.



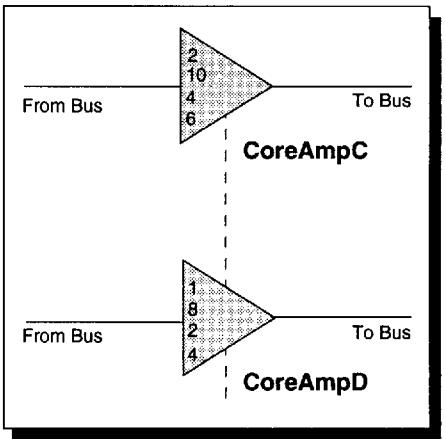
IMP50E10 EPAC (Electrically Programmable Analog Circuit)

Core Modules

Core Amplifier Modules C & D

Key features:

- Programmable gain settings of 1, 1.5, 2, 3, 4, 6, 8, 10
- Choose inverting or non-inverting configurations
- Utilizes group switching so that up to four different gain settings can be programmed, with the amplification level depending upon which group is selected
- Cascadable to increase total gain
- Local offset and 1/f noise cancellation



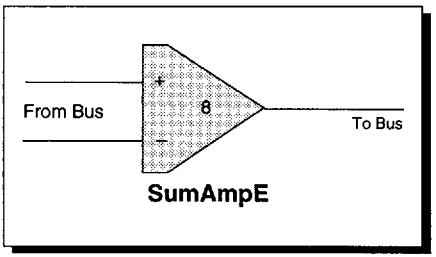
Performance Characteristics of Core Modules C & D

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Power Supply Current	Normal power Low power		250 32		µA µA
Offset Voltage			±1		mV
Gain Error			0.15		%
Propagation Delay	Normal power		4		µs

Summing-Amplifier Module E

Key features:

- Programmable gain settings of 1, 1.5, 2, 3, 4, 6, 8, 10
- Choose to utilize one or two inputs and inverting or non-inverting configurations
- Cascadable with other core amplifiers to increase total gain
- Local auto-zero offset and 1/f noise cancellation

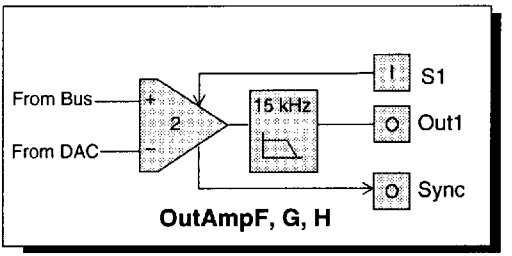


All electrical specifications are identical to those of Core Amplifier Modules C & D

IMP50E10 EPAC (Electrically Programmable Analog Circuit)

Output Modules

Output Modules F, G, H, & MagicProbe[1]



Key features:

- Use as an amplifier, T&H, comparator, or reference
- Fixed ± 2 gain amplifier
- Single-ended output to V_{SS} or 2.5V
- Optional LP-filtered output (15kHz)
- Track&Hold mode with dedicated control pins
- Comparator with optional 75mV hysteresis
- Optional enhanced slew rate capability (Turbo mode)

Performance Characteristics of Modules F, G, H and MagicProbe

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Quiescent Supply Current	Normal power, no load Turbo power, no load		0.6 1.4	1.0 2.0	mA mA
Propagation Delay	Normal Power		4		µs
Input Offset Voltage			±5		mV
Output Impedance	Normal power @ DC Turbo power @ DC		3 1		Ω Ω
Short Circuit Output Current			40		mA
Slew Rate	C_L = 50pF Normal power Turbo power	 1	 1.5 3		 V/µs V/µs
PSRR	Vout = 0.5 - 4V		55		dB
Output Voltage Range	R_L = 100Ω to ground	V_{SS} + 0.05		V_{DD} - 0.05	V
	R_L = 1kΩ to ground	V_{SS} + 0.05		V_{DD} - 0.5	V
Amplifier Mode					
Gain			±2		V/V
Gain Error			0.2		%
Gain Drift			15		ppm/°C
Output Filter Cut-off Frequency	Filter = ON		15		kHz
	Filter = OFF		363		kHz
Droop Rate	T&H mode	5	10	20	µV/s
Acquisition Time	to 0.1%, T&H mode			2	µs

1. The comparator mode does not apply to the MagicProbe. The track and hold specifications apply to module F only.

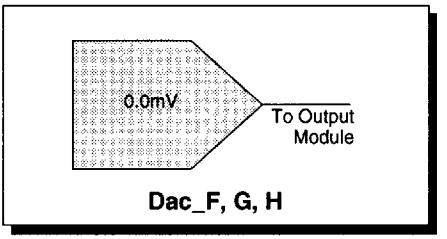
Performance Characteristics of Modules F, G, H and MagicProbe (Continued)

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Comparator Mode					
Hysteresis	Hysteresis = ON		75		mV
Delay	C_L = 50pF, normal power, 10mV overdrive		2	4	µs
Open Loop Gain			90		dB
Resolution			170		µV

DAC Modules F, G, & H

Key features:

- 32 voltage settings (= 4 bit + sign).
- One DAC for each Output Module, which is useful for setting thresholds, trip-points, and reference voltages.



Performance Characteristics of DAC Modules F, G, & H

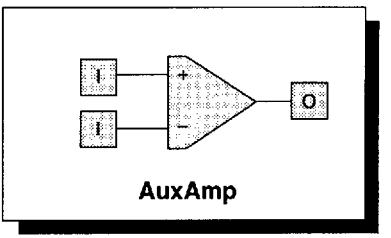
PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Power Supply Current	Total for three DACs			300	µA
Output Voltage		0		±2.0	V
Step Size			133		mV
Voltage Error			3		%
Voltage Drift	T_A = 0-70°C, V_{CM} = 2.5		100		ppm/°C
PSRR			55		dB

Other Modules

Auxiliary Amplifier Module

Key features:

- Inputs/Output externally accessible for adding external feedback
- Optional enhanced drive capability ("Turbo" Mode)
- Low power consumption



Performance Characteristics of the Auxiliary Amplifier

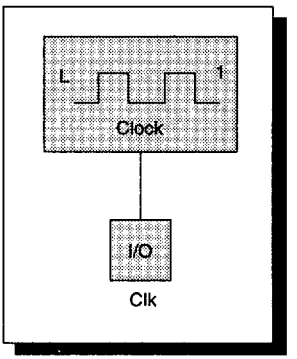
PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Quiescent Supply Current	Normal power Turbo power			1 3	mA mA
Input Offset Voltage			±1.5		mV
Input Offset Drift			tbd		
Input Resistance			500		MΩ
Output Resistance	Normal power Turbo power		3 1		Ω Ω
Open Loop Gain	Turbo OFF		90		dB
Unity-Gain Bandwidth	Turbo ON, C_L=100pF Turbo OFF, C_L=100pF		2.0 1.4		MHz MHz
CMRR			tbd		
PSRR	@ 60Hz		60		dB
Common-Mode Input Voltage Range		0		3	V
Output Voltage Range	I_{OUT} = ±50µA	V_{SS} + 0.05 V		V_{DD} – 0.05 V	V
	I_{OUT} = ±5mA	V_{SS} + 0.5 V		V_{DD} – 0.5 V	V
Slew Rate	C_L=30pF Normal power Turbo power		0.75 3		V/µs V/µs
Phase Margin	C_L=100pF, Normal or Turbo power	45	60		degrees
Input Bias Current			1.0		nA

IMP50E10 EPAC (Electrically Programmable Analog Circuit)

Clock Module

Key features:

- Master mode (On-chip oscillator), can drive off-chip logic
- Generates output frequencies from 62kHz to 500kHz
- Slave mode (follows external clock)
- Accepts external clock frequency from 500kHz to 4MHz
- Programmable input/output divider (N = 1,2,4,8)
- No external components

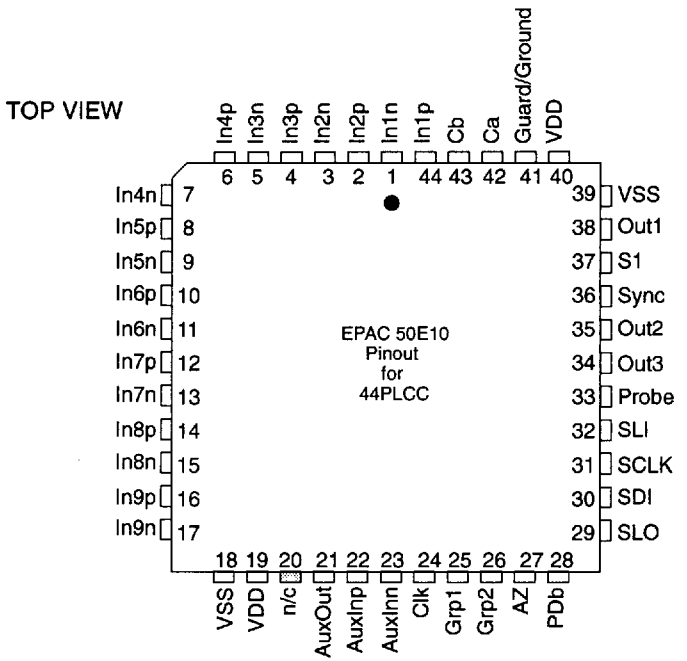


Performance Characteristics of the Clock Module

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Power Supply Current	External load = 10pF		0.5		mA
Output Frequency	Normal power, divider = 1	450	500	550	kHz
	Normal power, divider = 8	56	62	68	kHz
Duty Cycle	Master mode	47.5	50	52.5	%
Power-Supply Sensitivity	for V_{DD} ±10%		1		kHz/V
Frequency Drift	T_A = 0-70°			5	%
Output Voltage	TTL/CMOS compatible Low (at pin) High (at pin)	 90		10	 % of V_{DD} % of V_{DD}
Rise Time				50	ns
Fall Time				50	ns

IMP50E10 EPAC (Electrically Programmable Analog Circuit)

Pin Assignments



IMP50E10 EPAC (Electrically Programmable Analog Circuit)

Pin Description

The following table provides a list of the pin names, the type of pin (P)ower, (D)igital, or (A)nalog, and a description of the pin functions.

PIN NAME	TYPE	DESCRIPTION
VDD	P	Analog VDD. Analog positive supply, i.e., 5V
VSS	P	Analog VSS. Analog negative supply, i.e., 0V
Digital Pins		
S1	D	Track & Hold Input for Output Module F. High = Track, Low = Hold
Sync	D	Output signal indicating when Output Module F is actually holding.
SLI	D	Serial Load Input. Used as "chip select" for the serial interface and latches serial data into internal registers. Data can be shifted in while SLI is low. Data is latched in when SLI goes high. Input is TTL compatible.
SCLK	D	Serial Interface Clock Input. Clock input for shifting in serial data for programming the EPAC. Input is TTL compatible.
SDI	D	Serial Data Input. Input for shifting in serial data. A low level corresponds to a logical "0". Data is sampled on a low to high transition of SCLK. Input is TTL compatible.
SLO	D	Serial Load Output. Provides SLI type of output for the next cascaded EPAC.
PDb	D	Power-Down (Bar) Input. A user-configurable Power-Down input. Powers down all or selected modules when low. Must be high if unused.
AZ	D	Auto-Zero Input. A user-controlled input to trigger an Auto-Zero sequence. Must be low if not used.
Grp1, Grp2	D	Digital inputs to control the group-selection (also affects the selected input channel)
CLK	D	Clock Input or Output. Depending on the user configuration, this pin can act as an input to the on-chip timing logic or as an output from the on-chip oscillator.

IMP50E10 EPAC (Electrically Programmable Analog Circuit)

PIN NAME	TYPE	DESCRIPTION
Analog Pins:		
In1n, In1p... In9n, In9p	A	Analog Inputs. Configurable for single-ended or differential signals. High impedance mode when unused.
Guard/Ground	A	Guard or Ground Reference ("Zero") Input. In differential mode, this input can be used to connect to the guard, or shield, of the incoming signals, otherwise connect to AVSS. In single-ended mode, this input is used as an external ground ("Zero") reference. Connect to analog ground if not used.
Ca, Cb	A	External capacitor ports. An optional external capacitor (bipolar type) can be connected to reduce the corner frequency of the Low Pass Filter Module. High impedance mode when unused.
Out1, Out2, Out3	A	Analog Outputs. The output signals of the three output modules (F, G, and H) are available at these pins. High impedance mode when unused.
Probe	A/D	Probe Output. Internal analog or digital signals can be routed to this test pin. It can also read out configuration registers. High impedance mode when unused.
AuxInn, AuxInp	A	Inverting and non-inverting inputs to the Auxiliary Amplifier Module.
AuxOut	A	Output of the Auxiliary Amplifier Module.

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