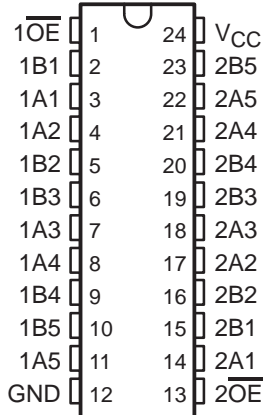


SN54CBTD3384, SN74CBTD3384 10-BIT FET BUS SWITCHES WITH LEVEL SHIFTING

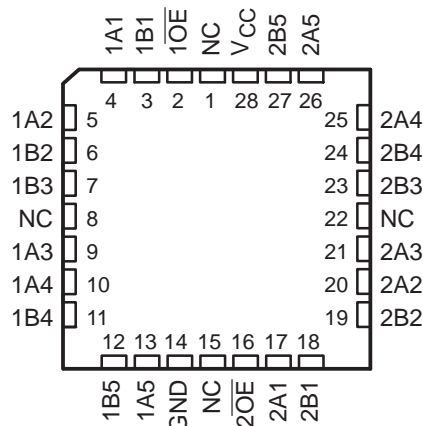
SCDS025R – MAY 1995 – REVISED JANUARY 2004

- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- Designed to Be Used in Level-Shifting Applications

SN54CBTD3384 . . . JT OR W PACKAGE
SN74CBTD3384 . . . DB, DBQ, DGV, DW, OR PW PACKAGE
(TOP VIEW)



SN54CBTD3384 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

The 'CBTD3384 devices provide ten bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switches allows connections to be made without adding propagation delay. A diode to V_{CC} is integrated on the die to allow for level shifting from 5-V signals at the device inputs to 3.3-V signals at the device outputs.

These devices are organized as two 5-bit switches with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the switch is on, and port A is connected to port B. When \overline{OE} is high, the switch is open, and the high-impedance state exists between the two ports.

ORDERING INFORMATION

T _A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOIC – DW	Tube	SN74CBTD3384DW	CBTD3384
		Tape and reel	SN74CBTD3384DWR	
	SSOP – DB	Tape and reel	SN74CBTD3384DBR	CC384
	SSOP (QSOP) – DBQ	Tape and reel	SN74CBTD3384DBQR	CBTD3384
	TSSOP – PW	Tube	SN74CBTD3384PW	CC384
		Tape and reel	SN74CBTD3384PWR	
	TVSOP – DGV	Tape and reel	SN74CBTD3384DGV	CC384
–55°C to 125°C	CDIP – JT	Tube	SNJ54CBTD3384JT	SNJ54CBTD3384JT
	CFP – W	Tube	SNJ54CBTD3384W	SNJ54CBTD3384W
	LCCC – FK	Tube	SNJ54CBTD3384FK	SNJ54CBTD3384FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2004, Texas Instruments Incorporated
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

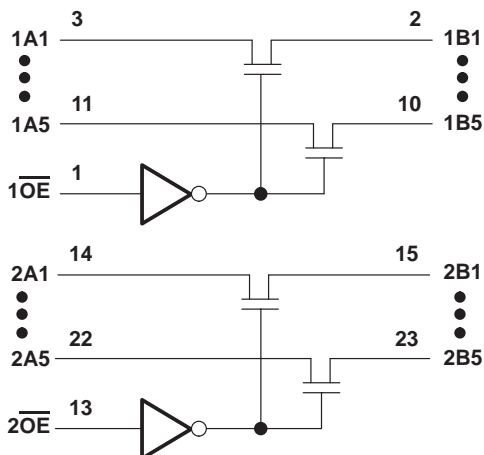
SN54CBTD3384, SN74CBTD3384 10-BIT FET BUS SWITCHES WITH LEVEL SHIFTING

SCDS025R – MAY 1995 – REVISED JANUARY 2004

FUNCTION TABLE
(each 5-bit bus switch)

INPUTS		INPUTS/OUTPUTS	
$\overline{1OE}$	$\overline{2OE}$	1B1–1B5	2B1–2B5
L	L	1A1–1A5	2A1–2A5
L	H	1A1–1A5	Z
H	L	Z	2A1–2A5
H	H	Z	Z

logic diagram (positive logic)



Pin numbers shown are for the DB, DBQ, DGV, DW, JT, PW, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Continuous channel current	128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	
DB package	63°C/W
DBQ package	61°C/W
DGV package	86°C/W
DW package	46°C/W
PW package	88°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.



SN54CBTD3384, SN74CBTD3384 10-BIT FET BUS SWITCHES WITH LEVEL SHIFTING

SCDS025R – MAY 1995 – REVISED JANUARY 2004

recommended operating conditions (see Note 3)

	SN54CBTD3384		SN74CBTD3384		UNIT
	MIN	MAX	MIN	MAX	
V _{CC} Supply voltage	4.5	5.5	4.5	5.5	V
V _{IH} High-level control input voltage	2		2		V
V _{IL} Low-level control input voltage		0.8		0.8	V
T _A Operating free-air temperature	-55	125	-40	85	°C

In applications with fast edge rates, multiple outputs switching, and operating at high frequencies, the output may have little or no level-shifting effect.

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54CBTD3384		SN74CBTD3384		UNIT	
		MIN	TYP†	MAX	MIN		TYP†
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA			-1.2		-1.2	V
V _{OH}	See Figure 2						
I _I	V _{CC} = 5.5 V, V _I = 5.5 V or GND			±1		±1	μA
I _{CC}	V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND			1.5		1.5	mA
ΔI _{CC} ‡	Control inputs V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND			2.5		2.5	mA
C _i	Control inputs V _I = 3 V or 0			3		3	pF
C _{io} (OFF)	V _O = 3 V or 0, \overline{OE} = V _{CC}			3.5		3.5	pF
r _{on} §	V _{CC} = 4.5 V	V _I = 0	I _I = 64 mA	5	5	7	Ω
			I _I = 30 mA	5	5	7	
		V _I = 2.4 V, I _I = 15 mA	35	35	50		

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54CBTD3384		SN74CBTD3384		UNIT
			MIN	MAX	MIN	MAX	
t _{pd} ¶	A or B	B or A		0.25		0.25	ns
t _{en}	\overline{OE}	A or B	2.2	9.7	2.3	7	ns
t _{dis}	\overline{OE}	A or B	1.5	8.6	1.7	5.3	ns

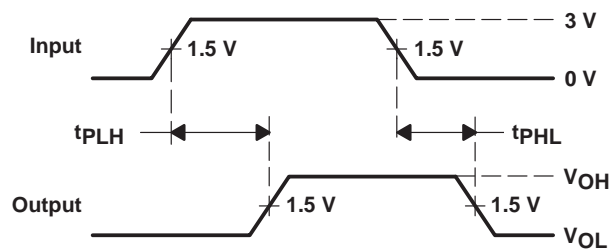
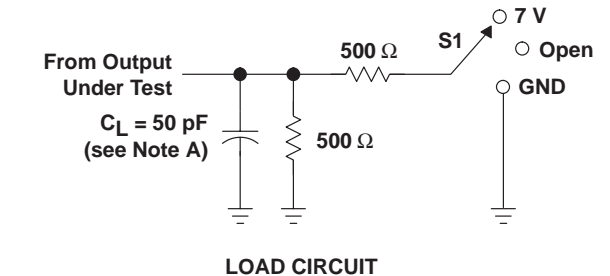
¶ The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



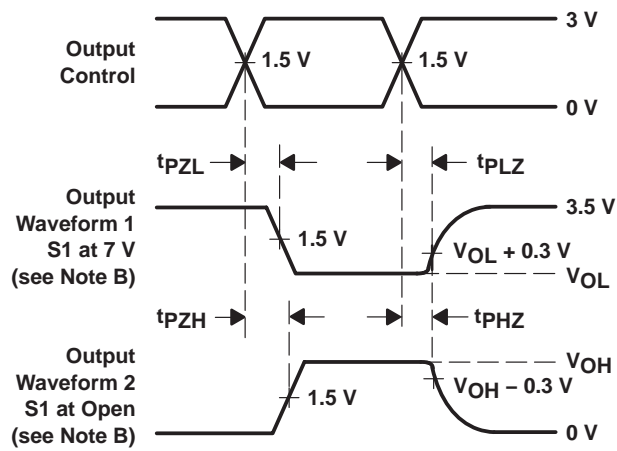
SN54CBTD3384, SN74CBTD3384 10-BIT FET BUS SWITCHES WITH LEVEL SHIFTING

SCDS025R – MAY 1995 – REVISED JANUARY 2004

PARAMETER MEASUREMENT INFORMATION



TEST	S1
t _{pd}	Open
t _{PLZ} /t _{PZL}	7 V
t _{PHZ} /t _{PZH}	Open



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis}.
 - t_{PZL} and t_{PZH} are the same as t_{en}.
 - t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

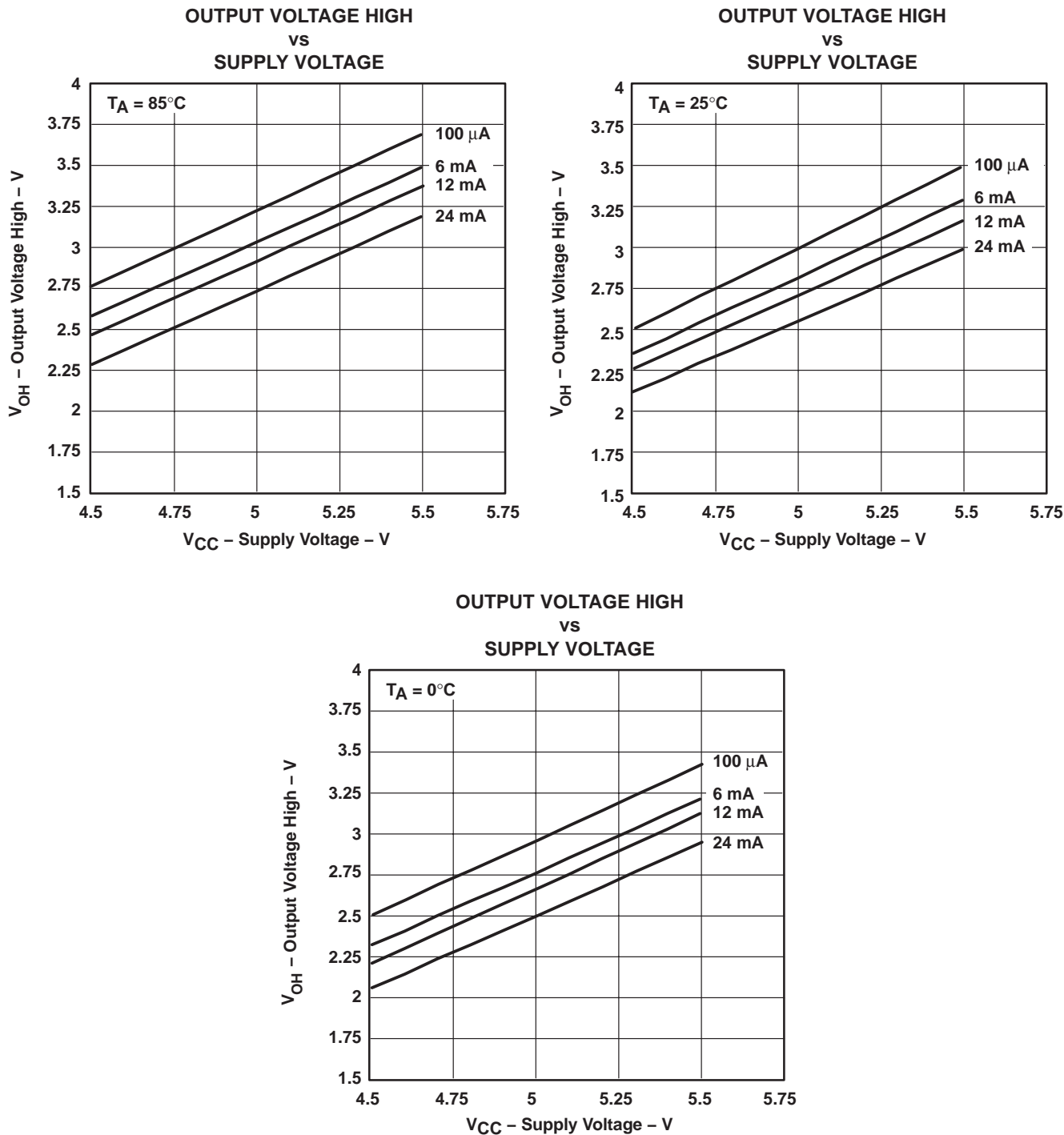


Figure 2. V_{OH} Values

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9752701Q3A	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9752701Q3A SNJ54CBTD 3384FK	Samples
SN74CBTD3384DBQR	ACTIVE	SSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CBTD3384	Samples
SN74CBTD3384DBR	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CC384	Samples
SN74CBTD3384DGVR	ACTIVE	TVSOP	DGV	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CC384	Samples
SN74CBTD3384DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTD3384	Samples
SN74CBTD3384DWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTD3384	Samples
SN74CBTD3384PW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CC384	Samples
SN74CBTD3384PWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CC384	Samples
SN74CBTD3384PWRE4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CC384	Samples
SN74CBTD3384PWRG4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CC384	Samples
SNJ54CBTD3384FK	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9752701Q3A SNJ54CBTD 3384FK	Samples
SNJ54CBTD3384JT	LIFEBUY	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9752701QL A SNJ54CBTD3384J T	
SNJ54CBTD3384W	LIFEBUY	CFP	W	24	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9752701QK A SNJ54CBTD3384W	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54CBTD3384, SN74CBTD3384 :

● Catalog: [SN74CBTD3384](#)

● Military: [SN54CBTD3384](#)

NOTE: Qualified Version Definitions:

● Catalog - TI's standard catalog product

- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBTD3384DBQR	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74CBTD3384DBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
SN74CBTD3384DGVR	TVSOP	DGV	24	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74CBTD3384DWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74CBTD3384PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

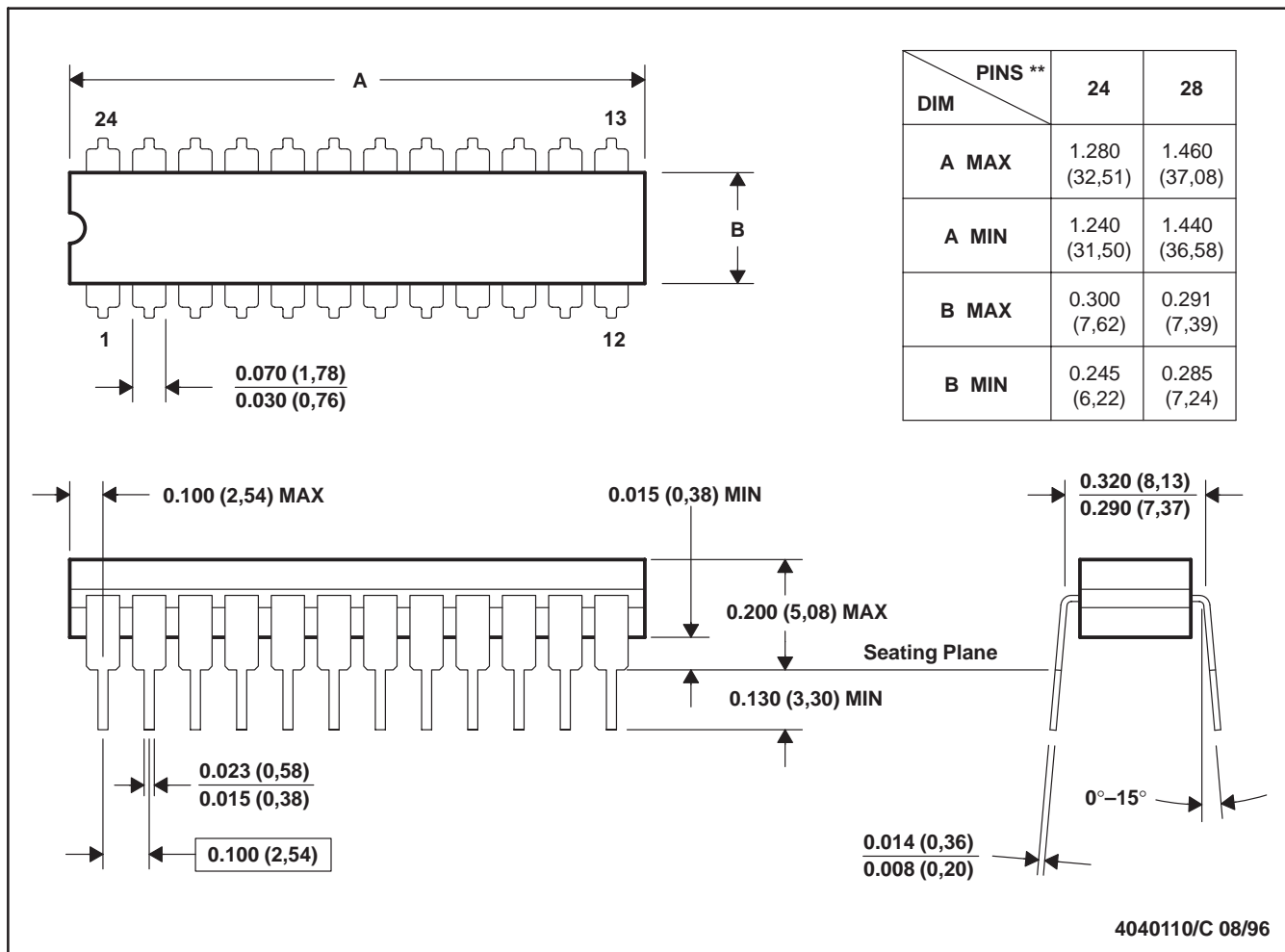

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CBTD3384DBQR	SSOP	DBQ	24	2500	367.0	367.0	38.0
SN74CBTD3384DBR	SSOP	DB	24	2000	367.0	367.0	38.0
SN74CBTD3384DGVR	TVSOP	DGV	24	2000	367.0	367.0	35.0
SN74CBTD3384DWR	SOIC	DW	24	2000	367.0	367.0	45.0
SN74CBTD3384PWR	TSSOP	PW	24	2000	367.0	367.0	38.0

JT (R-GDIP-T**)

CERAMIC DUAL-IN-LINE

24 LEADS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification.
 E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

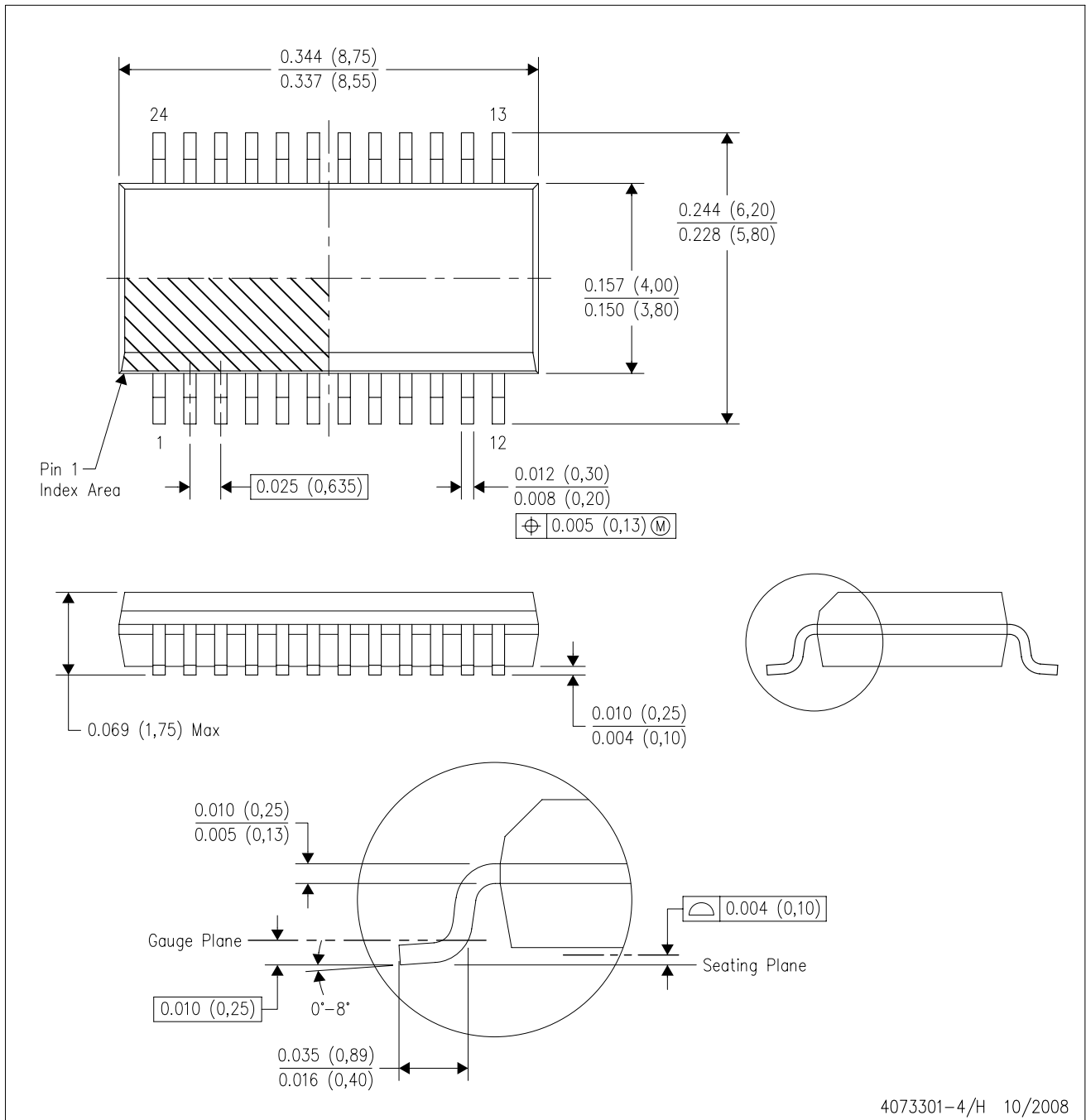


4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

DBQ (R-PDSO-G24)

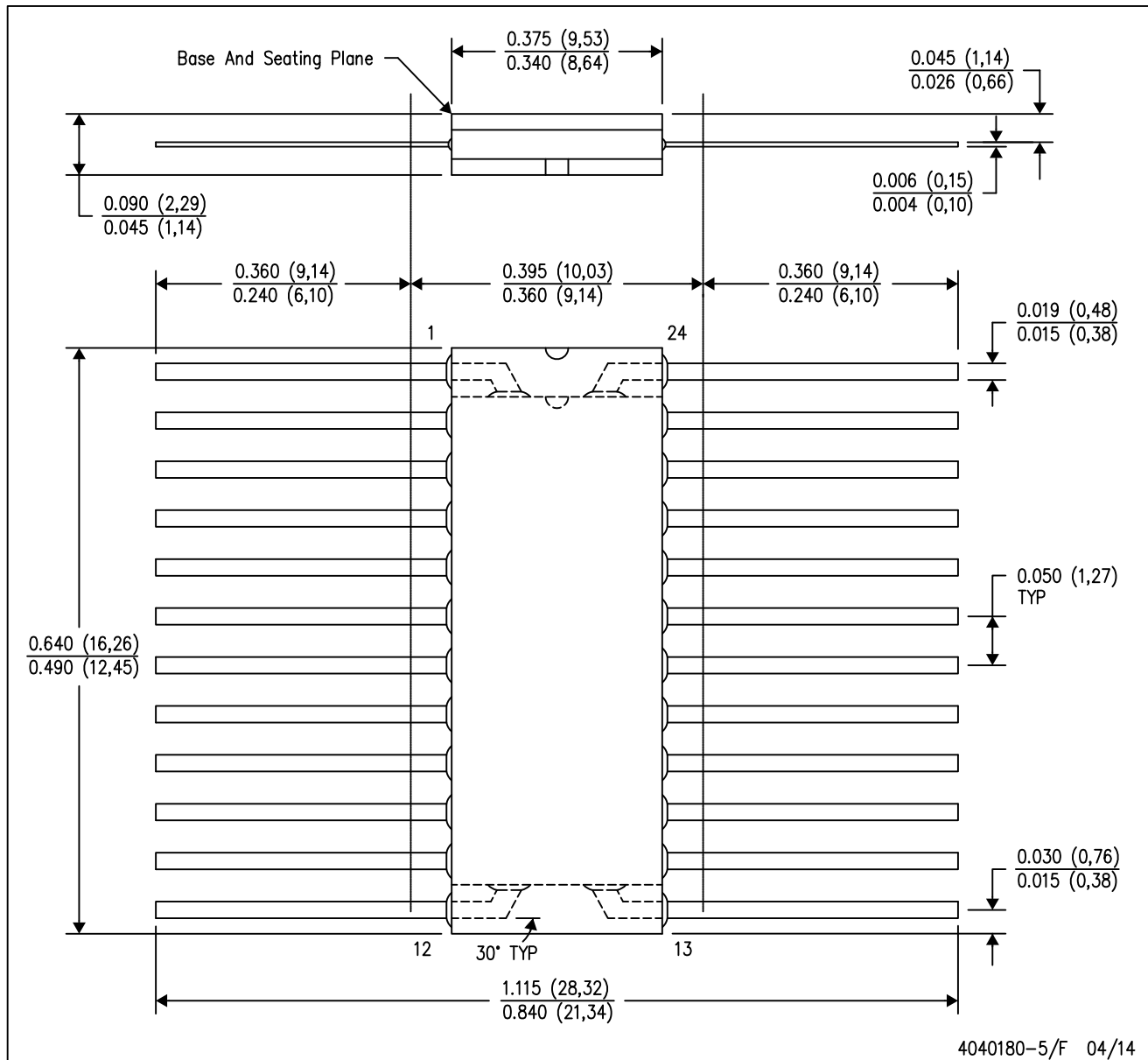
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
 - D. Falls within JEDEC MO-137 variation AE.

W (R-GDFP-F24)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within Mil-Std 1835 GDFP2-F20

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AD.

PW (R-PDSO-G24)

PLASTIC SMALL OUTLINE

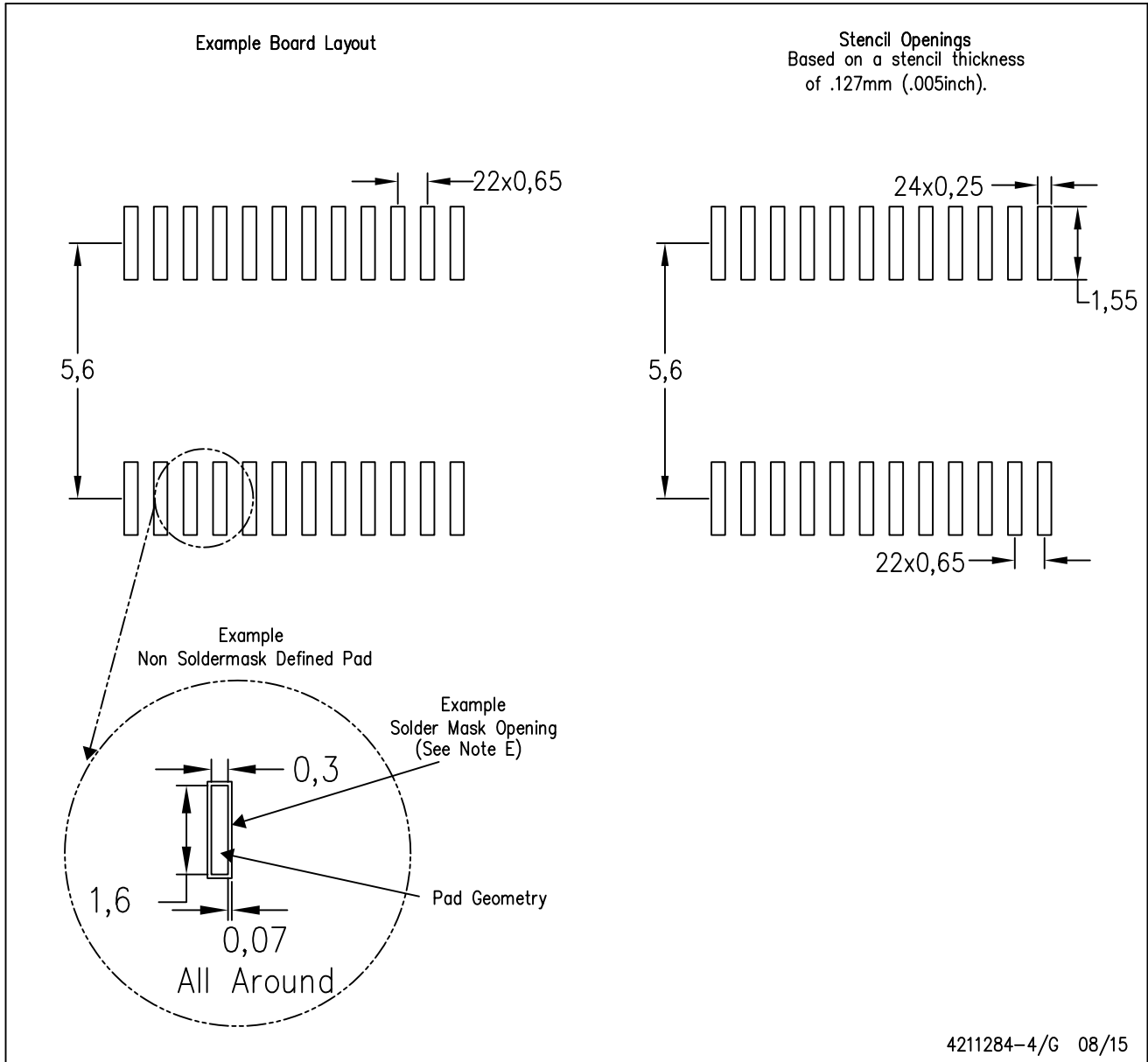


4040064-6/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G24)

PLASTIC SMALL OUTLINE

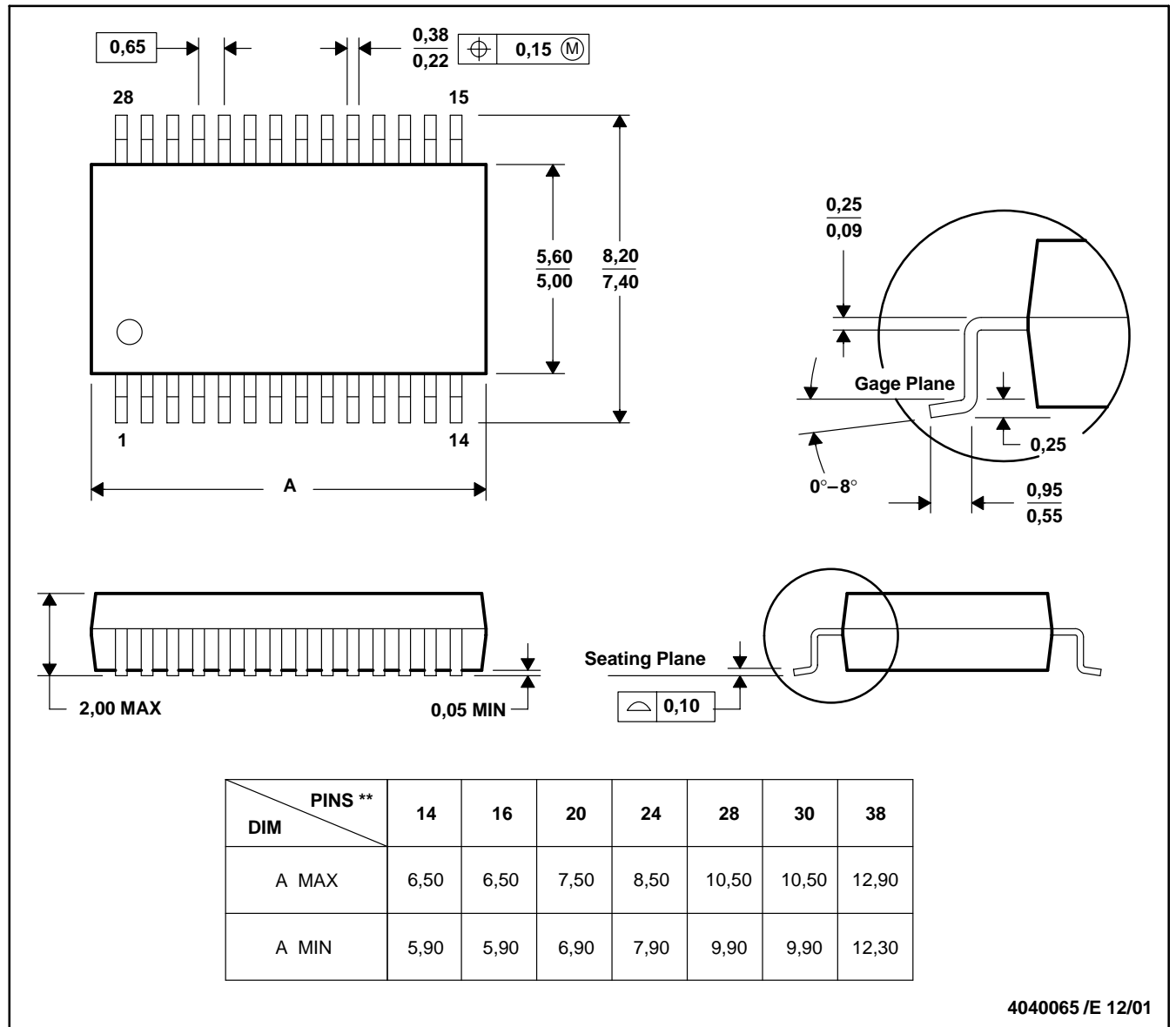


- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate design.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2018, Texas Instruments Incorporated