Rockwell

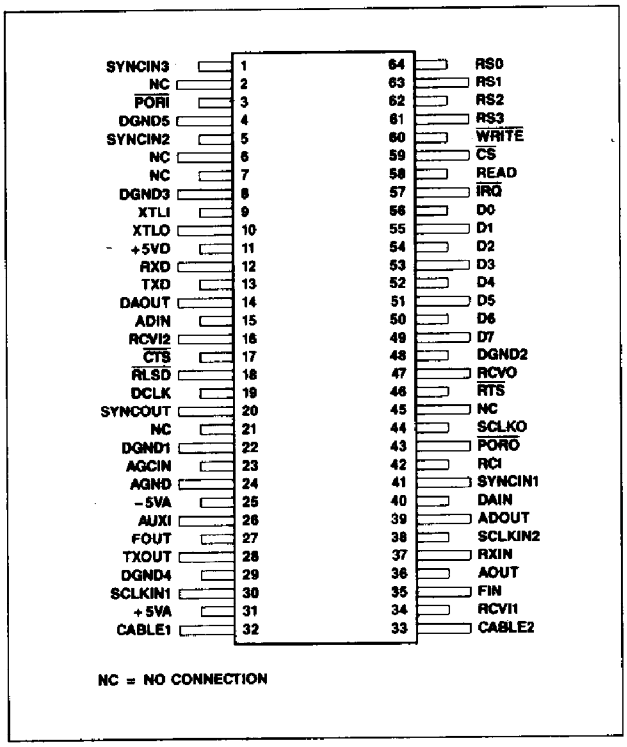
R24MFX 2400 bps MONOFAX™ Modem

INTRODUCTION

The R24MFX MONOFAX 24 is a synchronous, serial/parallel, 2400 bps modem in a single 64-pin quad in-line package (QUIP). The modem is designed for operation over the public switched telephone network with appropriate line terminations, such as a data access arrangement, provided externally.

The R24MFX satisfies the telecommunications requirements specified in CCITT Recommendation V.27 ter fallback (2400 bps), T.4 and the binary signaling capabilities of Recommendation T.30.

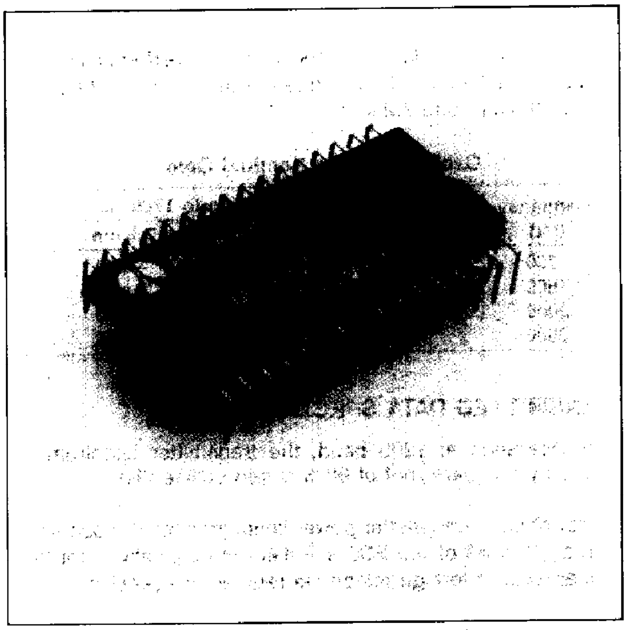
The R24MFX is optimized for use in compact Group 3 facsimile machines. Its small size and low power consumption offer the user flexibility in creating a 2400 bps modem customized for specific packaging and functional requirements.



R24MFX Pin Assignments

FEATURES

- Single 64-Pin QUIP
- CCITT V.27 ter Fallback, T.30, V.21 Channel 2, T.4
- Group 3 Facsimile Transmission/Reception
- Half-Duplex (2-Wire)
- Programmable Dual Tone Generation
- Programmable Tone Detection
- Dynamic Range: −43 dBm to 0 dBm
- Diagnostic Capability
  - — Provides Telephone Line Quality Monitoring Statistics
- Equalization
  - — Automatic Adaptive
  - — Compromise Cable (Selectable)
- DTE Interface: Two Alternate Ports
  - — Microprocessor Bus
  - — CCITT V.24 (RS-232-C Compatible)
- Low Power Consumption: 1W (Typical)
- Programmable Transmit Output Level
- TTL and CMOS Compatible



R24MFX 2400 bps MONOFAX Modem

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TECHNICAL CHARACTERISTICS

TONE GENERATION

Under control of the host processor, the R24MFX can generate single or dual frequency voice band tones up to 3600 Hz with a resolution of 0.11 Hz and an accuracy of 0.01%. The transmit level and frequency of each tone is independently programmable.

TONE DETECTION

Single frequency tones are detected by a programmable filter. The presence of energy at the selected frequency is indicated by a bit in the interface memory.

SIGNALING AND DATA RATES

Signaling/Date Rates

Configuration	Parameter	Specification (±0.01%)
V.27	Signaling Rate Data Rate	1200 Baud 2400 bps
V.21	Signaling Rate Data Rate	300 Baud 300 bps

DATA ENCODING

At 1200 baud, the 2400 bps data stream is encoded into dibits per CCITT V.27 ter.

At 300 baud, the data stream is 300 bps FSK per CCITT V.21 channel 2.

COMPROMISE CABLE EQUALIZERS

In addition to the adaptive equalizer, the R24MFX provides selectable compromise cable equalizers to optimize performance over three different lengths of non-loaded cable of 0.4 mm diameter (1.8 km, 3.6 km, and 7.2 km).

Cable Equalizer Nominal Gain

Frequency (Hz)	Gain (dB) Relative to 1700 Hz		
	1.8 km	3.6 km	7.2 km
700	−0.99	−2.39	−3.93
1500	−0.20	−0.65	−1.22
2000	+0.15	+0.87	+1.90
3000	+1.43	+3.06	+4.58

TRANSMITTED DATA SPECTRUM

When operating at 1200 baud, the transmitter spectrum is shaped by a square root of 90% raised cosine filer.

The out-of-band transmitter power limitations meet those specified by Part 68 of the FCC's Rules, and typically meet the requirements of foreign telephone regulatory agencies.

SCRAMBLER/DESCRAMBLER

The R24MFX incorporates a self-synchronizing scrambler/descrambler. This facility is in accordance with CCITT V,27 ter.

RECEIVE LEVEL

The receiver circuit of the R24MFX satisfies all specified performance requirements for received line signal levels from 0 dBm to −43 dBm. An external input buffer and filter must be supplied between the receiver analog input (RXA) and the R24MFX RXIN pin. The received line signal level is measured at RXA.

RECEIVE TIMING

In the receive state, the R24MFX provides a Data Clock (DCLK) output in the form of a square wave. The low to high transitions of this output coincide with the centers of received data bits. The timing recovery circuit is capable of tracking a ±0.01% frequency error in the associated transmit timing source. DCLK duty cycle is 50% ±1%.

TRANSMIT LEVEL

The transmitter output level is programmable. An external output buffer and filter must be supplied between the R24MFX TXOUT pin and the transmitter analog output (TXA). The default level at TXA is +5 dBm ±1 dB. When driving a 600 ohm load the TXA output requires a 600 ohm series resistor to provide −1 dBm ±1 dB to the load.

TRANSMIT TIMING

In the transmit state, the R24MFX provides a Data Clock (DCLK) output with the following characteristics:

1. *Frequency:* Selected data rate of 2400 or 300 Hz (±0.01%).
2. *Duty Cycle:* 50% ±1%.

Transmit Data (TXD) must be stable during the 1 microsecond periods immediately preceding and following the rising edge of DCLK.

TURN-ON SEQUENCE

Three turn-on sequences are generated by the R24MFX, as defined in the following table:

Turn-On Sequences

No.	Bit Rate.	$\overline{RTS}$-$\overline{CTS}$ Time (ms)	Comments
1	300 bps	<14	No Training Sequence
2	2400 bps[2]	943	No Echo Protector Tone
3	2400 bps[2]	1148	Preceded[1] By Echo Protector Tone

Notes:
1. Turn-on sequence 3 is used on lines with protection against talker echo.
2. V.27 ter long training sequence only.

TURN-OFF SEQUENCE

For V.27 ter, the turn-off sequence consists of approximately 10 ms of remaining data and scrambled ones at 1200 baud, followed by a 20 ms period of no transmitted energy. In V.21 the transmitter turns off within 7 ms after $\overline{RTS}$ goes false.

CLAMPING

The following clamps are provided with the R24MFX:

1. *Received Data (RXD).* RXD is clamped to a constant mark (1) whenever RLSD is off.
2. *Received Line Signal Detector (RLSD).* RLSD is clamped off (squelched) whenever RTS is on.

RESPONSE TIMES OF CLEAR-TO-SEND (CTS)

The time between the off-to-on transition of RTS and the off-to-on transition of CTS is dictated by the length of the training sequence. Response time is 943 ms for V.27 ter at 2400 bps. In V.21 CTS turns on in 14 ms or less.

The time between the on-to-off transition of RTS and the on-to-off transition of CTS in the data state is a maximum of 2 baud times for all configurations.

RECEIVED LINE SIGNAL DETECTOR (RLSD)

RLSD turns on at the end of the training sequence. If training is not detected at the receiver, the RLSD off-to-on response time is 674 ±10 ms. The RLSD on-to-off response time is 10 ±5 ms. Response times are measured with a signal at least 3 dB above the actual RLSD on threshold or at least 5 dB below the actual RLSD off threshold.

The RLSD on-to-off response time ensures that all valid data bits have appeared on RXD.

Receiver threshold is programmable over the range 0 dBm to −50 dBm, however, performance may be at a reduced level when the received signal is less than −43 dBm.

A minimum hysteresis action of 2 dB exists between the actual off-to-on and on-to-off transition levels. The threshold levels and hysteresis action are measured with an unmodulated 2100 Hz tone applied to RXA.

POWER

Voltage	Tolerance	Current (Max) @ 25°C	Current (Max) @ 60°C
+5 Vdc	±5%	250 mA @ 5.0 Vdc	225 mA @ 5.0 Vdc
-5 Vdc	±5%	25 mA @ -5.0 Vdc	25 mA @ -5.0 Vdc

Note: All voltages must have ripple ≤0.1 volts peak-to-peak. If a switching supply is chosen, user may select any frequency between 20 kHz and 150 kHz so long as no component of the switching frequency is present outside of the power supply with an amplitude greater than 500 microvolts peak.

ENVIRONMENTAL

Parameter	Specification
Temperature	
Operating	0°C to +60°C (32°F to 140°F)
Storage	−40°C to +80°C (−40°F to 176°F) (Stored in suitable antistatic container)
Relative Humidity	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less.

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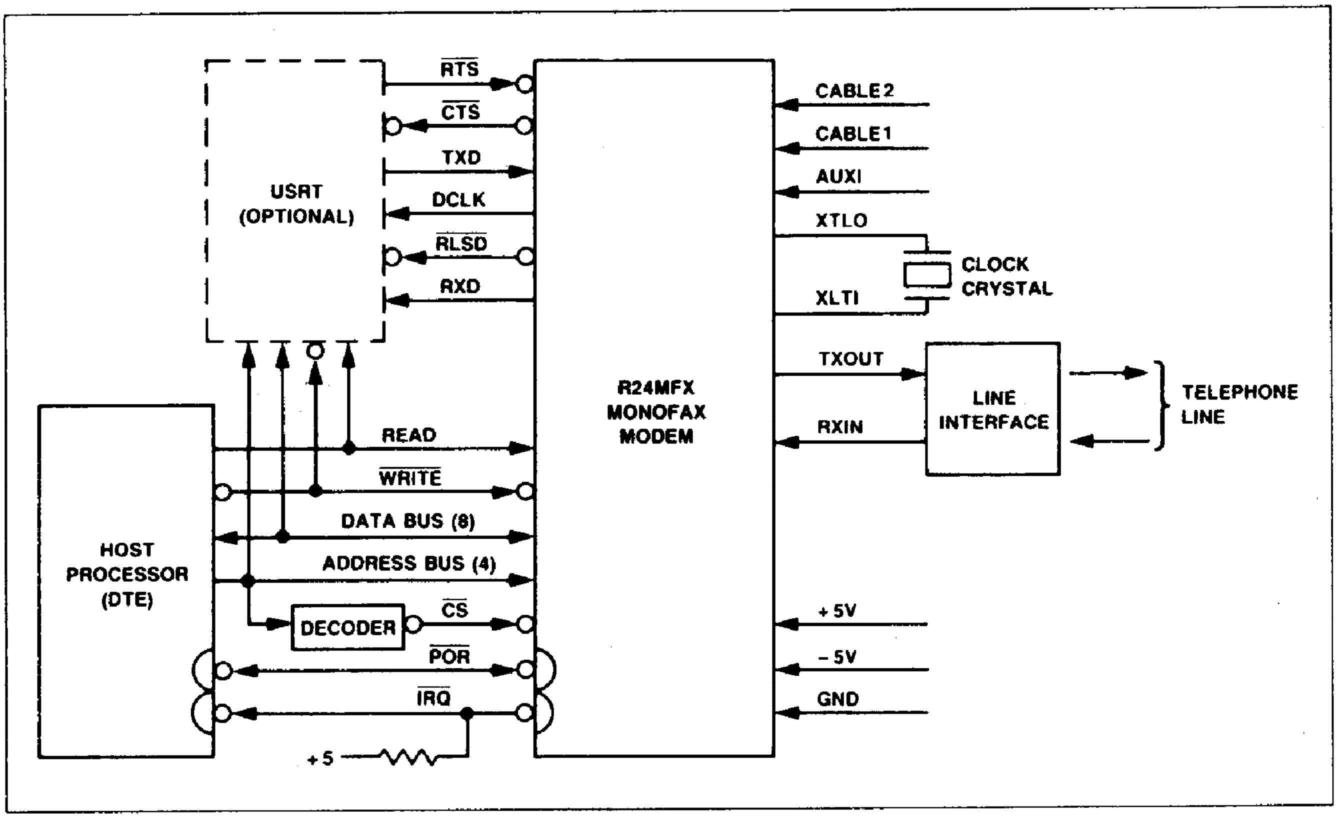


R24MFX Functional Interconnect Diagram

INTERFACE CHARACTERISTICS

The modem interface comprises both hardware and software circuits. Hardware circuits are assigned to specific pins on the 64-pin QUIP. Software circuits are assigned to specific bits in a 16-byte interface memory.

HARDWARE CIRCUITS

Signal names and descriptions of the hardware circuits, including the microprocessor interface, are listed in the R24MFX Hardware Circuits table; the table column titled 'Type' refers to designations found in the Digital and Analog Interface Characteristics tables.

Microprocessor Interface

Sixteen hardware circuits provide address (RS0-RS3), data (D0-D7), control ($\overline{CS}$, READ and $\overline{WRITE}$) and interrupt ($\overline{IRQ}$) signals for implementing a parallel interface compatible with an 8080 microprocessor. (Refer to the Microprocessor Interface Timing Waveforms figure and Microprocessor Interface Timing Requirements table.) With the addition of a few external logic gates, the interface can be made compatible with a wide variety of microprocessors such as 6500, 6800, or 68000.

The microprocessor interface allows a host microprocessor to change modem configuration, read or write channel data as well as diagnostic data, and supervise modem operation by means of software strappable control bits and modem status bits. The significance of the control and status bits and methods of data interchange are discussed in the Software Circuits section.

V.24 Interface

Seven hardware circuits provide timing, data and control signals for implementing a serial interface compatible with CCITT Recommendation V.24. These signals interface directly with circuits using TTL logic levels (0, +5 volt). These TTL levels are suitable for driving the short wire lengths or printed circuitry normally found within stand-alone modem enclosures or equipment cabinets.

In applications where the modem is operated in parallel data mode only (i.e., where the V.24 signals are unused), all V.24 pins may remain unterminated.

R24MFX Hardware Circuits

Name	Type	Pin No.	Description
A. POWER:			
AGND	GND	24	Connect to Analog Ground
DGND1	GND	22	Connect to AGND Ground
DGND2	GND	48	Connect to Digital Ground
DGND3	GND	8	Connect to Digital Ground
DGND4	GND	29	Connect to Digital Ground
DGND5	GND	4	Connect to Digital Ground
+5 VA	PWR	31	Connect to Analog +5V Power
+5 VD	PWR	11	Connect to Digital +5V Power
−5 VA	PWR	25	Connect to Analog −5V Power
B. MICROPROCESSOR INTERFACE:			
D7	I/OA	49	Data Bus (8 Bits)
D6	I/OA	50	
D5	I/OA	51	
D4	I/OA	52	
D3	I/OA	53	
D2	I/OA	54	
D1	I/OA	55	
D0	I/OA	56	
RS3	IA	61	Register Select (4 Bits) Select Reg. 0 – F
RS2	IA	62	
RS1	IA	63	
RS0	IA	64	
$\overline{CS}$	IA	59	Chip Select
READ	IA	58	Read Strobe
$\overline{WRITE}$	IA	60	Write Strobe
$\overline{IRQ}$	OB	57	Interrupt Request
C. V.24 INTERFACE:			
DCLK	OC	19	Data Clock
$\overline{RTS}$	IB	46	Request-to-Send
$\overline{CTS}$	OC	17	Clear-to-Send
TXD	IB	13	Transmitter Data Signal
RXD	OC	12	Receiver Data Signal
$\overline{RLSD}$	OC	18	Received Line Signal Detector
D. CABLE EQUALIZER:			
CABLE1	IC	32	Cable Select 1
CABLE2	IC	33	Cable Select 2

Name	Type	Pin No.	Description
E. ANALOG SIGNALS:			
TXOUT	AA	28	Connect to Output Op Amp
RXIN	AB	37	Connect to Input Op Amp
AUXI	AC	26	Auxiliary Analog Input
F. OVERHEAD			
$\overline{PORO}$	I/OB	43	Power-On-Reset Output
$\overline{PORI}$	I/OB	3	Power-On-Reset Input
XTLO	R*	10	Connect to Crystal Circuit
XTLI	R*	9	Connect to Crystal Circuit
RCVO	R*	47	Receive Mode Output
RCVI1	R*	34	Connect to RCVO
RCVI2	R*	16	Connect to RCVO
SCLKO	R*	44	Switched Capacitor Clock Output
SCLKIN1	R*	30	Connect to SCLKO
SCLKIN2	R*	38	Connect to SCLKO
AOUT	R*	36	Smoothing Filter Output
AGCIN	R*	23	AGC Input
DAOUT	R*	14	DAC/AGC Data Out
DAIN	R*	40	Connect to DAOUT
ADOUT	R*	39	ADC Output
ADIN	R*	15	Connect to ADOUT
FOUT	R*	27	Smoothing Filter Output
FIN	R*	35	Connect to FOUT
SYNCOUT	R*	20	Sample Clock Output
SYNCIN1	R*	41	Connect to SYNCOUT
SYNCIN2	R*	5	Connect to SYNCOUT
SYNCIN3	R*	1	Connect to SYNCOUT
RCI	R*	42	RC Junction for POR Time Constant
G. RESERVED			
	R*	2	Do Not Connect
	R*	6	Do Not Connect
	R*	7	Do Not Connect
	R*	21	Do Not Connect
	R*	45	Do Not Connect

***R = Required overhead connection; no connection to host equipment.**

Unused inputs tied to +5V or ground require individual 10K Ω series resistors.

Digital Interface Characteristics

Symbol	Parameter	Units	Type: Input IA	Input IB	Input IC	Output OA	Output OB	Output OC	Input/Output I/OA	Input/Output I/OB
V_{IH}	Input Voltage, High	V	2.0 min.	2.0 min.	2.0 min				2.0 min.	5.25 max. 2.0 min.
V_{IL}	Input Voltage, Low	V	0.8 max.	0.8 max.	0.8 max.				0.8 max.	0.8 max.
V_{OH}	Output Voltage, High	V				2.4 min.[1]			2.4 min.[1]	2.4 min.[3]
V_{OL}	Output Voltage, Low	V				0.4 max.[2]	0.4 max.[2]	0.4 max.[2]	0.4 max.[2]	0.4 max.[5]
I_{IN}	Input Current, Leakage	µA	±2.5 max.						±12.5 max.[4]	
I_{OH}	Output Current, High	mA				−0.1 max.				
I_{OL}	Output Current, Low	mA				1.6 max.	1.6 max.	1.6 max.		
I_L	Output Current, Leakage	µA					±10 max.			
I_{PU}	Pull-up Current (Short Circuit)	µA		−240 max. −10 min.	−240 max. −10 min.			−240 max. −10 min.		−260 max. −100 min.
C_L	Capacitive Load	pF	5	5	20				10	40
C_D	Capacitive Drive	pF				100	100	100	100	100
	Circuit Type		TTL	TTL w/Pull-up	TTL w/Pull-up	TTL	Open-Drain	Open Drain w/Pull-up	3 State Transceiver	Open-Drain w/Pull-up

Notes
1. I load = −100 µA
2. I load = 1.6 mA
3. I load = −40 µA
4. V_{IN} = 0.4 to 2.4 Vdc, V_{CC} = 5.25 Vdc
5. I load = 0.36 mA

Analog Interface Characteristics

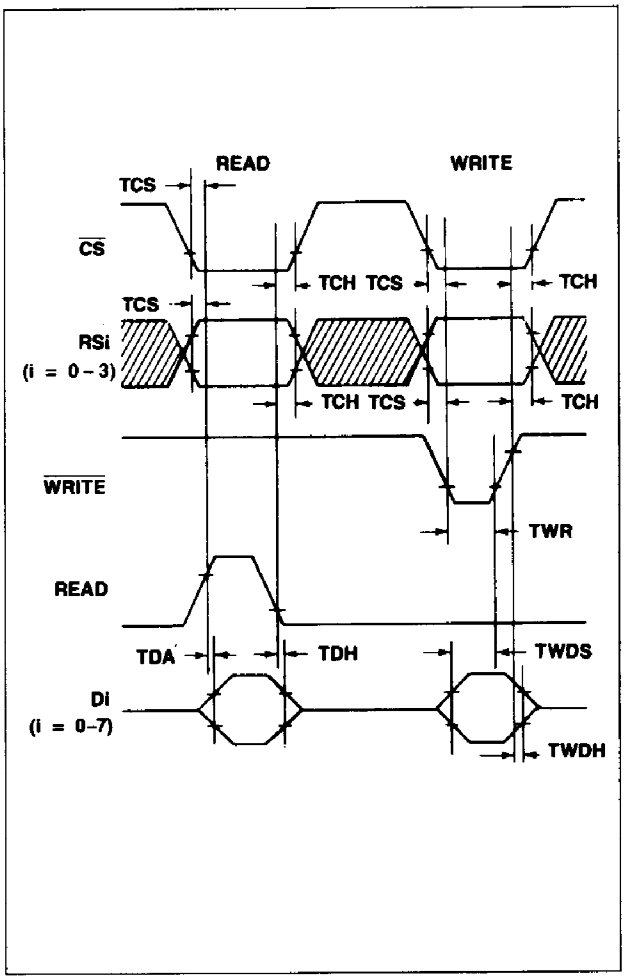
Analog Interface Characteristics

Name	Type	Characteristics
TXOUT	AA	The transmitter output can supply a maximum of ±3.03 volts into a load resistance of 10k Ω minimum. In order to match to 600 Ω, an external smoothing filter with a transfer function of 15726.43/(S + 11542.44) and 604 Ω series resistor are required.
RXIN	AB	The receiver input impedance is greater than 1M Ω. An external antialiasing filter with a transfer function of 19533.88/(S + 11542.44) is required.
AUXI	AC	The auxiliary analog input allows access to the transmitter for the purpose of interfacing with user provided equipment. Because this is a sampled data input, any signal above 3600 Hz will cause aliasing errors. The input impedance is 1M Ω, and the gain to transmitter output (TXA) is +5.6 dB ±1 dB.

Note: Absolute maximum voltage ratings for analog inputs are: $(-5\ VA - 0.3) \le V_{IN} \le (+5\ VA + 0.3)$

Microprocessor Interface Timing Requirements

Characteristic	Symbol	Min	Max	Units
$\overline{CS}$, RSi setup time prior to READ or $\overline{WRITE}$	TCS	30	—	ns
Data Access time after READ	TDA	—	140	ns
Data hold time after READ	TDH	10	50	ns
$\overline{CS}$, RSi hold time after READ or $\overline{WRITE}$	TCH	10	—	ns
Write data setup time	TWDS	75	—	ns
Write data hold time	TWDH	10	—	ns
$\overline{WRITE}$ strobe pulse width	TWR	75	—	ns



Microprocessor Interface Timing Waveforms

Cable Equalizers

Modems may be connected by direct wiring, such as leased telephone cable or through the public switched telephone network, by means of a data access arrangement. In either case, the modem analog signal is carried by copper wire cabling for at least some part of its route. The cable characteristics shape the passband response so that the lower frequencies of the passband (300 Hz to 1700 Hz) are attenuated less than the higher frequencies (1700 Hz to 3300 Hz). The longer the cable the more pronounced the effect.

To minimize the impact of this undesired passband shaping, a compromise equalizer with more attenuation at lower frequencies than at higher frequencies can be placed in series with the analog signal. The modem includes three such equalizers designed to compensate for cable distortion.

Cable Equalizer Selection

CABLE1	CABLE2	Length of 0.4mm Diameter Cable
0	0	0.0
0	1	1.8 km
1	0	3.6 km
1	1	7.2 km

Analog Signals

Three analog signals provide the interface point for telephone company audio circuits and host audio inputs. Signals TXOUT and RXIN require buffering and filtering to be suitable for driving and receiving the communication channel. Signal AUXI provides access to the transmitter for summing host audio signals with the modem analog output.

The filters required for anti-aliasing on the receiver input and smoothing on the transmitter output have a single pole located at 11,542 radians. Although this pole is located within the modem passband, internal filters compensate for its presence and, therefore, the pole location must not be changed. Some variation from recommended resistor and capacitor values is permitted as long as the pole is not moved, overall gain is preserved, and the device is not required to drive a load of less than 10k Ω.

Notice that when reference is made to signals TXA, RXA, and AUXIN, these signals are not electrically identical to TXOUT, RXIN, and AUXI. The schematic of the recommended modem interface circuit illustrates the differences.

Overhead

Except for the power-on-reset signal $\overline{\text{PORO}}$, the overhead signals are intended for internal use only. The various required connections are illustrated in the recommended modem interface circuit schematic. No host connections should be made to overhead signals other than $\overline{\text{PORO}}$.

SOFTWARE CIRCUITS

The R24MFX contains 16 memory mapped registers to which an external (host) microprocessor has access. The host may read data out of or write data into these registers. Refer to the R24MFX Host Processor Interface figure.

When information in these registers is being discussed, the format Z:Q is used. The register is specified by Z(0-F), and the bit by Q(0-7, 0 = LSB). A bit is considered to be "on" when set to a one (1) and "off" when reset to a zero (0).

Status/Control Bits

The operation of the R24MFX is affected by a number of software control inputs. These inputs are written into registers within the interface memory via the host microprocessor bus. Modem operation is monitored by various software flags that are read from interface memory via the host microprocessor bus.

All status and control bits are defined in the R24MFX Interface Memory Map table. Bits designated by ' — ' are reserved for modem use only and must not be changed by the host.

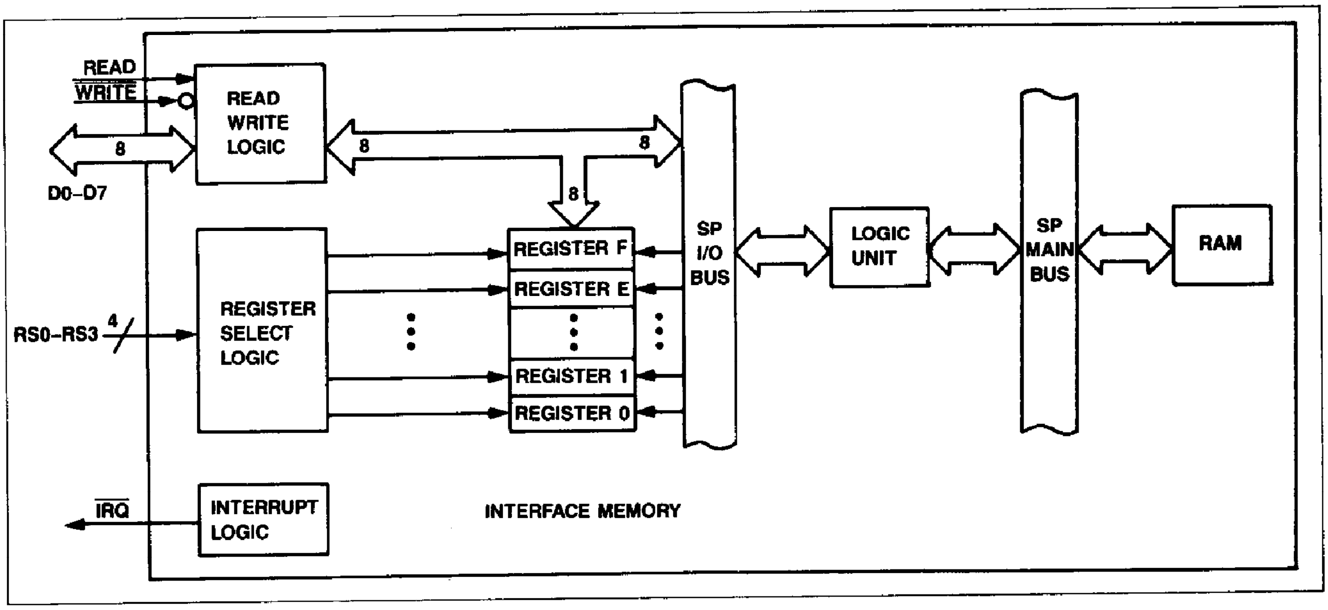
Any one of the registers may be read or written on any host read or write cycle, but all eight bits of that register are affected. In order to read a single bit or a group of bits in a register, the host processor must mask out unwanted data. When writing a single bit or group of bits in a register the host processor must perform a read-modify-write operation. That is, the entire register is read, the necessary bits are set or reset in the accumulator of the host, then the original unmodified bits and the modified bits are written back into the register of the interface memory.

Configuration Control

Three configurations are available in the R24MFX modem: V.27, V.21, and Tone. These three configurations are selected by writing an 8-bit binary code into the configuration field (CONF) of the interface memory. The configuration field consists of bits 7 through 0 of register D. The code for these bits is: 0 = V.21, 4 = V.27, and 8 = Tone. All other codes represent invalid states.

When the modem is initialized by power-on-reset, the configuration defaults to V.27. When the host wants to change configuration, the new code is written to the configuration field and the SETUP bit (E:3) is set to a one. Once the new configuration takes effect, the SETUP bit is reset to zero by the modem.

The information in the interface memory is serviced by the modem at either 1200 times per second or 7200 times per second depending on configuration. In V.21, the rate is 7200 times per second. In both V.27 and Tone configuration, the rate is 1200 times per second.



R24MFX Host Processor Interface

R24MFX Interface Memory Map

Register \ Bit	7	6	5	4	3	2	1	0
F	RAMA							
E	IA	CDIE	CDREQ	—	SETUP	DDIE	—	DDREQ
D	CONF							
C	RTSP	EPT	TPDM	TDIS	EQSV	EQFZ	—	RAMW
B	RX	FED		GHIT	—	—	—	—
A	TDET	—	—	—	—	—	—	—
9	—	—	—	—	—	—	—	—
8	—	—	CDET	—	PN	—	—	—
7	—	—	—	—	—	—	—	—
6	—	—	—	—	—	—	—	—
5	RXCD							
4	TXCD							
3	DDXM							
2	DDXL							
1	DDYM							
0	DDYL							
Register / Bit	7	6	5	4	3	2	1	0

Channel Data Transfer

Data sent to or received from the data channel may be transferred between the modem and host processor in either serial or parallel form. The receiver operates in both serial and parallel mode simultaneously and requires no mode control bit selection. The transmitter operates in either serial or parallel mode as selected by mode control bit C:5 (TPDM).

To enable the transmitter parallel mode, TPDM must be set to a 1. The modem automatically defaults to the serial mode (TPDM = 0) at power-on. In either transmitter serial or parallel mode, the R24MFX is configured by the host processor via the microprocessor bus.

Serial Mode—The serial mode uses a standard V.24 (RS-232-C) hardware interface (optional USRT) to transfer channel data. Transmitter data can be sent serially only when TPDM is set to a zero.

Parallel Mode—Parallel data is transferred via two registers in the interface memory. Register 5 (RXCD) is used for receiver channel data, and Register 4 (TXCD) is used for transmitter channel data. Register 5 is continuously written every eight bit times when in the receive state. Register 4 is used as the source of channel transmitter data only when bit C:5 (TPDM) is set to a one by the host. Otherwise the transmitter reads data from the V.24 interface. Both $\overline{RTS}$ and RTSP remain enabled, however, regardless of the state of TPDM.

When performing parallel data transfer of channel data, the host and modem can synchronize their operations by handshaking bits in register E. Bit E:5 (CDREQ) is the channel data request bit. This bit is set to a one by the modem when receiver data is available in RXCD or when transmitter data is required in TXCD. Once the host has finished reading RXCD or writing TXCD, the host processor must reset CDREQ by writing a zero to that bit location.

When set to a one by the host, Bit E:6 (CDIE) enables the CDREQ bit to cause an $\overline{IRQ}$ interrupt when set. While the $\overline{IRQ}$ line is driven to a TTL low level by the modem, bit E:7 (IA) is a one.

If the host does not respond to the channel data request within eight bit times, the RXCD register is over written or the TXCD register is sent again.

Refer to Channel Data Parallel Mode Control flow chart for recommended software sequence.

R24MFX Interface Memory Definitions

Mnemonic	Name	Memory Location	Description
CDET	Carrier Detector	8:5	The one state of CDET indicates passband energy is being detected, and a training sequence is not present. CDET goes to one at the start of the data state, and returns to zero at the end of the received signal. CDET activates one baud time before $\overline{RLSD}$ and deactivates one baud time after $\overline{RLSD}$.
CDIE	Channel Data Interrupt Enable	E:6	When set to a one, CDIE enables an $\overline{IRQ}$ interrupt to be generated when the channel data request bit (CDREQ) is a one.
CDREQ	Channel Data Request	E:5	Parallel data mode handshaking bit. Set to a one when the modem receiver writes data to RXCD, or the modem transmitter reads data from TXCD. CDREQ must be reset to zero by the host processor when data service is complete.
CONF	Configuration	D:0-7	The 8-bit field CONF controls the configuration of the modem according to the following table: **Hex Code** — **Configuration** 0 — V.21 4 — V.27 8 — Tone All else — Invalid **Configuration Definitions** *V.21*—The modem operates as a CCITT T.30 compatible 300 bps FSK modem having characteristics of the CCITT V.21 Channel 2 modulation system. *Tone*—The modem sends single or dual frequency tones in response to the $\overline{RTS}$ or RTSP signals. Tone frequencies and amplitudes are controlled by RAM locations written by the host. When not transmitting tones the Tone configuration allows detection of single frequency tones by the TDET bit. The tone detector frequency can be changed by the host by altering the contents of several RAM locations. *V.27*—The modem operates as specified in CCITT Recommendation V.27 for a 2400 bps data rate.
DDIE	Diagnostic Data Interrupt Enable	E:2	When set to a one, DDIE enables an IRQ interrupt to be generated when the diagnostic data request bit (DDREQ) is a one.
DDREQ	Diagnostic Data Request	E:0	DDREQ goes to a one when the modem reads from or writes to DDYL. DDREQ goes to a zero when the host processor reads from or writes to DDYL. Used for diagnostic data handshaking bit.
DDXL	Diagnostic Data X Least	2:0-7	Least significant byte of 16-bit word used in reading XRAM locations.
DDXM	Diagnostic Data X Most	3:0-7	Least significant byte of 16-bit word used in reading XRAM locations.
DDYL	Diagnostic Data Y Least	0:0-7	Least significant byte of 16-bit word used in reading YRAM locations or writing XRAM and YRAM locations.
DDYM	Diagnostic Data Y Most	1:0-7	Most significant byte of 16-bit word used in reading YRAM locations or writing XRAM and YRAM locations.
EPT	Echo Protector Tone	C:6	When EPT is a one, an unmodulated carrier is transmitted for 185 ms followed by 20 ms of no transmitted energy at the beginning of the training sequence.
EQFZ	Equalizer Freeze	C:2	When EQFZ is a one, the adaptive equalizer taps stop updating and remain frozen.
EQSV	Equalizer Save	C:3	When EQSV is a one, the adaptive equalizer taps are not zeroed when reconfiguring the modem or when entering the training state.
FED	Fast Energy Detector	B:5,6	FED consists of a 2-bit field that indicates the level of received signal according to the following code. **Code** — **Energy Level** 0 — None 1 — Invalid 2 — Above Turn-off Threshold 3 — Above Turn-on Threshold While receiving a signal, FED normally alternates between Codes 2 and 3.

R24MFX Interace Memory Definitions (continued)

Mnemonic	Name	Memory Location	Description
GHIT	Gain Hit	B:4	The gain hit bit goes to one when the receiver detects a sudden increase in passband energy faster than the AGC circuit can correct. GHIT returns to zero when the AGC output returns to normal.
IA	Interrupt Active	E:7	IA is a one when the modem is driving the interrupt request line ($\overline{IRQ}$) to a low TTL level.
PN	Period N	8:3	PN sets to a one at the start of the received PN sequence. PN resets to zero at the start of the receiver data state. PN does not operate when EQFZ (C:2), EQSV (C:3) or TDIS (C:4) is set to one.
RAMA	RAM Access	F:0-7	The RAMA register is written by the host when reading or writing diagnostic data. The RAMA code determines the RAM location with which the diagnostic read or write is performed.
RAMW	RAM Write	C:0	RAMW is set to a one by the host processor when performing diagnostic writes to the modem RAM. RAMW is set to a zero by the host when reading RAM diagnostic data.
RTSP	Request to Send Parallel	C:7	The one state of RTSP begins a transmit sequence. The modem continues to transmit until RTSP is turned off and the turn-off sequence has been completed. RTSP parallels the operation of the hardware $\overline{RTS}$ control input. These inputs are ORed by the modem.
RXCD	Receiver Channel Data	5:0-7	RXCD is written to by the modem every eight bit times. This byte of channel data can be read by the host when the receiver sets the channel data request bit (CDREQ).
RX	Receive State	B:7	RX is a one when the modem is in the receive state (i.e., not transmitting).
SETUP	Setup	E:3	The host processor must set the SETUP bit to a one when reconfiguring the modem, i.e., when changing CONF (D:0-7).
TDET	Tone Detected	A:7	The one state of TDET indicates reception of a tone. The filter can be retuned by means of the diagnostic write routine.
TDIS	Training Disable	C:4	If TDIS is a one in the receive state, the modem is prevented from entering the training phase. If TDIS is a one when $\overline{RTS}$ or RTSP go active, the generation of a training sequence is prevented at the start of transmission.
TPDM	Transmitter Parallel Data Mode	C:5	When control bit TPDM is a one, the transmitter accepts data for transmission from the TXCD register rather than the serial hardware data input.
TXCD	Transmitter Channel Data	4:0-7	The host processor conveys output data to the transmitter in parallel data mode by writing a data byte to the TXCD register when the channel data request bit (CDREQ) goes to a one. Data is transmitted as single bits in V.21 or as dibits in V.27 starting with bit 0 or dibit 0,1.

3

Diagnostic Data Transfer

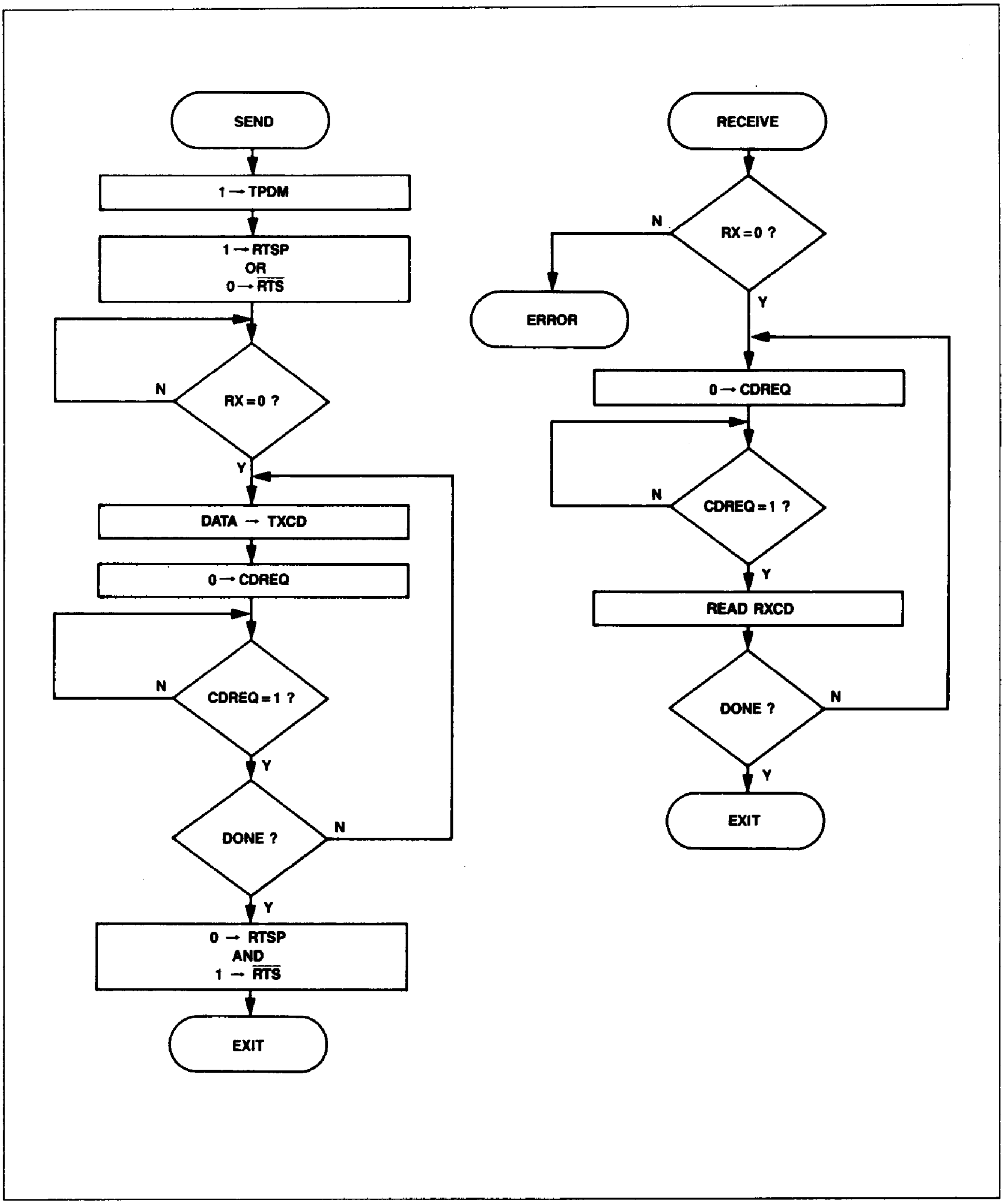
The modem contains 128 words of random access memory (RAM). Each word is 32-bits wide. Because the modem is optimized for performing complex arithmetic, the RAM words are frequently used for storing complex numbers. Therefore, each word is organized into a real part (16 bits) and an imaginary part (16-bits) that can be accessed independently. The portion of the word that normally holds the real value is referred to as XRAM. The portion that normally holds the imaginary value is referred to as YRAM. The entire contents of XRAM and YRAM may be read by the host processor via the microprocessor interface.

The interface memory acts as an intermediary during these host to signal processor RAM data exchanges. The RAM address to be read from or written to is determined by the contents of register F (RAMA). The R24MFX RAM Access Codes table lists 27 access codes for storage in register F and the corresponding diagnostic functions. The R24MFX Diagnostic Data Scaling table provides scaling information for these diagnostic functions. Each RAM word transferred to the interface memory is 32 bits long.

These bits are written into interface memory registers 3, 2, 1 and 0 in that order. Registers 3 and 2 contain the most and least significant bytes of XRAM data, respectively, while registers 1 and 0 contain the most and least significant bytes of YRAM data respectively.

When set to a one, bit C:0 (RAMW) causes the modem to suspend transfer of RAM data to the interface memory, and instead, to transfer data from interface memory to RAM. When writing into the RAM, only 16 bits are transferred, not 32 bits as for a read operation. The 16 bits written in XRAM or YRAM come from registers 1 and 0, with register 1 being the more significant byte. Selection of XRAM or YRAM for the destination is by means of the code stored in the RAMA bits of register F. When bit F:7 is set to one, the XRAM is selected. When F:7 equals zero, YRAM is selected.

When the host processor reads or writes register 0, the diagnostic data request bit E:0 (DDREQ) is reset to zero. When the modem reads or writes register 0, DDREQ is set to a one. When set to a one by the host, bit E:2 (DDIE) enables the DDREQ bit to cause an $\overline{IRQ}$ interrupt when set. While the $\overline{IRQ}$ line is driven to a TTL low level by the modem, bit E:7 (IA) goes to a one.



Channel Data Parallel Mode Control

R24MFX RAM Access Codes

Node	Function	RAMA	Reg. No.
1	AGC Gain Word	B1	2,3
2	Average Power	F2	2,3
3	Receiver Sensitivity	F1	2,3
4	Receiver Hysteresis	84	2,3
5	Equalizer Input	5B	0,1,2,3
6	Equalizer Tap Coefficients	1B-2A	0,1,2,3
7	Unrotated Equalizer Output	6B	0,1,2,3
8	Rotated Equalizer Output	0A	0,1,2,3
9	Decision Points	6C	0,1,2,3
10	Error Vector	6D	0,1,2,3
11	Rotation Angle	87	2,3
12	Frequency Correction	8B	2,3
13	EQM	B0	2,3
14	Alpha (α)	36	0,1
15	Beta One (β_1)	37	0,1
16	Beta Two (β_2)	38	0,1
17	Alpha Prime (α')	39	0,1
18	Beta One Prime (β_1')	3A	0,1
19	Beta Two Prime (β_2')	3B	0,1
20	Alpha Double Prime (α'')	B6	2,3
21	Beta Double Prime (β'')	B7	2,3
22	Output Level	43	0,1
23	Tone 1 Frequency	8E	2,3
24	Tone 1 Level	44	0,1
25	Tone 2 Frequency	8F	2,3
26	Tone 2 Level	45	0,1
27	Checksum	02	0,1

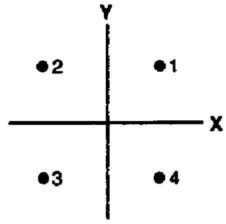
R24MFX Diagnostic Data Scaling

Node	Parameter/Scaling
1	**AGC Gain Word** (16-bit unsigned). AGC Gain in dB = 50 − [(AGC Gain Word/64) x 0.098] Range: $(16C0)_{16}$ to $(7FFF)_{16}$. For −43 dBm Threshold
2.	**Average Power** (16-bit unsigned) Post-AGC Average Power in dBm = 10 Log (Average Power Word/2185) Typical Value = $(0889)_{16}$, corresponding to 0 dBm Pre-AGC Power in dBm = (Post-AGC Average Power–AGC Gain)
3	**Receiver Sensitivity** (16-bit twos complement) On-Number = 655.36 (52.38 + P_{ON}) where: P_{ON} = Turn-on threshold in dB Convert On-Number to hexadecimal and store at access code F1
4	**Receiver Hysteresis** (16-bit twos complement) Off-Number = $[65.4 (10^A)]^2/2$ where: A = (P_{OFF} − P_{ON} − 0.5)/20 P_{ON} = Turn-on threshold in dB P_{OFF} = Turn-off threshold in dB Convert Off-Number to hexadecimal and store at access code 84.

R24MFX Diagnostic Data Scaling

Node	Parameter/Scaling
5,7–9	**All base-band signal point nodes** (i.e., Equalizer Input, Unrotated Equalizer Output, Rotated Equalizer Output, and Decision Points) are 32-bit, complex, twos complement numbers.

Point	X	Y
1	1600	1600
2	EA00	1600
3	EA00	EA00
4	1600	EA00



Node	Parameter/Scaling
6	**Equalizer Tap Coefficients** (32-bit, complex, twos complement) Complex numbers with X = real part, Y = imaginary part X and Y range: 0000 to $(FFFF)_{16}$ representing ± full scale in hexadecimal twos complement.
10	**Error Vector** (32-bit, complex, twos complement) Complex number with X = real part, Y = imaginary part. X and Y range: $(8000)_{16}$ to $(7FFF)_{16}$
11	**Rotation Angle** (16-bit, signed, twos complement) Rotation Angle in deg. = (Rot. Angle Word/65,536) x 360
12	**Frequency Correction** (16-bit signed twos complement) Frequency correction in Hz = (Freq. Correction Word/65,536) x Baud Rate Range: $(FC00)_{16}$ to $(400)_{16}$ representing ± 18.75 Hz
13	**EQM** (16-bit, unsigned) Filtered squared magnitude of error vector. Proportionality to BER determined by particular application.
14–21	**Filter Tuning Parameters** (16-bit unsigned) Alpha, Beta One, Beta Two, Alpha Prime, Beta One Prime, Beta Two Prime, Alpha Double Prime, and Beta Double Prime are set according to instructions in application note 668. Use a sample rate of 7200 samples per second for all calculations.
22	**Output Level** (16-bit unsigned) Output Number = 27573.6 $[10^{(Po/20)}]$ Po = output power in dBm with series 600 ohm resistor into 600 ohm load. Convert Output Number to hexadecimal and store at access code 43
24 and 26	**Tone 1 and Tone 2 Levels** Calculate the power of each tone independently by using the equation for Output Number given at node 22. Convert these numbers to hexadecimal then store at access codes 44 and 45. Total power transmitted in tone mode is the result of both tone 1 power and tone 2 power.
23 and 25	**Tone 1 and 2 Frequency** (16-bit unsigned) N = 9.1022 (Frequency in Hz) Convert N to hexadecimal then store at access code 8E or 8F.
27	**Checksum** (16-bit unsigned) ROM checksum number determined by revision level.

3

POWER-ON INITIALIZATION

When power is applied to the R24MFX, a period of 50 to 350 ms is required for power supply settling. The power-on-reset signal ($\overline{POR}$) remains low during this period. Approximately 10 ms after the low to high transition of $\overline{POR}$, the modem is ready to be configured, and $\overline{RTS}$ may be activated. If the 5 Vdc power supply drops below approximately 3 Vdc for more than 30 msec, the $\overline{POR}$ cycle is repeated.

At $\overline{POR}$ time the modem defaults to the following configuration: V.27/2400 bps, serial mode, training enabled, echo protector tone enabled, interrupts disabled, RAM access code 0A, transmitter output level set for +5 dBm at TXA, receiver turn-on threshold set for -43.5 dBm, receiver turn-off threshold set for -47.0 dBm, tone 1 and tone 2 set for 0 Hz and 0 volts output, and tone detector parameters zeroed.

$\overline{POR}$ can be connected to a user supplied power-on-reset signal in a wire-or configuration. A low active pulse of 3 μsec or longer applied to the $\overline{POR}$ pin causes the modem to reset. The modem is ready to be configured 10 msec after the low active pulse is removed from $\overline{POR}$.

PERFORMANCE

Whether functioning as a V.27 ter or V.21 type modem, the R24MFX provides the user with unexcelled high performance.

TYPICAL BIT ERROR RATES

The Bit Error Rate (BER) performance of the modem is specified for a test configuration conforming to that illustrated in CCITT Recommendation V.56. Bit error rates are measured at a received line signal level of -20 dBm.

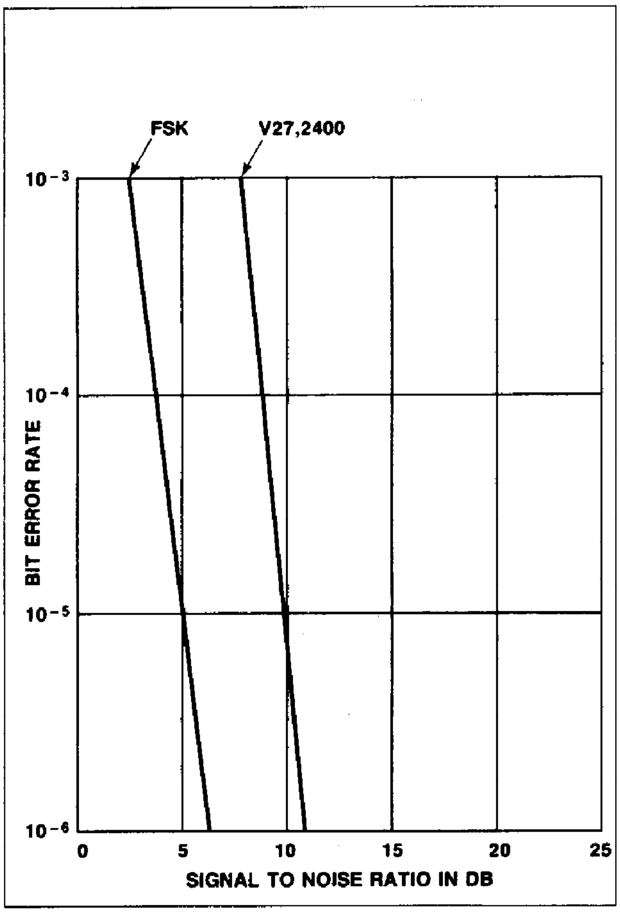
RECEIVED SIGNAL FREQUENCY TOLERANCE

The receiver circuit of the R24MFX can adapt to received frequency error of ±10 Hz with less than 0.2 dB degradation in BER performance.

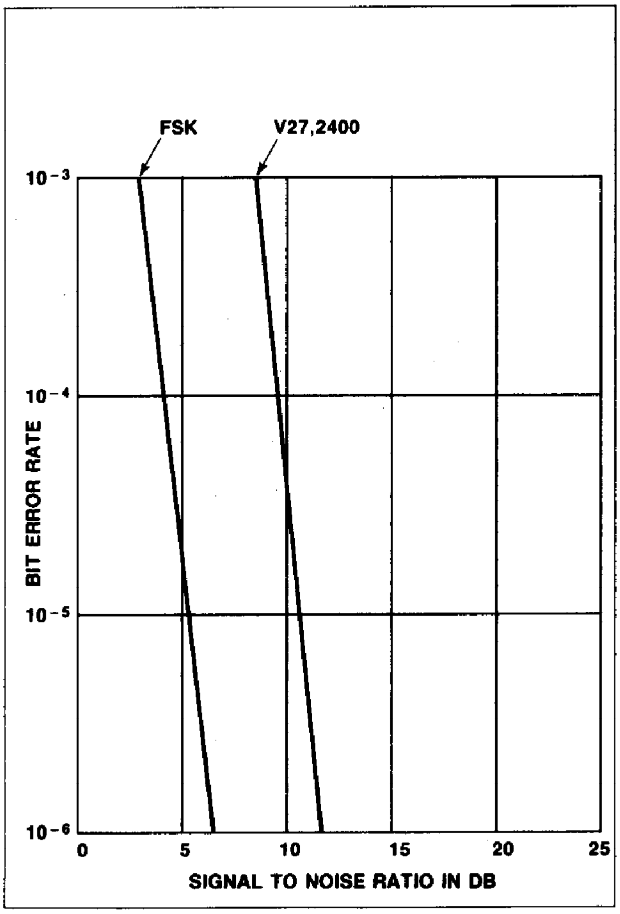
TYPICAL PHASE JITTER

At 2400 bps, the modem exhibits a BER of 10^{-6} or less with a signal-to-noise ratio of 12.5 dB in the presence of 15° peak-to-peak phase jitter at 150 Hz or with a signal-to-noise ratio of 15 dB in the presence of 30° peak-to-peak phase jitter at 120 Hz (scrambler inserted).

An example of the BER performance capabilities is given in the following diagrams:

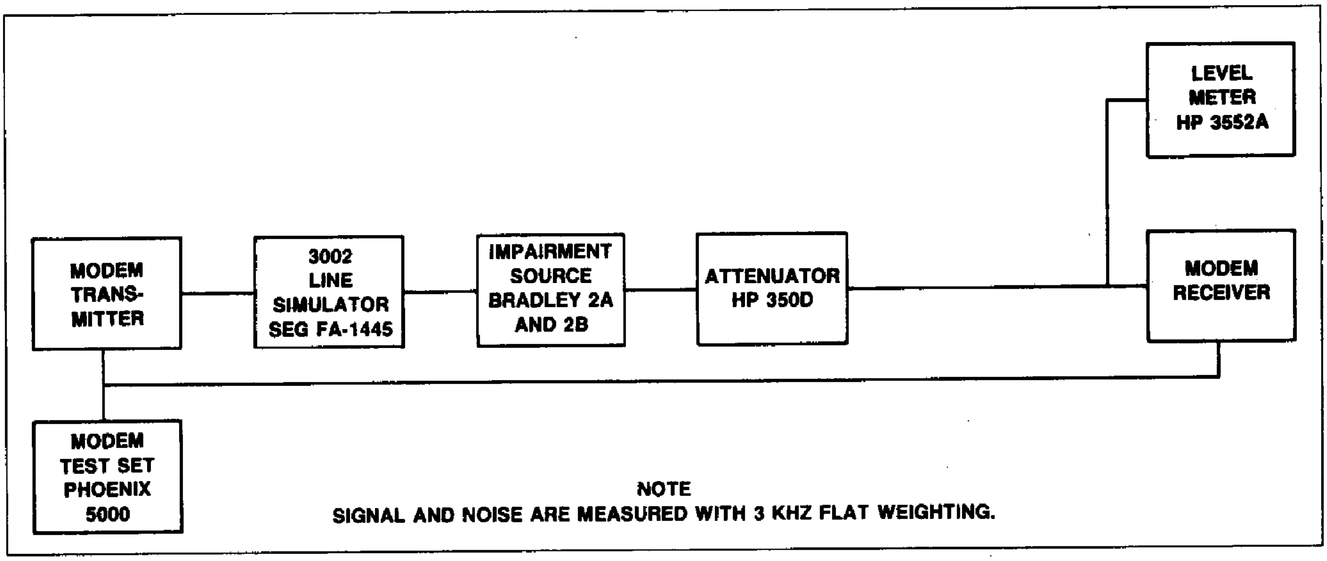


Typical Bit Error Rate
(Back-to-Back, Level -20 dBm)



Typical Bit Error Rate
(Unconditioned 3002 Line, Level -20 dBm)

The BER performance test set-up is show in the following diagram:



BER Performance Test Set-up

3

APPLICATION

Recommended Modem Interface Circuit

The R24MFX is supplied as a 64-pin QUIP device to be designed into original equipment manufacturer (OEM) circuit boards. The recommended modem interface circuit and parts list illustrate the connections and components required to connect the modem to the OEM electronics.

If the auxiliary analog input (pin 26) is not used, resistors R2 and R3 can be eliminated and pin 26 must be connected to analog ground (pin 24). When the cable equalizer controls CABLE1 and CABLE2 are connected to long leads that are subject to picking up noise spikes, a 3k Ω series resistor should be used on each input (Pins 32 and 33) for isolation.

Resistors R4 and R9 can be used to trim the transmit level and receive threshold to the accuracy required by the OEM equipment. For a tolerance of ±1 dB the 1% resistor values shown are correct for more than 99.8% of the units.

Typical Modem Interface Parts List

Component	Manufacturer's Part Number	Manufacturer
C3,C5,C7,C9	592CX7R104M050B	Sprague
C2	N511BY100JW	San Fernando/ Wescap
C1	C114C330J2G5CA	Kemet
C11	SA405C274MAA	AVX
Y1	333R14-002	Uniden
Z1	LM1458N	National
R5,R6	CML 1/10 T86.6K ohm ±1%	Dale Electronics
R4	5MA434.0K ±1%	Corning Electronics
R11	5043CX3R000J	Mepco Electra
R10	5043CX2M700J	Mepco Electra
R1	5043CX47K00J	Mepco Electra
R7	5043CX3K00J	Mepco Electra
R2,R3	5043CX1K00J	Mepco Electra
C10	ECEBEF100	Panasonic
C8	SMC50T1R0M5X12	United Chem-Con
C4,C6	C124C102J5G5CA	Kemet
CR1	IN751D	I.T.T.
R9	CRB ¼XF47K5	R-Ohm
R8	ER025QKF2370	Matsushita Electric
R14	Determined by $\overline{IRQ}$ characteristics	

PC Board Layout Considerations

1. The R24MFX and all supporting analog circuitry, including the data access arrangement if required, should be located on the same area of printed circuit board (PCB).
2. All power traces should be at least 0.1 inch width.
3. If power source is located more than approximately 5 inches from the R24MFX, a decoupling capacitor of 10 microfarad or greater should be placed in parallel with C11 near pins 11 and 48.
4. All circuitry connected to pins 9 and 10 should be kept short to prevent stray capacitance from affecting the oscillator.
5. Pin 22 should be tied directly to pin 24 at the R24MFX package. Pin 24 should tie directly, by a unique path, to the common ground point for analog and digital ground.
6. An analog ground plane should be supplied beneath all analog components. The analog ground plane should connect to pin 24 and all analog ground points shown in the recommended circuit diagram.
7. Pins 4, 8, 29, and 48 should tie together at the R24MFX package. Pin 48 should tie directly, by a unique path, to the common ground point for analog and digital ground.
8. A digital ground plane should be supplied to cover the remaining allocated area. The digital ground plane should connect to pin 48 and all digital ground points shown in the recommended circuit diagram plus the crystal-can ground.
9. The R24MFX package should be oriented relative to the two ground planes so that the end containing pin 1 is toward the digital ground plane and the end containing pin 32 is toward the analog ground plane.
10. As a general rule, digital signals should be routed on the component side of the PCB while analog signals are routed on the solder side. The sides may be reversed to match a particular OEM requirement.
11. Routing of R24MFX signals should provide maximum isolation between noise sources and sensitive inputs. When layout requirements necessitate routing these signals together, they should be separated by neutral signals. Refer to the table of noise characteristics for a list of pins in each category.

Pin Noise Characteristics

Noise Source			Noise Sensitive	
High	Low	Neutral	Low	High
1	6	3	26	23
2	7	4	28	27
5	9	8	32	35
14	10	11	33	36
15	12	16		37
20	13	22		
21	17	24		
30	18	25		
38	19	29		
39	45	31		
40	46	34		
41	49	42		
44	50	43		
	51	47		
	52	48		
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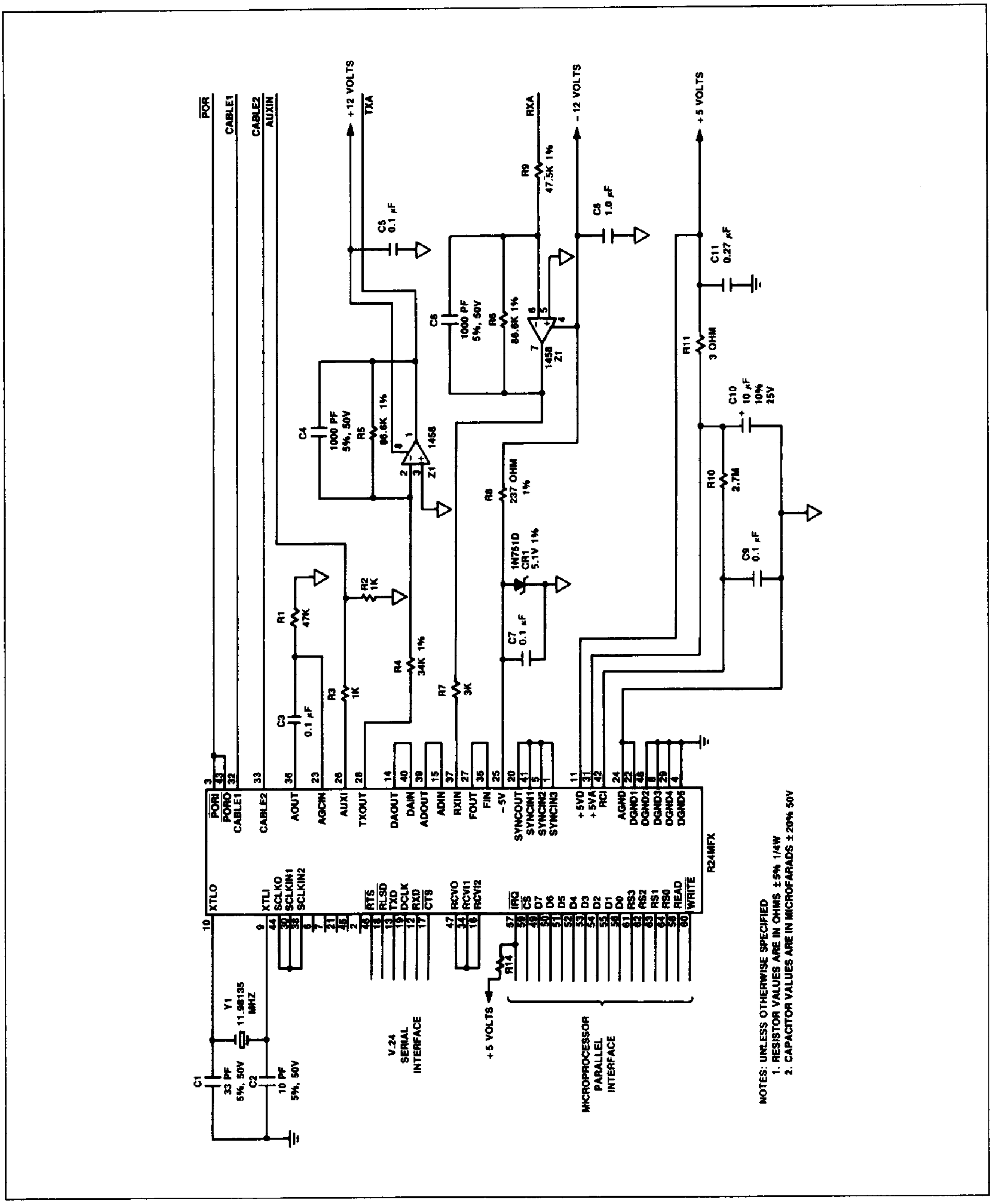
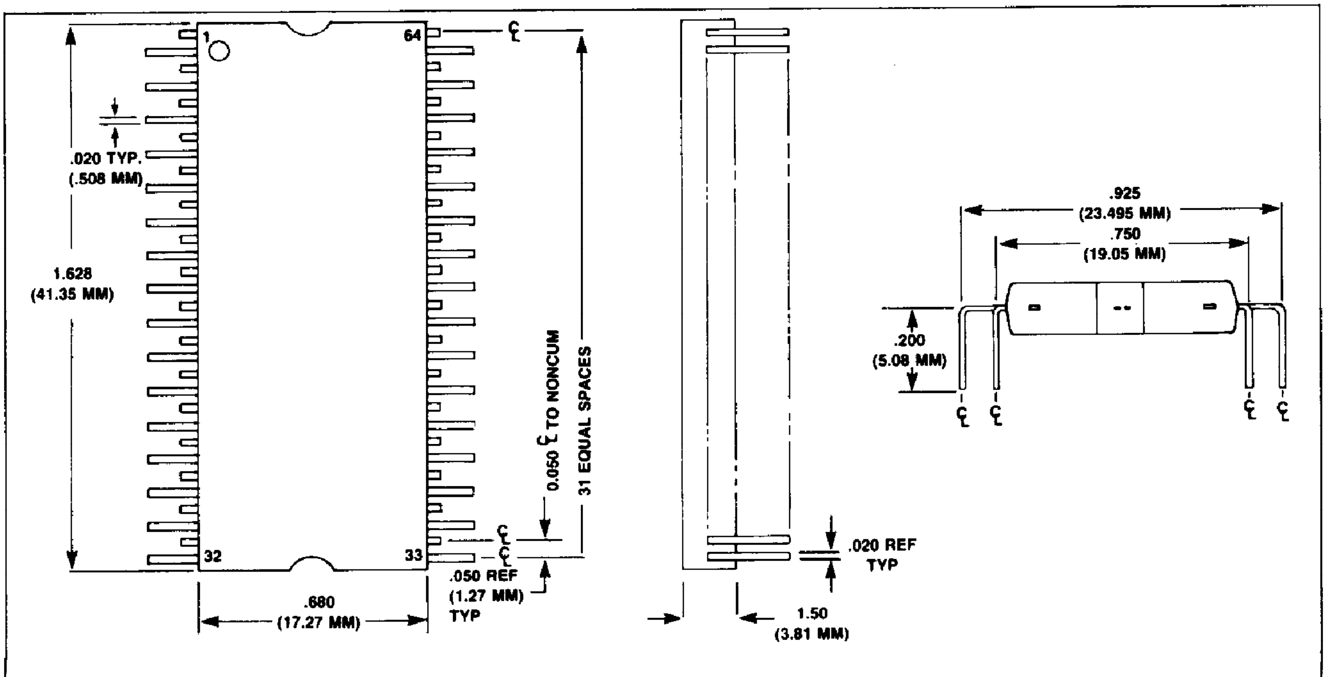


Recommended Modem Interface Circuit

PACKAGE DIMENSIONS



64-Pin QUIP