STC11F/10Fxx series MCU
STC11L/10Lxx series MCU
Data Sheet

Content

Chapter 1. Introduction

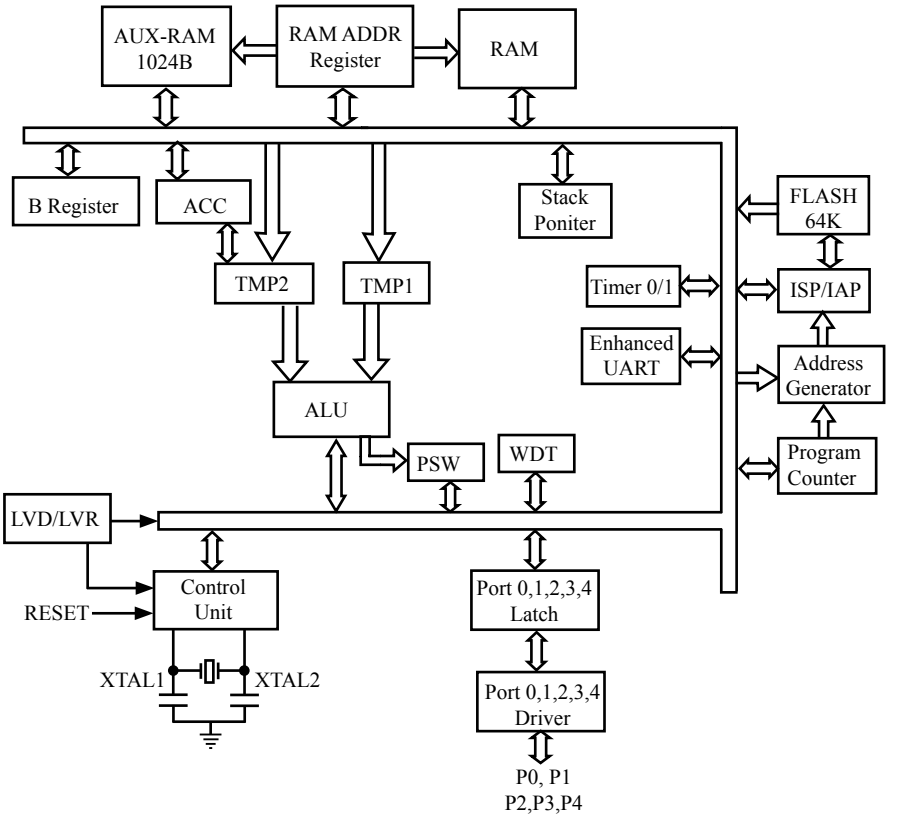
STC11F/10Fxx series are a single-chip microcontroller based on a high performance 1T architecture 80C51 CPU, which is produced by STC MCU Limited. With the enhanced kernel, STC11F/10Fxx series execute instructions in 1~6 clock cycles (about 6~7 times the rate of a standard 8051 device), and have an fully compatible instruction set with industrial-standard 80C51 series microcontroller . In-System-Programming (ISP) and In-Application-Programming (IAP) support the users to upgrade the program and data in system. ISP allows the user to download new code without removing the microcontroller from the actual end product; IAP means that the device can write non-valatile data in Flash memory while the application program is running. The STC11F/10Fxx series retain all features of the standard 80C51. In addition, the STC11F/10Fxx series have a extra I/O port (P4), a 6-sources, 2-priority-level interrupt structure, on-chip crystal oscillator,and a one-time enabled Watchdog Timer.

1.1 Features

- Enhanced 80C51 Central Processing Unit ,1T per machine cycle, faster 6~7 times than the rate of a standard 8051.
- Operating voltage range: 5.5~4.1V/3.7V or 2.1V/2.4V ~ 3.6V (STC11L/10Lxx series)
- Operating frequency range: 0- 35MHz, is equivalent to standard 8051:0~420MHZ
- On-chip 4/8/12/14/16/20/32/40/48/52/56/62K Flash program memory with flexible ISP/IAP capability,
- On-chip 1280/512/256 byte RAM
- Be capable of addressing up to 64K byte of external RAM
- Dual Data Pointer (DPTR) to speed up data movement
- Code protection for flash memory access
- two 16-bit timer/counter, as the same as Timer0/Timer1 of standard 8051,one BRT(Baud-rate-generator)
- 6 vector-address, 2 level priority interrupt capability
- One enhanced UART with hardware address-recognition, frame-error detection function, and with self baud-rate generator.
- One 15 bits Watch-Dog-Timer with 8-bit pre-scaler (one-time-enabled)
- Simple internal RC oscillator
- Three power management modes: idle mode, slow down mode and power-down mode
- Power down mode can be woken-up by INT0/P3.0 pin, INT1/P3.3 pin, T0/P3.4, T1/P3.5, RXD/P3.0 pin (or RXD/P1.6 pin)
- Maximum 40 programmable I/O ports are available
- Programable clock output Function. T0 output the clock on P3.4, T1 output the clock on P3.5, BRT output the clock on P1.0.
- Five package type : LQFP-44, PDIP-40, PLCC-44, QFN-40

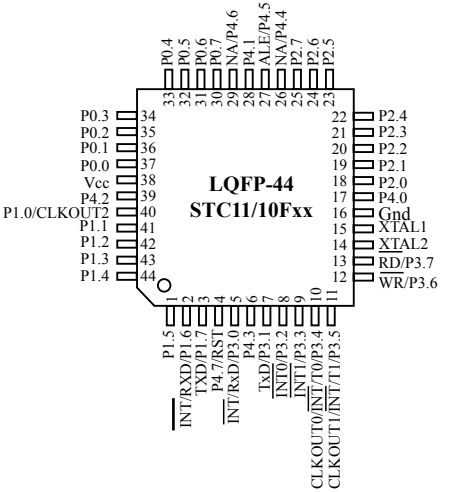
1.2 Block diagram

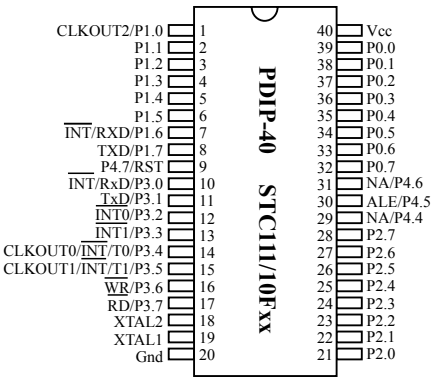
The CPU kernel of STC11/10Fxx series are fully compatible to the standard 8051 microcontroller, maintains all instruction mnemonics and binary compatibility. With some great architecture enhancements, STC11/10Fxx series execute the fastest instructions per clock cycle. Improvement of individual programs depends on the actual instructions used.

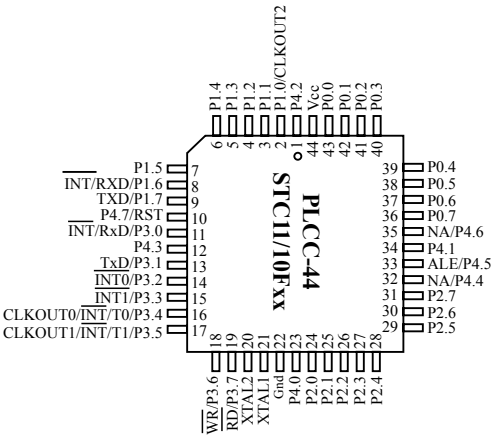


STC11/10Fxx Block Diagram

1.3 Pin Configurations





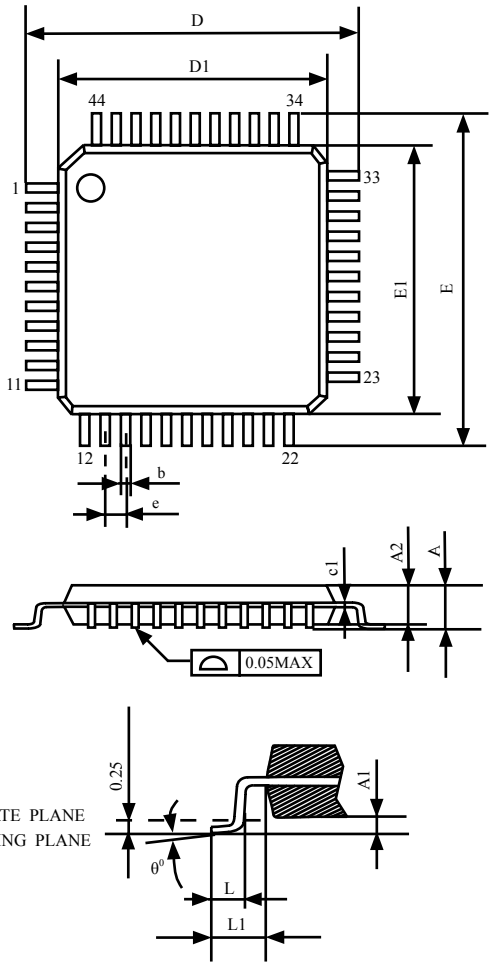


1.4 Pin Descriptions

MNEMONIC	LQFP44	PDIP40	PLCC44	DESCRIPTION
P0.0 ~ P0.7	30-37	32-39	36~43	Port0 : Port0 is an 8-bit bi-directional I/O port with pull-up resistance. Except being as GPIO, Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory.
P1.0 ~ P1.7	40~44 1~3	1-8	2~9	Port1 : General-purposed I/O with weak pull-up resistance inside. When 1s are written into Port1, the strong output driving CMOS only turn-on two period and then the weak pull-up resistance keep the port high.
P2.0 ~ P2.7	18-25	21-28	24~31	Port2 : Port2 is an 8-bit bi-directional I/O port with pull-up resistance. Except being as GPIO, Port2 emits the high-order address byte during accessing to external program and data memory.
P3.0 ~ P3.7	5 7~13	10-17	11 13~19	Port3 : General-purposed I/O with weak pull-up resistance inside. When 1s are written into Port1, the strong output driving CMOS only turn-on two period and then the weak pull-up resistance keep the port high. Port3 also serves the functions of various special features .
P4.0~P4.3 P4.0 P4.1 P4.2 P4.3	 17 28 39 6		 23 34 1 12	Port4 : Port4 are extended I/O ports such like Port1.
RST/P4.7	4	9	10	RESET : A high on this pin for at least two machine cycles will reset the device.
P4.6	29	31	35	
P4.4	26	29	32	
ALE/P4.5	27	30	33	Address Latch Enable : It is used for external data memory cycles (MOVX)
XTAL1	15	19	21	Crystal 1: Input to the inverting oscillator amplifier.Receives the external oscillator signal when an external oscillator is used.
XTAL2	14	18	20	Crystal 2: Output from the inverting amplifier. This pin should be floated when an external oscillator is used.
VCC	38	40	44	Power
Gnd	16	20	22	Ground

1.5 Pin Package Drawings

LQFP-44 OUTLINE PACKAGE

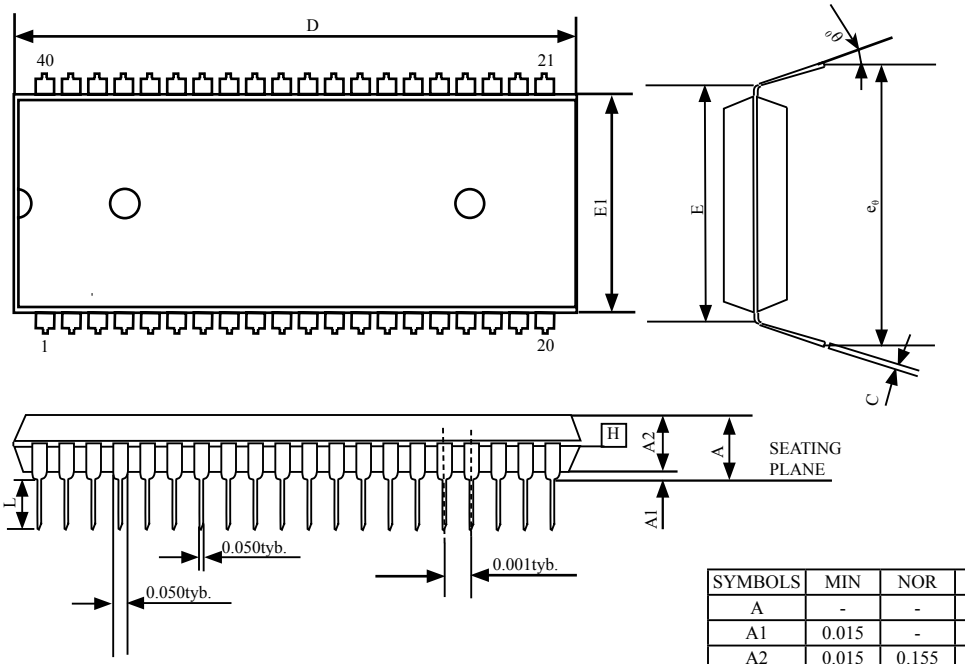


VARIATIONS (ALL DIMENSIONS SHOWN IN MM

SYMBOLS	MIN.	NOM	MAX.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
c1	0.09	-	0.16
D		12.00	
D1		10.00	
E		12.00	
E1		10.00	
e		0.80	
b(w/o plating)	0.25	0.30	0.35
L	0.45	0.60	0.75
L1		1.00REF	
θ^0	0^0	3.5^0	7^0

NOTES:
1.JEDEC OUTLINE:MS-026 BSB
2.DIMENSIONS D1 AND E1 D0 NOT INCLUDE MOLD PROTRUSION. ALLOWBLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS IMCLUDING MOLD MISMATCH.
3.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.ALLOWBLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUN b DIMNSION BY MORE THAN 0.08mm.

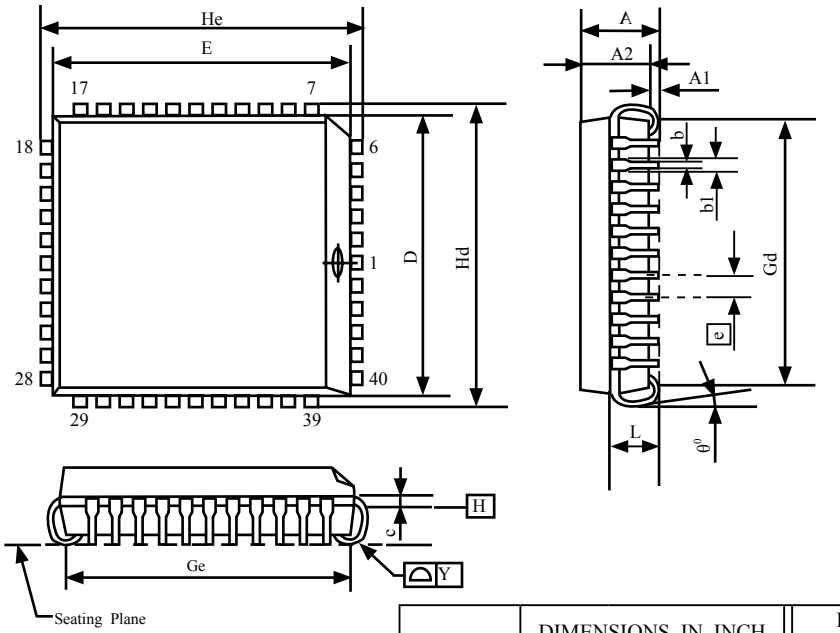
PDIP-40 OUTLINE PACKAGE



SYMBOLS	MIN	NOR	MAX
A	-	-	0.190
A1	0.015	-	-
A2	0.015	0.155	0.160
C	0.008	-	0.015
D	2.025	2.060	2.070
E		0.600	
E1	0.540	0.545	0.550
L	0.120	0.130	0.140
e_b	0.630	0.650	0.670
θ	0	7	15

NOTE:
1.JEDEC OUTLINE :MS-011 AC

PLCC-44 OUTLINE PACKAGE



SYMBOLS	DIMENSIONS IN INCH			DIMENSIONS IN MILLMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.165	-	0.180	4.191	-	4.572
A1	0.020	-	-	0.508	-	-
A2	0.147	-	0.158	3.734	-	4.013
b1	0.026	0.028	0.032	0.660	0.711	0.813
b	0.013	0.017	0.021	0.330	0.432	0.533
c	0.007	0.010	0.0013	0.178	0.254	0.330
D	0.650	0.653	0.656	16.510	16.586	16.662
E	0.650	0.653	0.656	16.510	16.586	16.662
e	0.050BSC			1.270BSC		
Gd	0.590	0.610	0.630	14.986	15.494	16.002
Ge	0.590	0.610	0.630	14.986	15.494	16.002
Hd	0.685	0.690	0.695	17.399	17.526	17.653
He	0.685	0.690	0.695	17.399	17.526	17.653
L	0.100	-	0.112	2.540	-	2.845
Y	-	-	0.004	-	-	0.102

NOTE:

1.JEDEC OUTLINE :M0-047 AC

2.DATUM PLANE H IS LACATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.

3.DIMENSIONS E AND D D0 NOT INCLUDE MODE PROTRUSION. ALLOWABLE PROTRUSION IS 10 MIL PRE SIDE.DIMENSIONS E AND D D0 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

4.DIMENSION b1 DOES NOT INCLUDE DAMBAR PROTRUSION.

Chapter 2. CLOCK, POWER MANAGENMENT, RESET

2.1 Clock Network

There are two clock sources available for STC11/10Fxx series. One is the clock from crystal oscillation and the other is from internal simple RC oscillation.

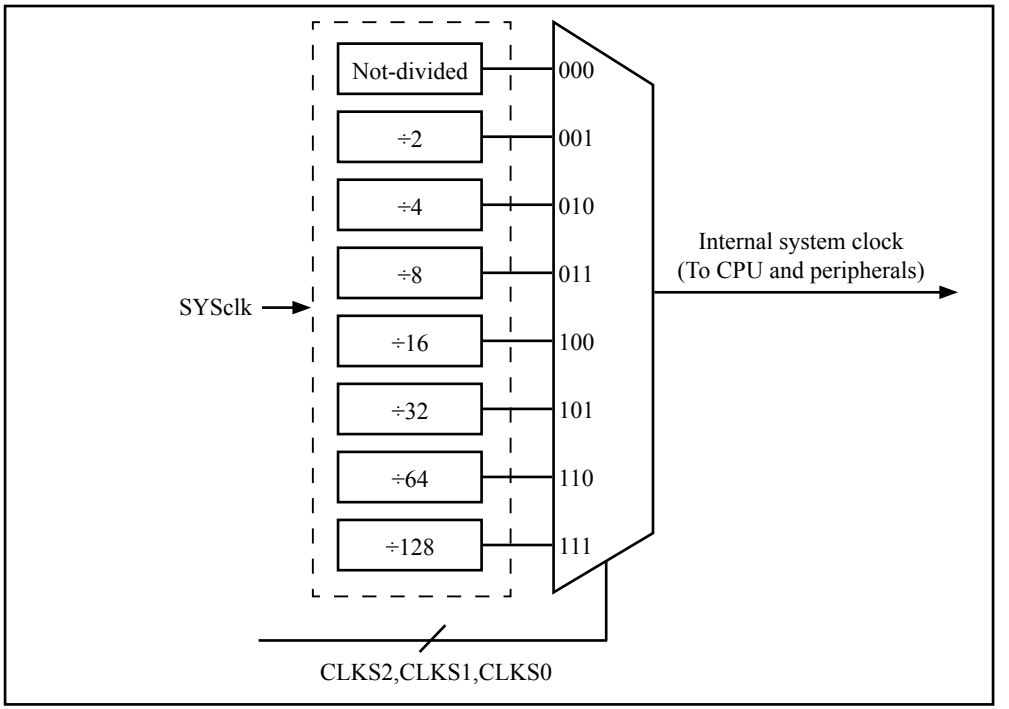
CLK_DIV register (Clock Divider)

LSB

bit	B7	B6	B5	B4	B3	B2	B1	B0
name	-	-	-	-	-	CLKS2	CLKS1	CLKS0

B2-B0 (CLKS2-CLKS0) :

000 clock source is not divided (default state)
001 clock source is divided by 2.
010 clock source is divided by 4.
011 clock source is divided by 8.
100 clock source is divided by 16.
101 clock souece is divided by 32.
110 clock source is divided by 64.
111 clock source is divided by 128.



Clock Structure

2.2 Power Management

PCON register

LSB

bit	B7	B6	B5	B4	B3	B2	B1	B0
name	SMOD	SMOD0	LVDF	POF	GF1	GF0	PD	IDL

SMOD : Double baud rate bit when the UART is used in mode 1,2 or 3.
SMOD0 : SM0/FE bit select for SCON.7
LVDF : Low-Voltage Flag. It is set if the voltage is below the LVD reference voltage.
POF : Power-On flag. It is set by power-off-on action and can only cleared by software.
GF1 : General-purposed flag 1
GF0 : General-purposed flag 0
PD : Power-Down bit.
IDL : Idle mode bit.

2.2.1 Idle Mode

An instruction that sets IDL/PCON.0 causes that to be the last instruction executed before going into the idle mode, the internal clock is gated off to the CPU but not to the interrupt, timer, WDT and serial port functions. The CPU status is preserved in its entirety: the Stack Pointer, Program Counter, Program Status Word, Accumulator, and all other registers maintain their data during Idle. The port pins hold the logical states they had at the time Idle was activated. ALE and PSEN hold at logic high levels.

There are two ways to terminate the idle. Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware, terminating the idle mode. The interrupt will be serviced, and following RETI, the next instruction to be executed will be the one following the instruction that put the device into idle.

The flag bits (GFO and GF1) can be used to give art indication if an interrupt occurred during normal operation or during Idle. For example, an instruction that activates Idle can also set one or both flag bits. When Idle is terminated by an interrupt, the interrupt service routine can examine the flag bits.

The other way to wake-up from idle is to pull RESET high to generate internal hardware reset.Since the clock oscillator is still running, the hardware reset neeeds to be held active for only two system clock cycles(24 system clock) to complete the reset.

2.2.2 Slow Down Mode

A divider is designed to slow down the clock source prior to route to all logic circuit. The operating frequency of internal logic circuit can therefore be slowed down dynamically , and then save the power.

2.2.3 Power Down (PD) Mode

An instruction that sets PCON.1 cause that to be the last instruction executed before going into the PD mode. In the PD mode, the on-chip oscillator is stopped. The contents of on-chip RAM and SFRs are maintained. The power-down mode can be woken-up by RESET pin, external interrupt INT0 ~ INT1, RXD pin, T0 pin, T1 pin and PCA input pins-cex0 and cex1. When it is woken-up by RESET, the program will execute from the address 0x0000. Be carefully to keep RESET pin active for at least 10ms in order for a stable clock. If it is woken-up from I/O, the CPU will rework through jumping to related interrupt service routine. Before the CPU rework, the clock is blocked and counted until 32768 in order for denouncing the unstable clock. To use I/O wake-up, interrupt-related registers have to be enabled and programmed accurately before power-down is entered. Pay attention to have at least one “NOP” instruction subsequent to the power-down instruction if I/O wake-up is used.

2.3 RESET Control

In STC12C5A60S2, there are 6 sources to generate internal reset. They are RESET (P4.7) pin, Watch-Dog-Timer, software reset, On-chip power-on-reset and On-chip MAX810 POR timing delay.

2.3.1 Reset pin

The P4.7 pin, if configured as RESET pin function(default), is input pin for chip reset. A level change of RESET pin have to keep at least 24 cycles plus 10us in order for CPU internal sampling use.

2.3.2 Power-On Reset (POR)

When VCC drops below the detection threshold of POR circuit, all of the logic circuits are reset.
When VCC goes back up again, an internal reset is released automatically after a delay of 32768 clocks. The nominal POR detection threshold is around 1.9V for 3V device and 3.3V for 5V device.

2.3.3 Watch-Dog-Timer

An overflow of Watch-Dog-Timer will generate a internal reset.

WDT_CONTR: Watch-Dog-Timer Control Register

bit	B7	B6	B5	B4	B3	B2	B1	B0
name	WDT_FLAG	-	EN_WDT	CLR_WDT	IDLE_WDT	PS2	PS1	PS0

WDT_FLAG : WDT reset flag.
0 : This bit should be cleared by software.
1 : When WDT overflows, this bit is set by hardware to indicate a WDT reset happened.

2.3.4 Software RESET

Writing an “1” to SWRST bit in IAP_CONTR register will generate a internal reset.

IAP_CONTR: ISP/IAP Control Register

bit	B7	B6	B5	B4	B3	B2	B1	B0
name	IAPEN	SWBS	SWRST	CMD_FAIL	-	WT2	WT1	WT0

IAPEN : ISP/IAP operation enable.
0 : Global disable all ISP/IAP program/erase/read function.
1 : Enable ISP/IAP program/erase/read function.
SWBS: software boot selection control.
0 : Boot from main-memory after reset.
1 : Boot from ISP memory after reset.
SWRST: software reset trigger control.
0 : No operation
1 : Generate software system reset. It will be cleared by hardware automatically.
CMD_FAIL: Command Fail indication for ISP/IAP operation.
0 : The last ISP/IAP command has finished successfully.
1 : The last ISP/IAP command fails. It could be caused since the access of flash memory was inhibited.

2.3.5 MAX810 power-on-reset delay

There is another on-chip POR delay circuit is integrated on STC11/10Fxx. This circuit is like MAX810 and is controlled by configuring flash Option Register. Very long POR delay time – around 200ms will be generated by this circuit once it is enabled.

Chapter 3. Memory Organization

3.1 Program Flash Memory

There is 60K-bytes of flash memory embedded for program and data storage. The design allows users to configure it as like there are three individual partition banks inside. They are called AP region, IAP region and ISP boot region. AP region is the space that user program is resided. IAP(In-Application-Program) region is the nonvolatile data storage space that may be used to save important parameters by AP program. In other words, the IAP capability of STC11/10Fxx series provide the user to read/write the user-defined on-chip data flash region to save the needing in use of external EEPROM device. ISP boot region is the space that allows a specific program we calls “ISP program” is resided. Inside the ISP region, the user can also enable read/write access to a small memory space to store parameters for specific purposes. This small space is called “ISP data flash” and can be enabled via programming NVM option registers. Generally, the purpose of ISP program is to fulfill AP program upgrade without the need to remove the device from system. STC11/10Fxx series hardware catches the configuration information since power-up duration and performs out-of-space hardware-protection depending on pre-determined criteria. The criteria is AP region can be accessed by ISP program only, IAP region can be accessed by ISP program and AP program, and ISP region is prohibited access from AP program and ISP program itself. But if the “ISP data flash is enabled”, ISP program can read/write this space. When wrong settings on ISP-IAP SFRs are done, The “out-of-space” happens and STC11/10Fxx series follow the criteria above, ignore the trigger command.

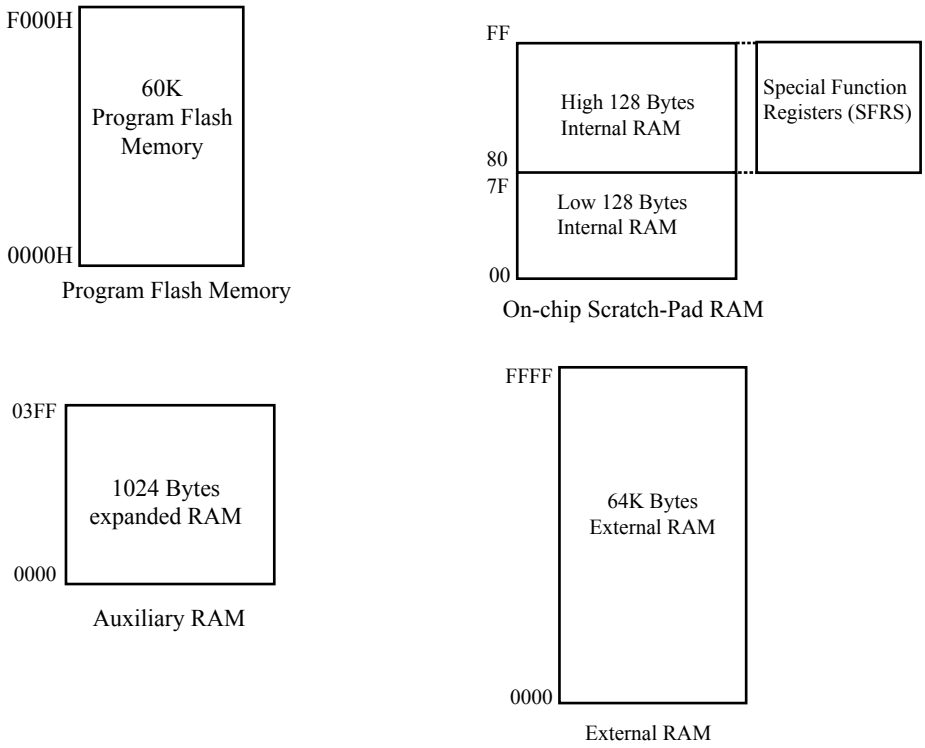


Figure 3b. The 8052 Data Memory

3.2 Data Memory

3.2.1 On-chip Scratch-Pad RAM

Just the same as the conventional 8051 micro-controller, there are 256 bytes of SRAM data memory plus 128 bytes of SFR space available on the STC11/10Fxx series. The lower 128 bytes of data memory may be accessed through both direct and indirect addressing. The upper 128 bytes of data memory and the 128 bytes of SFR space share the same address space. The upper 128 bytes of data memory may only be accessed using indirect addressing. The 128 bytes of SFR can only be accessed through direct addressing. The lower 32 bytes of data memory are grouped into 4 banks of 8 registers each. The RS0 and RS1 bits in PSW register select which register bank is in use. Instructions using register addressing will only access the currently specified bank.

3.2.2 Auxiliary RAM

There are 1024 bytes of additional data RAM available on STC11/10Fxx series. They may be accessed by the instructions MOVX @Ri or MOVX @DPTR. A control bit – XRAM located in AUXR.1 register is to control access of auxiliary RAM. When set, disable the access of auxiliary RAM. When clear (ERAM=0), this auxiliary RAM is the default target for the address range from 0x0000 to 0x03FF. If ERAM=0 and the target address is over 0x03FF, switches to access external RAM automatically. When ERAM=0, the content in DPH is ignored when the instruction MOVX @Ri is executed.

3.2.3 External RAM

There is 64K-byte addressing space available for STC11/10Fxx series to access external data RAM. Just the same as the design in the conventional 8051, the port – P2, P0, ALE, P3.6 and P3.7 have alterative function for external data RAM access. In addition, a new register BUS_SPEED (address: 0x8F) is design to stretch the cycle time of MOVX instruction. In BUS_SPEED register, {ALES1 and ALES0} is to stretch the setup time and hold time with respect to ALE negative edge and {RW2, RW1, RW0} is to stretch the pulse width of /WR(P3.6) and /RD(P3.7). By using BUS_SPEED to change the instruction cycle time, STC11/10Fxx series can conformed to communicate with both of fast and slow peripheral devices without loss of communication efficiency.

3.2.4 Special Function Register for RAM

For fast data movement, STC11/10Fxx series support two data pointers. They share the same SFR address and are switched by the register bit – DPS.

AUXR register

LSB

bit	B7	B6	B5	B4	B3	B2	B1	B0
name	T0x12	T1x12	UART_M0x6	BRTR	-	BRTx12	XRAM	S1BRS

T0x12

0 : The clock source of Timer 0 is SYSclk/12.

1 : The clock source of Timer 0 is SYSclk/1.

T1x12

0 : The clock source of Timer 1 is SYSclk/12.

1 : The clock source of Timer 1 is SYSclk/1.

UART_M0x6

0 : The baud-rate of UART in mode 0 is SYSclk/12.

1 : The baud-rate of UART in mode 0 is SYSclk/2.

BRTR

0 : The baud-rate generator of UART is stopped.

1 : The baud-rate generator of UART is enabled.

B3 : resevered.

BRTx12

0 : The baud-rate generator is incremented every 12 system clocks.

1 : The baud-rate generator is incremented every system clock.

XRAM

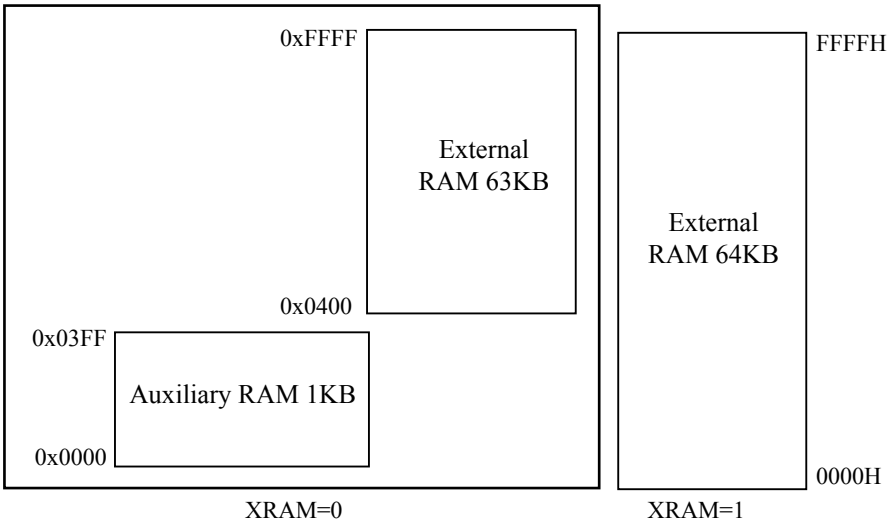
0 : On-chip auxiliary RAM is enabled and located at the address 0x0000 to 0x03FF.
For address over 0x03FF, off-chip external RAM becomes the target automatically.

1 : On-chip auxiliary RAM is always disabled.

S1BRS

0 : Timer 1 is used for the baud-rate generator.

1 : Timer 1 is released to use in other functions, and enhanced UART is used for the baud-rate generator.



AUXR1 register

LSB

bit	B7	B6	B5	B4	B3	B2	B1	B0
name	UART_P1	-	-	-	GF2	-	-	DPS

GF2 : General Flag. It can be used by software.

DPS : DPTR registers select bit.
0 : DPTR0 is selected(Default).
1 : The secondary DPTR(DPTR 1) is switched to use.

BUS_SPEED register

LSB

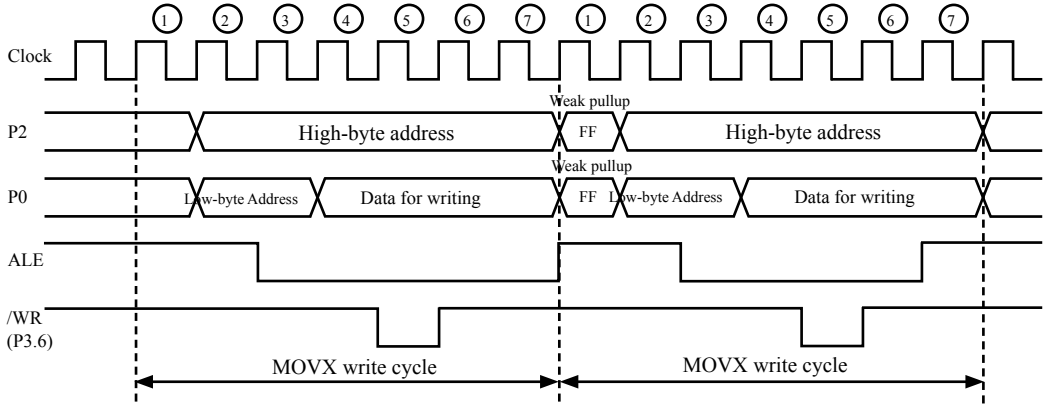
bit	B7	B6	B5	B4	B3	B2	B1	B0
name	-	-	ALES1	ALES0	-	RWS2	RWS1	RWS0

{ALES1 and ALES0} :
00 : The P0 address setup time and hold time to ALE negative edge is one clock cycle
01 : The P0 address setup time and hold time to ALE negative edge is two clock cycles.
10 : The P0 address setup time and hold time to ALE negative edge is three clock cycles. (default)
11 : The P0 address setup time and hold time to ALE negative edge is four clock cycles.

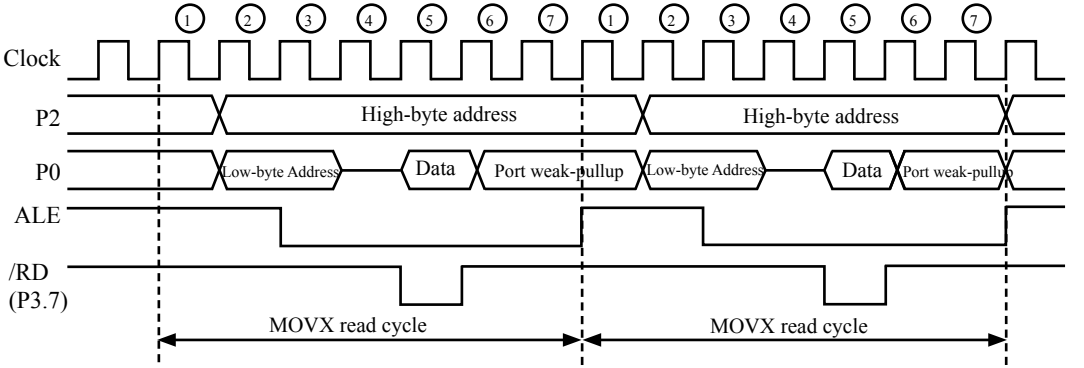
{RWS2,RWS1,RWS0} :
000 : The MOVX read/write pulse is 1 clock cycle.
001 : The MOVX read/write pulse is 2 clock cycles.
010 : The MOVX read/write pulse is 3 clock cycles.
011 : The MOVX read/write pulse is 4 clock cycles. (default)
100 : The MOVX read/write pulse is 5 clock cycles.
101 : The MOVX read/write pulse is 6 clock cycles.
110 : The MOVX read/write pulse is 7 clock cycles.
111 : The MOVX read/write pulse is 8 clock cycles.

When the target is on-chip auxiliary RAM, the setting on BUS_SPEED register is discarded by hardware.

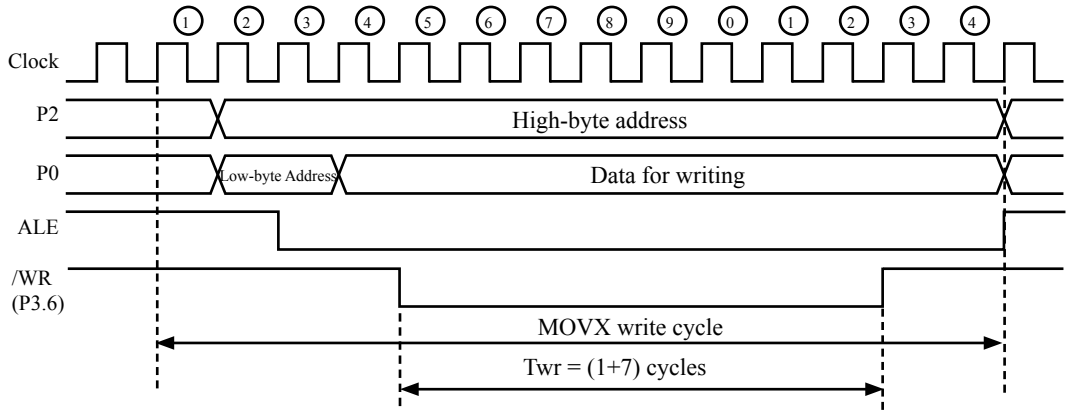
Timing diagram for MOVX @DPTR, A without stretch



Timing diagram for MOVX A, @DPTR without stretch

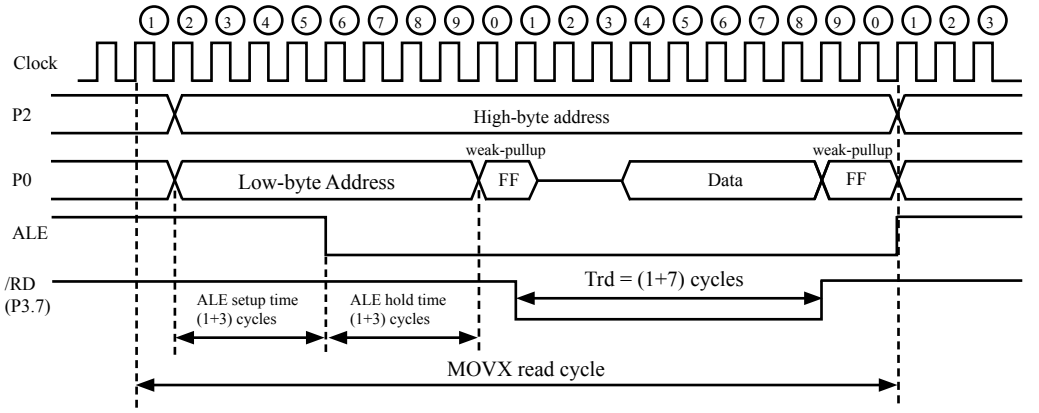


Timing diagram for MOVX @DPTR, A with stretch {RWS2,RWS1,RWS0} = 3'b111
Twr = 8 clock cycles (Twr is stretched by 7 cycles).



Timing diagram for MOVX @DPTR, A with stretch {RWS2,RWS1,RWS0} = 3'b111 and {ALES1,ALES0} == 2'b11

The Trd is stretched by 7, so Twr = 8 clock cycles. TALES is stretched by 3, so TALES = 4 clock cycles and TALEH = 4 clock cycles.



Chapter 4. Configurable I/O Ports

4.1 I/O Port Configurations

All port pins on STC11/10Fxx series may be independently configured to one of four modes : quasi-bidirectional (standard 8051 port output), push-pull output, input-only or open-drain output .All port pins default to quasi-bidirectional after reset. Each one has a Schmitt-triggered input for improved input noise rejection.

P4.5, and P4.7 are located at the pins-ALE, and RST of conventional 80C51. Pay attention that additional control bits on P4SW register are used to enable the I/O port functions of these pins. Prior to use them as I/O port, the users must set the corresponding bit to enable it.

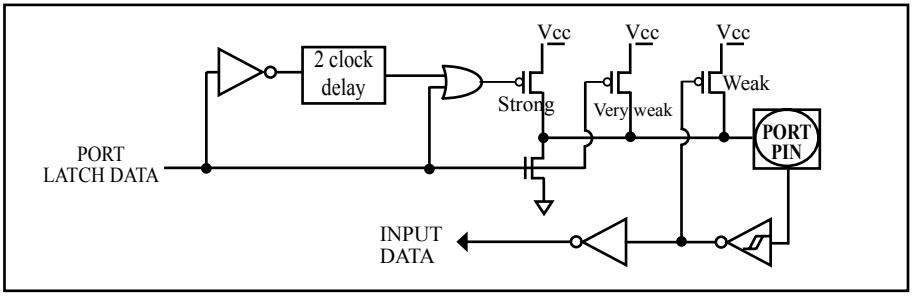
4.1.1 Quasi-bidirectional I/O

Port pins in quasi-bidirectional output mode function similar to the standard 8051 port pins. A quasi-bidirectional port can be used as an input and output without the need to reconfigure the port. This is possible because when the port outputs a logic high, it is weakly driven, allowing an external device to pull the pin low. When the pin outputs low, it is driven strongly and able to sink a large current. There are three pull-up transistors in the quasi-bidirectional output that serve different purposes.

One of these pull-ups, called the “very weak” pull-up, is turned on whenever the port register for the pin contains a logic “1”. This very weak pull-up sources a very small current that will pull the pin high if it is left floating.

A second pull-up, called the “weak” pull-up, is turned on when the port register for the pin contains a logic “1” and the pin itself is also at a logic “1” level. This pull-up provides the primary source current for a quasi-bidirectional pin that is outputting a 1. If this pin is pulled low by the external device, this weak pull-up turns off, and only the very weak pull-up remains on. In order to pull the pin low under these conditions, the external device has to sink enough current to over-power the weak pull-up and pull the port pin below its input threshold voltage.

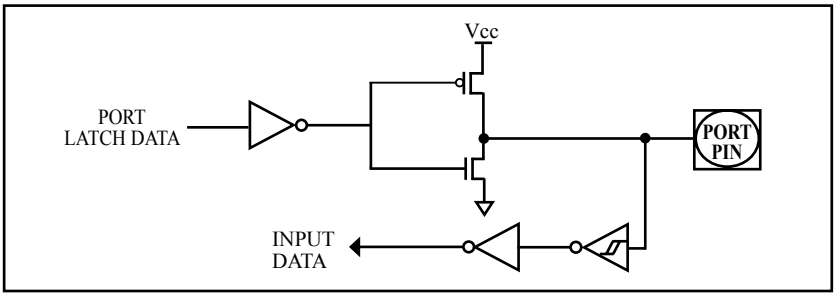
The third pull-up is referred to as the “strong” pull-up. This pull-up is used to speed up low-to-high transitions on a quasi-bidirectional port pin when the port register changes from a logic “0” to a logic “1”. When this occurs, the strong pull-up turns on for two CPU clocks, quickly pulling the port pin high.



Quasi-bidirectional output

4.1.2 Push-pull Output

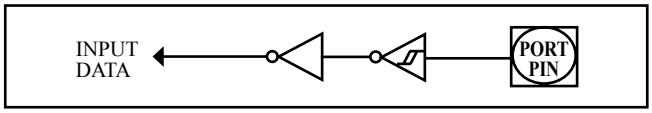
The push-pull output configuration has the same pull-down structure as both the open-drain and the quasi-bidirectional output modes, but provides a continuous strong pull-up when the port register conatins a logic “1”. The push-pull mode may be used when more source current is needed from a port output. In addition, input path of the port pin in this configuration is also the same as quasi-bidirectional mode.



Push-pull output

4.1.3 Input-only Mode

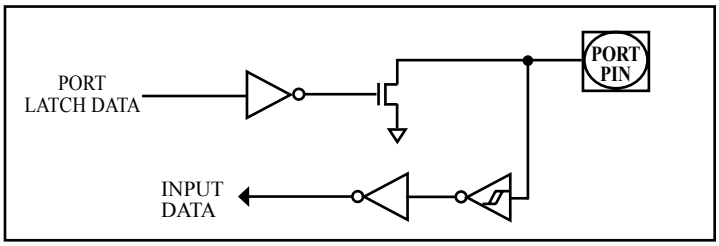
The input-only configuration is a Schmitt-triggered input without any pull-up resistors on the pin.



Input-only Mode

4.1.4 Open-drain Output

The open-drain output configuration turns off all pull-ups and only drives the pull-down transistor of the port pin when the port register contains a logic “0”. To use this configuration in application, a port pin must have an external pull-up, typically tied to VCC. The input path of the port pin in this configuration is the same as quasi-bidirection mode.



Open-drain output

4.2 I/O Port Registers

All port pins on STC11/10Fxx series may be independently configured by software to one of four types on a bit-by-bit basis,as shown in next Table.Two mode registers for each port select the output mode for each port pin.

Table: Configuration of I/O port mode.

PxM1.n	PxM0.n	Port Mode
0	0	Quasi-bidirectional
0	1	Push-Pull output
1	0	Input Only (High-impedance)
1	1	Open-Drain Output

P0M0 register

bit	7	6	5	4	3	2	1	0
name	P0M0.7	P0M0.6	P0M0.5	P0M0.4	P0M0.3	P0M0.2	P0M0.1	P0M0.0

P0M1 register

bit	7	6	5	4	3	2	1	0
name	P0M1.7	P0M1.6	P0M1.5	P0M1.4	P0M1.3	P0M1.2	P0M1.1	P0M1.0

P1M0 register

bit	7	6	5	4	3	2	1	0
name	P1M0.7	P1M0.6	P1M0.5	P1M0.4	P1M0.3	P1M0.2	P1M0.1	P1M0.0

P1M1 register

bit	7	6	5	4	3	2	1	0
name	P1M1.7	P1M1.6	P1M1.5	P1M1.4	P1M1.3	P1M1.2	P1M1.1	P1M1.0

P2M0 register

bit	7	6	5	4	3	2	1	0
name	P2M0.7	P2M0.6	P2M0.5	P2M0.4	P2M0.3	P2M0.2	P2M0.1	P2M0.0

P2M1 register

bit	7	6	5	4	3	2	1	0
name	P2M1.7	P2M1.6	P2M1.5	P2M1.4	P2M1.3	P2M1.2	P2M1.1	P2M1.0

P3M0 register

bit	7	6	5	4	3	2	1	0
name	P3M0.7	P3M0.6	P3M0.5	P3M0.4	P3M0.3	P3M0.2	P3M0.1	P3M0.0

P3M1 register

bit	7	6	5	4	3	2	1	0
name	P3M1.7	P3M1.6	P3M1.5	P3M1.4	P3M1.3	P3M1.2	P3M1.1	P3M1.0

P4M0 register

bit	7	6	5	4	3	2	1	0
name	P4M0.7	P4M0.6	P4M0.5	P4M0.4	P4M0.3	P4M0.2	P4M0.1	P4M0.0

P4M1 register

bit	7	6	5	4	3	2	1	0
name	P4M1.7	P4M1.6	P4M1.5	P4M1.4	P4M1.3	P4M1.2	P4M1.1	P4M1.0

P4SW register

bit	D7	D6	D5	D4	D3	D2	D1	D0
name	-	NA_P4.6	ALE_P4.5	NA_P4.4	-	-	-	-

NA_P4.6: Set this bit to enable P4.6. (Pin Location : Convention 80C51's EA).
0 : the pin is always kept at weak-high state.
1 : the pin functions as P4.6.

ALE_P4.5 : Set this bit to switch ALE to become P4.5. (Pin Location : Convention 80C51's ALE)
0 : the pin functions as ALE output for use in MOVX instruction only.
1 : the pin functions as P4.5.

NA_P4.4 : Set this bit to enable P4.4. (Pin Location : Convention 80C51's PSEN)
0 : the pin is always kept at weak-high state.
1 : the pin functions as P4.4

Chapter 5 Instruction System

5.1 Special Function Registers

	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	
0F8H									0FFH
0F0H	B 0000,0000								0F7H
0E8H									0EFH
0E0H	ACC 0000,0000								0E7H
0D8H									0DFH
0D0H	PSW 0000,0000								0D7H
0C8H									0CFH
0C0H	P4 1111,1111	WDT_CONR xx00,0000	IAP_DATA 1111,1111	IAP_ADDRH 0000,0000	IAP_ADDRL 0000,0000	IAP_CMD xxxx,xx00	IAP_TRIG xxxx,xxxx	IAP_CONTR 0000,0000	0C7H
0B8H	IP x0x0,0000	SADEN 0000,0000		P4SW x000,xxxx					0BFH
0B0H	P3 1111,1111	P3M1 0000,0000	P3M0 0000,0000	P4M1 0000,0000	P4M0 0000,0000				0B7H
0A8H	IE 00x0,0000	SADDR 0000,0000	WKTCL 0000,0000	WKTCH 0xxx,0000					0AFH
0A0H	P2 1111,1111	BUS_SPEED xx10,x011	AUXR1 xxxx,0xx0					Don't use	0A7H
098H	SCON 0000,0000	SBUF xxxx,xxxx			BRT 0000,0000				09FH
090H	P1 1111,1111	P1M1 0000,0000	P1M0 0000,0000	P0M1 0000,0000	P0M0 0000,0000	P2M1 0000,0000	P2M0 0000,0000	CLK_DIV xxxx,x000	097H
088H	TCON 0000,0000	TMOD 0000,0000	TL0 0000,0000	TL1 0000,0000	TH0 0000,0000	TH1 0000,0000	AUXR 0000,x000	WAKE_CLKO x000,x000	08FH
080H	P0 1111,1111	SP 0000,0111	DPL 0000,0000	DPH 0000,0000				PCON 0011,0000	087H
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	

Symbol	Description	Address	Bit Address and Symbol MSB LSB								Value after Power-on or Reset
P0	Port 0	80H	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0	1111 1111B
SP	Stack Pointer	81H									0000 0111B
DPTR DPL	Data Pointer Low	82H									0000 0000B
DPTR DPH	Data Pointer High	83H									0000 0000B
PCON	Power Control	87H	SMOD	SMOD0	LVDF	POF	GF1	GF0	PD	IDL	0011 0000B
TCON	Timer Control	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	0000 0000B
TMOD	Timer Mode	89H	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0	0000 0000B
TL0	Timer Low 0	8AH									0000 0000B
TL1	Timer Low 1	8BH									0000 0000B
TH0	Timer High 0	8CH									0000 0000B
TH1	Timer High 1	8DH									0000 0000B
AUXR	Auxiliary register	8EH	T0x12	T1x12	UART_M0x6	BRTR	-	BRTx12	XRAM	S1BRS	0000 0000B
WAKE_CLKO	CLK_Output Power down Wake-up control register	8FH	-	RXD_PIN_IE	T1_PIN_IE	T0_PIN_IE	-	BRTCLKO	T1CLKO	T0CLKO	0000 0000B
P1	Port 1	90H	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0	1111 1111B
P1M1	P1 configuration 1	91H									0000 0000B
P1M0	P1 configuration 0	92H									0000 0000B
P0M1	P0 configuration 1	93H									0000 0000B
P0M0	P0 configuration 0	94H									0000 0000B
P2M1	P2 configuration 1	95H									0000 0000B
P2M0	P2 configuration 0	96H									0000 0000B
CLK_DIV	Clock Divder	97h	-	-	-	-	-	CLKS2	CLKS1	CLKS0	xxxx x000B
SCON	Serial Control	98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI	0000 0000B
SBUF	Serial Buffer	99H									xxxx xxxxB
BRT	dedicated Baud-Rate Timer	9CH									0000 0000B
P2	Port 2	A0H	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0	1111 1111B
BUS_SPEED	Bus-Speed Control	A1H	-	-	ALES1	ALES0	-	RWS2	RWS1	RWS0	xx10 x011B
AUXR1	Auxiliary register1	A2H	UART_P1	-	-	-	GF2	-	-	DPS	0xxx 0xx0B
IE	Interrupt Enable	A8H	EA	ELVD	-	ES	ET1	EX1	ET0	EX0	0x00 0000B
SADDR	Slave Address	A9H									0000 0000B
P3	Port 3	B0H	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0	1111 1111B
P3M1	P3 configuration 1	B1H									0000 0000B

Symbol	Description	Address	Bit Address and Symbol MSB LSB								Value after Power-on or Reset
P3M0	P3 configuration 0	B2H									0000 0000B
P4M1	P4 configuration 1	B3H									0000 0000B
P4M0	P4 configuration 0	B4H									0000 0000B
IP	Interrupt Priority Low	B8H	-	PLVD	PADC	PS	PT1	PX1	PT0	PX0	0000 0000B
SADEN	Slave Address Mask	B9H									0000 0000B
P4SW	Port 4 switch	BBH	-	NA_P4.6	ALE_P4.5	NA_P4.4	-	-	-	-	x000 xxxxB
P4	Port 4	C0H	P4.7	P4.6	P4.5	P4.4	P4.3	P4.2	P4.1	P4.0	1111 1111B
WDT_CONTR	Watch-Dog-Timer Control Register	C1H	WDT_FLAG	-	EN_WDT	CLR_WDT	IDLE_WDT	PS2	PS1	PS0	xx00 0000B
IAP_DATA	ISP/IAP Flash Data Register	C2H									1111 1111B
IAP_ADDRH	ISP/IAP Flash Address High	C3H									0000 0000B
IAP_ADDRL	ISP/IAP Flash Address Low	C4H									0000 0000B
IAP_CMD	ISP/IAP Flash Command Register	C5H	-	-	-	-	-	-	MS1	MS0	xxxx x000B
IAP_TRIG	ISP/IAP Flash Command Trigger	C6H									xxxx xxxxB
IAP_CONTR	ISP/IAP Control Register	C7H	IAPEN	SWBS	SWRST	CMD_FAIL	-	WT2	WT1	WT0	0000 x000B
PSW	Program Status Word	D0H	CY	AC	F0	RS1	RS0	OV	F1	P	0000 0000B
B	B Register	F0H									0000 0000B

Accumulator

ACC is the Accumulator register. The mnemonics for accumulator-specific instructions, however, refer to the accumulator simply as A.

B-Register

The B register is used during multiply and divide operations. For other instructions it can be treated as another scratch pad register.

Stack Pointer

The Stack Pointer register is 8 bits wide. It is incrementde before data is stored during PUSH and CALL executions. While the stack may reside anywhee in on-chip RAM, the Stack Pointer is initialized to 07H after a reset. This causes the stack to begin at location 08H.

Program Status Word(PSW)

The program status word(PSW) contains several status bits that reflect the current state of the CPU. The PSW, shown below, resides in the SFR space. It contains the Carry bit, the Auxiliary Carry(for BCD operation), the two register bank select bits, the Overflow flag, a Parity bit and two user-definable status flags.

The Carry bit, other than serving the function of a Carry bit in arithmetic operations, also serves as the "Accumulator" for a number of Boolean operations.

The bits RS0 and RS1 are used to select one of the four register banks shown in the previous page. A number of instructions refer to these RAM locations as R0 through R7.

The Parity bit reflects the number of 1s in the Accumulator. P=1 if the Accumulator contains an odd number of 1s and otherwise P=0.

PSW register

bit	7	6	5	4	3	2	1	0
name	CY	AC	F0	RS1	RS0	OV	F1	P

CY : Carry flag.
AC : Auxilliary Carry Flag.(For BCD operations)
F0 : Flag 0.(Available to the user for general purposes)
RS1: Register bank select control bit 1.
RS0: Register bank select control bit 0.
OV : Overflow flag.
F1 : Flag 1. User-defined flag.
P : Parity flag.

Data Pointer

The Data Pointer (DPTR) consists of a high byte (DPH) and a low byte (DPL). Its intended function is to hold a 16-bit address. It may be manipulated as a 16-bit register or as two independent 8-bit registers.

5.2 Addressing Modes

Direct Addressing(DIR)
In direct addressing the operand is specified by an 8-bit address field in the instruction. Only internal data RAM and SFRs can be direct addressed.

Indirect Addressing(IND)
In indirect addressing the instruction specified a register which contains the address of the operand. Both internal and external RAM can be indirectly addressed.

The address register for 8-bit addresses can be R0 or R1 of the selected bank, or the Stack Pointer.
The address register for 16-bit addresses can only be the 16-bit data pointer register – DPTR.

Register Instruction(REG)
The register banks, containing registers R0 through R7, can be accessed by certain instructions which carry a 3-bit register specification within the opcode of the instruction. Instructions that access the registers this way are code efficient because this mode eliminates the need of an extra address byte. When such instruction is executed, one of the eight registers in the selected bank is accessed.

Register-Specific Instruction
Some instructions are specific to a certain register. For example, some instructions always operate on the accumulator or data pointer,etc. No address byte is needed for such instructions. The opcode itself does it.

Immediate Constant(IMM)
The value of a constant can follow the opcode in the program memory.

Index Addressing
Only program memory can be accessed with indexed addressing and it can only be read. This addressing mode is intended for reading look-up tables in program memory. A 16-bit base register(either DPTR or PC) points to the base of the table, and the accumulator is set up with the table entry number. Another type of indexed addressing is used in the conditional jump instruction.
In conditional jump, the destination address is computed as the sum of the base pointer and the accumulator.

5.3 Instruction Set Summary

Mnemonic		Description	Byte	Execution cycles of conventional 8051	Execution cycles of STC11F60XE
ARITHMETIC OPERATIONS					
ADD	A, Rn	Add register to Accumulator	1	12	2
ADD	A, direct	Add ditect byte to Accumulator	2	12	3
ADD	A, @Ri	Add indirect RAM to Accumulator	1	12	3
ADD	A, #data	Add immediate data to Accumulator	2	12	2
ADDC	A, Rn	Add register to Accumulator with Carry	1	12	2
ADDC	A, direct	Add direct byte to Accumulator with Carry	2	12	3
ADDC	A, @Ri	Add indirect RAM to Accumulator with Carry	1	12	3
ADDC	A, #data	Add immediate data to Acc with Carry	2	12	2
SUBB	A, Rn	Subtract Register from Acc wih borrow	1	12	2
SUBB	A, direct	Subtract direct byte from Acc with borrow	2	12	3
SUBB	A, @Ri	Subtract indirect RAM from ACC with borrow	1	12	3
SUBB	A, #data	Substract immediate data from ACC with borrow	2	12	2
INC	A	Increment Accumulator	1	12	2
INC	Rn	Increment register	1	12	3
INC	direct	Increment direct byte	2	12	4
INC	@Ri	Increment direct RAM	1	12	4
DEC	A	Decrement Accumulator	1	12	2
DEC	Rn	Decrement Register	1	12	3
DEC	direct	Decrement direct byte	2	12	4
DEC	@Ri	Decrement indirect RAM	1	12	4
INC	DPTR	Increment Data Pointer	1	24	1
MUL	AB	Multiply A & B	1	48	4
DIV	AB	Divde A by B	1	48	5
DA	A	Decimal Adjust Accumulator	1	12	4

Mnemonic		Description	Byte	Execution cycles of conventional 8051	Execution cycles of STC11F60XE
LOGICAL OPERATIONS					
ANL	A, Rn	AND Register to Accumulator	1	12	2
ANL	A, direct	AND direct btye to Accumulator	2	12	3
ANL	A, @Ri	AND indirect RAM to Accumulator	1	12	3
ANL	A, #data	AND immediate data to Accumulator	2	12	2
ANL	direct, A	AND Accumulator to direct byte	2	12	4
ANL	direct,#data	AND immediate data to direct byte	3	24	4
ORL	A, Rn	OR register to Accumulator	1	12	2
ORL	A,direct	OR direct byte to Accumulator	2	12	3
ORL	A,@Ri	OR indirect RAM to Accumulator	1	12	3
ORL	A, #data	OR immediate data to Accumulator	2	12	2
ORL	direct, A	OR Accumulator to direct byte	2	12	4
ORL	direct,#data	OR immediate data to direct byte	3	24	4
XRL	A, Rn	Exclusive-OR register to Accumulator	1	12	2
XRL	A, direct	Exclusive-OR direct byte to Accumulator	2	12	3
XRL	A, @Ri	Exclusive-OR indirect RAM to Accumulator	1	12	3
XRL	A, #data	Exclusive-OR immediate data to Accumulator	2	12	2
XRL	direct, A	Exclusive-OR Accumulator to direct byte	2	12	4
XRL	direct,#data	Exclusive-OR immediate data to direct byte	3	24	4
CLR	A	Clear Accumulator	1	12	1
CPL	A	Complement Accumulator	1	12	2
RL	A	Rotate Accumulator Left	1	12	1
RLC	A	Rotate Accumulator Left through the Carry	1	12	1
RR	A	Rotate Accumulator Right	1	12	1
RRC	A	Rotate Accumulator Right through the Carry	1	12	1
SWAP	A	Swap nibbles within the Accumulator	1	12	1

Mnemonic		Description	Byte	Execution cycles of conventional 8051	Execution cycles of STC11F60XE
DATA TRANSFER					
MOV	A, Rn	Move register to Accumulator	1	12	1
MOV	A, direct	Move direct byte to Accumulator	2	12	2
MOV	A,@Ri	Move indirect RAM to	1	12	2
MOV	A, #data	Move immediate data to Accumulator	2	12	2
MOV	Rn, A	Move Accumulator to register	1	12	2
MOV	Rn, direct	Move direct byte to register	2	24	4
MOV	Rn, #data	Move immediate data to register	2	12	2
MOV	direct, A	Move Accumulator to direct byte	2	12	3
MOV	direct, Rn	Move register to direct byte	2	24	3
MOV	direct,direct	Move direct byte to direct	3	24	4
MOV	direct, @Ri	Move indirect RAM to direct byte	2	24	4
MOV	direct,#data	Move immediate data to direct byte	3	24	3
MOV	@Ri, A	Move Accumulator to indirect RAM	1	12	3
MOV	@Ri, direct	Move direct byte to indirect RAM	2	24	4
MOV	@Ri, #data	Move immediate data to indirect RAM	2	12	3
MOV	DPTR,#data16	Move immdiate data to indirect RAM	2	12	3
MOVC	A,@A+DPTR	Move Code byte relative to DPTR to Acc	1	24	4
MOVC	A, @A+PC	Move Code byte relative to PC to Acc	1	24	4
MOVX	A,@Ri	Move External RAM(16-bit addr) to Acc	1	24	4
MOVX	A,@DPTR	Move External RAM(16-bit addr) to Acc	1	24	3
MOVX	@Ri, A	Move Acc to External RAM(8-bit addr)	1	24	3
MOVX	@DPTR,A	Move Acc to External RAM (16-bit addr)	1	24	3
PUSH	direct	Push direct byte onto stack	2	24	4
POP	direct	POP direct byte from stack	2	24	3
XCH	A,Rn	Exchange register with Accumulator	1	12	3
XCH	A, direct	Exchange direct byte with Accumulator	2	12	4
XCH	A, @Ri	Exchange indirect RAM with Accumulator	1	12	4
XCHD	A, @Ri	Exchange low-order Digit indirect RAM with Acc	1	12	4

Mnemonic		Description	Byte	Execution cycles of conventional 8051	Execution cycles of STC11F60XE
BOOLEAN VARIABLE MANIPULATION					
CLR	C	Clear Carry	1	12	1
CLR	bit	Clear direct bit	2	12	4
SETB	C	Set Carry	1	12	1
SETB	bit	Set direct bit	2	12	4
CPL	C	Complement Carry	1	12	1
CPL	bit	Complement direct bit	2	12	4
ANL	C, bit	AND direct bit to Carry	2	24	3
ANL	C, /bit	AND complement of direct bit to Carry	2	24	3
ORL	C, bit	OR direct bit to Carry	2	24	3
ORL	C, /bit	OR complement of direct bit to Carry	2	24	3
MOV	C, bit	Move direct bit to Carry	2	12	3
MOV	bit, C	Move Carry to direct bit	2	24	4
JC	rel	Jump if Carry is set	2	24	3
JNC	rel	Jump if Carry not set	2	24	3
JB	bit, rel	Jump if direct bit is set	3	24	4
JNB	bit,rel	Jump if direct bit is not set	3	24	4
JBC	bit, rel	Jump if direct bit is set & clear bit	3	24	5
PROGRAM BRANCHING					
ACALL	addr11	Absolute Subroutine Call	2	24	6
LCALL	addr16	Long Subroutine Call	3	24	6
RET		Return from Subroutine	1	24	4
RETI		Return from interrupt	1	24	4
AJMP	addr11	Absolute Jump	2	24	3
LJMP	addr16	Long Jump	3	24	4
SJMP	rel	Short Jump (relative addr)	2	24	3
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	24	3
JZ	rel	Jump if Accumulator is Zero	2	24	3
JNZ	rel	Jump if Accumulator is not Zero	2	24	3
CJNE	A,direct,rel	Compare direct byte to Acc and jump if not equal	3	24	5
CJNE	A,#data,rel	Compare immediate to Acc and Jump if not equal	3	24	4
CJNE	Rn,#data,rel	Compare immediate to register and Jump if not equal	3	24	4
CJNE	@Ri,#data,rel	Compare immediate to indirect and jump if not equal	3	24	5
DJNZ	Rn, rel	Decrement register and jump if not Zero	2	24	4
DJNZ	direct, rel	Decrement direct byte and Jump if not Zero	3	24	5
NOP		No Operation	1	12	1

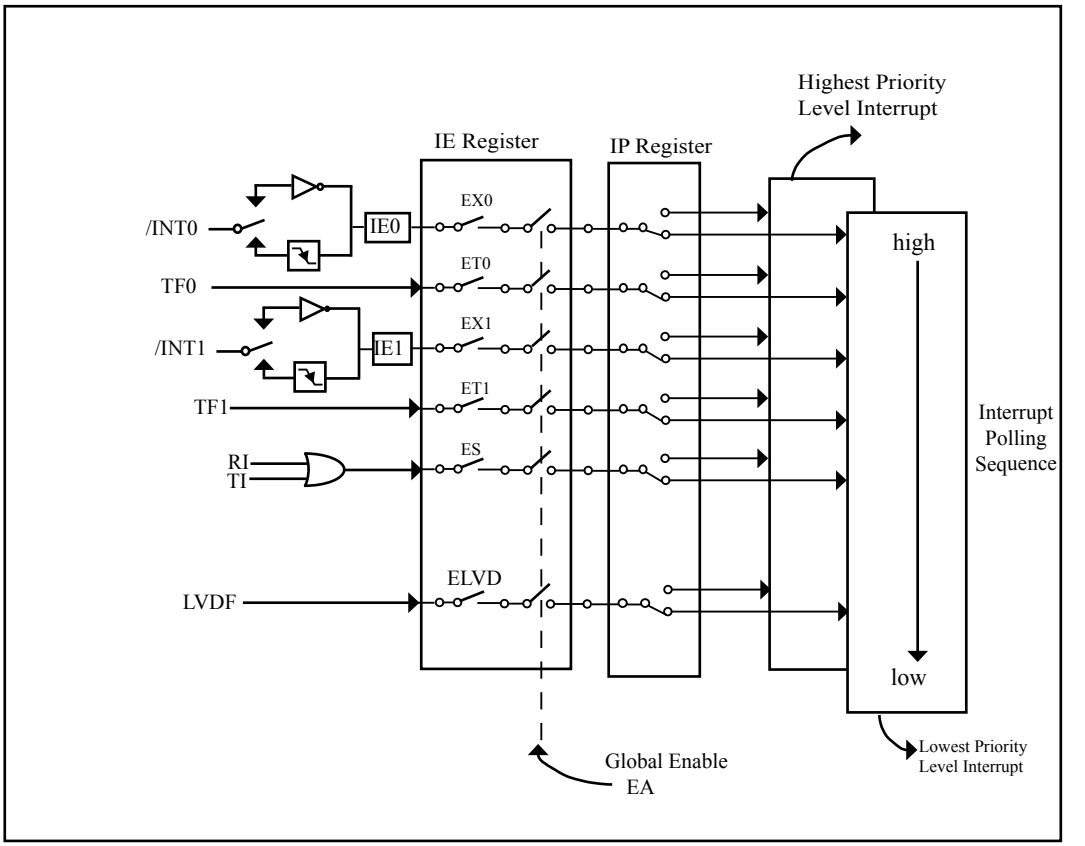
Chapter 6. Interrupt

There are 6 interrupt vector addresses available in STC11/10Fxx series. Associating with each interrupt vector, the interrupt sources can be individually enabled or disabled by setting or clearing a bit in the registers IE. The register also contains a global disable bit(EA), which can be cleared to disable all interrupts at once.

Each interrupt source has two corresponding bits to represent its priority. Higher-priority interrupt will be not interrupted by lower-priority interrupt request. If two interrupt requests of different priority levels are received simultaneously, the request of higher priority is serviced. If interrupt requests of the same priority level are received simultaneously, an internal polling sequence determine which request is serviced. The following table shows the internal polling sequence in the same priority level and the interrupt vector address.

Interrupt Source	Vector address	Polling Sequence	Interrupt Priority setting(IP)	Priority 0 (lowest)	Priority 1	Interrupt Request	Interrupt Enable Control Bit
/INT0 (External interrupt 0)	0003H	0(highest)	PX0	0	1	IE0	EX0/EA
Timer 0	000BH	1	PT0	0	1	TF0	ET0/EA
/INT1 (External interrupt 1)	0013H	2	PX1	0	1	IE1	EX1/EA
Timer1	001BH	3	PT1	0	1	TF1	ET1/EA
UART (Serial Interface)	0023H	4	PS	0	1	RI+TI	ES/EA
NA	002BH	5			1		
LVD	0033H	6	PLVD	0	1	LVDF	ELVD/EA

6.1 Interrupt Structure



Interrupt system diagram of STC11/10Fxx series

The External Interrupts $\overline{INT0}$ and $\overline{INT1}$ can each be either level-activated or transition-activated, depending on bits IT0 and IT1 in Register TCON. The flags that actually generate these interrupts are bits IE0 and IE1 in TCON. When an external interrupt is generated, the flag that generated it is cleared by the hardware when the service routine is vectored to if and only if the interrupt was transition –activated, otherwise the external requesting source is what controls the request flag, rather than the on-chip hardware.

The Timer 0 and Timer1 Interrupts are generated by TF0 and TF1, which are set by a rollover in their respective Timer/Counter registers in most cases. When a timer interrupt is generated, the flag that generated it is cleared by the on-chip hardware when the service routine is vectored to.

The Serial Port Interrupt is generated by the logical OR of RI and TI. Neither of these flags is cleared by hardware when the service routine is vectored to. In fact, the service routine will normally have to determine whether it was RI and TI that generated the interrupt, and the bit will have to be cleared by software.

The Low Voltage Detect interrupt is generated by the flag – LVDF in PCON register. It should be cleared by software.

All of the bits that generate interrupts can be set or cleared by software, with the same result as though it had been set or cleared by hardware. In other words, interrupts can be generated or pending interrupts can be canceled in software.

6.2 Interrupt Register

Symbol	Description	Address	Bit Address and Symbol MSB LSB								Value after Power-on or Reset
IE	Interrupt Enable	A8H	EA	ELVD	-	ES	ET1	EX1	ET0	EX0	0x00 0000B
IP	Interrupt Priority Low	B8H	-	PLVD	-	PS	PT1	PX1	PT0	PX0	0000 0000B
TCON	Timer Control	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	0000 0000B
SCON	Serial Control	98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI	0000 0000B
AUXR	Auxiliary register	8EH	T0x12	T1x12	UART_M0x6	BRTR	-	BRTx12	EXTRAM	S1BRS	0000 0000B
PCON	Power Control	87H	SMOD	SMOD0	LVDF	POF	GF1	GF0	PD	IDL	0001 0000B
WAKE_CLKO	CLK_Output Power down Wake-up control register	8FH	PCAWAKEUP	RXD_PIN_IE	T1_PIN_IE	T0_PIN_IE	-	BRTCLKO	T1CLKO	T0CLKO	0000 0000B

IE: Interrupt Enable Rsgister

(MSB) (LSB)

EA	ELVD	-	ES	ET1	EX1	ET0	EX0

Enable Bit = 1 enables the interrupt .
Enable Bit = 0 disables it .

Symbol	Position	Function
EA	IE.7	disables all interrupts. if EA = 0,no interrupt will be acknowledged. if EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
ELVD	IE.6	Low volatge detection interrupt enable bit.
ES	IE.4	Serial Port interrupt enable bit
ET1	IE.3	Timer 1 interrupt enable bit
EX1	IE.2	External interrupt 1 enable bit
ET0	IE.1	Timer 0 interrupt enable bit
EX0	IE.0	External interrupt 0 enable bit

IP: Interrupt Priority Register

(MSB) (LSB)

-	PLVD	-	PS	PT1	PX1	PT0	PX0

Priority bit = 1 assigns high priority .
Priority bit = 0 assigns low priority.

Symbol	Position	Function
PLVD	IP.6	Low voltage detection interrupt priority.
PS	IP.4	Serial Port interrupt priority bit.
PT1	IP.3	Timer 1 interrupt priority bit
PX1	IP.2	External interrupt 1 priority bit
PT0	IP.1	Timer 0 interrupt priority bit
PX0	IP.0	External interrupt 0 priority bit

6.3 Interrupt Priorities

Each interrupt source can also be individually programmed to one of two priority levels by setting or clearing a bit in Special Function Register IP. A low-priority interrupt can itself be interrupted by a high-pority interrupt, but not by another low-priority interrupt. A high-priority interrupt can't be interrupted by any other interrupt source.

If two requests of different priority levels are received simultaneously, the request of higher priority level is serviced. If requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence,as follows:

	Source	Priority Within Level
0.	IE0	(highest)
1.	TF0	
2.	IE1	
3.	TF1	
4.	RI +Tl	
5.		
6.	LVDF	

Note that the "priority within level" structure is only used to resolve *simultaneous requests of the same prionty level.*

6.4 How Interrupts Are Handled

External interrupt pins and other interrupt sources are sampled at the rising edge of each instruction *OPcode fetch cycle.* The samples are polled during the next instruction *OPcode fetch cycle*. If one of the flags was in a set condition of the first cycle, the second cycle of polling cycles will find it and the interrupt system will generate an hardware LCALL to the appropriate service routine as long as it is not blocked by any of the following conditions.

Block conditions :

- An interrupt of equal or higher priority level is already in progress.
- The current cycle(polling cycle) is not the final cycle in the execution of the instruction in progress.
- The instruction in progress is RETI or any write to the IE or IP registers.
- The ISP/IAP activity is in progress.

Any of these four conditions will block the generation of the hardware LCALL to the interrupt service routine. Condition 2 ensures that the instruction in progress will be completed before vectoring into any service routine. Condition 3 ensures that if the instruction in progress is RETI or any access to IE or IP, then at least one or more instruction will be executed before any interrupt is vectored to.

The polling cycle is repeated with the last clock cycle of each instruction cycle. Note that if an interrupt flag is active but not being responded to for one of the above conditions, if the flag is not still active when the blocking condition is removed, the denied interrupt will not be serviced. In other words, the fact that the interrupt flag was once active but not being responded to for one of the above conditions, if the flag is not still active when the blocking condition is removed, the denied interrupt will not be serviced. The interrupt flag was once active but not serviced is not kept in memory. Every polling cycle is new.

Note that if an interrupt of higher priority level goes active prior to S5P2 of the machine cycle labeled C3, then in accordance with the above rules it will be vectored to during C5 and C6, without any instruction of the lower priority routine having been executed.

Thus the processor acknowledges an interrupt request by executing a hardware-generated LCALL to the appropriate servicing routine. In some cases it also clears the flag that generated the interrupt, and in other cases it doesn't. It never clears the Serial Port flags. This has to be done in the user's software. It clears an external interrupt flag (IE0 or IE1) only if it was transition-activated. The hardware-generated LCALL pushes the contents of the Program Counter onto the stack (but it does not save the PSW) and reloads the PC with an address that depends on the source of the interrupt being vectored to, as shown be low.

Source	Vector Address
IE0	0003H
TF0	000BH
IE1	0013H
TF1	001BH
RI+TI	0023H
None	002BH
LVDF	0033H

Execution proceeds from that location until the RETI instruction is encountered. The RETI instruction informs the processor that this interrupt routine is no longer in progress, then pops the top two bytes from the stack and reloads the Program Counter. Execution of the interrupted program continues from where it left off.

Note that a simple RET instruction would also have returned execution to the interrupted program, but it would have left the interrupt control system thinking an interrupt was still in progress.

6.5 External Interrupts

The external sources can be programmed to be level-activated or transition-activated by setting or clearing bit IT1 or IT0 in Register TCON. If ITx = 0, external interrupt x is triggered by a detected low at the $\overline{\text{INTx}}$ pin. If ITx=1, external interrupt x is edge-triggered. In this mode if successive samples of the $\overline{\text{INTx}}$ pin show a high in one cycle and a low in the next cycle, interrupt request flag IEx in TCON is set. Flag bit IEx then requests the interrupt.

Since the external interrupt pins are sampled once each machine cycle, an input high or low should hold for at least 12 oscillator periods to ensure sampling. If the external interrupt is transition-activated, the external source has to hold the request pin high for at least one machine cycle, and then hold it low for at least one machine cycle to ensure that the transition is seen so that interrupt request flag IEx will be set. IEx will be automatically cleared by the CPU when the service routine is called.

If the external interrupt is level-activated, the external source has to hold the request active until the requested interrupt is actually generated. Then it has to deactivate the request before the interrupt service routine is completed, or else another interrupt will be generated.

6.6 Response Time

The $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$ levels are inverted and latched into the interrupt flags IE0 and IE1 at rising edge of every syetem clock cycle.

The Timer 0 and Timer 1 flags, TF0 and TF1, are set after which the timers overflow. The values are then polled by the circuitry at rising edge of the next system clock cycle.

If a request is active and conditions are right for it to be acknowledged, a hardware subroutine call to the requested service routine will be the next instruction to be executed. The call itself takes six system clock cycles. Thus, a minimum of seven complete system clock cycles elapse between activation of an external interrupt request and the beginning of execution of the first instruction of the service routine.

A longer response time would result if the request is blocked by one of the four previously listed conditions. If an interrupt of equal or higher priority level is already in progress, the additional wait time obviously depends on the nature of the other interrupt's service routine. If the instruction in progress is not in its final cycle, the additional wait time cannot be more than 3 cycles, since the longest instructions (LCALL) are only 6 cycles long, and if the instruction in progress is RETI or an access to IE or IP, the additional wait time cannot be more than 5 cycles (a maximum of one more cycle to complete the instruction in progress, plus 6 cycles to complete the next instruction if the instruction is LCALL).

Thus, in a single-interrupt system, the response time is always more than 7 cycles and less than 12 cycles.

Chapter 7. Timer/Counter 0/1

Timer 0 and timer 1 are like the ones in the conventional 8051, both of them can be individually configured as timers or event counters.

In the “Timer” function, the register is incremented every 12 cycles or every cycle depending on AUXR.7(T0x12) bit and AUXR.6(T1x12). In the default state, it is fully the same as the conventional 8051. In the x12 mode, the count rate equals to the oscillator frequency.

In the “Counter” function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T0 or T1. In this function, the external input is sampled once at the positive edge of every clock cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during S3P1 of the cycle following the one in which the transition was detected. Since it takes 2 machine cycles(24 oscillator periods) to recognize a l-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. There are no restrictions on the duty cycle of the external input signal, but to ensure that a given level is sampled at least once before it changes, it should be held for at least one full machine cycle.

In addition to the “Timer” or “Counter” selection, Timer 0 and Timer 1 have four operating modes from which to select. The “Timer” or “Counter” function is selected by control bits $C/\overline{T}$ in the Speciai Function Register TMOD. These two Timer/Counter have four operating modes, which are selected by bit-pairs (M1, M0) in TMOD. Modes 0, 1, and 2 are the same for both Timer/Counters. Mode 3 is different.The four operating modes are described in the following text.

Symbol	**Description**	**Address**	Bit Address and Symbol MSB LSB								Value after Power-on or Reset
TCON	Timer Control	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	0000 0000B
TMOD	Timer Mode	89H	GATE	$C/\overline{T}$	M1	M0	GATE	$C/\overline{T}$	M1	M0	0000 0000B
TL0	Timer Low 0	8AH									0000 0000B
TL1	Timer Low 1	8BH									0000 0000B
TH0	Timer High 0	8CH									0000 0000B
TH1	Timer High 1	8DH									0000 0000B
AUXR	Auxiliary register	8EH	T0x12	T1x12	UART_M0x6	BRTR	-		BRTx12	XRAM	S1BRS	0000 0000B
WAKE_CLKO	CLK_Output Power down Wake-up control register	8FH	-	RXD_PIN_IE	T1_PIN_IE	T0_PIN_IE	-		BRTCLKO	T1CLKO	T0CLKO	0000 0000B

AUXR register

LSB

	B7	B6	B5	B4	B3	B2	B1	B0
	T0x12	T1x12	UART_M0x6	BRTR	-	BRTx12	XRAM	S1BRS

T0x12

0 : The clock source of Timer 0 is SYSclk/12.

1 : The clock source of Timer 0 is SYSclk/1.

T1x12

0 : The clock source of Timer 1 is SYSclk/12.

1 : The clock source of Timer 1 is SYSclk/1.

WAKE_CLKO:CLK_Output Power down Wake-up control register

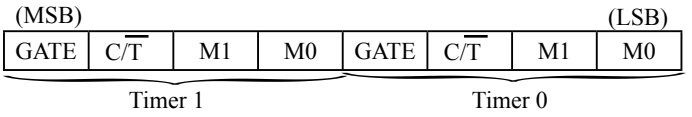
B7	B6	B5	B4	B3	B2	B1	B0
-	RXD_PIN_IE	T1_PIN_IE	T0_PIN_IE	-	BRTCLKO	T1CLKO	T0CLKO

BRTCLKO : When set, P1.0 is enabled to be the clock output of Baud-Rate Timer (BRT). The clock rate is BRT overflow rate divided by 2.

T1CLKO : When set, P3.5 is enabled to be the clock output of Timer 1. The clock rate is Timer1 overflow rate divided by 2.

T0CLKO : When set, P3.4 is enabled to be the clock output of Timer 0. The clock rate is Timer0 overflow rate divided by 2.

TMOD register : Timer/Counter Mode Control Register



GATE — Gating control when set. Timer/Counter "x" is enabled only while "$\overline{INTx}$ " pin is high and "TRx"control pin is set.When cleared Timer "x" is enabled whenever "TRx" control bit is set.

C/$\overline{T}$ — Timer or Counter Selector cleared for Timer operation (input from internal system clock). Set for Counter operation (input from "Tx" input pin).

M0	M1	Operating Mode
0	0	B-bit Timer/Counter "THx" with "TLx" as 5-bit prescaler.
0	1	16-bit Timer/Counter"THx"and"TLx"are cascaded;there is no prescaler
1	0	8-bit auto-reload Timer/Counter “THx” holds a value which is to be reloaded into “TLx” each time it overflows.
1	1	(Timer 0) TL0 is an 8-bit Timer/Counter controlled by the standard Timer 0 control bits TH0 is an 8-bit timer only controlled by Timer 1 control bits.
1	1	(Timer 1) Timer/Counter 1 stopped

TCON register: Timer/Counter Control Register

(MSB) (LSB)

TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Symbol	Position	Name and Significance	Symbol	Position	Name and Significance
TF1	TCON.7	Timer 1 overflow Flag. Set by hardware on Timer/Counter overflow. cleared by hardware when processor vectors to interrupt routine.	IE1	TCON.3	Interrupt 1 Edge flag. Set by hardware when external interrupt edge detected.Cleared when interrupt processed.
TR1	TCON.6	Timer 1 Run control bit. Set/cleared by software to turn Timer/Counter on/off.	IT1	TCON.2	Intenupt 1 Type control bit. Set/ cleared by software to specify falling edge/low level triggered external interrupts.
TF0	TCON.5	Timer 0 overflow Flag. Set by hardware on Timer/Counter overflow. cleared by hardware when processor vectors to interrupt routine.	IE0	TCON.1	Interrupt 0 Edge flag. Set by hardware when external interrupt edge detected.Cleared when interrupt processed.
TR0	TCON.4	Timer 0 Run control bit. Set/cleared by software to turn Timer/Counter on/off.	IT0	TCON.0	Intenupt 0 Type control bit. Set/ cleared by software to specify falling edge/low level triggered external interrupts.

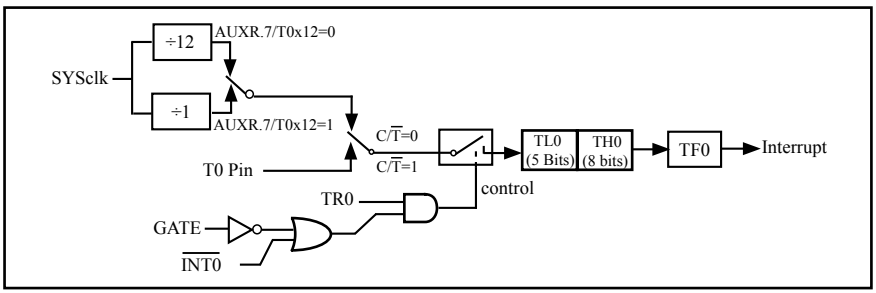
7.1 Timer/Counter 0 Mode of Operation

Mode 0

In this mode, the timer register is configured as a 13-bit register. As the count rolls over from all 1s to all 0s, it sets the timer interrupt flag TF0. The counted input is enabled to the timer when TR0 = 1 and either GATE=0 or $\overline{INT0}$ = 1.(Setting GATE = 1 allows the Timer to be controlled by external input $\overline{INT0}$, to facilitate pulse width measurements.) TR0 is a control bit in the Special Function Register TCON. GATE is in TMOD.

The 13-Bit register consists of all 8 bits of TH0 and the lower 5 bits of TL0. The upper 3 bits of TL0 are indeterminate and should be ignored. Setting the run flag (TR0) does not clear the registers.

There are two different GATE bits. one for Timer 1 (TMOD.7) and one for Timer 0 (TMOD.3).



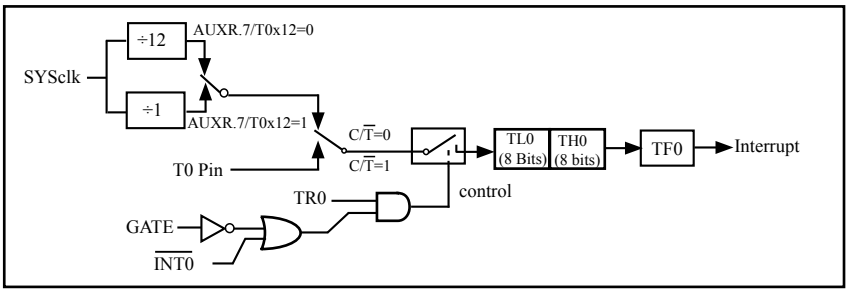
Timer/Counter 0 Mode 0: 13-Bit Counter

Mode 1

In this mode, the timer register is configured as a 16-bit register. As the count rolls over from all 1s to all 0s, it sets the timer interrupt flag TF0. The counted input is enabled to the timer when TR0 = 1 and either GATE=0 or $\overline{\text{INT0}}$ = 1.(Setting GATE = 1 allows the Timer to be controlled by external input $\overline{\text{INT0}}$, to facilitate pulse width measurements.) TR0 is a control bit in the Special Function Register TCON. GATE is in TMOD.

The 16-Bit register consists of all 8 bits of TH0 and the lower 8 bits of TL0. Setting the run flag (TR0) does not clear the registers.

Mode 1 is the same as Mode 0, except that the timer register is being run with all 16 bits.



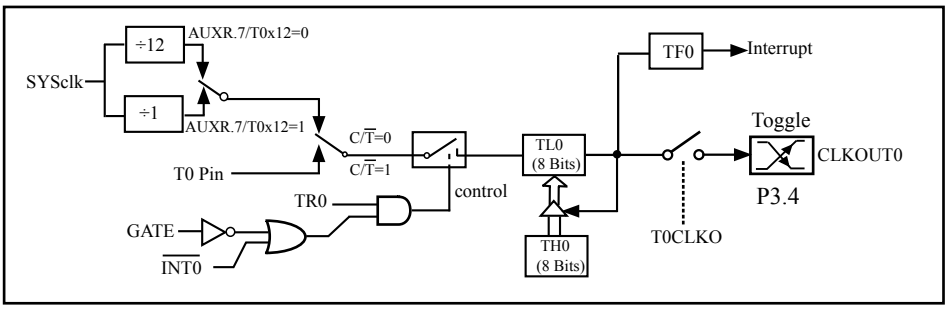
Timer/Counter 0 Mode 1 : 16-Bit Counter

Mode 2

Mode 2 configures the timer register as an 8-bit counter(TL0) with automatic reload. Overflow from TL0 not only set TF0, but also reload TL0 with the content of TH0, which is preset by software. The reload leaves TH0 unchanged.

STC12C5A60S2 is able to generate a programmable clock output on P3.4. When T0CLKO bit in WAKE_CLKO SFR is set, T0 timer overflow pulse will toggle P3.4 latch to generate a 50% duty clock. The frequency of clock-out is as following :

(SYSclk/2) / (256 – TH0), when T0x12=1
or **(SYSclk/2/12) / (256 – TH0) , when T0x1=0**

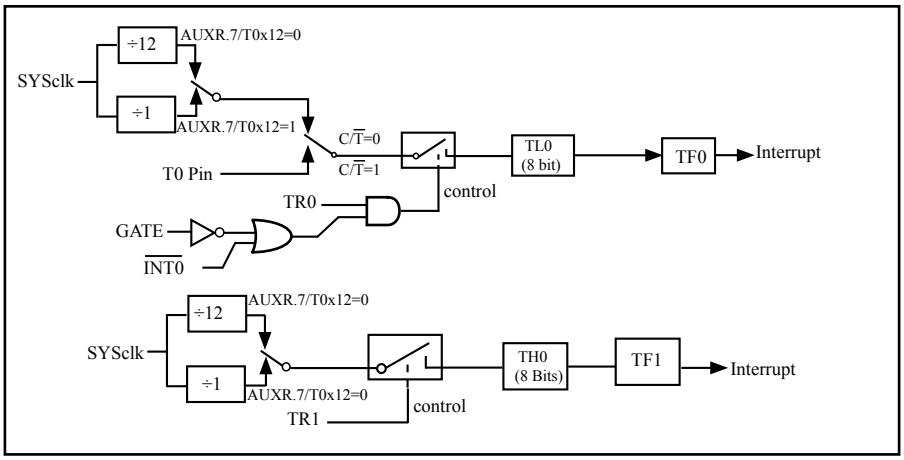


Timer/Counter 0 Mode 2: 8-Bit Auto-Reload

Mode 3

Timer 1 in Mode 3 simply holds its count, the effect is the same as setting TR1 = 0. Timer 0 in Mode 3 established TL0 and TH0 as two separate 8-bit counters. TL0 use the Timer 0 control bits: $C/\overline{T}$,GATE,TR0, $\overline{INT0}$ and TF0. TH0 is locked into a timer function (counting machine cycles) and takes over the use of TR1 from Tmer 1. Thus, TH0 now controls the "Timer 1" interrupt.

Mode 3 is provided for applications requiring an extra 8-bit timer or counter. When Timer 0 is in Mode 3, Timer 1 can be turned on and off by switching it out of and into its own Mode 3, or can still be used by the serial port as a baud rate generator, or in fact, in any application not requiring an interrupt.



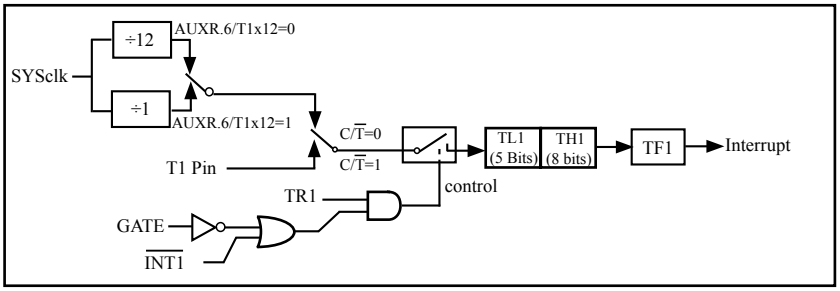
Timer/Counter 0 Mode 3: Two 8-Bit Counters

7.2 Timer/Counter 1 Mode of Operation

Mode 0

In this mode, the timer register is configured as a 13-bit register. As the count rolls over from all 1s to all 0s, it sets the timer interrupt flag TF1. The counted input is enabled to the timer when TR1 = 1 and either GATE=0 or $\overline{INT1}$ = 1.(Setting GATE = 1 allows the Timer to be controlled by external input $\overline{INT1}$, to facilitate pulse width measurements.) TR0 is a control bit in the Special Function Register TCON. GATE is in TMOD.

The 13-Bit register consists of all 8 bits of TH1 and the lower 5 bits of TL1. The upper 3 bits of TL1 are indeterminate and should be ignored. Setting the run flag (TR1) does not clear the registers.



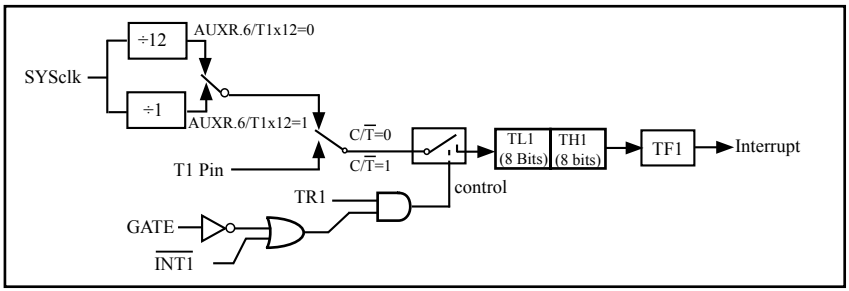
Timer/Counter 1 Mode 0: 13-Bit Counter

Mode 1

In this mode, the timer register is configured as a 16-bit register. As the count rolls over from all 1s to all 0s, it sets the timer interrupt flag TF1. The counted input is enabled to the timer when TR1 = 1 and either GATE=0 or $\overline{INT1}$ = 1.(Setting GATE = 1 allows the Timer to be controlled by external input $\overline{INT1}$, to facilitate pulse width measurements.) TRl is a control bit in the Special Function Register TCON. GATE is in TMOD.

The 16-Bit register consists of all 8 bits of THl and the lower 8 bits of TL1. Setting the run flag (TR1) does not clear the registers.

Mode 1 is the same as Mode 0, except that the timer register is being run with all 16 bits.



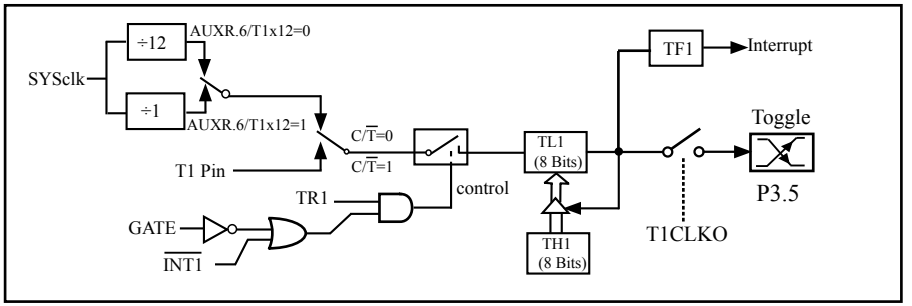
Timer/Counter 1 Mode 1 : 16-Bit Counter

Mode 2

Mode 2 configures the timer register as an 8-bit counter(TL1) with automatic reload. Overflow from TL1 not only set TFx, but also reload TL1 with the content of TH1, which is preset by software. The reload leaves TH1 unchanged.

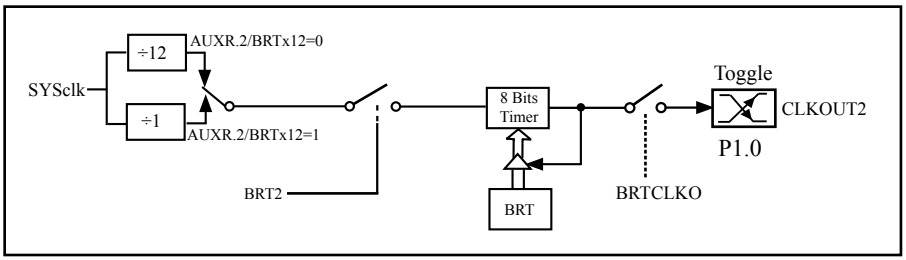
STC11/10Fxx series is able to generate a programmable clock output on P3.5. When T0CLKO bit in WAKE_CLKO SFR is set, T1 timer overflow pulse will toggle P3.5 latch to generate a 50% duty clock. The frequency of clock-out is as following :

(SYSclk/2) / (256 – TH1), when T1x12=1
or **(SYSclk/2/12) / (256 – TH1) , when T1x1=0**



Timer/Counter 1 Mode 2: 8-Bit Auto-Reload

7.3 Baud Rate Generator and Programmable Clock Output on P1.0



STC11/10Fxx series are able to generate a programmable clock output on P1.0. When BRTCLKO bit in WAKE_CLKO is set, BRT timer overflow pulse will toggle P1.0 latch to generate a 50% duty clock. The frequency of clock-out is as following :

(SYSclk/2) / (256 –BRT), when BRTx12=1

or **(SYSclk/2/12) / (256 – BRT) , when BRTx1=0**

Chapter 8. UART with enhanced function

The serial port is full duplex,meaning it can transmit and receive simultaneously. It is also receive-buffered, meaning it can commence reception of a second byte before a previously received byte has been read from the reeeive register. (However,if the first byte still hasn't been read by the time reception of the second byte is complete, one of the bytes will be lost). The serial port receive and transmit share the same SFR – SBUF, but actually there is two SBUF in the chip, one is for transmit and the other is for receive. The serial port can be operated in 4 different modes.

Symbol	Description	Address	Bit Address and Symbol MSB LSB								Value after Power-on or Reset
BRT	Baud-Rate Timer	9CH									0000 0000B
AUXR	Auxiliary register	8EH	T0x12	T1x12	UART_M0x6	BRTR	-	BRTx12	XRAM	S1BRS	0000 0000B
SCON	Serial Control	98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI	0000 0000B
SBUF	Serial Buffer	99H									xxxx xxxxB
PCON	Power Control	87H	SMOD	SMOD0	LVDF	POF	GF1	GF0	PD	IDL	0001 0000B
IE	Interrupt Enable	A8H	EA	ELVD	-	ES	ET1	EX1	ET0	EX0	0x00 0000B
IP	Interrupt Priority Low	B8H	-	PLVD	-	PS	PT1	PX1	PT0	PX0	0000 0000B
SADEN	Slave Address Mask	B9H									0000 0000B
SADDR	Slave Address	A9H									0000 0000B
TCON	Timer Control	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	0000 0000B
TMOD	Timer Mode	89H	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0	0000 0000B
TL1	Timer Low 1	8BH									0000 0000B
TH1	Timer High 1	8DH									0000 0000B
AUXR1	Auxiliary register1	A2H	UART_P1	-	-	-	GF2	-	-	DPS	0xxx 0xx0B
WAKE_CLKO	CLK_Output Power down Wake-up control register	8FH	-	RXD_PIN_IE	T1_PIN_IE	T0_PIN_IE	-	BRTCLKO	T1CLKO	T0CLKO	0000 0000B

SCON register

LSB

bit	7	6	5	4	3	2	1	0
name	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI

FE: Framing Error bit. The SMOD0 bit must be set to enable access to the FE bit
0: The FE bit is not cleared by valid frames but should be cleared by software.
1: This bit set by the receiver when an invalid stop bit id detected.

SM0,SM1 : Serial Port Mode Bit 0/1.

SM0	SM1	Description	Baud rate
0	0	8-bit shift register	SYSclk/12
0	1	8-bit UART	variable
1	0	9-bit UART	SYSclk/64 or SYSclk/32(SMOD=1)
1	1	9-bit UART	variable

SM2 : Enable the automatic address recognition feature in mode 2 and 3. If SM2=1, RI will not be set unless the received 9th data bit is 1, indicating an address, and the received byte is a Given or Broadcast address. In mode1, if SM2=1 then RI will not be set unless a valid stop Bit was received, and the received byte is a Given or Broadcast address. In mode 0, SM2 should be 0.
REN : When set enables serial reception.
TB8 : The 9th data bit which will be transmitted in mode 2 and 3.
RB8 : In mode 2 and 3, the received 9th data bit will go into this bit.
TI : Transmit interrupt flag.
RI : Receive interrupt flag.

SBUF register

LSB

bit	7	6	5	4	3	2	1	0
name								

It is used as the buffer register in transmission and reception.

BRT register

LSB

bit	7	6	5	4	3	2	1	0
name								

It is used as the reload register for generating the baud-rate of the secondary UART.

PCON: Power Control register

LSB

bit	7	6	5	4	3	2	1	0
name	SMOD	SMOD0	LVDF	POF	GF1	GF0	PD	IDL

SMOD: double Baud rate control bit.
0 : Disable double Baud rate of the UART.
1 : Enable double Baud rate of the UART in mode 1,2,or 3.
SMOD0: Frame Error select.
0 : SCON.7 is SM0 function.
1 : SCON.7 is FE function. Note that FE will be set after a frame error regardless of the state of SMOD0.

AUXR register

LSB

bit	B7	B6	B5	B4	B3	B2	B1	B0
name	T0x12	T1x12	UART_M0x6	BRTR	-	BRTx12	XRAM	S1BRS

T1x12

0 : The clock source of Timer 1 is SYSclk/12.

1 : The clock source of Timer 1 is SYSclk/1.

UART_M0x6 : Serial Port mode 0 baud rate selector.

0 : Clear to select SYSclk/12 as the baud rate for UART Mode 0.

1 : Set to select SYSclk/2 as the baud rate for UART Mode 0.

BRTR: Independent Baud-rate generator control bit.

0 : The independent baud-rate generator is stoped

1 : The independent baud-rate generator is stoped

BRTx12

0 : The independent baud-rate is incremented every 12 system clocks.

1 : The independent baud-rate is incremented every system clock.

S1BRS

0 : select Timer 1 as the baud-rate generator of the enhanced UART .

1 : Timer 1 is replaced by the independent baud-rate generator for use of the enhanced UART. In other word, time1 is released to use in other functions.

SADEN: Slave Address Mask register

LSB

bit	B7	B6	B5	B4	B3	B2	B1	B0
name								

SADDR: Slave Address register

LSB

bit	B7	B6	B5	B4	B3	B2	B1	B0
name								

SADDR register is combined with SADEN register to form Given/Broadcast Address for automatic address recognition. In fact, SADEN function as the "mask" register for SADDR register. The following is the example for it.

SADDR = 1100 0000

SADEN = 1111 1101

Given = 1100 00x0 ⟶ The Given slave address will be checked except bit 1 is treated as "don't care".

The Broadcast Address for each slave is created by taking the logical OR of SADDR and SADEN. Zero in this result is considered as "don't care" and a Broad cast Address of all " don't care". This disables the automatic address detection feature.

AUXR1 register

LSB

bit	B7	B6	B5	B4	B3	B2	B1	B0
name	UART_P1	-	-	-	GF2	-	-	DPS

UART_P1

0 : UART on Port 3(RXD/P3.0, TXD/P3.1).

1 : UART on Port 1(RXD/P1.6,TXD/P1.7).

GF2 : General Flag. It can be used by software.

DPS

0 : DPTR0 is selected(Default).

1 : The secondary DPTR(DPTR1) is switched to use.

WAKE_CLKO register

bit	B7	B6	B5	B4	B3	B2	B1	B0
name	-	RXD_PIN_IE	T1_PIN_IE	T0_PIN_IE	-	BRTCKLO	T1CKLO	T0CKLO

RXD_PIN_IE :When set and the associated-UART interrupt control registers is configured correctly, the RXD pin (P3.0) is enabled to wake up MCU from power-down state.

T1_PIN_IE :When set and the associated-Timer1 interrupt control registers is configured correctly, the T1 pin (P3.5) is enabled to wake up MCU from power-down state.

T0_PIN_IE :When set and the associated-Timer0 interrupt control registers is configured correctly, the T1 pin (P3.4) is enabled to wake up MCU from power-down state.

BRTCKLO : When set, P1.0 is enabled to be the clock output of Baud-Rate Timer (BRT). The clock rate is BRG overflow rate divided by 2.

T1CKLO : When set, P3.5 is enabled to be the clock output of Timer 1. The clock rate is Timer 1overflow rate divided by 2.

T0CKLO : When set, P3.4 is enabled to be the clock output of Timer 0. The clock rate is Timer 0overflow rate divided by 2.

8.1 UART Mode of Operation

Mode 0

Serial data enters and exits through RXD. TXD outputs the shift clock. Eight data bits are transmitted/ received with the LSB first. The baud rate is fixed at 1/12 the System clock cycle in the default state. If AUXR.5(UART_M0x6) is set, the baud rate is 1/2 System clock cycle.

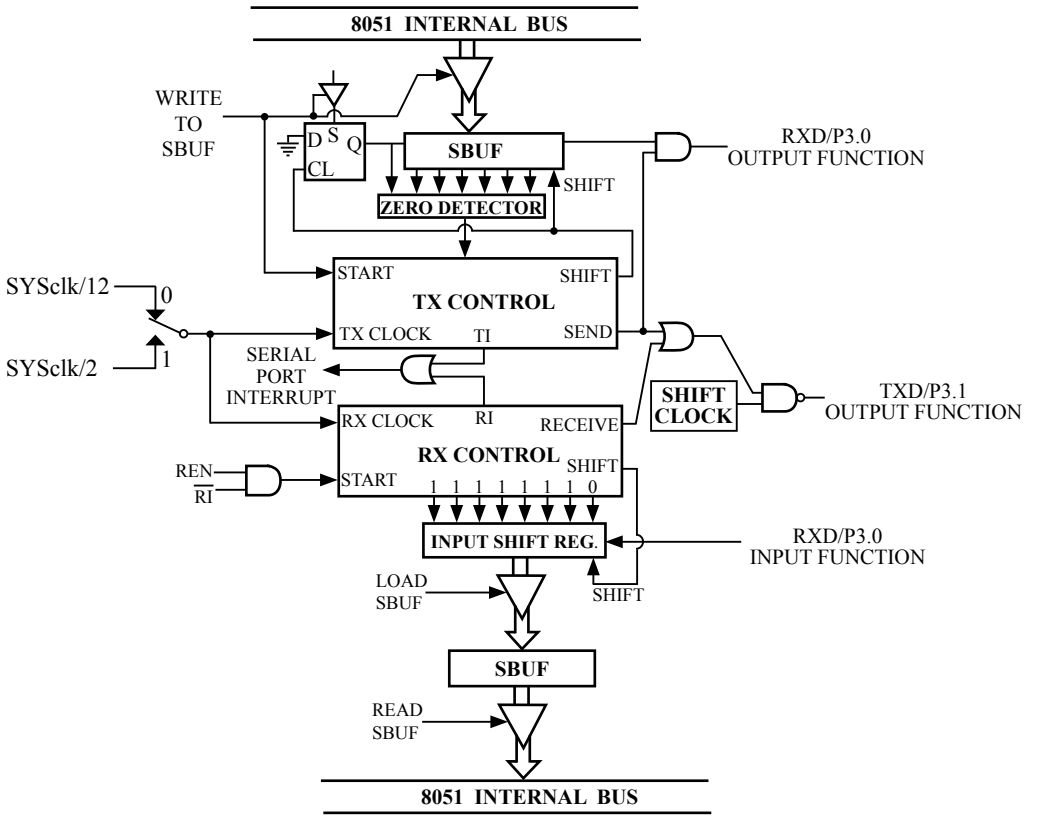
Transmission is initiated by any instruction that uses SBUF as a destination register. The “write to SBUF” signal also loads a “1” into the 9th position of the transmit shift register and tells the TX Control block to commence a transmission. The internal timing is such that one full system clock cycle will elapse between "write to SBUF," and activation of SEND.

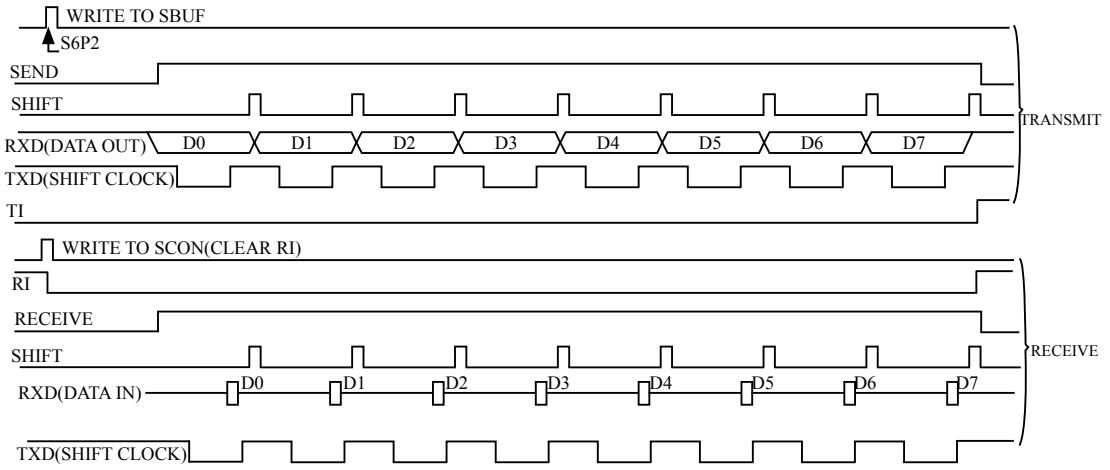
SEND transfers the output of the shift register to the alternate output function line of P3.0, and also transfers Shift Clock to the alternate output function line of P3.1. At the falling edge of the Shift Clock, the contents of the shift register are shifted one position to the right.

As data bits shift out to the right, “0” come in from the left. When the MSB of the data byte is at the output position of the shift register, then the “1” that was initially loaded into the 9th position is just to the left of the MSB, and all positions to the left of that contains zeroes. This condition flags the TX Control block to do one last shift and then deactivate SEND and set TI. Both of these actions occur after "write to SBUF".

Reception is initiated by the condition REN=1 and RI=0. After that, the RX Control unit writes the bits 11111110 to the receive shift register, and in the next clock phase activates RECEIVE. RECEIVE enables SHIFT CLOCK to the alternate output function line of P3.1.At RECEIVE is active, the contents of the receive shift register are shifted to the left one position. The value that comes in from the right is the value that was sampled at the P3.0 pin the rising edge of Shift clock.

As data bits come in from the right, “1”s shift out to the left. When the “0” that was initially loaded into the right-most position arrives at the left-most position in the shift register, it flags the RX Control block to do one last shift and load SBUF. Then RECEIVE is cleared and RI is set.





Serial Port Mode 0

Mode 1

10 bits are transmitted through TXD or received through RXD. The frame data includes a start bit(0), 8 data bits and a stop bit(1). One receive, the stop bit goes into RB8 in SFR – SCON. The baud rate is determined by the Timer 1 or BRT overflow rate.

Baud rate in mode 1 = $(2^{SMOD}/32)$ x timer 1 overflow rate (if AUXR.0/S1BRS=0)
= $(2^{SMOD}/32)$ x BRT overflow rate (if AUXR.0/S1BRS=1)

Transmission is initiated by any instruction that uses SBUF as a destination register. The "write to SBUF" signal also loads a "1" into the 9th bit position of the transmit shift register and flags the TX Control unit that a transmission is requested. Transmission actually happens at the next rollover of divided-by-16 counter. Thus the bit times are synchronized to the divided-by-16 counter, not to the "write to SBUF" signal.

The transmission begins with activation of $\overline{SEND}$, which puts the start bit at TXD. One bit time later, DATA is activated, which enables the output bit of the transmit shift register to TXD. The first shift pulse occurs one bit time after that.

As data bits shift out to the right, zeroes are clocked in from the left. When the MSB of the data byte is at the output position of the shift register, then the 1 that was initially loaded into the 9th position is just to the left of the MSB, and all positions to the left of that contain zeroes. This condition flags the TX Control unit to do one last shift and then deactivate $\overline{SEND}$ and set TI. This occurs at the 10th divide-by-16 rollover after "write to SBUF."

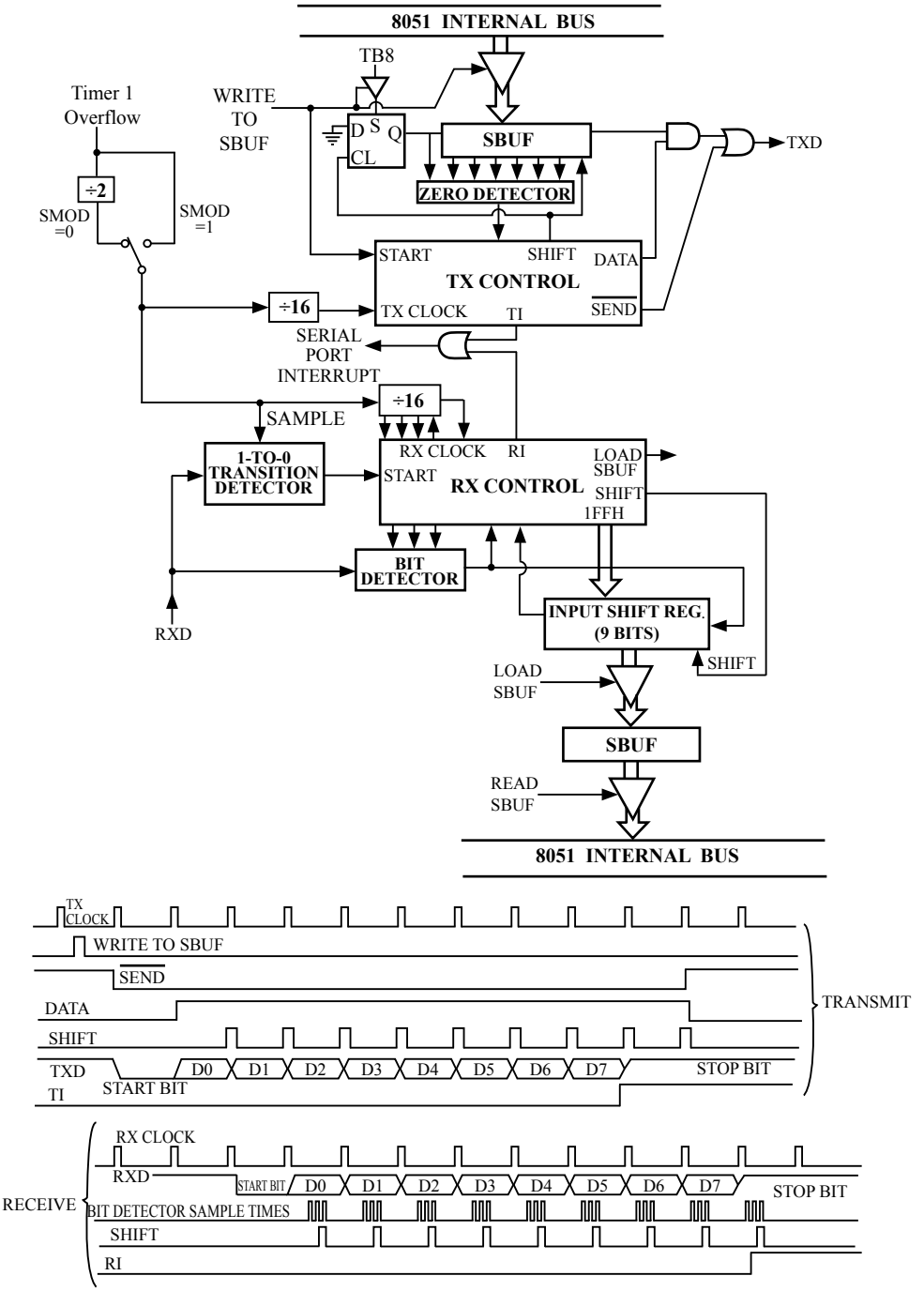
Reception is initiated by a 1-to-0 transition detected at RXD. For this purpose, RXD is sampled at a rate of 16 times the established baud rate. When a transition is detected, the divided-by-16 counter is immediately reset, and 1FFH is written into the input shift register. Resetting the divided-by-16 counter aligns its roll-overs with the boundaries of the incoming bit times.

The 16 states of the counter divide each bit time into 16ths. At the 7th, 8th and 9th counter states of each bit time, the bit detector samples the value of RXD. The value accepted is the value that was seen in at least 2 of the 3 samples. This is done to reject noise. In order to reject false bits, if the value accepted during the first bit time is not a 0, the receive circuits are reset and the unit continues looking for another 1-to-0 transition. This is to provide rejection of false start bits. If the start bit is valid, it is shifted into the input shift register, and reception of the rest of the frame proceeds.

As data bits come in from the right, "1"s shift out to the left. When the start bit arrives at the left most position in the shift register,(which is a 9-bit register in Mode 1), it flags the RX Control block to do one last shift, load SBUF and RB8, and set RI. The signal to load SBUF and RB8 and to set RI is generated if, and only if, the following conditions are met at the time the final shift pulse is generated.

1) RI=0 and
2) Either SM2=0, or the received stop bit = 1

If either of these two conditions is not met, the received frame is irretrievably lost. If both conditions are met, the stop bit goes into RB8, the 8 data bits go into SBUF, and RI is activated. At this time, whether or not the above conditions are met, the unit continues looking for a 1-to-0 transition in RXD.



Serial Port Mode 1

Mode 2

11 bits are transmitted through TXD or received through RXD. The frame data includes a start bit(0), 8 data bits, a programmable 9th data bit and a stop bit(1). On transmit, the 9th data bit comes from TB8 in SCON. On receive, the 9th data bit goes into RB8 in SCON. The baud rate is programmable to either 1/32 or 1/64 the System clock cycle.

Baud rate in mode 2 = $(2^{SMOD}/64)$ x SYSclk

Transmission is initiated by any instruction that uses SBUF as a destination register. The "write to SBUF" signal also loads TB8 into the 9th bit position of the transmit shift register and flags the TX Control unit that a transmission is requested. Transmission actually happens at the next rollover of divided-by-16 counter. Thus the bit times are synchronized to the divided-by-16 counter, not to the "write to SBUF" signal.

The transmission begins when /SEND is activated, which puts the start bit at TXD. One bit time later, DATA is activated, which enables the output bit of the transmit shift register to TXD. The first shift pulse occurs one bit time after that. The first shift clocks a "1"(the stop bit) into the 9th bit position on the shift register. Thereafter, only "0"s are clocked in. As data bits shift out to the right, "0"s are clocked in from the left. When TB8 of the data byte is at the output position of the shift register, then the stop bit is just to the left of TB8, and all positions to the left of that contains "0"s. This condition flags the TX Control unit to do one last shift, then deactivate /SEND and set TI. This occurs at the 11th divided-by-16 rollover after "write to SBUF".

Reception is initiated by a 1-to-0 transition detected at RXD. For this purpose, RXD is sampled at a rate of 16 times whatever baud rate has been estabished. When a transition is detected, the divided-by-16 counter is immediately reset, and 1FFH is written into the input shift register.

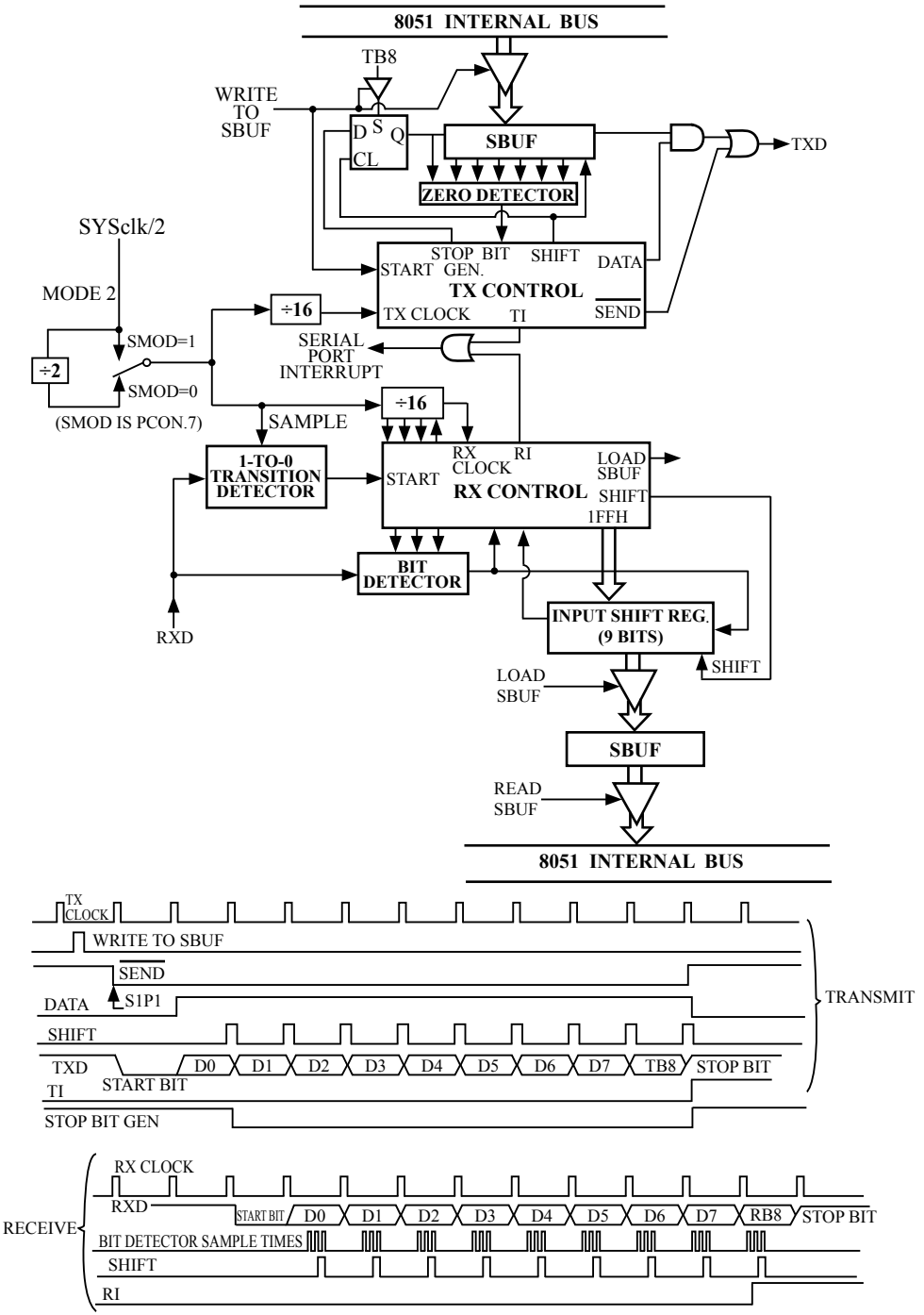
At the 7th, 8th and 9th counter states of each bit time, the bit detector samples the value of RXD. The value accepted is the value that was seen in at least 2 of the 3 samples. This is done to reject noise. In order to reject false bits, if the value accepted during the first bit time is not a 0, the receive circuits are reset and the unit continues looking for another 1-to-0 transition. If the start bit is valid, it is shifted into the input shift register, and reception of the rest of the frame proceeds.

As data bits come in from the right, "1"s shift out to the left. When the start bit arrives at the leftmost position in the shift register,(which is a 9-bit register in Mode-2 and 3), it flags the RX Control block to do one last shift, load SBUF and RB8, and set RI. The signal to load SBUF and RB8 and to set RI is generated if, and only if, the following conditions are met at the time the final shift pulse is generated.:

1) RI=0 and
2) Either SM2=0, or the received 9th data bit = 1

If either of these two conditions is not met, the received frame is irretrievably lost. If both conditions are met, the stop bit goes into RB8, the first 8 data bits go into SBUF, and RI is activated. At this time, whether or not the above conditions are met, the unit continues looking for a 1-to-0 transition at the RXD input.

Note that the value of received stop bit is irrelevant to SBUF, RB8 or RI.



Serial Port Mode 2

Mode 3

Mode 3 is the same as mode 2 except the baud rate is variable.

$$\text{Baud rate in mode 3} = (2^{SMOD}/32) \times \text{timer 1overflow rate} \quad (\text{if AUXR.0/S1BRS=0})$$
$$= (2^{SMOD}/32) \times \text{BRT overflow rate} \quad (\text{if AUXR.0/S1BRS=1})$$

In all four modes, transmission is initiated by any instruction that use SBUF as a destination register. Reception is initiated in mode 0 by the condition RI = 0 and REN = 1. Reception is initiated in the other modes by the incoming start bit with 1-to-0 transition if REN=1.

8.2 Frame Error Detection

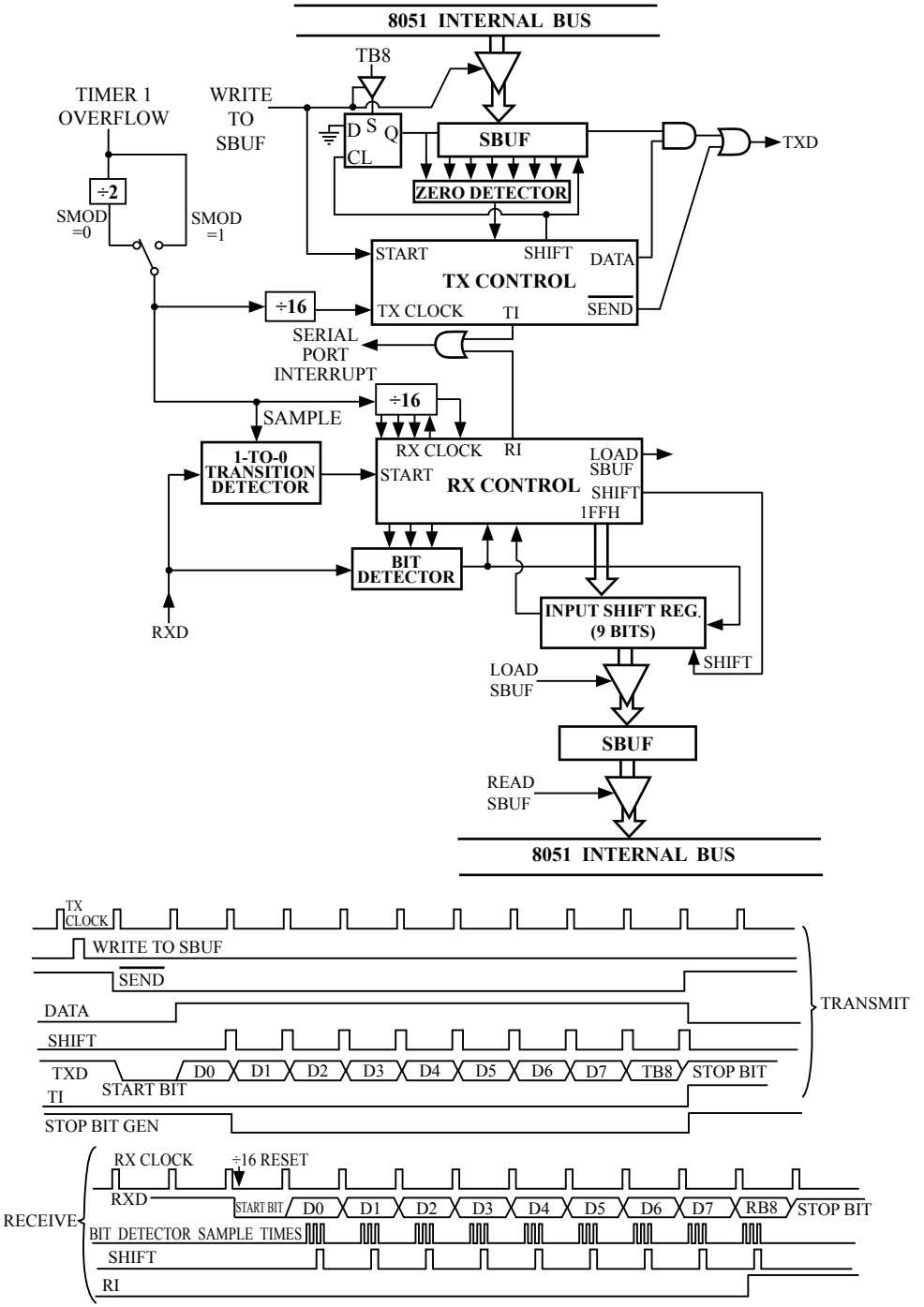
When used for frame error detect, the UART looks for missing stop bits in the communication. A missing bit will set the FE bit in the SCON register. The FE bit shares the SCON.7 bit with SM0 and the function of SCON.7 is determined by PCON.6(SMOD0). If SMOD0 is set then SCON.7 functions as FE. SCON.7 functions as SM0 when SMOD0 is cleared. When used as FE, SCON.7 can only be cleared by software.

8.3 Multiprocessor Communications

Modes 2 and 3 have a special provision for multiproceasor communications. In these modes 9 data bits are received.The 9th one goes into RB8. Then comes a stop bit. The port can be programmed such that when the stop bit is received,the serial port interrupt will be activated only if RB8 = 1. This feature is enabled by setting bit SM2 in SCON. A way to use this feature in multiprocessor systems is as follows.

When the master processor wants to transmit a block of data to one of several slaves, it first sends out an address byte which identifies the target slave.An address byte differs from a data byte in that the 9th bit is 1 in an address byte and 0 in a data byte.With SM2 = 1, no slave will be interrupted by a data byte. An address byte, however,will interrupt all slaves, so that each slave can examine the received byte and see if it is being addressed.The addressed slave will clear its SM2 bit and prepare to receive the data bytes that will be coming. The slaves that weren't being addressed leave their SM2s set and go on about their business, ignoring the coming data bytes.

SM2 has no effect in Mode 0,and in Mode 1 can be used to check the validity of the stop bit. In a Mode 1 reception, if SM2 = 1, the receive interrupt will not be activated unless a vatid stop bit is received.



Serial Port Mode 3

8.4 Automatic Address Recognition

Automatic Address Recognition is a future which allows the UART to recognize certain addresses in the serial bit stream by using hardware to make the comparisons. This feature saves a great deal of software overhead by eliminating the need for the software to examine every serial address which passes by the serial port. This feature is enabled by setting the SM2 bit in SCON. In the 9-bit UART modes, Mode 2 and Mode 3, the Receive interrupt flag(RI) will be automatically set when the received byte contains either the "Given" address or the "Broadcast" address. The 9-bit mode requires that the 9th information bit is a "1" to indicate that the received information is an address and not data.

The 8-bit mode is called Mode 1. In this mode the RI flag will be set if SM2 is enabled and the information received has a valid stop bit following the 8 address bits and the information is either a Given or Broadcast address.

Mode 0 is the Shift Register mode and SM2 is ignored.

Using the Automatic Address Recognition feature allows a master to selectively communicate with one or more slaves by invoking the given slave address or addresses. All of the slaves may be contacted by using the broadcast address. Two special function registers are used to define the slave's address, SADDR, and the address mask, SADEN. SADEN is used to define which bits in the SADDR are to be used and which bits are "don't care". The SADEN mask can be logically ANDed with the SADDR to create the "Given" address which the master will use for addressing each of the slaves. Use of the Given address allows multiple slaves to be recognized which excluding others. The following examples will help to show the versatility of this scheme :

Slave 0 SADDR = 1100 0000
SADEN = 1111 1101
GIVEN = 1100 00x0

Slave 1 SADDR = 1100 0000
SADEN = 1111 1110
GIVEN = 1100 000x

In the previous example SADDR is the same and the SADEN data is used to differentiate between the two slaves. Slave 0 requires a "0" in bit 0 and it ignores bit 1. Slave 1 requires a "0" in bit 1 and bit 0 is ignored. A unique address for slave 0 would be 11000010 since slave 1 requires a "0" in bit 1. A unique address for slave 1 would be 11000001 since a "1" in bit 0 will exclude slave 0. Both slaves can be selected at the same time by an address which has bit 0=0 (for slave 0) and bit 1 =0 (for salve 1). Thus, both could be addressed with 11000000.

In a more complex system the following could be used to select slaves 1 and 2 while excluding slave 0:

Slave 0 SADDR = 1100 0000
SADEN = 1111 1001
GIVEN = 1100 0xx0

Slave 1 SADDR = 1110 0000
SADEN = 1111 1010
GIVEN = 1110 0x0x

Slave 2 SADDR = 1110 0000
SADEN = 1111 1100
GIVEN = 1110 00xx

In the above example the differentiation among the 3 slaves is in the lower 3 address bits.Slave 0 requires that bit0 = 0 and it can be uniquely addressed by 11100110. Slave 1 requires that bit 1=0 and it can be uniquely addressed by 11100101. Slave 2 requires that bit 2=0 and its unique address is 11100011. To select Salve 0 and 1 and exclude Slave 2, use address 11100100, since it is necessary to make bit2=1 to exclude Slave 2.

The Broadcast Address for each slave is created by taking the logic OR of SADDR and SADEN. Zeros in this result are trended as don't cares. In most cares, interpreting the don't cares as ones, the broadcast address will be FF hexadecimal.

Upon reset SADDR and SADEN are loaded with "0"s. This produces a given address of all "don't cares as well as a Broadcast address of all "don't cares". This effectively disables the Automatic Addressing mode and allows the microcontroller to use standard 80C51-type UART drivers which do not make use of this feature.

8.5 Buad Rates

The baud rate in Mode 0 is fixed:

$$\text{Mode 0 Baud Rate} = \frac{\text{SYSclk}}{12} \quad \text{when AUXR.5/UART\_M0x6 =0}$$

$$\text{or} = \frac{\text{SYSclk}}{2} \quad \text{when AUXR.5/UART\_M0x6 =1}$$

The baud rate in Mode 2 depends on the value of bit SMOD in Special Function Register PCON. If SMOD =0 (which is the value on reset), the baud rate $^1/_{64}$ the System clock cycle. If SMOD = 1, the baud rate is $^1/_{32}$ the System clock cycle .

$$\text{Mode 2 Baud Rate} = \frac{2^{SMOD}}{64} \times (\text{SYSclk})$$

In the STC11F60XE, the baud rates in Modes 1 and 3 are determined by Timer1 or BRT overflow rate.
The baud rate in Mode 1 and 3 are fixed:

Mode 1,3 Baud rate = $(2^{SMOD}/32)$ x timer 1 overflow rate (if AUXR.0/S1BRS=0)
= $(2^{SMOD}/32)$ x BRT overflow rate (if AUXR.0/S1BRS=1)

Timer 1 overflow rate = (SYSclk/12)/(256 - TH1);
BRT overflow rate = (SYSclk/2) / (256 –BRT), when AUXR.2/BRTx12=1
or = (SYSclk/2/12) / (256 – BRT) , when AUXR.2/BRTx12=0

When Timer 1 is used as the baud rate generator, the Timer 1 interrupt should be disabled in this application. The Timer itself can be configured for either "timer" or "cormter" operation, and in any of its 3 running modes. In the most typcial applications, it is configured for "timer" operation, in the auto-reload mode (high nibble of TMOD = 0010B).
One can achieve very low baud rate with Timer 1 by leaving the Timer 1 interrupt enabled, and configuring the Timer to run as a 16-bit timer (high nibble of TMOD = 0001B), and using the Timer 1 interrupt to do a l6-bit software reload.

The following figure lists various commonly used baud rates and how they can be obtained from Timer 1.

Baud Rate	SYSclk	SMOD	Timer 1		
			C/$\overline{T}$	Mode	Reload Value
Mode 0 MAX:1MHZ	12MHZ	X	X	X	X
Mode 2 MAX:375K	12MHZ	1	X	X	X
Mode 1,3:62.5K	12MHZ	1	0	2	FFH
19.2K	11.059MHZ	1	0	2	FDH
9.6K	11.059MHZ	0	0	2	FDH
4.8K	11.059MHZ	0	0	2	FAH
2.4K	11.059MHZ	0	0	2	F4H
1.2K	11.059MHZ	0	0	2	E8H
137.5	11.986MHZ	0	0	2	1DH
110	6MHZ	0	0	2	72H
110	12MHZ	0	0	1	FEEBH

Timer 1 Generated Commonly Used Baud Rates

Chapter 9 IAP / EEPROM

The ISP in STC11Fxx/10xx series makes it possible to update the user's application program and non-volatile application data (in IAP-memory) without removing the MCU chip from the actual end product. This useful capability makes a wide range of field-update applications possible. (Note ISP needs the loader program pre-programmed in the ISP-memory.) In general, the user needn't know how ISP operates because STC has provided the standard ISP tool and embedded ISP code in STC shipped samples.

IAP / ISP Control Register

The following special function registers are related to the IAP/ISP operation. All these registers can be accessed by software in the user's application program.

Symbol	Description	Address	Bit Address and Symbol MSB LSB								Value after Power-on or Reset
IAP_DATA	ISP/IAP Flash Data Register	C2H									1111 1111B
IAP_ADDRH	ISP/IAP Flash Address High	C3H									0000 0000B
IAP_ADDRL	ISP/IAP Flash Address Low	C4H									0000 0000B
IAP_CMD	ISP/IAP Flash Command Register	C5H	-	-	-	-	-	-	MS1	MS0	xxxx x000B
IAP_TRIG	ISP/IAP Flash Command Trigger	C6H									xxxx xxxxB
IAP_CONTR	ISP/IAP Control Register	C7H	IAPEN	SWBS	SWRST	CMD_FAIL	-	WT2	WT1	WT0	0000 x000B
PCON	Power Control	87H	SMOD	SMOD0	LVDF	POF	GF1	GF0	PD	IDL	0011 0000B

IAP_DATA: ISP/IAP Flash Data Register

LSB

bit	B7	B6	B5	B4	B3	B2	B1	B0
name								

IAP_DATA is the data port register for ISP/IAP operation. The data in IAP_DATA will be written into the desired address in operating ISP/IAP write and it is the data window of readout in operating ISP/IAP read.

IAP_ADDRH: ISP/IAP Flash Address High

LSB

bit	B7	B6	B5	B4	B3	B2	B1	B0
name								

IAP_ADDRH is the high-byte address port for all ISP/IAP modes.

IAP_ADDRL: ISP/IAP Flash Address Low

LSB

bit	B7	B6	B5	B4	B3	B2	B1	B0
name								

IAP_ADDRL is the low port for all ISP/IAP modes. In page erase operation, it is ignored.

IAP_CMD: ISP/IAP Flash Command Register

LSB

bit	B7	B6	B5	B4	B3	B2	B1	B0
name	-	-	-	-	-	-	MS1	MS0

B7~B2: Reserved.

MS1, MS0 : ISP/IAP operating mode selection. IAP_CMD is used to select the flash mode for performing numerous ISP/IAP function or used to access protected SFRs.

0, 0 : Standby

0, 1 : Data Flash/EEPROM read.

1, 0 : Data Flash/EEPROM program.

1, 1 : Data Flash/EEPROM page erase.

IAP_TRIG: ISP/IAP Flash Command Trigger.

LSB

bit	B7	B6	B5	B4	B3	B2	B1	B0
name								

IAP_TRIG is the command port for triggering ISP/IAP activity and protected SFRs access. If IAP_TRIG is filled with sequential 0x5Ah, 0xA5h and if IAPEN(IAP_CONTR.7) = 1, ISP/IAP activity or protected SFRs access will triggered.

IAP_CONTR: ISP/IAP Control Register

LSB

bit	B7	B6	B5	B4	B3	B2	B1	B0
name	IAPEN	SWBS	SWRST	CMD_FAIL	-	WT2	WT1	WT0

IAPEN : ISP/IAP operation enable.

0 : Global disable all ISP/IAP program/erase/read function.

1 : Enable ISP/IAP program/erase/read function.

SWBS: software boot selection control.

0 : Boot from main-memory after reset.

1 : Boot from ISP memory after reset.

SWRST: software reset trigger control.

0 : No operation

1 : Generate software system reset. It will be cleared by hardware automatically.

CMD_FAIL: Command Fail indication for ISP/IAP operation.

0 : The last ISP/IAP command has finished successfully.

1 : The last ISP/IAP command fails. It could be caused since the access of flash memory was inhibited.

B3: Reserved. Software must write “0” on this bit when IAP_CONTR is written.

WT2~WT0 : ISP/IAP programming clock source selection.

Setting wait times			CPU wait times			
WT2	WT1	WT0	Read	Program <=55uS	Sector Erase <=21mS	Recommended System Clock Frequency (MHz)
1	1	1	2 SYSclks	55 SYSclks	21012 SYSclks	< 1MHz
1	1	0	2 SYSclks	110 SYSclks	42024 SYSclks	< 2MHz
1	0	1	2 SYSclks	165 SYSclks	63036 SYSclks	< 3MHz
1	0	0	2 SYSclks	330 SYSclks	126072 SYSclks	< 6MHz
0	1	1	2 SYSclks	660 SYSclks	252144 SYSclks	< 12MHz
0	1	0	2 SYSclks	1100 SYSclks	420240 SYSclks	< 20MHz
0	0	1	2 SYSclks	1320 SYSclks	504288 SYSclks	< 24MHz
0	0	0	2 SYSclks	1760 SYSclks	672384 SYSclks	< 30MHz

STC11Fxx / STC11Lxx series MCU internal EEPROM Selection Table				
Type	**EEPROM (Byte)**	**Sector Numbers**	**Begin_Sector Begin_Address**	**End_Sector Ene_Address**
STC11F01E/STC11L01E	2K	4	0000H	0FFFH
STC11F02E/STC11L02E	2K	4	0000H	0FFFH
STC11F03E/STC11L03E	2K	4	0000H	0FFFH
STC11F04E/STC11L04E	1K	2	0000H	3FFH
STC11F05E/STC11L05E	1K	2	0000H	3FFH
STC11Fxx / STC11Lxx series MCU internal EEPROM Selection Table				
Type	**EEPROM (Byte)**	**Sector Numbers**	**Begin_Sector Begin_Address**	**End_Sector Ene_Address**
STC11F08XE/STC11L08XE	32K	64	0000H	7FFFH
STC11F16XE/STC11L16XE	32K	64	0000H	7FFFH
STC11F20XE/STC11L20XE	29K	58	0000H	73FFH
STC11F32XE/STC11L32XE	29K	58	0000H	73FFH
STC11F40XE/STC11L40XE	21K	42	0000H	53FFH
STC11F48XE/STC11L48XE	13K	26	0000H	33FFH
STC11F52XE/STC11L52XE	9K	18	0000H	23FFH
STC11F56XE/STC11L56XE	5K	10	0000H	13FFH
STC11F60XE/STC11L60XE	1K	2	0000H	3FFH
STC10Fxx / STC10Lxx series MCU internal EEPROM Selection Table				
Type	**EEPROM (Byte)**	**Sector Numbers**	**Begin_Sector Begin_Address**	**End_Sector Ene_Address**
STC10F02XE/STC10L02XE	5K	10	0000H	13FFH
STC10F04XE/STC10L04XE	5K	10	0000H	13FFH
STC10F06XE/STC10L06XE	5K	10	0000H	13FFH
STC10F08XE/STC10L08XE	5K	10	0000H	13FFH
STC10F10XE/STC10L10XE	3K	6	0000H	0BFFH
STC10F12XE/STC10L12XE	1K	2	0000H	3FFH

Chapter 10 STC10/11 xx series Selection Table

Type 1T 8051 MCU	Operating voltage (V)	Flash (B)	SARM (B)	TIMER	UART	PCA/ PWM D/A	A/D	WDT	EEPROM (B)	Internal low voltage interrupt	Internal Reset threshold voltage can be configured	External interrupts which can wake up power down mode	Special timer for waking power down mode	Package of 40-pin (36 I/O ports)	Package of 44-pin (40 I/O ports)
STC10F04	5.5~3.3	4K	256	2	1-2	N	N	Y	N	Y	Y	5	N	PDIP	LQFP/ PLCC
STC10F04XE	5.5~3.3	4K	512	2	1-2	N	N	Y	5K	Y	Y	5	N	PDIP	LQFP/ PLCC
STC10F06	5.5~3.3	6K	256	2	1-2	N	N	Y	N	Y	Y	5	N	PDIP	LQFP/ PLCC
STC10F06XE	5.5~3.3	6K	512	2	1-2	N	N	Y	5K	Y	Y	5	N	PDIP	LQFP/ PLCC
STC10F08	5.5~3.3	8K	256	2	1-2	N	N	Y	N	Y	Y	5	N	PDIP	LQFP/ PLCC
STC10F08XE	5.5~3.3	8K	512	2	1-2	N	N	Y	5K	Y	Y	5	N	PDIP	LQFP/ PLCC
STC10F10	5.5~3.3	10K	256	2	1-2	N	N	Y	N	Y	Y	5	N	PDIP	LQFP/ PLCC
STC10F10XE	5.5~3.3	10K	512	2	1-2	N	N	Y	3K	Y	Y	5	N	PDIP	LQFP/ PLCC
STC10F12	5.5~3.3	12K	256	2	1-2	N	N	Y	N	Y	Y	5	N	PDIP	LQFP/ PLCC
STC10F12XE	5.5~3.3	12K	512	2	1-2	N	N	Y	1K	Y	Y	5	N	PDIP	LQFP/ PLCC
STC10F14X	5.5~3.7	14K	512	2	1-2	N	N	Y	IAP	Y	Y	5	N	PDIP	LQFP/ PLCC
STC10L04	3.6~2.1	4K	256	2	1-2	N	N	Y	N	Y	Y	5	N	PDIP	LQFP/ PLCC
STC10L04XE	3.6~2.1	4K	512	2	1-2	N	N	Y	5K	Y	Y	5	N	PDIP	LQFP/ PLCC
STC10L06	3.6~2.1	6K	256	2	1-2	N	N	Y	N	Y	Y	5	N	PDIP	LQFP/ PLCC
STC10L06XE	3.6~2.1	6K	512	2	1-2	N	N	Y	5K	Y	Y	5	N	PDIP	LQFP/ PLCC
STC10L08	3.6~2.1	8K	256	2	1-2	N	N	Y	N	Y	Y	5	N	PDIP	LQFP/ PLCC
STC10L08XE	3.6~2.1	8K	512	2	1-2	N	N	Y	5K	Y	Y	5	N	PDIP	LQFP/ PLCC
STC10L10	3.6~2.1	10K	256	2	1-2	N	N	Y	N	Y	Y	5	N	PDIP	LQFP/ PLCC
STC10F10XE	3.6~2.1	10K	512	2	1-2	N	N	Y	3K	Y	Y	5	N	PDIP	LQFP/ PLCC
STC10L12	3.6~2.1	12K	256	2	1-2	N	N	Y	N	Y	Y	5	N	PDIP	LQFP/ PLCC
STC10L12XE	3.6~2.1	12K	512	2	1-2	N	N	Y	1K	Y	Y	5	N	PDIP	LQFP/ PLCC
STC10L14X	3.6~2.4	14K	512	2	1-2	N	N	Y	IAP	Y	Y	5	N	PDIP	LQFP/ PLCC

Type 1T 8051 MCU	Operating voltage (V)	Flash (B)	SARM (B)	TIMER	UART	PCA/ PWM D/A	A/D	WDT	EEPROM (B)	Internal low voltage interrupt	Internal Reset threshold voltage can be configured	External interrupts which can wake up power down mode	Special timer for waking power down mode	Package of 40-pin (36 I/O ports)	Package of 44-pin (40 I/O ports)
STC11F16XE	5.5~3.7	16K	1280	2	1-2	N	N	Y	45K	Y	Y	5	Y	PDIP	LQFP/ PLCC
STC11F32XE	5.5~3.7	32K	1280	2	1-2	N	N	Y	29K	Y	Y	5	Y	PDIP	LQFP/ PLCC
STC11F40XE	5.5~3.7	40K	1280	2	1-2	N	N	Y	21K	Y	Y	5	Y	PDIP	LQFP/ PLCC
STC11F48XE	5.5~3.7	48K	1280	2	1-2	N	N	Y	13K	Y	Y	5	Y	PDIP	LQFP/ PLCC
STC11F52XE	5.5~3.7	52K	1280	2	1-2	N	N	Y	9K	Y	Y	5	Y	PDIP	LQFP/ PLCC
STC11F56XE	5.5~3.7	56K	1280	2	1-2	N	N	Y	5K	Y	Y	5	Y	PDIP	LQFP/ PLCC
STC11F60XE	5.5~3.7	60K	1280	2	1-2	N	N	Y	1K	Y	Y	5	Y	PDIP	LQFP/ PLCC
IAP11F62XE	5.5~4.1	62K	1280	2	1-2	N	N	Y	IAP	Y	Y	5	Y	PDIP	LQFP/ PLCC
STC11F08XE	5.5~3.7	8K	1280	2	1-2	N	N	Y	53K	Y	Y	5	Y	PDIP	LQFP/ PLCC
STC11L16XE	3.6~2.1	16K	1280	2	1-2	N	N	Y	45K	Y	Y	5	Y	PDIP	LQFP/ PLCC
STC11L32XE	3.6~2.1	32K	1280	2	1-2	N	N	Y	29K	Y	Y	5	Y	PDIP	LQFP/ PLCC
STC11L40XE	3.6~2.1	40K	1280	2	1-2	N	N	Y	21K	Y	Y	5	Y	PDIP	LQFP/ PLCC
STC11L48XE	3.6~2.1	48K	1280	2	1-2	N	N	Y	13K	Y	Y	5	Y	PDIP	LQFP/ PLCC
STC11L52XE	3.6~2.1	52K	1280	2	1-2	N	N	Y	9K	Y	Y	5	Y	PDIP	LQFP/ PLCC
STC11L56XE	3.6~2.1	56K	1280	2	1-2	N	N	Y	5K	Y	Y	5	Y	PDIP	LQFP/ PLCC
STC11L60XE	3.6~2.1	60K	1280	2	1-2	N	N	Y	1K	Y	Y	5	Y	PDIP	LQFP/ PLCC
IAP11L62XE	3.6~2.4	62K	1280	2	1-2	N	N	Y	IAP	Y	Y	5	Y	PDIP	LQFP/ PLCC
STC11L08XE	3.6~2.1	8K	1280	2	1-2	N	N	Y	53K	Y	Y	5	Y	PDIP	LQFP/ PLCC