INTERSIL

AM2502/3/4
AM25L02/3/4
Successive Approximation Registers

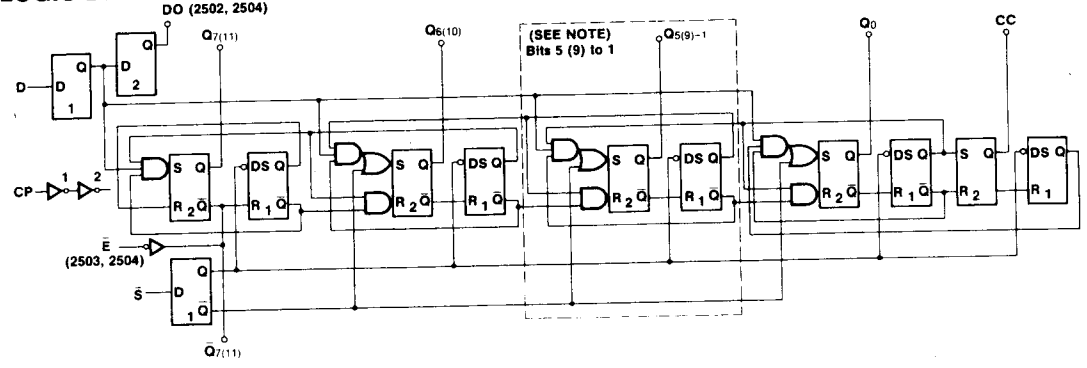
FEATURES
- **Contains all the storage and control for successive approximation A to D converters.**
- **Provision for register extension or truncation.**
- **Can be operated in START-STOP or continuous conversion mode.**
- **100% reliability assurance testing in compliance with MIL-STD-883.**
- **Can be used as serial-to-parallel counter or ring counters.**
- **Electrically tested and optically inspected dice for the assemblers of hybrid products.**

GENERAL DESCRIPTION
The AM2502/3/4 are 8-bit and 12-bit TTL Successive Approximation Registers. They contain all the digital control and storage necessary for successive approximation analog to digital conversion and can also be used in digital systems as the control and storage element in recursive digital routines.

The registers consist of a set of master latches which act as the control elements and change state when the input clock is LOW, and a set of slave latches that hold the register data and change on the input clock LOW to HIGH transition. Externally the device acts as a special purpose serial to parallel converter which accepts data at the D input of the register and sends the data to the appropriate slave latch to appear at the register output and the DO output on the 2502 and 2504 when the clock goes from LOW to HIGH. There are no restrictions on the data input; it can change state at any time except during the set-up time just prior to the clock transition. At the same time data enters the register bit the next less significant bit is set to a LOW, ready for the next iteration.

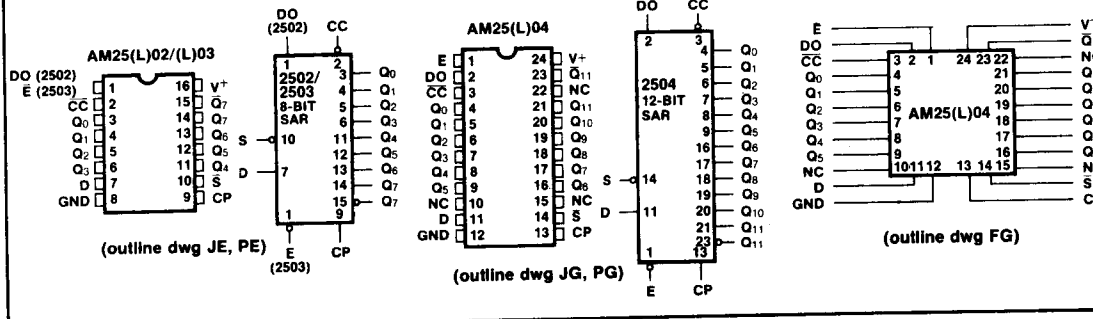
The AM25L02/L03/L04 are low power equivalents of the AM2502/03/04.

LOGIC DIAGRAM



NOTES
1. CELL LOGIC IS REPEATED FOR REGISTER STAGES.
   Q_5 TO Q_1 2502/3
   Q_9 TO Q_1 2504
2. NUMBERS IN PARENTHESES ARE FOR 2504

PIN CONFIGURATIONS AND LOGIC SYMBOLS



ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... −0.5V to +7V
DC Voltage Applied to Outputs for High Output State ..... −0.5V to V^+
DC Input Voltage ..... −0.5V to +5.5V
Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA
Storage Temperature ..... −65°C to +150°C
Operating Temperatures
M devices ..... −55°C to +125°C
C devices ..... 0°C to +70°C
Lead Temperature (soldering, 10s) ..... 300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CHARACTERISTICS $V^+ = 5V$, T_A = Operating Temperature Range unless otherwise specified

PARAMETER		SYMBOL	TEST CONDITIONS			LIMITS MIN.	LIMITS TYP.(1)	LIMITS MAX.	UNIT
Output high voltage		V_{OH}	V^+ = min, I_{OH} = −0.48mA, V_{IN} = V_{IL} or V_{IH}			2.4	3.6		V
Output low voltage		V_{OL}	V^+ = min, I_{OH} = 0.96mA, V_{IN} = V_{IL} or V_{IH}				0.2	0.4	V
Input high voltage		V_{IH}	Guaranteed input logic HIGH voltage for all inputs			2.0			V
Input low voltage		V_{IL}	Guaranteed input logic LOW voltage for all inputs					0.8	V
Unit load input low current (2)	AM2502/3/4	I_{IL}	V^+ = max, V_{IN} = 0.4V				−1.0	−1.6	mA
	AM25L02/3/4						−0.25	−0.4	
Unit load input high current (2)	AM2502/3/4	I_{IH}	V^+ = max, V_{IN} = 2.4V				6.0	40	μA
	AM25L02/3/4						2.0	20	
Input high current		I_{IH}	V^+ = max, V_{IN} = 5.5V					1.0	mA
Output short circuit current		I_{SC}	V^+ = max, V_O = 0V	2502/3/4		−10	−25	−45	mA
				25L02/3/4		−3	−7	−16	
Power Supply Current		I^+	V^+ = max	AM2502/3	C		65	95	mA
					M		65	85	
				AM25L02/3	C		25	35	mA
					M		25	33	
				AM2504	C		90	124	mA
					M		90	110	
				AM25L04	C		30	45	mA
					M		30	42	

NOTES: 1. Typical limits are with V^+ = 5.0V, T_A = 25°C and maximum loading.
2. Actual input currents are obtained by multiplying unit load current by input load factor (see Loading Rules).

SWITCHING CHARACTERISTICS T_A = 25°C, V^+ = 5.0V, C_L = 15pF

PARAMETERS	DESCRIPTION		AM2502/3/4 MIN	AM2502/3/4 TYP	AM2502/3/4 MAX	AM25L02/3/4 MIN	AM25L02/3/4 TYP	AM25L02/3/4 MAX	UNITS
t_{pd+}	Turn Off Delay CP to Output HIGH		10	26	38	20	75	110*	ns
t_{pd-}	Turn On Delay CP to Output LOW		10	18	28	20	75	100	ns
t_s(D)	Set-up Time Data Input		−10	4	8	−15	8	20	ns
t_s($\overline{S}$)	Set-up Time Start Input		0	9	16	0	20	25	ns
t_{pd+}(E)	Turn Off Delay E to $Q_{7(11)}$	(AM25L)03/4)		13	19		50	75	ns
t_{pd-}(E)	Turn On Delay E to $Q_{7(11)}$ LOW	C_P = H, $\overline{S}$ = L		16	24		60	75	ns
t_{pwL}(CP)	Minimum LOW Clock Pulse Width			28	46		100	150	ns
t_{pwH}(CP)	Minimum HIGH Clock Pulse Width			12	20		70	100	ns
f_{max}	Maximum Clock Frequency		15	25		3.5	5.0		MHz

*Q_{11}, $\overline{Q}_{11}$ 30 ns slower

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25(L)02/3 LOADING RULES (IN UNIT LOADS)

INPUT/ OUTPUT	PIN NO.'s	INPUT UNIT LOAD		FANOUT	
		LOW	HIGH	OUTPUT HIGH	OUTPUT LOW
$\overline{E}$ (2503)	1	2	2	—	—
DO (2502)	1	—	—	12	6
$\overline{CC}$	2	—	—	12	6
Q_0	3	—	—	12	6
Q_1	4	—	—	12	6
Q_2	5	—	—	12	6
Q_3	6	—	—	12	6
D	7	2	2	—	—
GND	8	—	—	—	—
CP	9	1	1	—	—
$\overline{S}$	10	1	2	—	—
Q_4	11	—	—	12	6
Q_5	12	—	—	12	6
Q_6	13	—	—	12	6
$\overline{Q_7}$	14	—	—	12	6
Q_7	15	—	—	12	6
V^+	16	—	—	—	—

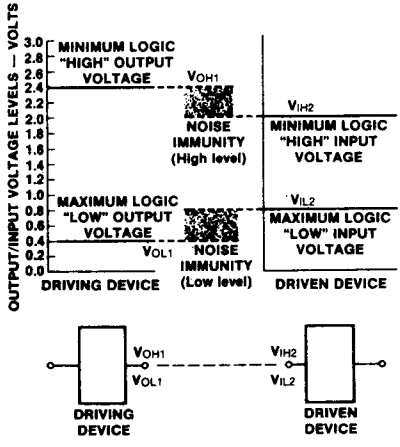
25(L)04 LOADING RULES (IN UNIT LOADS)

INPUT/ OUTPUT	PIN NO.'s	INPUT UNIT LOAD		FANOUT	
		LOW	HIGH	OUTPUT HIGH	OUTPUT LOW
$\overline{E}$	1	2	2	—	—
DO	2	—	—	12	6
$\overline{CC}$	3	—	—	12	6
Q_0	4	—	—	12	6
Q_1	5	—	—	12	6
Q_2	6	—	—	12	6
Q_3	7	—	—	12	6
Q_4	8	—	—	12	6
Q_5	9	—	—	12	6
NC	10	—	—	—	—
D	11	2	2	—	—
GND	12	—	—	—	—
CP	13	1	1	—	—
$\overline{S}$	14	1	2	—	—
NC	15	—	—	—	—
Q_6	16	—	—	12	6
Q_7	17	—	—	12	6
Q_8	18	—	—	12	6
Q_9	19	—	—	12	6
Q_{10}	20	—	—	12	6
$\overline{Q_{11}}$	21	—	—	12	6
NC	22	—	—	—	—
Q_{11}	23	—	—	12	6
V^+	24	—	—	—	—

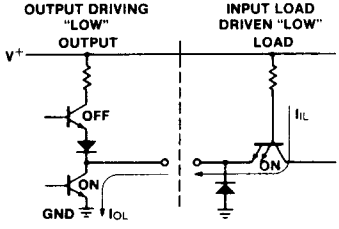
NC = No Connection

INPUT/OUTPUT INTERFACE CONDITIONS

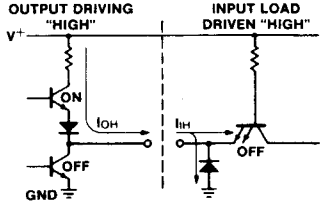
VOLTAGE INTERFACE CONDITIONS — LOW & HIGH



CURRENT INTERFACE CONDITIONS — LOW



CURRENT INTERFACE CONDITIONS — HIGH



AM25(L)02/3 TRUTH TABLE

TIME	INPUTS			OUTPUTS									
t_n	D	S	E	D_0	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0	CC
0	X	L	L	X	X	X	X	X	X	X	X	X	X
1	D_7	H	L	X	L	H	H	H	H	H	H	H	H
2	D_6	H	L	D_7	D_7	L	H	H	H	H	H	H	H
3	D_5	H	L	D_6	D_7	D_6	L	H	H	H	H	H	H
4	D_4	H	L	D_5	D_7	D_6	D_5	L	H	H	H	H	H
5	D_3	H	L	D_4	D_7	D_6	D_5	D_4	L	H	H	H	H
6	D_2	H	L	D_3	D_7	D_6	D_5	D_4	D_3	L	H	H	H
7	D_1	H	L	D_2	D_7	D_6	D_5	D_4	D_3	D_2	L	H	H
8	D_0	H	L	D_1	D_7	D_6	D_5	D_4	D_3	D_2	D_1	L	H
9	X	H	L	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	L
10	X	X	L	X	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	L
	X	X	H	X	H	NC	NC	NC	NC	NC	NC	NC	NC

H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

NC = No Change

Note: Truth Table for 25(L)04 is extended to include 12 outputs.

USER NOTES FOR A/D CONVERSION

1. The register can be used with current switches which are either active high or active low. If active low current switches are used, the resulting digital output from the register is active LOW. That is, a logic "1" is represented as a low voltage level. If active high current switches are used then the digital output is active HIGH; a logic "1" is represented as a high voltage level.
2. For a maximum digital error of ±1/2 LSB the comparator must be biased. If active high current switches are used, the comparator should be biased +1/2 LSB and if the current switches are active low, the comparator must be biased −1/2 LSB.
3. The register, by suitable selection of resistor ladder network, can be used to perform either binary or BCD conversion.
4. The register can also be used to perform 2's complement conversion by offsetting the comparator 1/2 full range +1/2 LSB and using the complement of the MSB Q_7(11) as the sign bit.
5. If the register is truncated and operated in the continuous conversion mode a lock-up condition may occur on power-on. This situation can be overcome by making the START input the OR function of $\overline{CC}$ and the appropriate register output.

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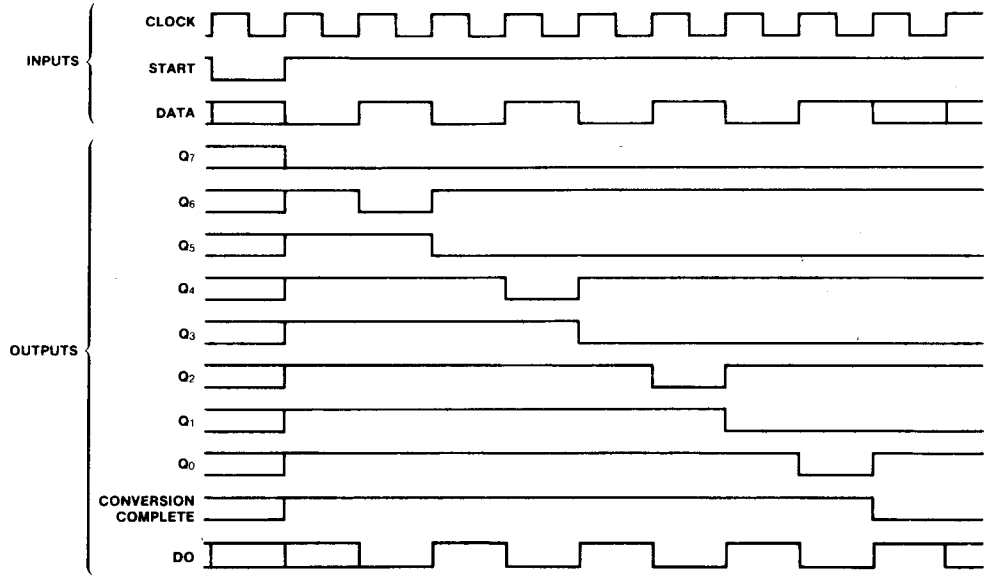
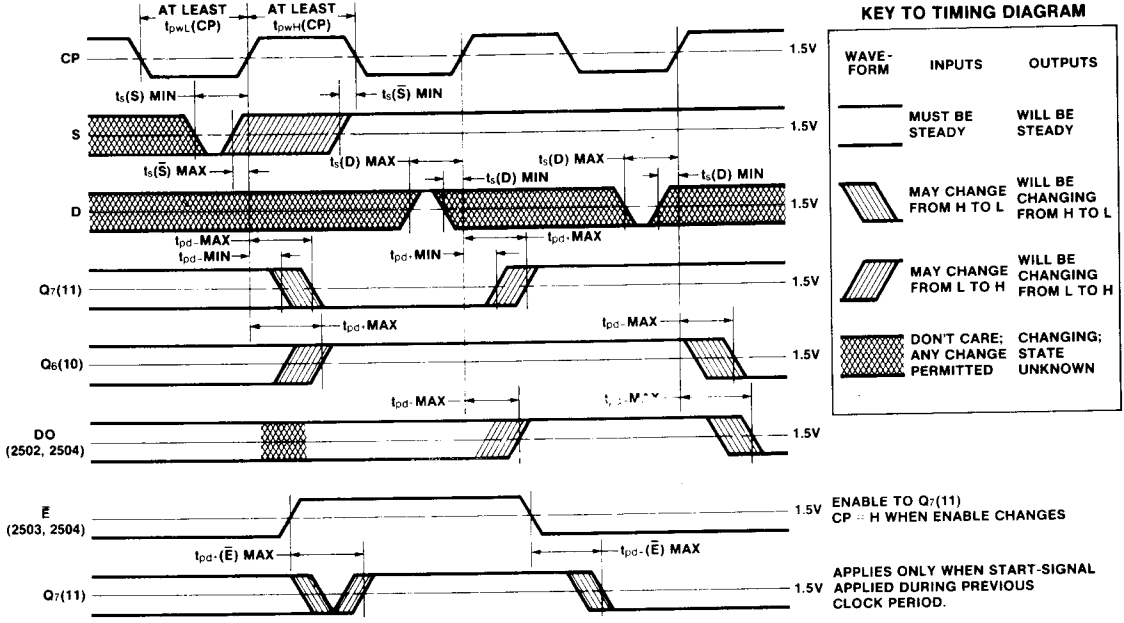
AM25(L)02/3 TIMING CHART



Note: Arbitrary Conversion shown. Timing chart for AM25(L)04 is extended to include 12 outputs, starting with Q_{11}.

SWITCHING TIME WAVEFORMS



DEFINITION OF TERMS

SUBSCRIPT TERMS:

H – HIGH, applying to a HIGH logic level or when used with V_{CC} to indicate high V_{CC} value.

I – Input.

L – LOW, applying to LOW logic level or when used with V_{CC} to indicate low V_{CC} value.

O – Output.

FUNCTIONAL TERMS:

Fan-Out – The logic HIGH or LOW output drive capability in terms of Input Unit Loads.

Input Unit Load One T^2L gate input load. In the HIGH state it is equal to I_{IH} and in the LOW state it is equal to I_{IL}.

CP – The clock input of the register.

$\overline{CC}$ – The conversion complete output. This output remains HIGH during a conversion and goes LOW when a conversion is complete.

D – The serial data input of the register.

$\overline{E}$ – The register enable. This input is used to expand the length of the register and when HIGH forces the $Q_7(11)$ register output HIGH and inhibits conversion. When not used for expansion the enable is held at a LOW logic level (Ground).

$Q_7(11)$ – The true output of the MSB of the register.

$\overline{Q}_7(11)$ – The complement output of the MSB of the register.

Q_i, i = 7(11) to 0 – The outputs of the register.

$\overline{S}$ – The start input. If the start input is held LOW for at least a clock period the register will be reset to $Q_7(11)$ LOW and all the remaining outputs HIGH. A start pulse that is LOW for a shorter period of time can be used if it meets the set-up time requirements of the $\overline{S}$ input.

DO – The serial data output. (The D input delayed one bit.)

OPERATIONAL TERMS:

I_{IL} – Forward input load current.

I_{OH} – Output HIGH current, forced out of output V_{OH} test.

I_{OL} – Output LOW current, forced into the output in V_{OL} test.

I_{IH} – Reverse input load current.

Negative Current – Current flowing out of the device.

Positive Current – Current flowing into the device.

V_{IH} – Minimum logic HIGH input voltage.

V_{IL} – Maximum logic LOW input voltage.

V_{OH} – Minimum logic HIGH output voltage with output HIGH current I_{OH} flowing out of output.

V_{OL} – Maximum logic LOW output voltage with output LOW current I_{OL} flowing into output.

SWITCHING TERMS: (Measured at the 1.5V logic level.)

t_{pd-} – The propagation delay from the clock signal LOW-HIGH transition to an output signal HIGH-LOW transition.

t_{pd+} – The propagation delay from the clock signal LOW-HIGH transition to an output signal LOW-HIGH transition.

$t_{pd-}(\overline{E})$ – The propagation delay from the Enable signal HIGH-LOW transition to the $Q_7(11)$ output signal HIGH-LOW transition.

$t_{pd+}(\overline{E})$ – The propagation delay from the Enable signal LOW-HIGH transition to $Q_7(11)$ output signal LOW-HIGH transition.

$t_s(D)$ – Set-up time required for the logic level to be present at the data input prior to the clock transition from LOW to HIGH in order for the register to respond. The data input should remain steady between t_s max, and t_s min. before the clock.

$t_s(\overline{S})$ – Set-up time required for a LOW level to be present at the $\overline{S}$ input prior to the clock transition from LOW to HIGH in order for the register to be reset, or time required for a HIGH level to be present on $\overline{S}$ before the HIGH to LOW clock transition to prevent resetting.

$t_{pw}(CP)$ – The minimum clock pulse width (LOW or HIGH) required for proper register operation.

ORDERING INFORMATION

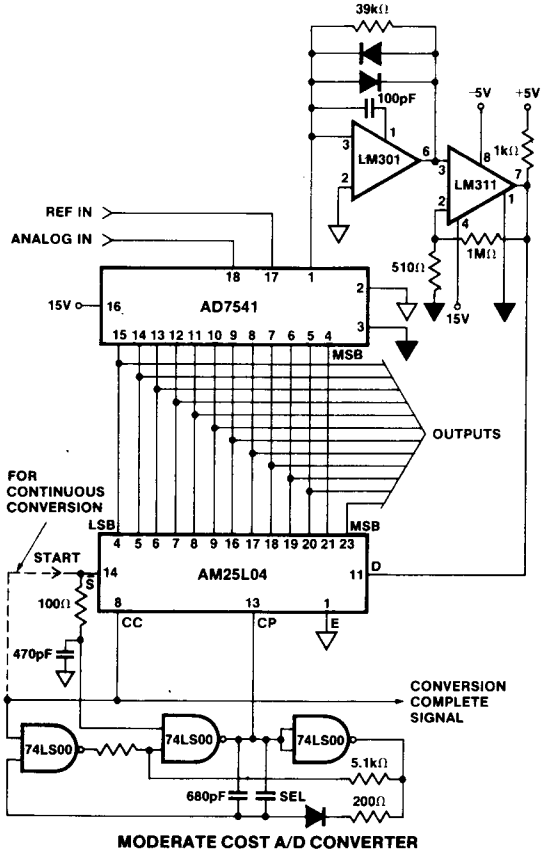
PART	16 PIN CERDIP	16 PIN PLASTIC DIP	DICE	
AM2502C	AM2502DC	AM2502PC	AM2502XC	
AM2502M	AM2502DM		AM2502XM	
AM2503C	AM2503DC	AM2503PC	AM2503XC	
AM2503M	AM2503DM		AM2503XM	
	24 pin CERDIP	24 pin plastic DIP	24 pin Flatpak	Dice
AM2504C	AM2504DC	AM2504PC		AM2504XC
AM2504M	AM2504DM		AM2504FM	AM2504XM

To order "L" devices, insert "L" following"25"; e.g., AM25L02DM

NOTES: C - Commercial Temperature Range (0°C to +70°C)
M - Military Temperature Range (−55°C to +125°C)

CIRCUIT DESCRIPTION

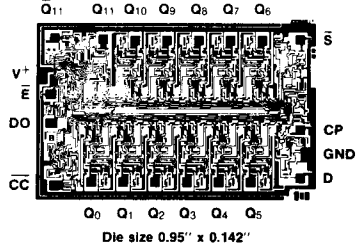
The register is reset by holding the $\overline{S}$ (Start) signal LOW during the clock LOW-to-HIGH transition. The register synchronously resets to the state $Q_7(11)$ LOW, (Note 2) and all the remaining register outputs HIGH. The $\overline{CC}$ (Conversion Complete) signal is also set HIGH at this time. The $\overline{S}$ signal should not be brought back HIGH until after the clock LOW-to-HIGH transition in order to guarantee correct resetting. After the clock has gone HIGH resetting the register, the $\overline{S}$ signal is removed. On the next clock LOW-to-HIGH transition the data on the D input is set into the $Q_7(11)$ register bit and the $Q_6(10)$ register bit is set to a LOW ready for the next clock cycle. On the next clock LOW-to-HIGH transition data enters the $Q_6(10)$ register bit and $Q_5(9)$ is set to a LOW. This operation is repeated for each register bit in turn until the register has been filled. When the data goes into Q_0, the $\overline{CC}$ signal goes LOW, and the register is inhibited from further change until reset by a START signal.



MODERATE COST A/D CONVERTER

To allow two's complement conversion the complementary output of the most significant register bit is made available. An active LOW enable input, $\overline{E}$, on the 2503 and 2504 allows devices to be connected together to form a longer register by connecting the clock, D, and $\overline{S}$ inputs together and connecting the $\overline{CC}$ output of one device to the $\overline{E}$ input of the next less significant device. When the START signal resets the register, the $\overline{E}$ signal goes HIGH, forcing the $Q_7(11)$ bit HIGH and inhibiting the device from accepting data until the previous device is full and its $\overline{CC}$ goes LOW. If only one device is used the $\overline{E}$ input should be held at a LOW logic level (Ground). If all the bits are not required, the register may be truncated and conversion time saved by using a register output going LOW rather than the $\overline{CC}$ signal to indicate the end of conversion.

CHIP TOPOGRAPHY



Die size 0.95" x 0.142"