MC34066, MC33066

High Performance Resonant Mode Controllers

The MC34066/MC33066 are high performance resonant mode controllers designed for off−line and dc−to−dc converter applications that utilize frequency modulated constant on−time or constant off−time control. These integrated circuits feature a variable frequency oscillator with programmable deadtime, precision retriggerable one−shot timer, temperature compensated reference, high gain wide−bandwidth error amplifier with a precision output clamp, steering flip−flop, and dual high current totem pole outputs ideally suited for driving power MOSFETs.

Also included are protective features consisting of a high speed fault comparator and latch, programmable soft−start circuitry, input undervoltage lockout with selectable thresholds, and reference undervoltage lockout.

These devices are available in dual−in−line and surface mount packages.

- Variable Frequency Oscillator with a Control Range Exceeding 1000:1
- Programmable Oscillator Deadtime Allows Constant Off−Time Operation
- Precision Retriggerable One−Shot Timer
- Internally Trimmed Bandgap Reference
- 5.0 MHz Error Amplifier with Precision Output Clamp
- Dual High Current Totem Pole Outputs
- Selectable Undervoltage Lockout Thresholds with Hysteresis
- Enable Input
- Programmable Soft−Start Circuitry
- Low Startup Current for Off−Line Operation

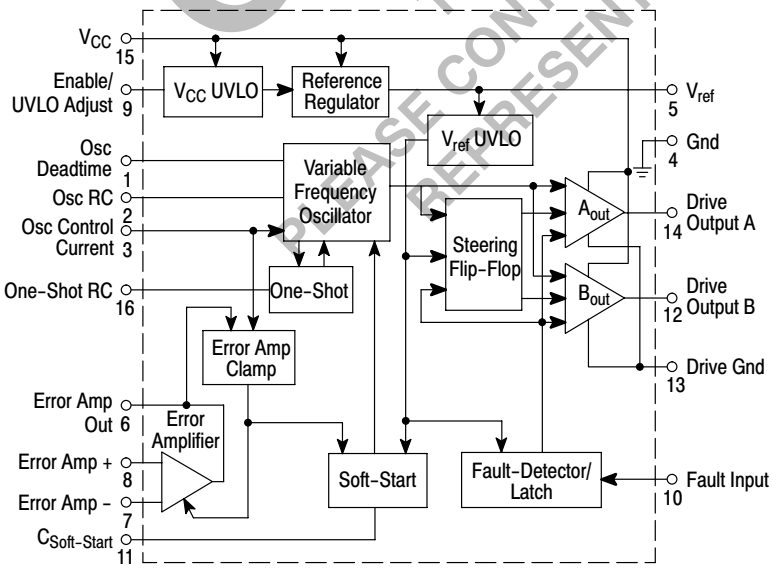

Figure 1. Simplified Block Diagram

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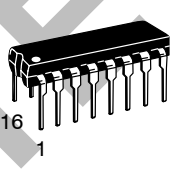
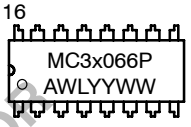
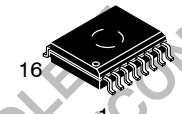
MARKING DIAGRAMS

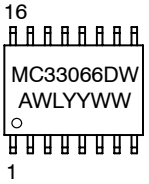


PDIP−16
P SUFFIX
CASE 648



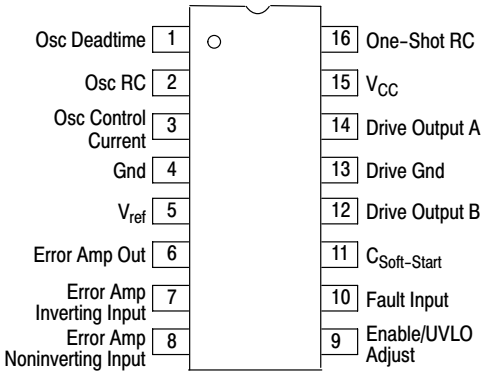


SO−16W
DW SUFFIX
CASE 751G



x = 3 or 4
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping
MC34066P	PDIP−16	25 Units/Rail
MC33066DW	SO−16W	47 Units/Rail
MC33066P	PDIP−16	25 Units/Rail

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Input Supply Voltage	V_{CC}	20	V
Drive Output Current, Source or Sink (Note 1) Continuous Pulsed (0.5 μs, 25% Duty Cycle)	I_O	 0.3 1.5	A
Error Amplifier, Fault, One−Shot, Oscillator, and Soft−Start Inputs	V_{in}	−1.0 to +6.0	V
UVLO Adjust Input	$V_{in(UVLO)}$	−1.0 to V_{CC}	V
Soft−Start Discharge Current	I_{dchg}	20	mA
Power Dissipation and Thermal Characteristics DW Suffix Package, Case 751G Maximum Power Dissipation @ T_A = 25°C Thermal Resistance, Junction−to−Air P Suffix Package, Case 648 Maximum Power Dissipation @ T_A = 25°C Thermal Resistance, Junction−to−Air	 P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	 862 145 1.25 100	 mW °C/W W °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature MC34066 MC33066	T_A	 0 to +70 −40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V [Note 2], R_{OSC} = 95.3 k, R_{DT} = 0 Ω, R_{VFO} = 5.62 k, C_{OSC} = 300 pF, R_T = 14.3 k, C_T = 300 pF, C_L = 1.0 nF, for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 3], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION					
Reference Output Voltage (I_O = 0 mA, T_A = 25°C)	V_{ref}	5.0	5.1	5.2	V
Line Regulation (V_{CC} = 10 V to 18 V)	Reg_{line}	–	1.0	20	mV
Load Regulation (I_O = 0 mA to 10 mA)	Reg_{load}	–	1.0	20	mV
Total Output Variation over Line, Load, and Temperature	V_{ref}	4.9	–	5.3	mV
Output Short Circuit Current	I_O	25	100	190	mA
Reference Undervoltage Lockout Threshold	V_{th}	3.8	4.3	4.8	V
ERROR AMPLIFIER					
Input Offset Voltage (V_{CM} = 1.5 V)	V_{IO}	–	1.0	10	mV
Input Bias Current (V_{CM} = 1.5 V)	I_{IB}	–	0.2	1.0	μA
Input Offset Current (V_{CM} = 1.5 V)	I_{IO}	–	0	0.5	μA
Open Loop Voltage Gain (V_{CM} = 1.5 V, V_O = 2.0 V)	A_{VOL}	70	100	–	dB
Gain Bandwidth Product (f = 100 kHz)	GBW	2.5	4.2	–	MHz
Input Common Mode Rejection Ratio (V_{CM} = 1.5 V to 5.0 V)	CMRR	70	95	–	dB
Power Supply Rejection Ratio (V_{CC} = 10 V to 18 V, f = 120 Hz)	PSRR	80	100	–	dB
Output Voltage Swing High State with Respect to Pin 3 (I_{Source} = 2.0 mA) Low State with Respect to Ground (I_{Sink} = 1.0 mA)	 V_{OH} V_{OL}	 2.3 –	 2.7 0.4	 3.1 0.6	V

1. Maximum package power dissipation limits must be observed.
2. Adjust V_{CC} above the Startup threshold before setting to 12 V.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
   T_{low} = 0°C for MC34066, −40°C for MC33066; T_{high} = +70°C for MC34066, +85°C for MC33066

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 12 V [Note 4], R_{OSC} = 95.3 k, R_{DT} = 0 Ω, R_{VFO} = 5.62 k, C_{OSC} = 300 pF, R_T = 14.3 k, C_T = 300 pF, C_L = 1.0 nF, for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 5], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
OSCILLATOR					
Frequency (Error Amp Output Low) T_A = 25°C Total Variation (V_{CC} = 10 V to 18 V, T_A = T_{Low} to T_{High})	$f_{OSC(low)}$	 90 85	 100 –	 110 115	kHz
Frequency (Error Amp Output High) T_A = 25°C Total Variation (V_{CC} = 10 V to 18 V, T_A = T_{Low} to T_{High})	$f_{OSC(high)}$	 900 850	 1000 –	 1100 1150	kHz
Oscillator Control Input Voltage, Pin 3 (I_{Sink} = 0.5 mA, T_A = 25°C)	V_{in}	1.3	1.4	1.5	V
Output Deadtime (Error Amp Output High) R_{DT} = 0 Ω R_{DT} = 1.0 k	DT	 – 600	 70 700	 100 800	ns
ONE−SHOT					
Drive Output On−Time (R_{DT} = 1.0 k) T_A = 25°C Total Variation (V_{CC} = 10 V to 18 V, T_A = T_{Low} to T_{High})	t_{OS}	 1.43 1.4	 1.5 –	 1.57 1.6	μs
DRIVE OUTPUTS					
Output Voltage Low State (I_{Sink} = 20 mA) (I_{Sink} = 200 mA) High State (I_{Source} = 20 mA) (I_{Source} = 200 mA)	 V_{OL} V_{OH} 	 – – 9.5 9.0	 0.8 1.5 10.3 9.8	 1.2 2.0 – –	V
Output Voltage with UVLO Activated (V_{CC} = 6.0 V, I_{Sink} = 1.0 mA)	$V_{OL(UVLO)}$	–	0.8	1.2	V
Output Voltage Rise Time (C_L = 1.0 nF)	t_r	–	20	50	ns
Output Voltage Fall Time (C_L = 1.0 nF)	t_f	–	20	50	ns
FAULT COMPARATOR					
Input Threshold	V_{th}	0.95	1.0	1.05	V
Input Bias Current ($V_{Pin\ 10}$ = 0 V)	I_{IB}	–	−2.0	−10	μA
Propagation Delay to Drive Outputs (100 mV Overdrive)	$t_{PLH(In/Out)}$	–	60	100	ns
SOFT−START					
Capacitor Charge Current ($V_{Pin\ 11}$ = 2.5 V)	I_{chg}	4.5	8.1	14	μA
Capacitor Discharge Current ($V_{Pin\ 11}$ = 2.5 V)	I_{Idchg}	1.0	8.0	–	mA
UNDERVOLTAGE LOCKOUT					
Startup Threshold, V_{CC} Increasing Enable/UVLO Adjust Pin Open Enable/UVLO Adjust Pin Connected to V_{CC}	$V_{th(UVLO)}$	 14.8 8.0	 16 9.0	 17.2 10	V
Minimum Operating Voltage after Turn−On Enable/UVLO Adjust Pin Open Enable/UVLO Adjust Pin Connected to V_{CC}	$V_{CC(min)}$	 8.0 7.6	 9.0 8.6	 10 9.6	V
Enable/UVLO Adjust Shutdown Threshold Voltage	$V_{th(Enable)}$	6.0	7.0	–	V
Enable/UVLO Adjust Input Current (Pin 9 = 0V)	$I_{in(Enable)}$	–	−0.2	−1.0	mA
TOTAL DEVICE					
Power Supply Current (Enable/UVLO Adjust Pin Open) Startup (V_{CC} = 13.5 V) Operating (f_{OSC} = 100 kHz) (Note 4)	I_{CC}	 – –	 0.45 21	 0.6 30	mA

4. Adjust V_{CC} above the Startup threshold before setting to 12 V.
5. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
   T_{low} = 0°C for MC34066, −40°C for MC33066; T_{high} = +70°C for MC34066, +85°C for MC33066

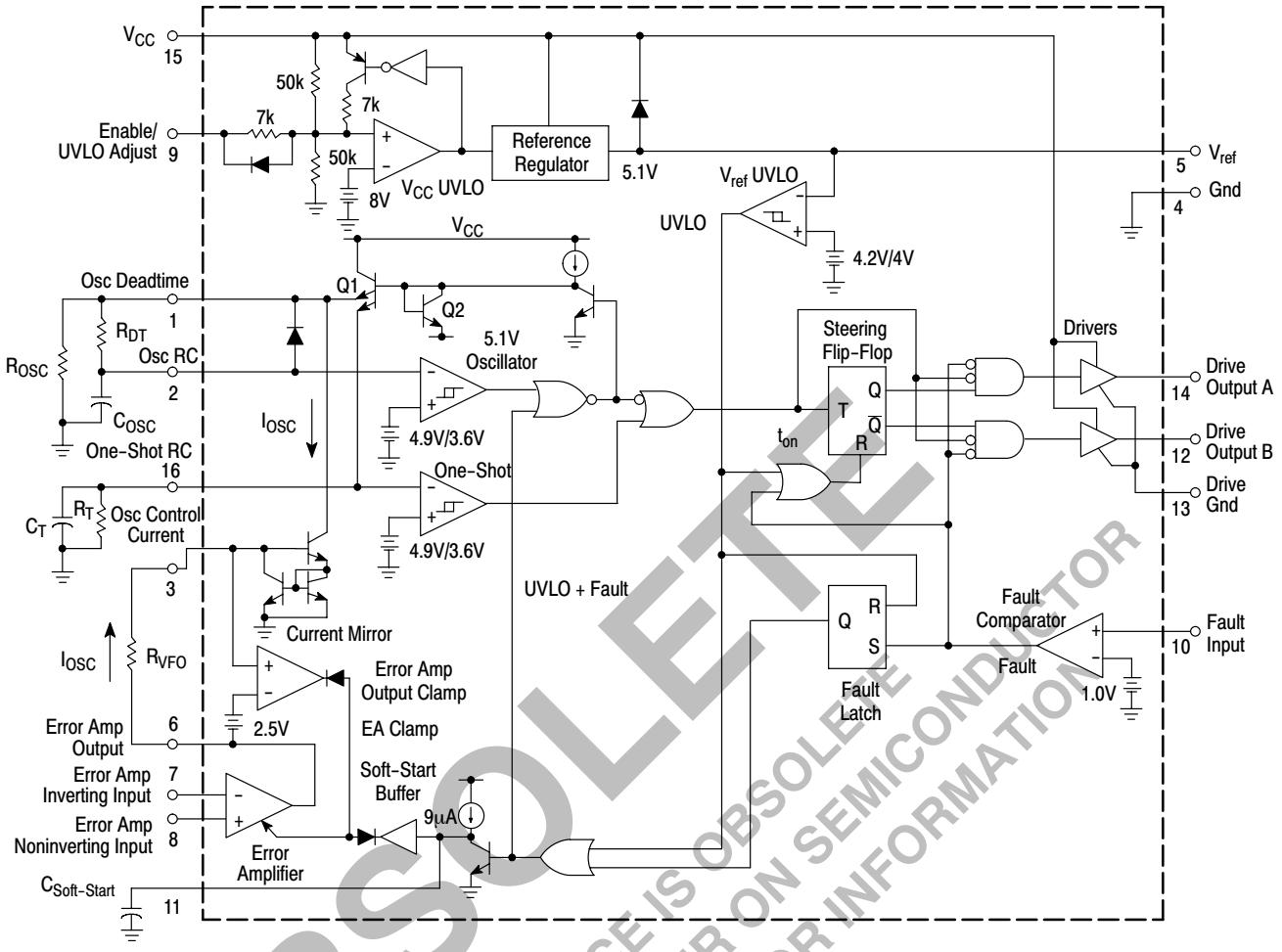


Figure 2. MC34066 Representative Block Diagram

OPERATING DESCRIPTION

Introduction

As power supply designers have strived to increase power conversion efficiency and reduce passive component size, high frequency resonant mode power converters have emerged as attractive alternatives to conventional square−wave control. When compared to square−wave converters, resonant mode control offers several benefits including lower switching losses, higher efficiency, lower EMI emission, and smaller size. This integrated circuit has been developed to support new trends in power supply design. The MC34066 Resonant Mode Controller is a high performance bipolar IC dedicated to variable frequency power control at frequencies exceeding 1.0 MHz. This integrated circuit provides the features, performance and flexibility for a wide variety of resonant mode power supply applications.

The primary purpose of the control chip is to supply precise pulses to the gates of external power MOSFETs at a repetition rate regulated by a feedback control loop. The MC34066 can be operated in any of three modes as follows: 1) fixed on−time, variable frequency; 2) fixed off−time, variable frequency; and 3) combinations of 1 and 2 that change from fixed on−time to fixed off−time as the frequency increases. Additional features of the IC ensure that system startup and fault conditions are administered in a safe, controlled manner.

A simplified block diagram of the IC is shown on the first page of this data sheet, which identifies the main functional blocks and the block−to−block interconnects. Figure 2 is a detailed functional diagram which accurately represents the internal circuitry. The various functions can be divided into two sections. The first section includes the primary control path which produces precise output pulses at the desired frequency Oscillator, a One−Shot, a pulse Steering Flip−Flop, a pair of power MOSFET Drivers, and a wide bandwidth Error Amplifier. The second section provides several peripheral support functions including a voltage reference, undervoltage lockout, Soft−Start circuit, and a fault detector.

Primary Control Path

The output pulse width and repetition rate are regulated through the interaction of the variable frequency Oscillator, One−Shot timer and Error Amplifier. The Oscillator triggers the One−Shot which generates a pulse that is alternately steered to a pair of totem−pole output drivers by a toggle Flip−Flop. The Error Amplifier monitors the output of the regulator and modulates the frequency of the Oscillator. High−speed Schottky logic is used throughout the primary control channel to minimize delays and enhance high frequency characteristics.

Oscillator

The characteristics of the variable frequency Oscillator are crucial for precise controller performance at high operating frequencies. In addition to triggering the One−Shot timer and initiating the output pulse, the Oscillator also determines the initial voltage for the One−Shot capacitor and defines the minimum deadtime between output pulses. The Oscillator is designed to operate at frequencies exceeding 1.0 MHz. The Error Amplifier can control the oscillator frequency over a 1000:1 frequency range, and both the minimum and maximum frequencies are easily and accurately programmed by the proper selection of external components. The Oscillator also includes an adjustable deadtime feature for applications requiring additional time between output pulses.

The functional diagram of the Oscillator and One−Shot timer is shown in Figure 3. The oscillator capacitor C_{OSC} is initially charged by transistor Q1 through the optional deadtime resistor R_{DT}. When C_{OSC} exceeds the 4.9 V upper threshold of the oscillator comparator, the base of Q1 is pulled low allowing C_{OSC} to discharge through the external resistors and the internal Current Mirror. When the voltage on C_{OSC} falls below the comparator's 3.6 V lower threshold, Q1 turns on and again charges C_{OSC}.

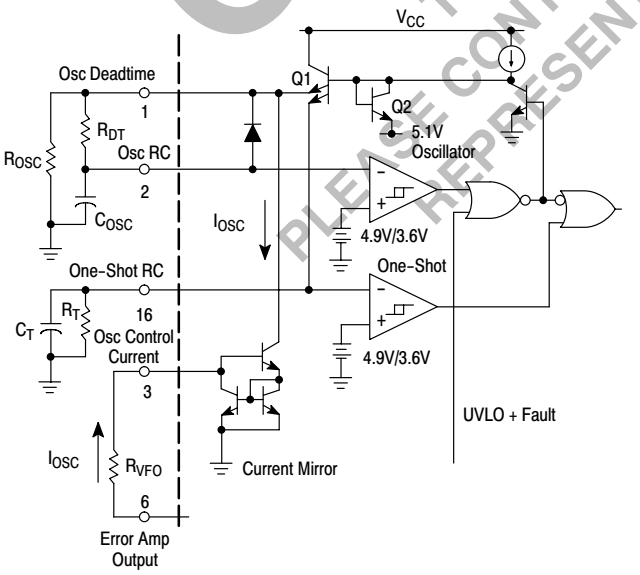


Figure 3. Oscillator and One−Shot Timer

If R_{DT} is 0 Ω, C_{OSC} charges from 3.6 V to 5.1 V in less than 50 ns. The high slew rate of C_{OSC} and the propagation delay of the comparator make it difficult to control the peak voltage. This accuracy issue is overcome by clamping the base of Q1 through diode Q2 to a voltage reference. The peak voltage of the oscillator waveform is thereby precisely set at 5.1 V.

The frequency of the Oscillator is modulated by varying the current I_{OSC} flowing through R_{VFO} into the Osc Control Current pin. The control current drives a unity gain Current Mirror which pulls an identical current from the C_{OSC} capacitor. As I_{OSC} increases, C_{OSC} discharges faster thus decreasing the Oscillator period and increasing the frequency. The maximum frequency occurs when the Error Amplifier output is at the upper clamp level, nominally 2.5 V above the voltage at the Osc Control Current pin. The minimum discharge time for C_{OSC}, which corresponds to the maximum oscillator frequency, is given by Equation 1.

$$t_{dchg(min)} = (R_{DT} + R_{OSC})C_{OSC}\ln\left[\frac{\frac{2.5ROSC}{RVFO} + 5.1}{\frac{2.5ROSC}{RVFO} + 3.6}\right] \quad (1)$$

The minimum oscillator frequency will result when the I_{OSC} current is zero, and C_{OSC} is discharged through the external resistors R_{OSC} and R_{DT}. This occurs when the Error Amplifier output voltage is less than the two diode drops required to bias the input of the Current Mirror. The maximum oscillator discharge time is given by Equation 2.

$$t_{dchg(max)} = (R_{DT} + R_{OSC})\ C_{OSC}\ln\left(\frac{5.1}{3.6}\right) \quad (2)$$

The outputs of the control IC are off whenever the oscillator capacitor C_{OSC} is being charged by transistor Q1. The minimum time between output pulses (deadtime) can be programmed by controlling the charge time of C_{OSC}. Resistor R_{DT} reduces the current delivered by Q1 to C_{OSC}, thus increasing the charge time and output deadtime. Varying R_{DT} from 0 Ω to 1000 Ω will increase the output deadtime from 80 ns to 680 ns with C_{OSC} equal to 300 pF. The general expression for the oscillator charge time is give by Equation 3.

$$t_{chg(max)} = R_{DT}\ C_{OSC}\ \ln\left(\frac{5.1-3.6}{5.1-4.9}\right) + 80\ ns \quad (3)$$

The minimum and maximum oscillator frequencies are programmed by the proper selection of resistor R_{OSC} and R_{VFO}. After selecting R_{DT} for the desired deadtime, the minimum frequency is programmed by R_{OSC} using Equations 2 and 3 in Equation 4:

$$\frac{1}{f_{OSC(min)}} = t_{dchg(max)} + t_{chg} \quad (4)$$

The maximum oscillator frequency is set by resistor R_{VFO} in a similar fashion using Equations 1 and 3 in Equation 5:

$$\frac{1}{f_{OSC(max)}} = t_{dchg(min)} + t_{chg} \quad (5)$$

The value chosen for resistor R_{DT} will affect the peak voltage of the oscillator waveform. As R_{DT} is increased from zero, the time required to charge C_{OSC} becomes large with respect to the propagation delay through the oscillator comparator. Consequently, the overshoot of the upper threshold is reduced and the peak voltage on the oscillator waveform drops from 5.1 V to 4.9 V. The best frequency accuracy is achieved when R_{DT} is zero ohms.

One−Shot Timer

The One−Shot capacitor C_T is charged concurrently with the oscillator capacitor by transistor Q1, as shown in Figure 3. The One−Shot period begins when the oscillator comparator turns off Q1, allowing C_T to discharge. The period ends when resistor R_T discharges C_T to the threshold of the One−Shot comparator. Discharging C_T from an initial voltage of 5.1 V to a threshold voltage of 3.6 V results in the One−Shot period given by Equation 6.

$$t_{OS} = R_T C_T \ln \left(\frac{5.1}{3.6}\right) = 0.348 R_T C_T \quad (6)$$

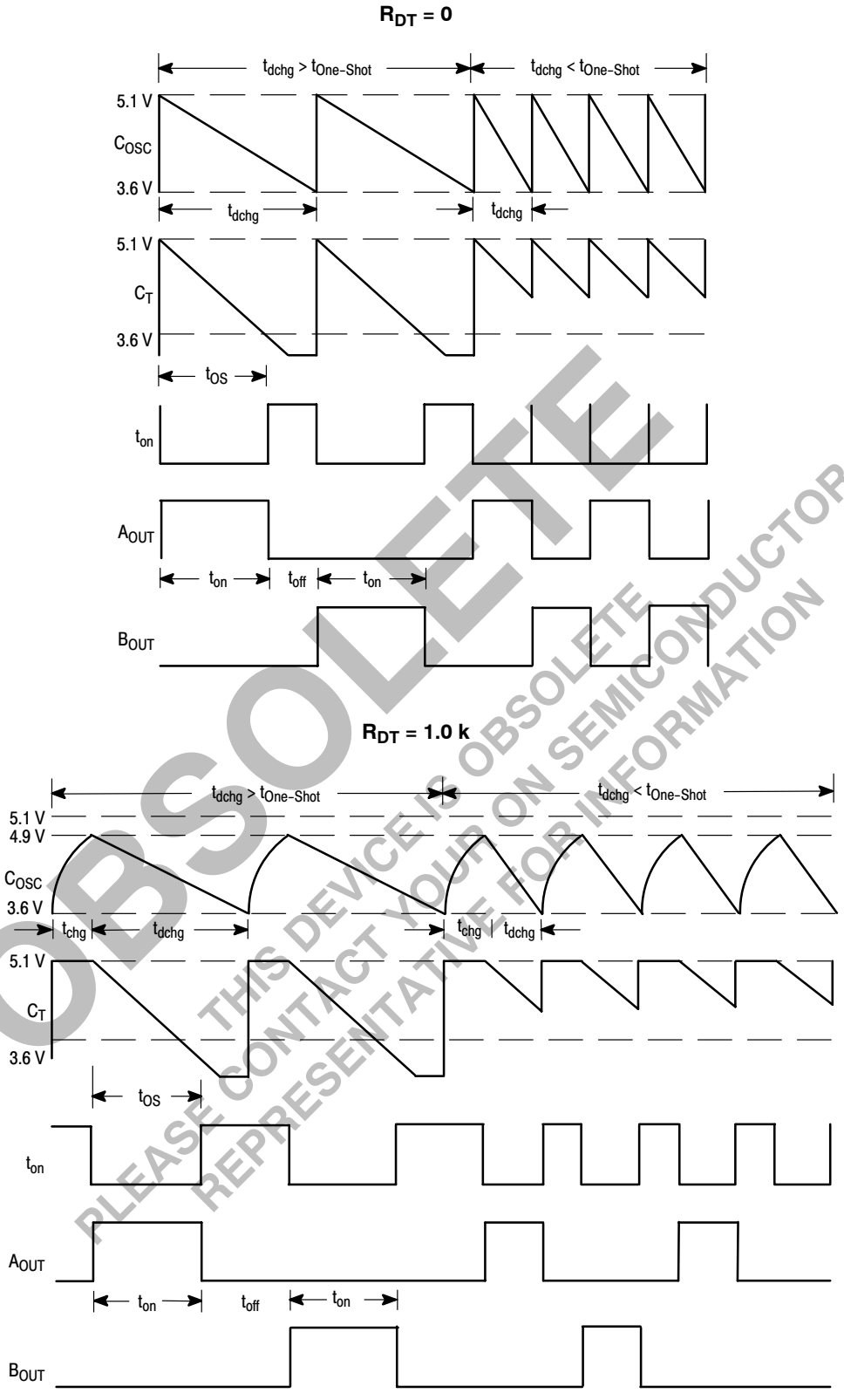


Figure 4. Timing Waveforms

Errors in the threshold voltage and propagation delays through the output drivers will affect the One−Shot period. To guarantee accuracy, the output pulse of the control ship is trimmed to within 5% of 1.5 μs with nominal values of R_T and C_T.

The outputs of the Oscillator and One−Shot comparators are OR'd together to produce the pulse t_{on}, which drives the Flip−Flop and output drivers. The output pulse t_{on} is initiated by the Oscillator, but either the oscillator comparator or the One−Shot comparator can terminate the pulse. When the oscillator discharge time exceeds the one−shot period, the complete one−shot period is delivered to the output section. If the oscillator discharge time is less than the one−shot period, then the oscillator comparator terminates the pulse prematurely and retriggers the One−Shot. The waveforms on the left side of Figure 4 correspond to nonretriggered operation with constant on−time and variable off−times. The right side of Figure 4 represents retriggered operation with variable on−time and constant off−time.

Error Amplifier

A fully accessible high performance Error Amplifier is provided for feedback control of the power supply system. The Error Amplifier is internally compensated and features dc open loop gain greater than 70 dB, input offset voltage less than 10 mV and guaranteed minimum gain−bandwidth product of 2.5 MHz. The input common mode range extends from 1.5 V to 5.1 V, which includes the reference voltage. For common mode voltages below 1.5 V, the Error Amplifier output is forced low providing minimum oscillator frequency.

The Oscillator Control Current pin is biased by the Error Amplifier output voltage through R_{VFO} as illustrated in Figure 5. The output swing of the Error Amplifier is restricted by a clamp circuit to limit the maximum oscillator frequency. The clamp circuit limits the voltage across R_{VFO} to 2.5 V, thus limiting I_{OSC} to 2.5 V/R_{VFO}. Oscillator accuracy is improved by trimming the clamp voltage to obtain the $f_{OSC(high)}$ specification of 1.0 MHz with nominal value external components.

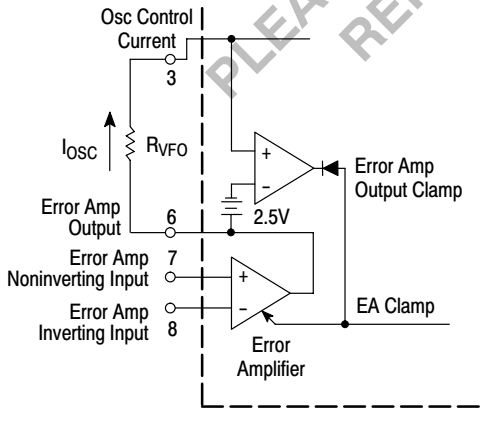


Figure 5. Error Amplifier and Clamp

Output Section

The pulse, t_{on}, generated by the Oscillator and One−Shot timer is gated to dual totem pole output drives by the Steering Flip−Flop shown in Figure 6. Positive transitions of t_{on} toggle the Flip−Flop, which causes the pulses to alternate between Output A and Output B. The flip−flop is reset by the undervoltage lockout circuit during startup to guarantee that the first pulse appears at Output A.

The totem−pole output drives are ideally suited for driving power MOSFETs and are capable of sourcing and sinking 1.5 A. Rise and fall times are typically 20 ns when driving a 1.0 nF load. High source/sink capability in a totem−pole driver normally increases the risk of high cross conduction current during output transitions. The MC34066 utilizes a unique design that virtually eliminates cross conduction, thus controlling the chip power dissipation at high frequencies. A separate ground terminal is provided for the output drivers to isolate the sensitive analog circuitry from large transient currents.

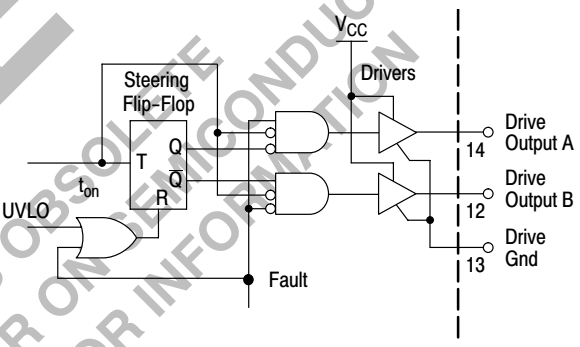


Figure 6. Steering Flip−Flop and Output Drivers

PERIPHERAL SUPPORT FUNCTIONS

The MC34066 Resonant Controller provides a number of support and protection functions including a precision voltage reference, undervoltage lockout comparators, soft−start circuitry, and a fault detector. These peripheral circuits ensure that the power supply can be turned on and off in a safe, controlled manner and that the system will be quickly disabled when a fault condition occurs.

Undervoltage Lockout and Voltage Reference

Separate undervoltage lockout comparators sense the input V_{CC} voltage and the regulated reference voltage as illustrated in Figure 7. When V_{CC} increases to the upper threshold voltage, the V_{CC} UVLO comparator enables the Reference Regulator. After the V_{ref} output of the Reference Regulator rises to 4.2 V, the V_{ref} UVLO comparator switches the UVLO signal to a logic zero state enabling the primary control path. Reducing V_{CC} to the lower threshold voltage causes the V_{CC} UVLO comparator to disable the Reference Regulator. The V_{ref} UVLO comparator then switches the UVLO output to a logic one state disabling the controller.

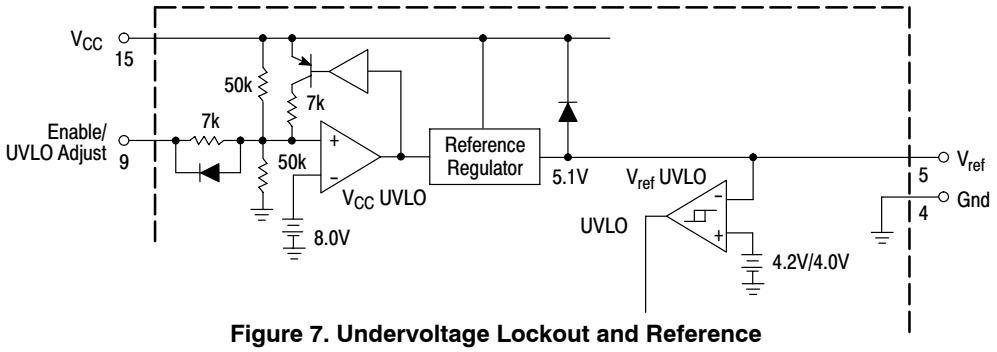


Figure 7. Undervoltage Lockout and Reference

The Enable/UVLO Adjust terminal allows the power supply designer to select the V_{CC} UVLO threshold voltages. When this pin is open, the comparator switches the controller on at 16 V and off at 9.0 V. If this pin is connected to the V_{CC} terminal, the upper and lower thresholds are reduced to 9.0 V and 8.6 V, respectively. Forcing the Enable/UVLO Adjust pin low will pull the V_{CC} UVLO comparator input low (through an internal diode) turning off the controller.

The Reference Regulator provides a precise 5.1 V reference to internal circuitry and can deliver up to 10 mA to external loads. The reference is trimmed to better than 2% initial accuracy and includes active short circuit protection.

Fault Detector

The high−speed Fault Comparator and Latch illustrated in Figure 8 can protect a power supply from destruction under fault conditions. The Fault Input pin connects to the input of the Fault Comparator. If this input exceeds the 1.0 V threshold of the comparator, the Fault Latch is set and two logic signals simultaneously disable the primary control path. The signal labeled Fault at the output of the Fault Comparator is connected directly to the output drivers. This direct path reduces the propagation delay from the Fault Input to the A and B outputs to typically 70 ns. The Fault Latch output is OR'd with UVLO output from the V_{ref} UVLO comparator to produce the logic output labeled UVLO + Fault. This signal disables the Oscillator and One−Shot by forcing both the C_{OSC} and C_T capacitors to be continually charged.

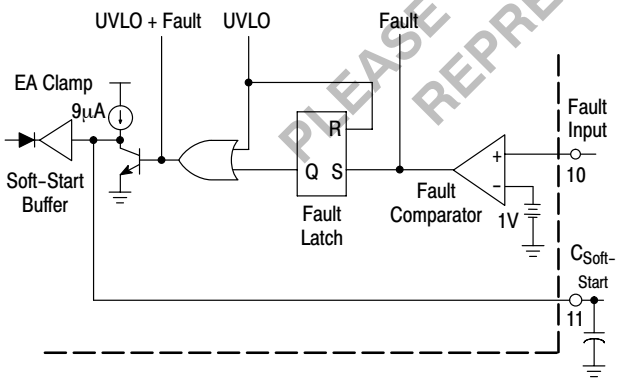


Figure 8. Fault Detector and Soft−Start

The Fault Latch is reset during startup by a logic one at the UVLO output of the V_{ref} UVLO comparator. The latch can also be reset after startup by pulling the Enable/UVLO Adjust pin momentarily low to disable the Reference Regulator.

Soft−Start Circuit

The Soft−Start circuit shown in Figure 8 forces the variable frequency Oscillator to start at the minimum frequency and ramp upward until regulated by the feedback control loop. The external capacitor at the $C_{Soft-Start}$ terminal is initially discharged by the UVLO + Fault signal. The low voltage on the capacitor pass through the Soft−Start Buffer to hold the Error Amplifier output low. After UVLO + Fault switches to a logic zero, the soft−start capacitor is charged by a 9.0 μA current source. The buffer allows the Error Amplifier output to follow the soft−start capacitor until it is regulated by the Error Amplifier inputs (or reaches the 2.5 V clamp). The soft−start function is generally applicable to controllers operating below resonance and can be disabled by simply opening the $C_{Soft-Start}$ terminal.

APPLICATIONS

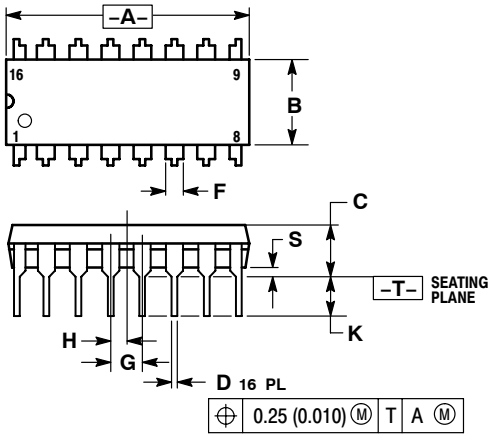
The MC34066 can be used for the control of series, parallel or higher order half/full bridge resonant converters. The IC is designed to provide control in discontinuous conduction mode (DCM) or continuous conduction mode (CCM) or a combination of the two. For example, in a parallel resonant converter (PRC) operating in the DCM, the IC is programmed to operate in fixed on−time, variable frequency mode of operation. For a PRC operating in the CCM, the IC can be programmed to operate in the variable frequency mode with a fixed off−time.

When operating with a wide input voltage range, such as a universal input power supply, a PRC can operate in the DCM for high input voltage and in the CCM for low input voltage. In this particular case, on−time is programmed corresponding to DCM. The deadtime of the chip is programmed to provide the desired off−time in the CCM. The frequency range is chosen to cover the complete frequency range from the DCM to the CCM. When programmed as such, the controller will operate in the fixed on−time, variable frequency mode at low frequencies. At the frequency which causes the Oscillator to retrigger the One−Shot, the control law changes to variable frequency with fixed off−time. At higher frequencies the supply will operate in the CCM with this control law.

Although the IC is designed and optimized for double ended push−pull type converters, it can also be used for single ended applications, such as forward and flyback resonant converters.

PACKAGE DIMENSIONS

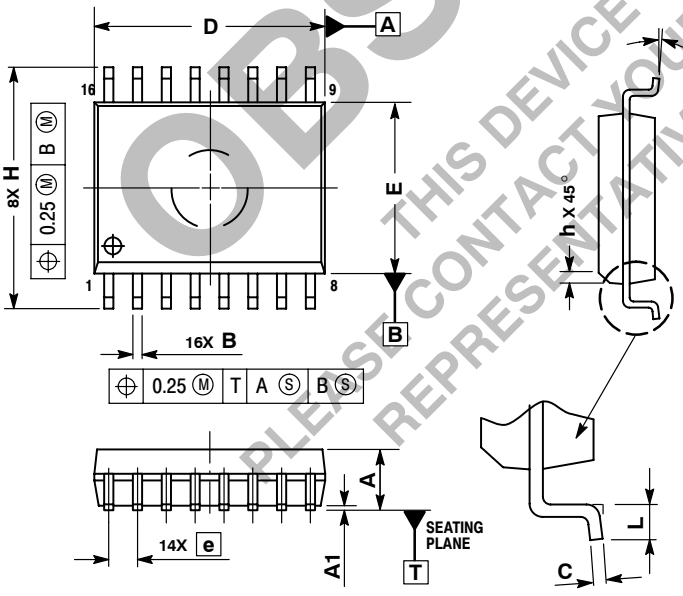
PDIP−16
P SUFFIX
CASE 648−08
ISSUE R



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0 °	10 °	0 °	10 °
S	0.020	0.040	0.51	1.01

SO−16W
DW SUFFIX
CASE 751G−03
ISSUE B



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INLCUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0 °	7 °

PUBLICATION ORDERING INFORMATION

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MC34066/D