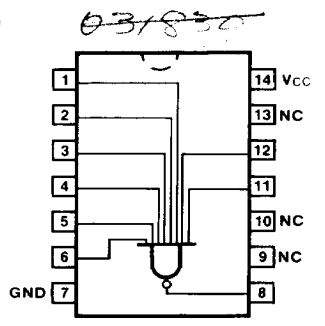


✓ 54/7430 010117 031680  
 ✓ 54H/74H30 010120  
 ✓ 54S/74S30 010121  
 ✓ 54LS/74LS30 010119  
**8-INPUT NAND GATE**

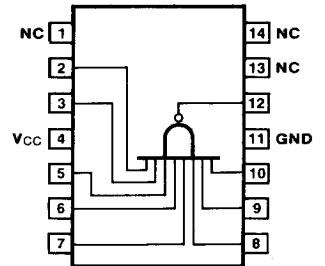
**CONNECTION DIAGRAMS  
 PINOUT A**



**ORDERING CODE:** See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V <sub>CC</sub> = +5.0 V ±5%, T <sub>A</sub> = 0°C to +70°C	V <sub>CC</sub> = +5.0 V ±10%, T <sub>A</sub> = -55°C to +125°C	
Plastic DIP (P)	A	7430PC, 74H30PC 74S30PC, 74LS30PC		9A
Ceramic DIP (D)	A	7430DC, 74H30DC 74S30DC, 74LS30DC	5430DM, 54H30DM 54S30DM, 54LS30DM	6A
Flatpak (F)	A	74S30FC, 74LS30FC	54S30FM, 54LS30FM	3I
	B	7430FC, 74H30FC	5430FM, 54H30FM	

**PINOUT B**



**INPUT LOADING/FAN-OUT:** See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74H (U.L.) HIGH/LOW	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	1.25/1.25	1.25/1.25	0.5/0.25
Outputs	20/10	12.5/12.5	25/12.5	10/5.0 (2.5)

**DC AND AC CHARACTERISTICS:** See Section 3\*

SYMBOL	PARAMETER	54/74	54/74H	54/74S	54/74LS	UNITS	CONDITIONS	
		Min Max	Min Max	Min Max	Min Max			
I <sub>CC</sub> H	Power Supply Current	2.0	4.2	5.0	0.5	mA	V <sub>IN</sub> = Gnd	V <sub>CC</sub> = Max
I <sub>CC</sub> L	Current	6.0	10	10	1.1		V <sub>IN</sub> = Open	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay	22 15	10 12	2.0 6.0 2.0 7.0	12 20	ns	Figs. 3-1, 3-4	

\*DC limits apply over operating temperature range; AC limits apply at T<sub>A</sub> = +25°C and V<sub>CC</sub> = +5.0 V.