RTL8208B-LF
RTL8208BF-LF

SINGLE-CHIP OCTAL 10/100BASE-TX/FX PHY TRANSCEIVER

DATASHEET

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USING THIS DOCUMENT

This document is intended for the engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2003/12/16	Draft release.
1.1	2004/08/30	First approved release.
1.2	2004/08/31	Change bias resistor value to 2K ohm in Figure 22 on page 49.
1.3	2006/09/22	1. Add Fiber Application information for RTL8208BF-LF. 2. Modify Figure 1, page 3, and Figure 2, page 4. 3. Modify Table 1. Pin Assignments, on page 5. 4. Modify Table 5. RMII/SMII/SS-SMII Pins, page 7. 5. Corrected SMI Clock frequency from 25MHz to 2.5MHz (Table 6, page 9, section 7.1.1, page 26, and Table 40, page 52). 6. Recommend LEDMODE Pin be pulled high or pulled low (see Table 8, page 10). 7. Add LED rise and fall timing (Figure 16, page 42). 8. Change 2SB1188 to 2SB1182 (Figure 20 and Table 35, page 47). 9. Modify Table 36. Absolute Maximum Ratings, and Table 37. Operating Range, on page 50. 10. Add power startup internal sequence (section 9.6 Power Start Up & Internal Reset Sequence, page 56). 11. Modify section 10 Mechanical Dimensions, page 58. 12. Modify section 11 Ordering Information, page 59.

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1. General Description

The RTL8208B-LF and RTL8208BF-LF (jointly referred to as the RTL8208B(F)-LF) are single-chip highly integrated 8-port, 10Base-T/100Base-TX (FX) Ethernet transceivers implemented in 0.18µm CMOS technology. They are currently the world's smallest Octal-PHY chip package. Realtek patented removal of traditional SD pins in 100Base-FX (RTL8208BF-LF only) allow us to obtain a lower pin-count. Flexible hardware settings are provided to configure the various operating modes of the chip.

The RTL8208B(F)-LF provides 8 separate and independent channels. Each channel consists of an RMII/SMII/SS-SMII interface-to-MAC controller, and hardware pins are used to configure the interface for RMII, SMII, or SS-SMII mode. In RMII mode, another hardware pin is used to set Port-Pair Loopback mode (PP-LPBK MODE, RTL8208BF-LF only), which can extend physical transmission length and perform physical media transport operations without a switch controller.

A PECL (Pseudo Emitter Coupled Logic) receiver accepts input from a fiber transceiver and directly passed to a clock recovery circuit for data/clock recovery. The chip utilizes an advanced CMOS process to meet low voltage and low power requirements. With on-chip DSP (Digital Signal Processing) technology, the chip provides excellent performance under all operating conditions.

A built-in UTP cable tester diagnoses an open/short fault in an attached cable. The RTL8208B(F)-LF also features very low power consumption (maximum of 1.6W). Additionally, pin-outs are designed to provide optimized direct routing, which simplifies the layout work and reduces EMI noise issues.

2. Features

- Supports 8-port integrated physical layer and transceiver for 10Base-T and 100Base-TX
- Up to 8 ports support 100Base-FX (RTL8208BF-LF only)
- Reduced 100Base-FX (RTL8208BF-LF only) interface (patented)
- Robust baseline wander correction for improved 100Base-TX performance
- Complies with IEEE 802.3/802.3u
- IEEE 802.3u compliant auto negotiation for 10/100Mbps control
- Hardware controlled Flow control advertisement ability
- Supports RMII/SMII/SS-SMII interfaces
- Very low power consumption
- Supports Port-Pair Loopback mode (PP-LPBK mode, RTL8208BF-LF only)
- Supports two power reduction methods:
  - Power saving mode (cable detection)
  - Power down mode
- Power-on auto reset function eliminates the need for external reset circuits
- Crossover detection and auto correction
- Polarity detection and Auto Correction
- Flexible serial/scan LED display modes
- Cable tester for diagnosing open/short faults in attached cables
- 128-pin QFP package
- 1.8V/3.3V power supply
- 0.18µm, CMOS technology

3. Applications

RTL8208B-LF

- Octal PHY for Fast Ethernet switch with twisted pair interface

RTL8208BF-LF

- Octal PHY for Fast Ethernet switch with twisted pair interface and fiber capability

4. Pin Assignments

4.1. Pin Assignments (RTL8208B-LF)

Octal PHY for Fast Ethernet Switch with Twisted Pair Interface

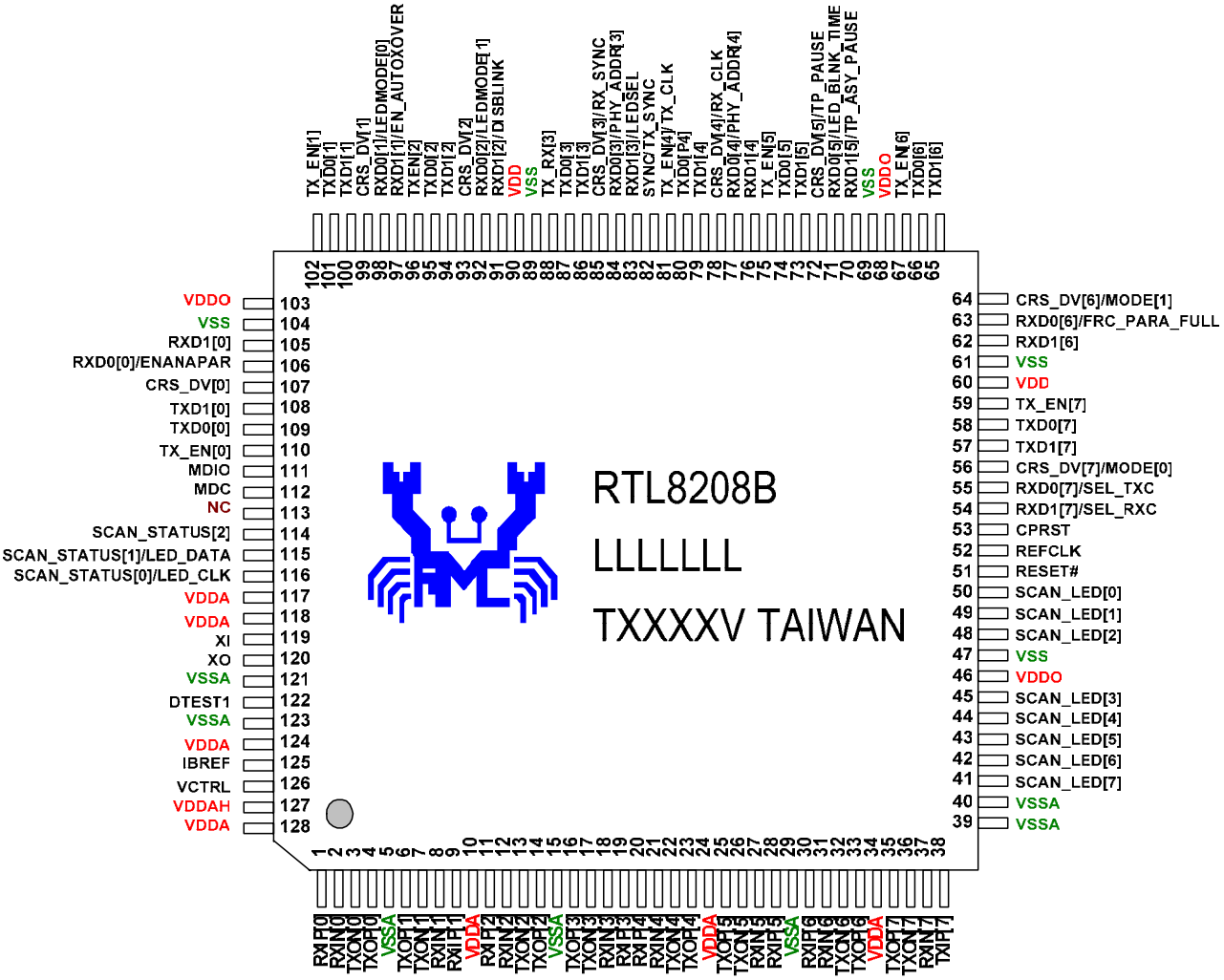


Figure 1. Pin Assignments (RTL8208B-LF)

Note: Signal type codes are listed in section 5 Pin Descriptions, page 6.

4.2. Lead (Pb)-Free Package Identification

Lead (Pb)-free package is indicated by an 'L' in the location marked 'T' in Figure 1.

4.3. Pin Assignments (RTL8208BF-LF)

Octal PHY for Fast Ethernet Switch with Twisted Pair Interface and Fiber Capability

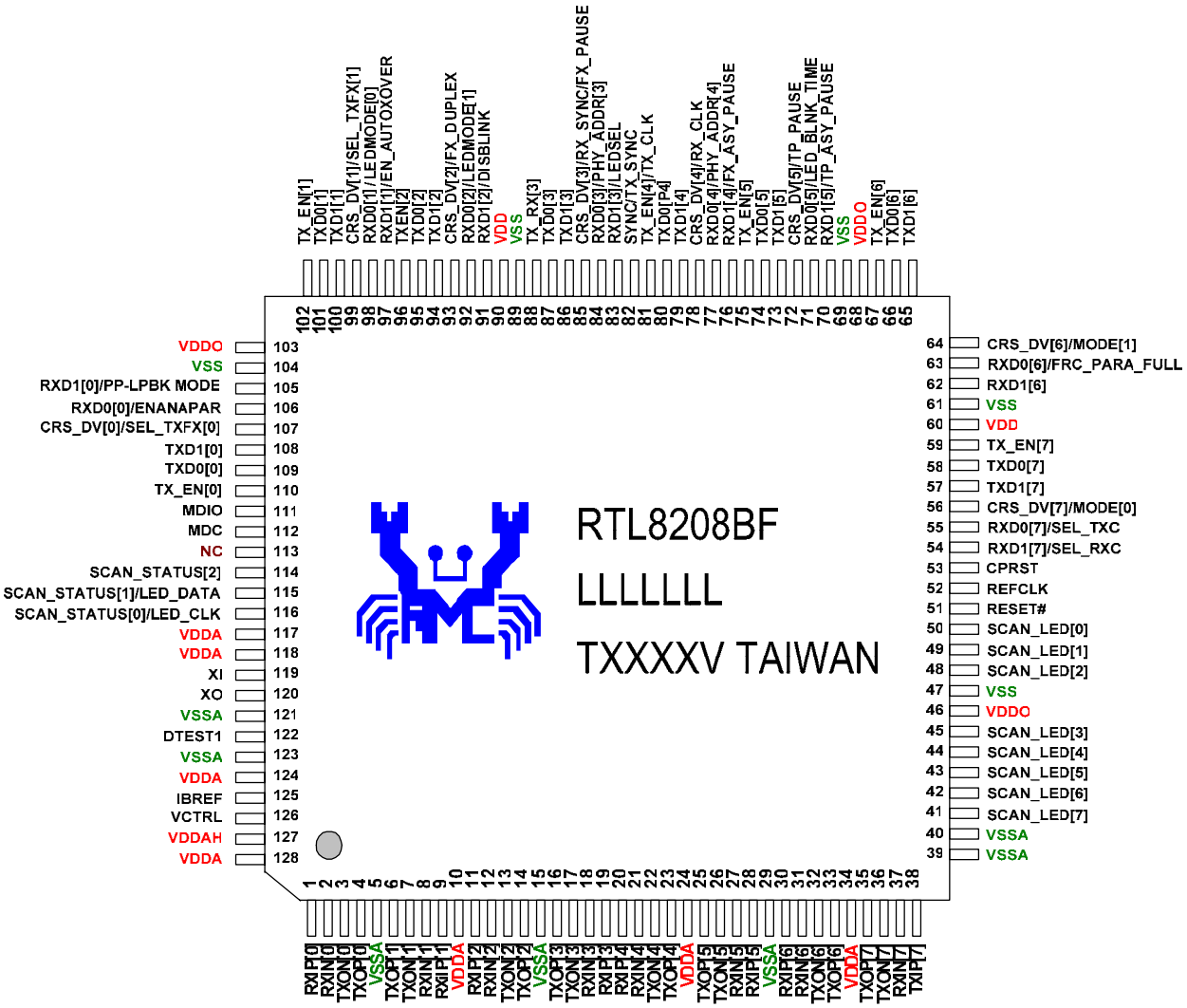


Figure 2. Pin Assignments (RTL8208BF-LF)

Note: Signal type codes are listed in section 5 Pin Descriptions, page 6.

4.4. Lead (Pb)-Free Package Identification

Lead (Pb)-free package is indicated by an 'L' in the location marked 'T' in Figure 2.

Table 1. Pin Assignments

Pin Name	Pin#	Function	Driver Capacity	Pin Name	Pin#	Type	Driver Capacity
RXIP[0]	1	AI	-	TXD1[6]	65	I,ND	-
RXIN[0]	2	AI	-	TXD0[6]	66	I,ND	-
TXON[0]	3	AO	-	TX_EN[6]	67	I,ND	-
TXOP[0]	4	AO	-	VDDO	68	DP	-
VSSA	5	AG	-	VSS	69	DG	-
TXOP[1]	6	AO	-	RXD1[5]/ TP_ASY_PAUSE	70	I/O,Pd	8mA
TXON[1]	7	AO	-	RXD0[5]/ LED_BLNK_TIME	71	I/O,Pu	8mA
RXIN[1]	8	AI	-	CRS_DV[5]/ TP_PAUSE	72	I/O,Pu	8mA
RXIP[1]	9	AI	-	TXD1[5]	73	I,ND	-
VDDA	10	AP	-	TXD0[5]	74	I,ND	
RXIP[2]	11	AI	-	TX_EN[5]	75	I,ND	-
RXIN[2]	12	AI	-	RXD1[4]/ FX_ASY_PAUSE	76	I/O,Pd	8mA
TXON[2]	13	AO	-	RXD0[4]/ PHY_ADDR[4]	77	I/O,Pd	8mA
TXOP[2]	14	AO	-	CRS_DV[4]/ RX_CLK	78	I/O,ND	16mA
VSSA	15	AG	-	TXD1[4]	79	I,ND	-
TXOP[3]	16	AO	-	TXD0[4]	80	I,ND	-
TXON[3]	17	AO	-	TX_EN[4]/ TX_CLK	81	I,ND	-
RXIN[3]	18	AI	-	SYNC/TX_SYNC	82	I,Pd	-
RXIP[3]	19	AI	-	RXD1[3]/ LEDSEL	83	I/O,Pd	8mA
RXIP[4]	20	AI	-	RXD0[3]/ PHY_ADDR[3]	84	I/O,Pu	8mA
RXIN[4]	21	AI	-	CRS_DV[3]/RX_SYNC/ FX_PAUSE	85	I/O,Pu	8mA
TXON[4]	22	AO	-	TXD1[3]	86	I,ND	-
TXOP[4]	23	AO	-	TXD0[3]	87	I,ND	-
VDDA	24	AP	-	TX_EN[3]	88	I,ND	-
TXOP[5]	25	AO	-	VSS	89	DG	-
TXON[5]	26	AO	-	VDD	90	DP	-
RXIN[5]	27	AI	-	RXD1[2]/ DISBLINK	91	I/O,Pd	8mA
RXIP[5]	28	AI	-	RXD0[2]/ LEDMODE[1]	92	I/O,Pd	8mA
VSSA	29	AG	-	CRS_DV[2]/ FX_DUPLEX	93	I/O,Pu	8mA
RXIP[6]	30	AI	-	TXD1[2]	94	I,ND	-
RXIN[6]	31	AI	-	TXD0[2]	95	I,ND	-
TXON[6]	32	AO	-	TX_EN[2]	96	I,ND	-
TXOP[6]	33	AO	-	RXD1[1]/ EN_AUTOXOVER	97	I/O,Pu	8mA
VDDA	34	AP	-	RXD0[1]/ LEDMODE[0]	98	I/O,Pd	8mA
TXOP[7]	35	AO	-	CRS_DV[1]/ SEL_TXFX[1]	99	I/O,Pd	8mA
TXON[7]	36	AO	-	TXD1[1]	100	I,ND	-
RXIN[7]	37	AI	-	TXD0[1]	101	I,ND	-
RXIP[7]	38	AI	-	TX_EN[1]	102	I,ND	-
VSSA	39	AG	-	VDDO	103	DP	-
VSSA	40	AG	-	VSS	104	DG	-
SCAN_LED[7]	41	O,Pu	8mA	RXD1[0]/ PP-LPBK MODE	105	I/O,Pd	8mA
SCAN_LED[6]	42	O,Pu	8mA	RXD0[0]/ ENANAPAR	106	I/O,Pd	8mA
SCAN_LED[5]	43	O,Pu	8mA	CRS_DV[0]/ SEL_TXFX[0]	107	I/O,Pd	8mA
SCAN_LED[4]	44	O,Pu	8mA	TXD1[0]	108	I,ND	-
SCAN_LED[3]	45	O,Pu	8mA	TXD0[0]	109	I,ND	-
VDDO	46	DP	-	TX_EN[0]	110	I,ND	-
VSS	47	DG	-	MDIO	111	I/O,Pu	8mA
SCAN_LED[2]	48	O,Pu	8mA	MDC	112	I,Pd	-
SCAN_LED[1]	49	O,Pu	8mA	NC	113	-	-
SCAN_LED[0]	50	O,Pu	8mA	SCAN_STATUS[2]	114	O,Pu	8mA
RESET#	51	I,Pu	-	SCAN_STATUS[1] /LED_DATA	115	O,Pu	8mA
REFCLK	52	I/O,Pd	8mA	SCAN_STATUS[0] /LED_CLK	116	O,Pu	8mA
CPRST	53	I,Pd	-	VDDA	117	AP	-
RXD1[7]/ SEL_RXC	54	I/O,Pd	8mA	VDDA	118	AP	-
RXD0[7]/ SEL_TXC	55	I/O,Pd	8mA	XI	119	I,ND	-
CRS_DV[7]/ MODE[0]	56	I/O,Pu	8mA	XO	120	O,ND	-
TXD1[7]	57	I,ND	-	VSSA	121	AG	-
TXD0[7]	58	I,ND	-	DTEST1	122	I/O,ND	-
TX_EN[7]	59	I,ND	-	VSSA	123	AG	-
VDD	60	DP	-	VDDA	124	AP	-
VSS	61	DG	-	IBREF	125	AO	-
RXD1[6]	62	I/O,Pd	8mA	VCTRL	126	AO	-
RXD0[6]/ FRC_PARA_FULL	63	I/O,Pd	8mA	VDDAH	127	AP	
CRS_DV[6]/ MODE[1]	64	I/O,Pu	8mA	VDDA	128	AP	-

5. Pin Descriptions

In order to reduce pin count, and therefore size and cost, some pins have multiple functions. In such cases the functions are separated with a " / " symbol. For the RTL8208B-LF refer to Figure 1, page 3; for the RTL8208BF-LF refer to Figure 2, page 4, for a graphical representation.

Signal type codes shown below are used in the previous and following tables:

I:	Input	P:	Power
O:	Output	G:	Ground
A:	Analog signal	Pu:	Internal pull up (30K ohm)
D:	Digital signal	Pd:	Internal pull down (30K ohm)
ND:	Not defined		

5.1. Media Connection Pins

Table 2. Media Connection Pins

Pin Name	Pin	Type	Description
RXIP[7:0]	38, 30, 28, 20, 19, 11 , 9, 1	AI	Receiver Input. Differential positive signal shared by 100Base-TX, 100Base-FX, and 10Base-T.
RXIN[7:0]	37, 31, 27, 21, 18, 12, 8, 2	AI	Receiver Input. Differential negative signal shared by 100Base-TX, 100Base-FX, and 10Base-T.
TXOP[7:0]	35, 33, 25, 23, 16, 14, 6, 4	AO	Transmitter Output. Differential positive signal shared by 100Base-TX, 100Base-FX, and 10Base-T.
TXON[7:0]	36, 32, 26, 22, 17, 13, 7, 3	AO	Transmitter Output. Differential negative signal shared by 100Base-TX, 100Base-FX, and 10Base-T.

5.2. Power and Ground Pins

Table 3. Power and Ground Pins

Pin Name	Pin	Type	Description
VDDA	10, 24, 34, 117, 118, 124, 128	AP	1.8V Power to analog.
VDDAH	127	AP	3.3V Power to regulator.
VSSA	5, 15, 29, 39, 40, 121, 123	AG	Analog ground.
VDD	60, 90	DP	1.8V Power to digital core.
VDDO	46, 68, 103	DP	3.3V Power to digital I/O.
VSS	47, 61, 69, 89, 104	DG	Digital ground.

5.3. Miscellaneous Pins

Table 4. Miscellaneous Pins

Pin Name	Pin	Type	Description
RESET#	51	I, (Pu)	Reset. This is an active low input. To complete the reset function, this pin must be asserted low for at least 10ms.
XI	119	I	25MHz Crystal input or 25MHz Oscillator clock input. The clock tolerance is ±50ppm. When XI is pulled low, XO must be floating. REFCLK will then be the chip clock input.
XO	120	O	25MHz Crystal output.
REFCLK	52	I/O (Pd)	Reference clock. If XI is 25MHz active, REFCLK is a 50MHz output. If XI is pulled-low (disabled), REFCLK is a clock input as described below: RMII mode = 50MHz ±50ppm clock input SMII/SS-SMII mode = 125MHz ±50ppm clock input. Pin driver capacity = 8mA.
IBREF	125	AO	Reference Bias Resistor. When using a 1:1 transformer on Tx/Rx, this pin must be tied to analog ground through an external 2KΩ resistor.
VCTRL	126	AO	Voltage control. This pin controls a PNP transistor to generate the 1.8V power supply for VDD and VDDA pins.
NC	113		Not Connected.

5.4. RMII/SMII/SS-SMII Pins

Table 5. RMII/SMII/SS-SMII Pins

Pin Name	Pin	Type	Description
TXD0[7:0]	58, 66, 74, 80, 87, 95, 101, 109	I	Transmit Data Input (bit 0). RMII: TXD0 and TXD1 are the di-bits input, transmitted and driven synchronously to REFCLK from the MAC. SMII: TXD0 inputs the data that is transmitted and is driven synchronously to REFCLK. In 100Mbps, TXD0 inputs a new 10-bit segment starting with SYNC. In 10Mbps, TXD0 must repeat each 10-bit segment 10 times. SS-SMII: TXD0 behaves as SMII except synchronous to TX_CLK instead of REFCLK and inputs a new 10-bit segment starting with TX_SYNC instead of SYNC.
TXD1[7:0]	57, 65, 73, 79, 86, 94, 100, 108	I	Transmit Data Input (bit 1). RMII: TXD1 and TXD0 are the input di-bits synchronously to REFCLK. SMII/SS-SMII: The I/O pin of TX_EN should not be used.

Pin Name	Pin	Type	Description
TX_EN[7:0] TX_CLK/TX_EN[4]	59, 67, 75, 81, 88, 96, 102, 110	I	Transmit Enable. RMII: TX_EN indicates the di-bits on TXD is valid and is synchronous to REFCLK. SMII: The I/O pin of TX_EN should not be used. SS-SMII: TX_EN[4] of RMII is used as TX_CLK, which is a 125MHz clock input from MAC. The I/O pin of TX_EN should not be used.
RXD0[7:0]	 55 63 71 77 84 92 98 106	O (Pd) (Pd) (Pu) (Pd) (Pu) (Pd) (Pd) (Pd)	Receive Data Input (bit 0). RMII: RXD0 and RXD1 output di-bits synchronously to REFCLK. SMII: RXD0 outputs data or in-band management information synchronously to REFCLK. In 100Mbps, RXD0 outputs a new 10-bit segment starting with SYNC. In 10Mbps, RXD0 must repeat each 10-bit segment 10 times. SS-SMII: RXD0 behaves as SMII except synchronous to RX_CLK instead of REFCLK and inputs a new 10-bit segment starting with RX_SYNC instead of SYNC. All pins driver capacity = 8mA
RXD1[7:0]	 54 62 70 76 83 91 97 105	O (Pd) (Pd) (Pd) (Pd) (Pd) (Pd) (Pu) (Pd)	Receive Data Input (bit 1). RMII: RXD1 and RXD0 output di-bits synchronously to REFCLK. SMII/SS-SMII: The I/O pin of RXD1 should not be used. All pins driver capacity = 8mA
CRS_DV[7:0] RX_SYNC/CRS_DV[3] RX_CLK/CRS_DV[4]	 56 64 72 78 (16mA) 85 93 99 07	O (Pu) (Pu) (Pu) (ND) (Pu) (Pu) (Pd) (Pd)	Carrier Sense and Data Valid. RMII: CRS_DV is asynchronous to REFCLK and asserts when the medium is non-idle. SMII: CRS_DV[7:0] are not used and driven low. SS-SMII: CRS_DV[3] of RMII is used as RX_SYNC which is a sync signal used to delimit the 10-bit segment of RXD0 for all ports. CRS_DV[4] of RMII is used as RX_CLK, which is a 125MHz clock output. CRS_DV[7:5] and CRS_DV[2:0] are not used. All pins driver capacity = 8mA, except pin 78 (16mA).
SYNC/ TX_SYNC	82	I (Pd)	Sync/Transmit Synchronous. SMII: SYNC is a sync signal used to delimit a 10-bit segment of RXD0 and TXD0 for all ports. SS-SMII: TX_SYNC is a sync signal used to delimit the 10-bit segment of TXD0 for all ports.

5.5. SMI (Serial Management Interface)

Table 6. SMI (Serial Management Interface)

Pin Name	Pin	Type	Description
MDIO	111	I/O, (Pu)	Management Data I/O. Bi-directional data interface. A 1.5KΩ pull-up resistor is required (as specified in IEEE802.3u). The MAC controller access of the MII registers should be delayed at least 700µs after completion of the reset because of the internal reset operation of the RTL8208B(F)-LF. Pin driver capacity = 8mA.
MDC	112	I, (Pd)	Management Data Clock. 0 to 2.5MHz clock sourced by MAC to sample MDIO. The MAC controller access of the MII registers should be delayed at least 700µs after completion of the reset because of the internal reset operation of the RTL8208B(F)-LF.

5.6. LED Pins

Table 7. LED Pins

Pin Name	Pin	Type	Description
SCAN_LED[7:0]	41, 42, 43, 44, 45, 48, 49, 50	O (Pu)	In scan LED mode, SCAN_LED[7:0] is the Scan LED port enable. See section 7.9 LED Configuration, page 38. All pins driver capacity = 8mA.
SCAN_STATUS[2:0] LED_CLK/SCAN_ STATUS[0] LED_DATA/SCAN_ STATUS[1]	114, 115, 116	O (Pu)	In scan LED mode, SCAN_STATUS[2:0] outputs (Col/Fulldup, Link/Act, Spd) for each port. In serial LED mode, SCAN_STATUS[0] is used as LED_CLK, which outputs the reference clock for the serial LED signals. In serial LED mode, SCAN_STATUS[1] is used as LED_DATA, which outputs serial status bits that can be shifted into a shift register to be displayed via LEDs. LED_DATA is output synchronously to LED_CLK. All pins driver capacity = 8mA.

5.7. Mode Control Pins

Table 8. Mode Control Pins

Pin Name	Pin	Type	Description
SEL_TXFX[1:0]/ CRS_DV[1:0]	99, 107	I/O, (Pd, Pd)	Select 10/100BaseTX or 100BaseFX (default = 2'b00). If PP-LPBK MODE = 0: 2'b00: All 8 ports (port0~port7) are 10Base-T/100Base-TX. 2'b01: Port 7 is 100FX, other ports are 10Base-T/100Base-TX. 2'b10: Ports 6 & 7 are 100FX, other ports are 10Base-T/ 100Base-TX. 2'b11: All 8 ports are 100Base-FX. If PP-LPBK MODE =1: 2'b00: All 8 ports (port0~port7) are 10Base-T/100Base-TX. 2'b01: Port 7 and 5 are 100FX, others are 10Base-T/100Base-TX. 2'b10: Ports 1, 3, 5 & 7 are 100FX, others are 10Base-T/100Base-TX. 2'b11: All 8 ports are 100Base-FX. *Note: RTL8208BF-LF only.*
PP-LPBK MODE/ RXD1[0]	105	I/O, (Pd)	Port-Pair Loopback mode (default =0). Upon power-on reset, this pin is input to assert PP-LPBK MODE. When set, all eight ports are port-pair looped back, acting like a signal regeneration/transformation repeater. See section 7.1.2 Port Pair-Loop Back Mode (PP-LPBK), page 26, covering PP-LPBK MODE. *Note: RTL8208BF-LF only.*
PHY_ADDR[4:3]/ RXD0[4:3]	77, 84	I/O, (Pd, Pu)	PHY Address (default = 2'b01). These 2 bits determine the highest 2 bits of the 5-bit PHY address upon reset. We recommend using a resistor to pull up or pull down.
MODE[1:0]/ CRS_DV[6:7]	64, 56	I/O, (Pu,Pu)	Select RMII/SMII/SS-SMII mode (default = 2'b11). 2'b1x: RMII 2'b00: SMII 2'b01: SS-SMII We recommend using a resistor to pull up or pull down.
TP_PAUSE/ CRS_DV[5]	72	I/O, (Pu)	Twisted Pair Pause capability (default =1). Sets the Flow control ability of Reg.4.10 for UTP ports upon power-on reset. 1: With flow control ability 0: Without flow control ability
FX_PAUSE/ CRS_DV[3]	85	I/O, (Pu)	100Base-FX Flow control capability (default =1). Forces the flow control capability of Reg.4.10 and Reg.5.10 upon power-on reset. 1: With flow control ability in 100Base-FX 0: Without flow control ability in 100Base-FX *Note: RTL8208BF-LF only.*
TP_ASY_PAUSE/ RXD1[5]	70	I/O, (Pd)	Twisted Pair Asymmetric Pause capability (default =0). Sets the Asymmetric Flow control ability of Reg.4.11 for UTP ports upon power-on reset. 1: With asymmetric flow control ability 0: Without asymmetric flow control ability.

Pin Name	Pin	Type	Description
FX_ASY_PAUSE/ RXD1[4]	76	I/O, (Pd)	100Base-FX Asymmetric Flow control capability (default =0). Forces the asymmetric flow control capability of Reg.4.11 and Reg.5.11 upon power-on reset. 1: Asymmetric flow control ability in 100Base-FX 0: No asymmetric flow control ability in 100Base-FX *Note: RTL8208BF-LF only.*
FX_DUPLEX/ CRS_DV[2]	93	I/O, (Pu)	FX_DUPLEX: Force 100Base-FX Full Duplex Mode (default =1). This pin sets 100Base-FX duplex and affects those ports in 100Base-FX mode. 1: Full duplex 0: Half duplex Upon reset, this pin sets the default values of Reg.0.8 of those ports in 100Base-FX. *Note: RTL8208BF-LF only.*
EN_AUTOXOVER/ RXD1[1]	97	I/O, (Pu)	Enable Auto Crossover Detection (default =1). 1: Enable auto crossover detection 0: Disable auto crossover detection
DISBLINK/ RXD1[2]	91	I/O, (Pd)	Disable power-on/reset LED blinking: (default = 0) 1: Disable power-on LED blinking 0: Blink
LED_BLNK_TIME/ RXD0[5]	71	I/O, (Pu)	LED Blink Time (default =1). Controls the blinking speed of activity and collision LEDs. 1: 43ms (recommended to use external 10K pull up resistor) 0: 120ms
LEDSEL/RXD1[3]	83	I/O, (Pd)	LED Selection (default=1'b0). LEDSEL 1'b1: Scan LED 1'b0: Serial LED
LEDMODE[1:0]/ RXD0[2:1]	92, 98	I/O, (Pd, Pd)	LEDMODE[1:0] (default = 00). When using the RTL8208B(F)-LF LED solution , we recommend using an external resister to pull high or pull low. In Serial LED, LEDMODE[1:0] controls the forms of serial LED status. LEDMODE Mode Output 2'b00 3-bit serial stream Col/Fulldup, Link/Act, Spd 2'b01 2-bit serial stream Spd, Link/Act 2'b10 3-bit for Bi-color LED Col/Fulldup, Link/Act, Spd 2'b11 1-bit serial stream Link/Act/Spd In Scan LED, LEDMODE[1:0] controls the output of SCAN_STATUS[2:0]. LEDMODE Mode Output 2'b00 Mode 0 Col/Fulldup, Link/Act, Spd 2'b01 Mode 1 RX, TX, Link 2'b10 Mode 2 NC, Bi-color Link/Act/Spd, NC 2'b11 Reserved
FRC_PARA_FULL/ RXD0[6]	63	I/O (Pd)	Force full duplex when link is established by parallel detection (default=0). 1: Force full duplex when link is established by parallel detection 0: Normal operation

Pin Name	Pin	Type	Description
SEL_RXC/RXD1[7]	54	I/O (Pd)	In SMII, SEL_RXC control the clock to output delay of RXD. 0: Clock out data on falling edge of receive clock 1: Clock out data on rising edge of receive clock Recommended to set SEL_RXC=1. In SS-SMII, SEL_RXC, must be set to 1.
SEL_TXC/RXD0[7]	55	I/O (Pd)	In SMII, SEL_TXC control the clock to output delay of TXD. 0: Clock out data on falling edge of transmit clock 1: Clock out data on rising edge of transmit clock Recommended to set SEL_TXC=1. In SS-SMII, SEL_TXC, must be set to 1.

5.8. Test Pins

Table 9. Test Pins

Pin Name	Pin	Type	Description
ENANAPAR/ RXD0[0]	106	I/O, (Pd)	Enable analog parameter write (default =0). 1: Enable analog parameter write operation 0: Disable analog parameter write operation
CPRST	53	I, (Pd)	Reserved for internal use. Must be left floating.
DTEST1	122	I/O	Reserved for internal use. Must be left floating.

6. Register Descriptions

The first six registers of the MII are defined by the MII specification. Other registers are defined by Realtek for internal use.

Signal type codes below are used in the following tables:

RO:	Read Only	LL:	Latch Low until cleared
RW:	Read/Write	LH:	Latch High until cleared
SC:	Self Clearing		

Table 10. Register Descriptions

Register	Description
0	Control Register.
1	Status Register.
2	PHY Identifier 1 Register.
3	PHY Identifier 2 Register.
4	Auto-Negotiation Advertisement Register.
5	Auto-Negotiation Link Partner Ability Register.
6	Auto-Negotiation Expansion Register.

6.1. Register0: Control

Table 11. Register0: Control

Reg. bit	Name	Description	Type	Default
0.15	Reset	1: PHY reset. This bit is self-clearing.	RW/SC	0
0.14	Loopback	This will loopback TXD to RXD and ignore all activity on the cable media. 1: Enable loopback 0: Normal operation	RW	0
0.13	Spd_Sel	When NWay is enabled, this bit reflects the auto negotiation result (Read Only). When NWay is disabled, this bit can be set by SMI*. (Read/Write). When 100FX is enabled, this bit =1 (Read Only). 1: 100Mbps 0: 10Mbps	RW	0
0.12	Auto Negotiation Enable	This bit can be set through SMI (Read/Write). When 100FX is enabled, this bit =0 (Read only). 1: Enable auto negotiation process 0: Disable auto negotiation process	RW	1 (0 for 100FX)
0.11	Power Down	1: Power down. All functions will be disabled except SMI read/write function 0: Normal operation	RW	0
0.10	Isolate	1: Electrically isolate the PHY from RMII/SMII/SS-SMII. PHY is still able to respond to MDC/MDIO 0: Normal operation	RW	0
0.9	Restart Auto Negotiation	1: Restart Auto-Negotiation process 0: Normal operation	RW/SC	0
0.8	Duplex Mode	When NWay is enabled, this bit reflects the result of auto negotiation (Read Only). When NWay is disabled, this bit can be set by SMI* (Read/Write). When 100FX is enabled, this bit is determined by the FX_DUPLEX pin (Read/Write). 1: Full duplex operation 0: Half duplex operation	RW	0
0.[7:0]	Reserved		RO	0

**SMI: Serial Management Interface composed of MDC, MDIO, that allows the MAC to manage the PHY.*

Reset – In order to reset the RTL8208B(F)-LF using software control, a '1' must be written to bit 15 using an SMI write operation. The bit clears itself after the reset process has completed. Writes to other Control register bits will have no effect until the reset process has completed (approximately 1μs). Writing a '0' to this bit has no effect. Because this bit is self-clearing after a few cycles from a write operation, it will return a '0' when read.

Loopback – The RTL8208B(F)-LF may be placed into loopback mode by writing a '1' to bit 14. Loopback mode may be cleared either by writing a '0' to bit 14 or by resetting the chip. When this bit is read, it will return a '1' when the chip is in software-controlled loopback mode, otherwise it will return a '0'.

Speed Selection – If auto negotiation is enabled, this bit has no effect on the speed selection. However, if auto negotiation is disabled using software control, the operating speed of the RTL8208B(F)-LF can be forced by writing the appropriate value to bit 13. Writing a '1' to this bit forces 100Base-X operation, while writing a '0' forces 10Base-T operation. When this bit is read, it returns the value of the software-controlled forced-speed selection only.

Auto Negotiation Enable – Default is auto negotiation enabled for all TP ports, and disabled for FX ports. Auto negotiation can be disabled via software control by setting 0.12=0.

Power Down – The RTL8208B(F)-LF supports a low power mode. Writing a '1' will enable power down mode, and writing a '0' will return the RTL8208B(F)-LF to normal operation. When read, this register will return a '1' when in power down mode, and a '0' during normal operation.

Isolate – Each PHY may be isolated from its MII by writing a '1' to bit 10. All MII outputs will be tri-stated and all MII inputs will be ignored. Since the MII management interface is still active, the isolate mode may be cleared either by writing a '0' to bit 10 or by resetting the chip. When this bit is read, it will return a '1' when the chip is in isolate mode, and return a '0' during normal operation.

Restart Auto Negotiation – Bit 9 is a self-clearing bit that allows the auto negotiation process to be restarted, regardless of the status of the auto negotiation state machine. In order for this bit to have an effect, auto negotiation must be enabled. Writing a '1' to this bit restarts auto negotiation. Writing a '0' to this bit has no effect. When this bit is read, it will always return a '0'.

Duplex Mode – By default, the RTL8208B(F)-LF powers up in half duplex mode. The chip can be forced into full duplex mode by writing a '1' to bit 8 while auto negotiation is disabled. Half duplex mode can be resumed either by writing a '0' to bit 8 or by resetting the chip. When NWay is enabled, this bit reflects the results of auto negotiation, and is in read-only mode. When NWay is disabled, this bit can be set through the SMI, and is in Read/Write mode. When 100FX is enabled, this bit can be set through the SMI or FX_DUPLEX pin and is in Read/Write mode.

Reserved Bits – All reserved MII register bits must be written as '0' at all times. Ignore the RTL8208B(F)-LF output when these bits are read.

6.2. Register1: Status

Table 12. Register1: Status

Reg. bit	Name	Description	Type	Default
1.15	100Base_T4	0: No 100Base-T4 capability (permanently =0)	RO	0
1.14	100Base_TX_FD	1: 100Base-TX full duplex capable 0: Not 100Base-TX full duplex capable	RO	1
1.13	100Base_TX_HD	1: 100Base-TX half duplex capable 0: Not 100Base-TX half duplex capable	RO	1
1.12	10Base_T_FD	1: 10Base-TX full duplex capable 0: Not 10Base-TX full duplex capable	RO	1
1.11	10Base_T_HD	1: 10Base-TX half duplex capable 0: Not 10Base-TX half duplex capable	RO	1
1.[10:7]	Reserved	Reserved.	RO	0
1.6	MF Preamble Suppression	The RTL8208B(F)-LF will accept management frames with preamble suppressed.	RO	1
1.5	Auto-negotiate Complete	1: Auto-negotiation process completed. Reg.4.5 are valid if this bit is set 0: Auto-negotiation process not completed	RO	0
1.4	Remote Fault	1: Remote fault indication from link partner has been detected. 0: No remote fault indication detected When in 100FX mode, this bit means in-band signal Far-End-Fault is detected. Refer to section 7.6.4 Far-End-Fault-Indication, page 32. This bit will remain set until it is cleared by reading register 1 via the management interface.	RO/LH	0
1.3	Auto-Negotiation Ability	1: NWay auto negotiation capable (permanently =1) 0: No auto negotiation capability	RO	1
1.2	Link Status	1: Link has not failed since previous read 0: Link has failed since previous read If the link fails, this bit will be set to 0 until read.	RO/LL	0
1.1	Jabber Detect	1: Jabber detected. 0: No Jabber detected The jabber function is disabled in 100Base-X mode. Jabber is supported only in 10Base-T mode.	RO/LH	0
1.0	Extended Capability	1: Extended register capable (permanently =1) 0: Not extended register capable	RO	1

100Base_T4 – The RTL8208B(F)-LF does not support the T4 function. Any reads to this bit will return a '0'.

100Base_TX_FD – The RTL8208B(F)-LF is capable of operating in 100Base-TX full duplex mode.

100Base_TX_HD – The RTL8208B(F)-LF is capable of operating in 100Base-TX half duplex mode.

10Base_T_FD – The RTL8208B(F)-LF is capable of operating in 10Base-T full duplex mode.

10Base_T_HD – The RTL8208B(F)-LF is capable of operating in 10Base-T half duplex mode.

Reserved – Ignore the output of the RTL8208B(F)-LF when these bits are read.

MF Preamble Suppression – Management Frame Preamble Suppression is permanently set in the RTL8208B(F)-LF, allowing subsequent MII management frames to be accepted, with or without the standard preamble pattern. Only two preamble bits are required between successive management commands, instead of the normal 32. However, a minimum of 32 preamble bits are required for the first SMI read/write transaction after reset. One idle bit is required between any two management transactions (as defined in the IEEE 802.3u spec). Reads of this bit will always return a '1'.

Auto-Negotiation Complete – Bit 5 will return a '1' if the auto negotiation process has been completed and the contents of registers 4 and 5 are valid.

Remote Fault – When the link partner detects a far-end fault, it sends a far-end indication stream pattern. When the RTL8208B(F)-LF receives this pattern, it sets Reg1.4=1.

Auto-Negotiation Ability – The RTL8208B(F)-LF is capable of performing IEEE auto negotiation, and will return a '1' when bit 4 is read, regardless of whether or not the auto negotiation function has been disabled.

Link Status – The RTL8208B(F)-LF will return a '1' on bit 2 when the link state machine is in Link Pass, indicating that a valid link has been established. Otherwise, it will return '0'. When a link failure occurs after the link pass state has been entered, the Link Status bit will be latched at '0' and will remain so until the bit is read. After the bit is read, it becomes '1' if the Link Pass state has been entered again.

Jabber Detect – The RTL8208B(F)-LF will return a '1' on bit 1 if a jabber condition has been detected. After the bit is read, or if the chip is reset, it reverts to '0'. This is for 10Base-T only. Jabber occurs when a predefined excessively long packet is detected in 10Base-T mode. When the duration of TX_EN exceeds the jabber timer (21ms), transmit and loopback functions are disabled and the COL LED starts blinking. After TX_EN goes low for more than 500ms, the transmitter is re-enabled and the COL LED stops blinking.

Extended Capability – The RTL8208B(F)-LF supports extended capability registers and will return a '1' when bit 0 is read. Several extended registers have been implemented in the RTL8208B(F)-LF.

6.3. Register2: PHY Identifier 1 Register

The PHY Identifier Registers #1 and #2 together form a unique identifier for the PHY section of this device. The Identifier consists of a concatenation of the Organizationally Unique Identifier (OUI), the vendor's model number, and the model revision number. A PHY may return a value of zero in each of the 32 bits of the PHY Identifier if desired. The PHY Identifier is intended to support network management.

Table 13. Register2: PHY Identifier 1 Register

Reg. bit	Name	Description	Type	Default
2.[15:0]	OUI	Composed of the 3rd to 18th bits of the Organizationally Unique Identifier (OUI).	RO	001C h

6.4. Register3: PHY Identifier 2 Register

Table 14. Register3: PHY Identifier 2 Register

Reg. bit	Name	Description	Type	Default
3.[15:10]	OUI	Assigned to the 19th through 24th bits of the OUI.	RO	110010
3.[9:4]	Model Number	Manufacturer's model number.	RO	001000
3.[3:0]	Revision Number	Manufacturer's revision number.	RO	0001

6.5. Register4: Auto-Negotiation Advertisement

This register contains the advertisement abilities of this device that will be transmitted during auto-negotiation.

Table 15. Register4: Auto-Negotiation Advertisement

Reg. bit	Name	Description	Type	Default
4.15	Next Page	1: Next Page enabled 0: Next Page disabled (Permanently =0)	RO	0
4.14	Acknowledge	Permanently =0.	RO	0
4.13	Remote Fault	1: Transmit remote fault 0: Do not transmit remote fault	RW	0
4.12	Reserved	Reserved.	RW	0
4.11	Asymmetric Pause	1: Advertises that the RTL8208B(F)-LF has asymmetric flow control capability 0: No asymmetric flow control capability In 100FX mode, this bit is set by FX_ASY_PAUSE upon reset. In 100/10TP mode, this bit is set by TP_ASY_PAUSE upon reset.	RW	Set by TP_ASY_PAUSE Or FX_ASY_PAUSE
4.10	Pause	1: Advertises that the RTL8208B(F)-LF has flow control capability 0: No flow control capability In 100FX mode, this bit is set by FX_PAUSE upon reset. In 100/10TP mode, this bit is set by TP_PAUSE upon reset.	RW	Set by TP_PAUSE Or FX_PAUSE
4.9	100Base-T4	1: 100Base-T4 capable 0: Not 100Base-T4 capable (permanently =0)	RO	0
4.8	100Base-TX-FD	1: 100Base-TX full duplex capable 0: Not 100Base-TX full duplex capable	RW	1
4.7	100Base-TX	1: 100Base-TX half duplex capable 0: Not 100Base-TX half duplex capable	RW	1
4.6	10Base-T-FD	1: 10Base-TX full duplex capable 0: Not 10Base-TX full duplex capable	RW	1
4.5	10Base-T	1: 10Base-TX half duplex capable 0: Not 10Base-TX half duplex capable	RW	1
4.[4:0]	Selector Field	[00001]=IEEE 802.3.	RO	00001

Next Page – The RTL8208B(F)-LF does not implement the Next Page function, so bit 15 will always return a '0' when read.

Acknowledge – Because the Next Page function is not implemented, bit 14 will always return a '0' when read.

Remote Fault –Writing a '1' to this bit causes a remote fault indicator to be sent to the link partner during auto-negotiation.

Reserved – Reserved bits are R/W to allow for forward compatibility with future IEEE standards.

Asymmetric Pause – Setting this bit indicates the availability of Asymmetric Flow Control capabilities when full duplex operation is in use. This bit is used by one MAC to communicate Asymmetric Pause Capability to its Link Partner and has no effect on PHY operation.

Pause –Setting this bit indicates the availability of Flow Control capabilities when full duplex operation is in use. This bit is used by one MAC to communicate Pause Capability to its Link Partner and has no effect on PHY operation.

100Base-T4 – Because the RTL8208B(F)-LF does not support the T4 function, any reads to this bit will return a '0'.

100Base-TX-FD – This bit advertises that the RTL8208B(F)-LF can operate in 100Base-TX full duplex mode. Writing a '0' to this bit will suppress advertising of this ability. Resetting the chip restores the default value. The default value is '1' and writing a '1' will set this bit to '1'. Reading this bit will return the last written value, or the default value if no write has been completed since the last reset.

100Base-TX – This bit advertises that the RTL8208B(F)-LF can operate in 100Base-TX half duplex mode. Writing a '0' to this bit will suppress advertising of this ability. Resetting the chip will restore the default value. The default value is '1' and writing a '1' will set this bit to '1'. Reading this bit will return the last written value, or the default value if no write has been completed since the last reset.

10Base-T-FD – This bit advertises that the RTL8208B(F)-LF can operate in 10Base-T full duplex mode. Writing a '0' to this bit will suppress advertising of this ability. Resetting the chip will restore the default value. The default value is '1' and writing a '1' will set this bit to '1'. Reading this bit will return the last written value, or the default value if no write has been completed since the last reset.

10Base-T – This bit advertises that the RTL8208B(F)-LF can operate in 10Base-T half duplex mode. Writing a '0' to this bit will suppress advertising of this ability. Resetting the chip will restore the default value. The default value is '1' and writing a '1' will set this bit to '1'. Reading this bit will return the last written value, or the default value if no write has been completed since the last reset.

Selector Field – Bits 4:0 contain a fixed value of 00001, indicating that the chip belongs to the IEEE 802.3 class of PHY transceivers.

6.6. Register5: Auto-Negotiation Link Partner Ability

This register contains the advertised abilities of the Link Partner as received during auto negotiation. The content changes after successful auto negotiation.

Table 16. Register5: Auto-Negotiation Link Partner Ability

Reg. bit	Name	Description	Type	Default
5.15	Next Page	1: Link partner desires Next Page transfer 0: Link partner does not desire Next Page transfer	RO	0
5.14	Acknowledge	1: Link Partner acknowledges reception of FLP words 0: No acknowledgement by Link Partner	RO	0
5.13	Remote Fault	1: Remote Fault indicated by Link Partner 0: No remote fault indicated by Link Partner	RO	0
5.12	Reserved	Reserved.	RO	0
5.11	Asymmetric Pause	1: Asymmetric Flow control supported by Link Partner 0: No Asymmetric flow control supported by Link Partner When auto-negotiation is enabled, this bit reflects Link Partner ability (read only). In 100FX mode, this bit is set by FX_ASY_PAUSE or SMI.	RW	0
5.10	Pause	1: Flow control supported by Link Partner 0: No flow control supported by Link Partner When auto-negotiation is enabled, this bit reflects Link Partner ability (read only). In 100FX mode, this bit is set by FX_PAUSE or SMI.	RW	0
5.9	100Base-T4	1: 100Base-T4 supported by Link Partner 0: 100Base-T4 not supported by Link Partner	RO	0
5.8	100Base-TX-FD	1: 100Base-TX full duplex supported by Link Partner 0: 100Base-TX full duplex not supported by Link Partner For 100FX mode, this bit is set when Reg.0.8=1 or FX_DUPLEX =1. When auto-negotiation is disabled, this bit is set when Reg.0.13=1 and Reg.0.8=1.	RO	0
5.7	100Base-TX	1: 100Base-TX half duplex supported by Link Partner 0: 100Base-TX half duplex not supported by Link Partner For 100FX mode, this bit is set when Reg.0.8=0 or FX_DUPLEX =0. When auto-negotiation is disabled, this bit is set when Reg.0.13=1 and Reg.0.8=0.	RO	0
5.6	10Base-T-FD	1: 10Base-TX full duplex supported by Link Partner 0: 10Base-TX full duplex not supported by Link Partner When auto-negotiation is disabled, this bit is set when Reg.0.13=0 and Reg.0.8=1.	RO	0
5.5	10Base-T	1: 10Base-TX half duplex supported by Link Partner 0: 10Base-TX half duplex not supported by Link Partner When auto-negotiation disabled, this bit is set when Reg.0.13=0 and Reg.0.8=0.	RO	0
5.[4:0]	Selector Field	[00001]=IEEE 802.3.	RO	00001

Note: The values are only guaranteed to be valid once auto-negotiation has successfully completed, as indicated by bit 5 of the MII Status Register.

Next Page – Bit 15 returns a value of '1' when the Link Partner implements the Next Page function and has Next Page information that it wants to transmit. However, since the RTL8208B(F)-LF does not implement the Next Page function, it ignores the Next Page bit, except to copy it to this register.

Acknowledge – Bit 14 is used by auto negotiation to indicate that a device has successfully received its Link Partner's Link Code Word.

Remote Fault – Bit 13 returns a value of '1' when the Link Partner signals that a fault has occurred.

Reserved – Not defined by the IEEE 802.3 standard.

Asymmetric Pause – Indicates that the Link Partner asymmetric pause bit is set.

Pause – Indicates that the Link Partner pause bit is set.

100Base-T4 – Though the RTL8208B(F)-LF does not support the T4 function, this bit reflects the T4 ability of the Link Partner.

100Base-TX-FD – This bit indicates that the Link Partner can support 100Base-TX full duplex mode. This bit is cleared any time auto negotiation is restarted or the RTL8208B(F)-LF is reset.

100Base-TX – This bit indicates that the Link Partner can support 100Base-TX half duplex mode. This bit is cleared any time auto negotiation is restarted or the RTL8208B(F)-LF is reset.

10Base-T-FD – This bit indicates that the Link Partner can support 10Base-T full duplex mode. This bit is cleared any time auto negotiation is restarted or the RTL8208B(F)-LF is reset.

10Base-T – This bit indicates that the Link Partner can support 10Base-T half duplex mode. This bit is cleared any time auto negotiation is restarted or the RTL8208B(F)-LF is reset.

Selector Field – Bits 4:0 reflect the value of the Link Partner's selector field. These bits are cleared each time auto negotiation is restarted or the chip is reset, and generally reflects the value 0001, indicating that the Link Partner is an IEEE 802.3 device.

6.7. Register6: Auto-Negotiation Expansion

Table 17. Register6: Auto-Negotiation Expansion

Reg. bit	Name	Description	Type	Default
6.[15:5]	Reserved		RO	0
6.4	Parallel Detection Fault	1: A fault has been detected via the Parallel Detection function 0: No fault has been detected via the Parallel Detection function	RO	0
6.3	Link Partner Next Page Able	1: Link Partner is Next Page able 0: Link Partner is not Next Page able	RO	0
6.2	Local Next Page Able	1: RTL8208B(F)-LF is Next Page able 0: RTL8208B(F)-LF is not Next Page able (permanently=0)	RO	0
6.1	Page Received	1: A New Page has been received 0: A New Page has not been received	RO/LH	0
6.0	Link Partner Auto-Negotiation Able	If Auto-Negotiation is enabled, this bit means: 1: Link Partner is Auto-Negotiation able 0: Link Partner is not Auto-Negotiation able In 100FX or auto-negotiation disabled, this bit is always 1.	RO	0 (Auto-Negotiation) or 1 (100FX)

Reserved – Ignore the output of the RTL8208B(F)-LF when these bits are read.

Parallel Detection Fault – Bit 4 is a read-only bit that is latched high when a parallel detection fault occurs in the auto negotiation state machine. For further details, consult the IEEE 802.3 standard. The bit is reset to '0' after the register is read, or when the chip is reset.

Link Partner Next Page Able – Bit 3 returns a '1' when the Link Partner has Next Page capabilities. It has the same value as bit 15 of the Link Partner Ability Register.

Local Next Page Able – The RTL8208B(F)-LF does not have Next Page capabilities, so it will always return a '0' when bit 2 is read.

Page Received – Bit 1 is latched high when a new link code word is received from the Link Partner, checked, and acknowledged. This bit is cleared when the link is lost or the chip is reset.

Link Partner Auto-Negotiation Able – Bit 0 returns a '1' once the Link Partner is known to have auto negotiation capabilities. Before any auto negotiation information is exchanged, or if the Link Partner does not comply with IEEE auto negotiation, the bit returns a value of '0'.

6.8. Port 1 Register24: Cable Tester Control Register0

Table 18. Port 1 Register24: Cable Tester Control Register0

Reg. bit	Name	Description	Type	Default
15:13	Port Selection	Port selection for cable test.	RW	000
12	Reserved	Must be set to the default value.	RW	0
11	ENRTCT	1: Run cable test 0: Stop cable test	RW	0
10:8	Reserved	Must be set to the default value.	RW	111
7:0	Reserved	Must be set to the default value.	RW	0x80

Port Selection	000 = Select Port 0 to run cable test 001 = Select Port 1 to run cable test 010 = Select Port 2 to run cable test 011 = Select Port 3 to run cable test 100 = Select Port 4 to run cable test 101 = Select Port 5 to run cable test 110 = Select Port 6 to run cable test 111 = Select Port 7 to run cable test

ENRTCT *– Set to '1' to run the UTP cable test, and set to '0' after completion of the cable test process.*

6.9. Port1 Register29: Cable Tester Control Register1

Table 19. Port1 Register29: Cable Tester Control Register1

Reg. bit	Name	Description	Type	Default
15	Reserved	Must be set to the default value.	RW	0
14	SELTX	1: Cable test on TX pair 0: Cable test on RX pair	RW	0
13	Reserved	Must be set to the default value.	RW	0
12	Reserved	Must be set to the default value.	RW	1
11:0	Reserved	Must be set to the default value.	RW	0x7d0

SELTX	0: Select RX_Pair (pair 1/2) to run cable test 1: Select TX_Pair (pair 3/6) to run cable test

6.10. Port1 Register30: Cable Status Register

Table 20. Port1 Register30: Cable Status Register

Reg. bit	Name	Description	Type	Default
15	RTCT_RDY	1: Cable test status is ready 0: Cable test status is not ready	RO	0
14	Reserved		RO	0
13:12	Status	Cable tester status. 00: Normal cable 01: Open in cable 10: Short in cable 11: Reserved	RO	00
11:9	Reserved		RO	0
8:0	Distance	Distance of Reflection.	RO	0

RTCT_RDY – This bit will return a '1' if the cable test process has been completed and the contents of Status and Distance are valid.

Status – Cable test status is valid after completion of cable test process.

Distance – These bits (in decimal) divided by 4 equal the approximate distance (meters) to the open/short fault location.

These bits are valid after completion of the cable test process.

7. Function Description

7.1. General

7.1.1. SMI (Serial Management Interface)

SMI (Serial Management Interface) is also known as MII Management Interface and consists of two signals, MDIO and MDC, which allow the MAC controller to control and monitor the state of the PHY. MDC is a clock input for PHY to latch MDIO on its rising edge. The clock can run from DC to 2.5MHz. MDIO is a bi-directional connection used to write data to, or read data from PHY. The PHY address base is set by pins PHY_ADDR[4:3], and the eight port addresses of the RTL8208B(F)-LF are internally 000, 001, 010, 011, 100, 101, 110, and 111.

Table 21. SMI Read/Write Cycles

	Preamble (32 bits)	Start (2 bits)	OP Code (2 bits)	PHYAD (5 bits)	REGAD (5 bits)	Turnaround (2 bits)	Data (16 bits)	Idle
Read	1……..1	01	10	AAAAA	RRRRR	Z0	D…….D	Z*
Write	1……..1	01	01	AAAAA	RRRRR	10	D…….D	Z*

*Note1: *Z: high-impedance. During idle time, MDIO state is determined by an external 1.5KΩ pull-up resistor.*

Note2: The RTL8208B(F)-LF supports Preamble Suppression, which allows the MAC to issue Read/Write Cycles without preamble bits (but needs at least one Idle for every cycle). However, for the first MII management cycle after power-on reset, a 32-bit preamble is needed. To guarantee the first successful SMI transaction after power-on reset, the MAC should be delayed at least 700μs to issue the first SMI Read/Write Cycle relative to the rising edge of reset.

7.1.2. Port Pair-Loop Back Mode (PP-LPBK) (RTL8208BF-LF Only)

Port Pair-Loop Back Mode (PP-LPBK) mode is enabled by pulling the pin high on reset. When in PP-LPBK mode, the ports of the RTL8208BF-LF are configured as four pairs, port0 & port1, port2 & port3, port4 & port5, and port6 & port7. Each pair is set as RMII interface loopback, acting as a signal regeneration /transformation repeater, so a switch controller is not necessary.

In PP-LPBK mode, TP port and FX port selection is different from that in normal mode. The TP and FX port selection configuration is as follows:

In Table 22, ‘U’ means UTP port, ‘F’ means Fiber port.

Table 22. Port Pair-Loop Back Mode (PP-LPBK) (RTL8208BF-LF Only)

PP-LPBK Mode (Pin 105)	SEL_TXFX[1:0] (Pin 99, 107)	Port0, Port1	Port2, Port3	Port4, Port5	Port6, Port7
0 (Normal Mode)	0 0	U U	U U	U U	U U
	0 1	U U	U U	U U	U F
	1 0	U U	U U	U U	F F
	1 1	F F	F F	F F	F F
1 (PP-LPBK)	0 0	U U	U U	U U	U U
	0 1	U U	U U	U F	U F
	1 0	U F	U F	U F	U F
	1 1	F F	F F	F F	F F

Since this configuration is a loopback connection, it uses full duplex only. Half duplex is not supported. The loopback-pair ports should be configured to the same speed. Although this mode does not effect normal NWay mode, in order to keep each pair's two ports at the same speed, there is an auto-detection scheme. This scheme specifies that if one port of the pair is already linked, when the other port is linked later, the earlier link-on port will re-start auto negotiation. When PP-LPBK mode is set, there are three requirements: it must be based upon RMII mode; no switch controller can be connected; and TX_EN[7:0] must be pulled down.

7.1.3. PHY Address

Each transceiver in the RTL8208B(F)-LF has a unique PHY address for MII management. The address is set through the PHY address pins. The pins are latched at the trailing end of a reset. Transceiver 1 will have the address AA000, where AA=PHYAD [4:3]. Each internal PHY address is AA000, AA001, AA010, AA011, AA100, AA101, AA110, AA111. Every time an SMI write or read operation is executed, the transceiver compares the PHY address with its own PHY address definition, and the operation is executed only when the addresses match.

7.1.4. Auto-Negotiation

For 10/100Mbps TP ports, the RTL8208B(F)-LF default setup is Auto-Negotiation enabled. Setting Register 0.12=0 via an SMI write will disable Auto-Negotiation. For a 100FX port, Auto-Negotiation is always disabled.

For an Auto-Negotiation enabled port, the RTL8208B(F)-LF will negotiate with its link partner to determine the speed and duplex status. The RTL8208B(F)-LF's ability is advertised in Register 4. After Auto-Negotiation is finished, the link partner's ability is stored in Register 5.

If the link partner is Auto-Negotiation disabled, the RTL8208B(F)-LF enters a parallel-detection state to identify the speed of the link partner. The RTL8208B(F)-LF will link at the same speed as the link partner, in half duplex mode if FRC_PARA_FULL=0 upon reset, or in full duplex mode if FRC_PARA_FULL=1 upon reset.

Auto-Negotiation is also used to determine full-duplex flow control. Flow control ability is advertised in Register 4.10. The link partner's flow control ability is stored in Register 5.10. See the following section for more information.

7.1.5. Full-Duplex Flow Control

If hardware pins TP_PAUSE or FX_PAUSE are enabled at power-on reset, Register 5.10=1 and Register 4.10=1. Therefore, after reset is completed:

When Auto-Negotiation is enabled -- Register 4.10 may be overwritten by the MAC, and Register 5.10 may be updated after NWay has completed. Register 5.10 is set as read-only for the MAC.

When Auto-Negotiation is disabled -- Register 5.10 is set to R/W for the MAC through the SMI interface. If the SMI does not write to Register 5.10, the Register remains 5.10=1, which means hardware forced flow control is enabled.

7.2. Initialization and Setup

7.2.1. Reset

The RTL8208B(F)-LF is initialized while in the reset state. During reset, each transceiver is reset simultaneously. There are three ways to reset the RTL8208B(F)-LF: Power-on auto reset; hardware pin reset; and software reset. The internal power-on auto-reset circuit can reset the chip while the reset pin is floating. The hardware reset signal must be asserted low for at least 10ms on the RESET# pin. A software reset is implemented by writing Register 0.15=1, which is self-clearing.

7.2.2. Setup and Configuration

The operational modes of the RTL8208B(F)-LF can be configured either by hardware pin (pulled high or low) upon reset, or by software programming via accessing the RTL8208B(F)-LF registers through the SMI (see section 5 Pin Descriptions, page 6 for details).

7.3. 10Base-T

7.3.1. Transmit Function

When TX_EN is active, TXD from RMII/SMII/SS-SMII is serialized, Manchester-encoded, and driven onto the network medium as a packet stream. An on-chip filtering and wave shaping circuit eliminates the need for external filtering. The transmit function is disabled when the link has failed or when the auto-negotiation process is in progress.

7.3.2. Receive Function

The Manchester decoder converts the incoming serial stream when the circuit detects the signal, and the digital serial stream is then converted to 2-bit (RMII) or 1-bit (SMII/SS-SMII) data format. The preamble of the incoming stream is stripped off and regenerated. SFD is generated into RXD once the incoming SFD is detected and data bits entering the elastic buffer are over threshold.

7.3.3. Link Monitor

The 10Base-T link pulse detection circuit continually monitors the RXIP/RXIN pins for the presence of valid link pulses. Auto-polarity is implemented to correct the detected reverse polarity of RXIP/RXIN signal pairs.

The 10Base-T link pulse detection circuit constantly monitors the RXIP/RXIN pins for the presence of valid link pulses. Auto-polarity is implemented for correcting the detected reverse polarity of the RXIP/RXIN signal pairs.

7.3.4. Jabber

Jabber occurs when TX_EN is asserted for longer than 21ms. Both transmit and loopback functions are disabled once jabber has occurred. The MII Register 1.1 (Jabber detect) bit is set high until jabber disappears and the bit is read again. The Jabber function is supported in 10-Base-T only, and is not implemented in 100Base-TX. The collision LED of the corresponding port will blink while Jabber occurs. Jabber is dismissed after TX_EN remains low for at least 500ms.

7.3.5. Loopback

Loopback mode can be achieved by writing to Register 0.14=1. Loopback mode routes transmitted data at the output of NRZ to the NRZI conversion module, back to the receiving path. This mode is used to check the device's connections at the 5-bit symbol bus, and verify the operation of the Phase-Locked Loop (PLL).

7.4. 100Base-TX

An internal 125MHz clock is generated by an on-chip PLL circuit to synchronize the transmit data or generate the clock signal for the incoming data stream.

7.4.1. Transmit Function

Upon detection of TX_EN high, the RTL8208B(F)-LF converts RMII/SMII/SS-SMII TXD to a 5-bit code-group and substitutes J/K code-groups for the first two code-groups (Start of Stream Delimiters (SSD)). As long as TX_EN is asserted high, 4B5B coding continues for all data. At the end of TX_EN, T/R code-groups are appended to the last data field. These are stripped off at the remote receiving end.

During the inter-packet gap, where TX_EN deasserted, IDLE code-groups are transmitted for clocking purposes of the remote receiver. The 5-bit serial data stream is 4B5B coded and then scrambled, as defined by the TP-PMD Stream Cipher function, to flatten the power spectrum energy such that EMI effects are significantly reduced.

The scrambled seed is unique for each port based on PHY addresses. After scrambling, the bit stream is driven onto the network media in the form of MLT-3 signaling. This multi-level signaling technology moves the power spectrum energy from high frequency to low frequency, which also benefits EMI emission. Scrambling is not implemented in 100Base-FX.

7.4.2. Receive Function

The receive path includes a receiver composed of an adaptive equalizer and DC restoration circuits. These circuits compensate for incoming distortion of the MLT-3 signal. An MLT-3 to NRZI, and NRZI to NRZ converter is used to convert analog signals to digital bit-streams. A PLL circuit is also included to clock data bits with minimum bit error rate. De-scrambler, 5B/4B decoder, and serial-to-parallel conversion circuits follow. CRS_DV is asserted no later than within a few bits time of when the SSD (Start-of-Stream-Delimiter) is detected (delay due to the elastic buffer as mentioned in the RMII section, page 34), and ends toggling once the data in the elastic buffer has been dumped to RXD.

Table 23. 4B/5B Coding

Name	4B Code	5B Code	Definition
0	0000	11110	Data 0
1	0001	01001	Data 1
2	0010	10100	Data 2
3	0011	10101	Data 3
4	0100	01010	Data 4
5	0101	01011	Data 5
6	0110	01110	Data 6
7	0111	01111	Data 7
8	1000	10010	Data 8
9	1001	10011	Data 9
A	1010	10110	Data A
B	1011	10111	Data B
C	1100	11010	Data C
D	1101	11011	Data D
E	1110	11100	Data E
F	1111	11101	Data F
I	0000*	11111	Idle
J	0101*	11000	Start of stream Delimiter, Part 1
K	0101*	10001	Start of stream Delimiter, Part 2
T	0000*	01101	End of stream Delimiter, Part 1
R	0000*	00111	End of stream Delimiter, Part 2
H	1000	00100	Transmit Error (used to force signaling errors)
V	0111	00000	Invalid code
V	0111	00001	Invalid code
V	0111	00010	Invalid code
V	0111	00011	Invalid code
V	0111	00101	Invalid code
V	0111	00110	Invalid code
V	0111	01000	Invalid code
V	0111	01100	Invalid code
V	0111	10000	Invalid code
V	0111	11001	Invalid code

**Treated as an invalid code (mapped to 0111) when received in data field.*

7.4.3. Link Monitor

In 100Base-TX mode, receive signal energy is detected by monitoring the receive pair for transitions in the signal level. Signal levels are qualified using squelch detect circuits. When no signal or valid signals are detected on the receive pair, the link monitor will enter and remain in the 'Link Fail' state where only idle codes will be transmitted. When a valid signal is detected on the receive pair, the link monitor will enter the 'Link Pass' state and the transmit and receive functions will be enabled.

7.5. Baseline Wander Compensation

The RTL8208B(F)-LF is ANSI TP-PMD compliant and supports input and Base Line Wander (BLW) compensation in 100Base-TX mode. The RTL8208B(F)-LF does not require external attenuation circuitry at its receive inputs, RXIP/RXIN. It accepts TP-PMD compliant waveforms directly, requiring only a 100Ω termination and a 1:1 transformer.

BLW is the change in the average DC content, over time, of an AC coupled digital transmission over a given transmission medium. BLW is a result of the interaction between the low frequency components of a transmitted bit stream and the frequency response of the AC coupling component(s) within the transmission system. If the low frequency content of the digital bit stream goes below the low frequency pole of the AC coupling transformers, then the droop characteristics of the transformers will dominate, resulting in potentially serious BLW. If BLW is not compensated for, packet loss will occur.

7.6. 100Base-FX (RTL8208BF-LF Only)

The RTL8208BF-LF (the RTL8208B-LF does not support fiber application) can be configured to 100Base-FX mode through SEL_TXFX[1:0] (PP-LPBK MODE should be 0), depending on the setting of SEL_TXFX[1:0], port 7 or port 6/7, or all eight ports can be configured for 100Base-FX operation.

Note: In compliance with IEEE 802.3u, 100Base-FX does not support Auto-Negotiation. In order to operate correctly, both sides of the connection should be set to the same duplex and flow control ability.

Table 24. 100Base-FX

PP-LPBK Mode=0 SEL_TXFX[1:0]	Medium Type							
	Port 0	Port 1	Port2	Port3	Port4	Port5	Port6	Port7
2'b00	UTP	UTP	UTP	UTP	UTP	UTP	UTP	UTP
2'b01	UTP	UTP	UTP	UTP	UTP	UTP	UTP	FX
2'b10	UTP	UTP	UTP	UTP	UTP	UTP	FX	FX
2'b11	FX	FX	FX	FX	FX	FX	FX	FX

UTP: 10Base-T/100Base-TX. FX: 100Base-FX.

The RTL8208BF-LF performs a link monitoring function with less pins required than regular 100Base-FX applications (it removes a pair of differential Signal Detect signals (Realtek patent)), which significantly reduces the pin count in this octal PHY.

Any of the RTL8208BF-LF transceivers may interface with an external 100Base-FX fiber optic device and receiver, instead of the magnetic module used with twisted-pair cable. The differential transmit and receive data pairs will operate at PECL (Positive Emitter Coupled Logic) voltage levels instead of those required for twisted-pair transmission. The data will be encoded using two-level NRZI instead of three-level MLT3. The data stream is not scrambled for fiber-optic transmission.

7.6.1. Transmit Function

In 100Base-FX transmission, TXD is processed as 100Base-TX, except without scrambling, before the NRZI stage. Instead of converting to MLT-3 signals, as in 100Base-TX, the serial data stream is driven out as NRZI PECL signals. These enter the fiber transceiver in differential-pairs form. The fiber transceiver only operates in a 3.3V environment. Refer to Figure 22, page 49 for more information.

Table 25. PECL DC Characteristics

Parameter	Symbol	Min	Max	Unit
PECL Input High Voltage	Vih	Vdd-1.16	Vdd-0.88	V
PECL Input Low Voltage	Vil	Vdd-1.81	Vdd-1.47	V
PECL Output High Voltage	Voh	Vdd-1.02		V
PECL Output Low Voltage	Vol		Vdd-1.62	V

7.6.2. Receive Function

Signals are received through PECL receiver inputs from a fiber transceiver and directly passed to a clock recovery circuit for data/clock recovery. Scrambling/de-scrambling is bypassed in 100Base-FX.

7.6.3. Link Monitor

In 100Base-FX mode, if the RTL8208BF-LF receive path detects a valid link word, it enters the link state. If no valid link word is detected, it is in a link down state. Therefore, SD+/- is not necessary. The RTL8208BF-LF uses a reduced 100Base-FX interface.

7.6.4. Far-End-Fault-Indication

The MII Register 1.4 (Remote Fault indication detected) is a Far-End-Fault-Indication (FEFI) bit when 100FX is enabled, and indicates that a FEFI has been detected. FEFI is an alternative in-band signaling that is composed of 84 consecutive 1's followed by one 0. When the RTL8208BF-LF has detected this pattern three times, Reg.1.4 is set, which means the transmit path (Remote side's receive path) has problems.

If the RTL8208BF-LF detects no valid link pulse on the RxOP/N pair, it sends out a FEFI stream pattern, which in turn will cause the remote side to detect a Far-End-Fault. This means the RTL8208BF-LF sees problems on the receive path.

The FEFI mechanism is used only in 100Base-FX applications.

7.6.5. Reduced Fiber Interface

The RTL8208BF-LF ignores the underlying SD signal of the fiber transceiver to complete link detection and connection. This is achieved by monitoring RD signals from the fiber transceiver and checking whether any link integrity events are encountered. This significantly reduces pin-count, especially for high-port PHY devices. This is a Realtek patent-pending technology and available only with Realtek products.

7.7. RMII/SMII/SS-SMII

The interface to the MAC can be RMII, SMII, or SS-SMII through MODE[1:0]. When floating MODE[1:0] upon power-on reset, the RTL8208B(F)-LF operates in RMII mode (default).

Table 26. RMII/SMII/SS-SMII Modes

MODE[1:0]	Operation Mode	REFCLK Clock Input
2'b1x	RMII	50MHz ±50ppm
2'b00	SMII	125MHz ±50ppm
2'b01	SS-SMII	125MHz ±50ppm

Table 27 illustrates the signals required for each interface:

Table 27. RMII/SMII/SS-SMII Signals

RMII	SMII	SS-SMII
REFCLK	REFCLK	REFCLK
	SYNC	TX_SYNC
CRS_DV[2:0]		
CRS_DV[3]		RX_SYNC
CRS_DV[4]		RX_CLK
CRS_DV[7:5]		
RXD0[7:0]	RXD0[7:0]	RXD0[7:0]
RXD1[7:0]		
TX_EN[3:0]		
TX_EN[4]		TX_CLK
TX_EN[7:5]		
TXD0[7:0]	TXD0[7:0]	TXD0[7:0]
TXD1[7:0]		

7.7.1. RMII (Reduced MII)

The RTL8208B(F)-LF meets all of the RMII requirements outlined in the RMII Consortium specifications. The main advantage introduced by RMII is pin count reduction; e.g., it operates with only one 50MHz reference clock for both the TX and RX sides, without separate clocks needed for both paths, as with the MII interface. However, some hardware modification is needed for this change, the most important of which is the presence of an elastic buffer for absorption of the frequency difference between the 50MHz reference clock and the clocking information of the incoming data stream. Another change implemented is that the MII RXDV and Carrier_Sense are merged into one signal, CRS_DV, which is asserted high while detecting incoming packet data. When internal Carrier_Sense is de-asserted, CRS_DV is de-asserted when the first di-bit of a nibble is presented onto RXD[1:0] synchronously to REFCLK. If there is still data in the FIFO that has not yet been presented onto RXD[1:0], then, on the second di-bit of a nibble, CRS_DV reasserts. This pattern of assertion and de-assertion continues until all received data in the FIFO has been presented onto RXD[1:0]

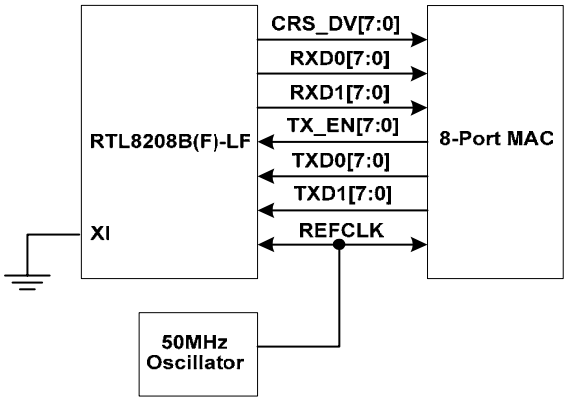


Figure 3. RMII Signal Diagram

7.7.2. SMII (Serial MII)

The RTL8208B(F)-LF also supports SMII interface to MAC, which allows a further reduction in the number of signals. As illustrated below, both the MAC and RTL8208B(F)-LF are synchronous to a 125MHz reference clock.

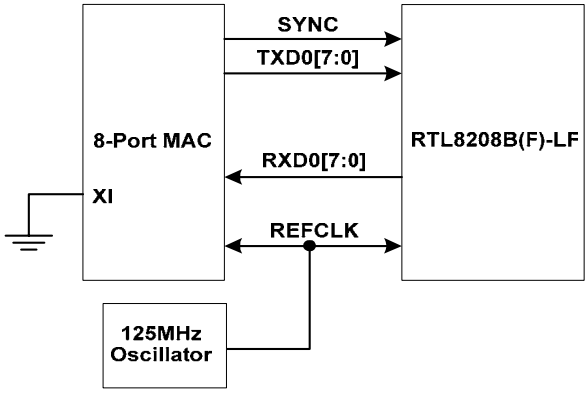


Figure 4. SMII Signal Diagram

Receive Path

Receive data and control information are signaled in 10-bit segments. The SYNC signal is used to delimit the 10-bit segments. The MAC is responsible for generating SYNC pulses every ten clocks. In 100Mbps mode, each segment represents a byte of data. In 10Mbps mode, each segment is repeated ten times to represent a byte of data. The receive sequence contains all of the information defined on the standard MII receive path.

Table 28. SMII Reception Encoding

CRS	RX_DV	RXD0	RXD1	RXD2	RXD3	RXD4	RXD5	RXD6	RXD7
X	0	RXER from Previous Frame	Speed 0: 10Mbps 1: 100Mbps	Duplex 0: Half 1: Full	Link 0: Down 1: Up	Jabber 0: OK 1: Detected	Upper Nibble 0: Invalid 1: Valid	False Carrier 0: OK 1: Detected	1
X	1	One Data Byte (Two MII Data Nibbles)							

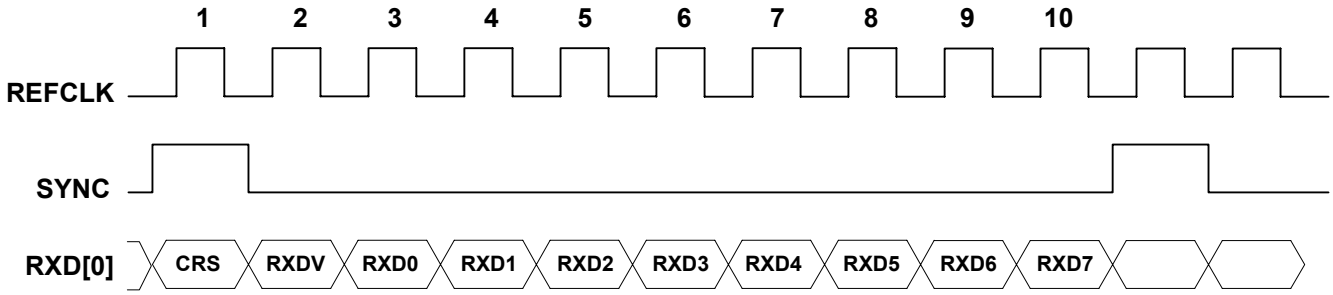


Figure 5. SMII Reception

Transmit Path

Transmit data and control information are signaled in 10-bit segments. SYNC signal is used to delimit the 10-bit segments. MAC is responsible to generate these SYNC pulses every ten clocks. For 100Mbps mode, each segment represents a byte of data. However, for 10Mbps mode, each segment is repeated ten times to represent a byte of data.

Table 29. SMII Transmission Encoding

TXER	TXEN	TXD0	TXD1	TXD2	TXD3	TXD4	TXD5	TXD6	TXD7
X	0	X	X	X	X	X	X	X	X
X	1	One Data Byte (Two MII Data Nibbles)							

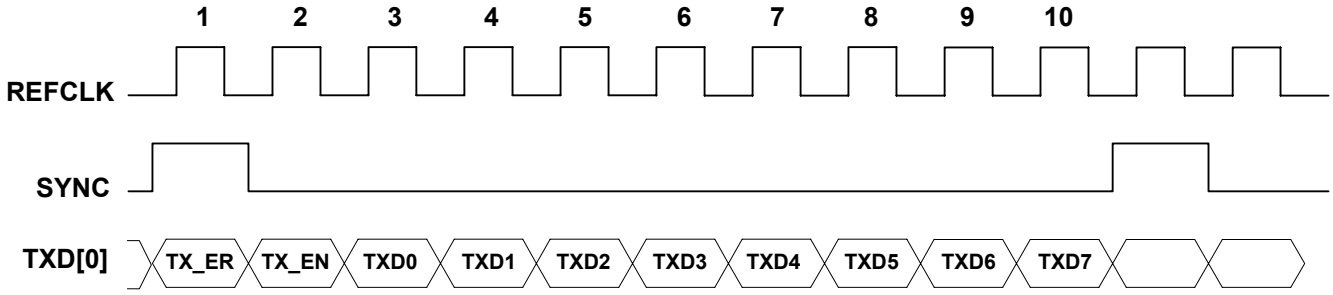


Figure 6. SMII Transmission

Collision Detection

The RTL8208B(F)-LF does not indicate that a collision has occurred. It is left to the MAC to detect the assertion of both CRS_DV and TX_EN.

7.7.3. SS-SMII (Source Synchronous -Serial MII)

Source-Synchronous SMII is designed for applications requiring a trace delay of more than 1ns. Three signals are added to the SMII interface: RX_SYNC, RX_CLK, TX_CLK; and the SYNC of SMII is modified to TX_SYNC in SS-SMII.

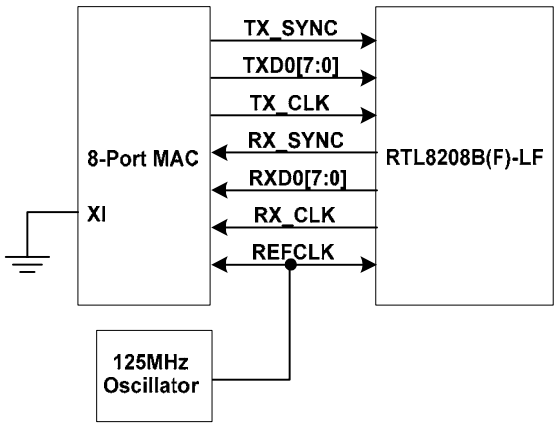


Figure 7. SS-SMII Signal Diagram

Receive Path

Receive data and control information are signaled in 10-bit segments. The RX_SYNC signal is used to delimit the 10-bit segments. The RTL8208B(F)-LF is responsible for generating these RX_SYNC pulses every ten clocks. In 100Mbps mode, each segment represents a byte of data. In 10Mbps mode, each segment is repeated ten times to represent a byte of data. The receive sequence contains all the information defined on the standard MII receive path.

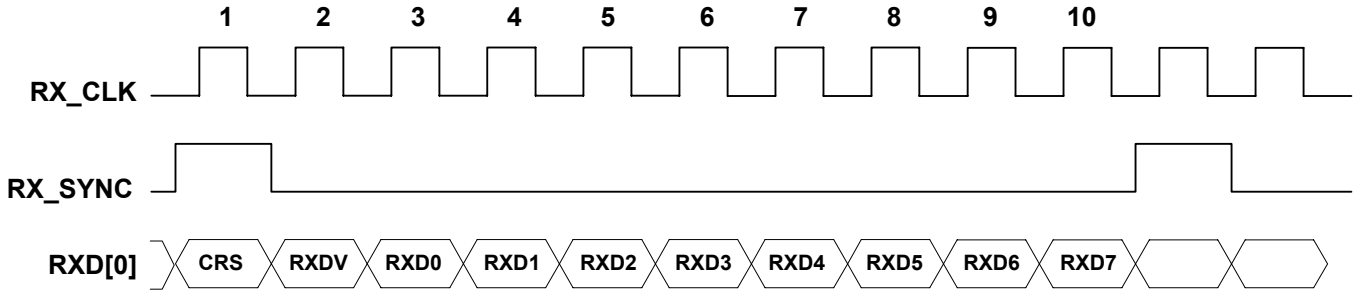


Figure 8. SS-SMII Reception

Transmit Path

Transmit data and control information are signaled in 10-bit segments. The TX_SYNC signal is used to delimit the 10-bit segments. The MAC is responsible for generating these TX_SYNC pulses every ten clocks. In 100Mbps mode, each segment represents a byte of data. In 10Mbps mode, each segment is repeated ten times to represent a byte of data. The receive sequence contains all the information defined on the standard MII receive path. The PHY can sample one of the ten segments.

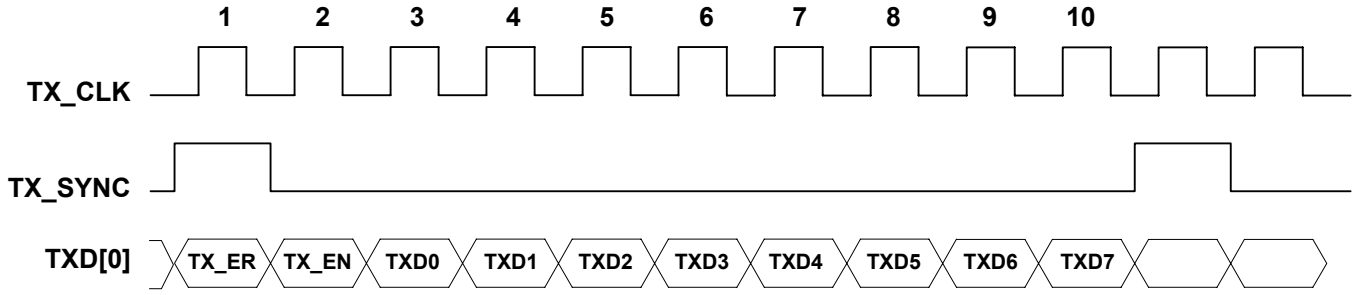


Figure 9. SS-SMII Transmission

Collision Detection

The RTL8208B(F)-LF does not indicate that a collision has occurred. It is left to the MAC to detect the assertion of both CRS_DV and TX_EN.

7.8. Power Saving and Power Down Mode

7.8.1. Power Saving Mode

The RTL8208B(F)-LF implements power saving mode on a per-port basis. A port automatically enters power saving mode ten seconds after the cable is disconnected from it. Once a port enters power saving mode, it transmits normal link pulses only on its TXOP/TXON pins and continues to monitor the RXIP/RXIN pins to detect incoming signals, which might be the 100Base-TX MLT-3 idle pattern, 10Base-T link pulses, or Auto-Negotiation's FLP (Fast Link Pulse). After it detects an incoming signal, it wakes up from power saving mode and operates in normal mode according to the result of the connection.

Power saving mode is not supported when in 100FX operation.

7.8.2. Reg0.11 Power Down Mode

The RTL8208B(F)-LF implements power- down mode on a per-port basis. Setting MII Reg.0.11 forces the corresponding port of the RTL8208B(F)-LF to enter power down mode. This disables all transmit/receive functions on that port.

7.9. LED Configuration

7.9.1. Serial LEDs

The RTL8208B(F)-LF supports serial LED status streams for LED display. The forms of LED status streams, shown below, are controlled by LEDMODE[1:0] pins, which are latched upon reset. All LED statuses are represented as active-low, except Link/Act in Bi-color LED mode, whose polarity depends on Spd status.

Table 30. Serial LED Mode

LEDMODE[1:0]	Mode	Output Sequences
00	3-bit serial stream	Col/Fulldup, Link/Act, Spd
01	2-bit serial stream	Spd, Link/Act
10	3-bit for Bi-color LED	Col/Fulldup, Link/Act, Spd
11	1-bit serial stream	Link/Act/Spd

Table 31. Serial LED Status

LED Status	Description
Col/Fulldup	Collision/Full duplex Indicator. Blinks every 43ms when collisions are occurring. Low for full duplex, and high for half duplex mode.
Link/Act	Link/Activity Indicator. In 3-bit serial stream mode, low for link established. In 3-bit Bi-color LED mode, Link/Act is high for link established when speed is low (100Mbps); Link/Act is low for link established when speed is high (10Mbps). Link/Act Blinks every 43ms when the corresponding port is transmitting or receiving.
Spd	Speed Indicator. Low for 100Mbps, high for 10Mbps.
Link/Act/Spd	Link/Activity/Speed Indicator. Low for link established. Blinking every 43ms for 100Mbps activity. Blinking every 120ms for 10Mbps activity.

LED Blinking Time

LED blinking time can be set to 120ms by setting LED_BLNK_TIME=0. The LED statuses supporting 43/120ms blink times are Col/Fulldup, Link/Act. For status Link/Act/Spd, LED blinking time is not affected by LED_BLNK_TIME.

Serial Stream Order

Every bit stream is output port by port, from port0 to port7 with Col/Fulldup as the first bit in a port stream. In 2-bit serial stream mode, the sequence is Spd, then Link/Act. The following diagrams illustrate the sequences in 3-bit and 2-bit serial stream mode.

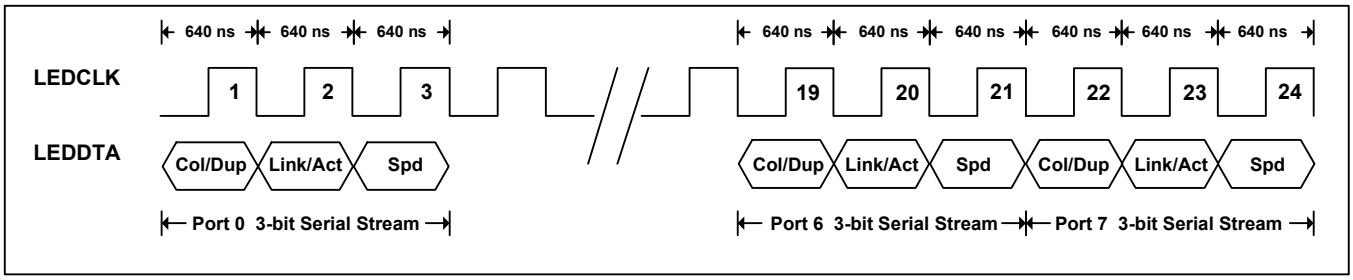


Figure 10. 3-Bit Serial Stream Mode

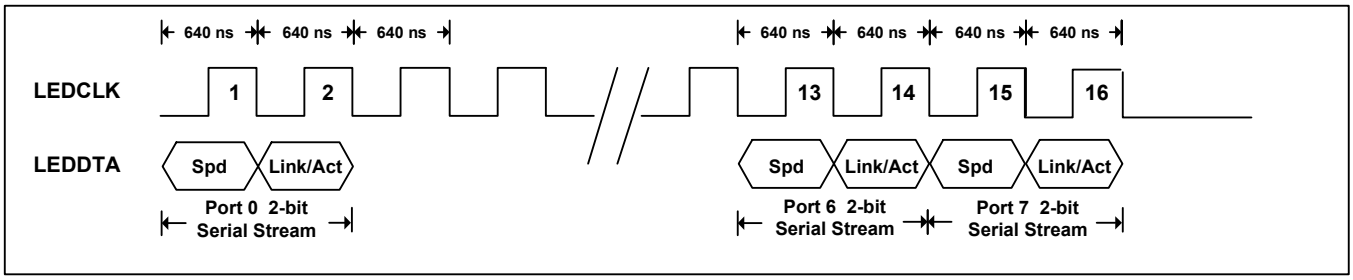


Figure 11. 2-Bit Serial Stream Mode

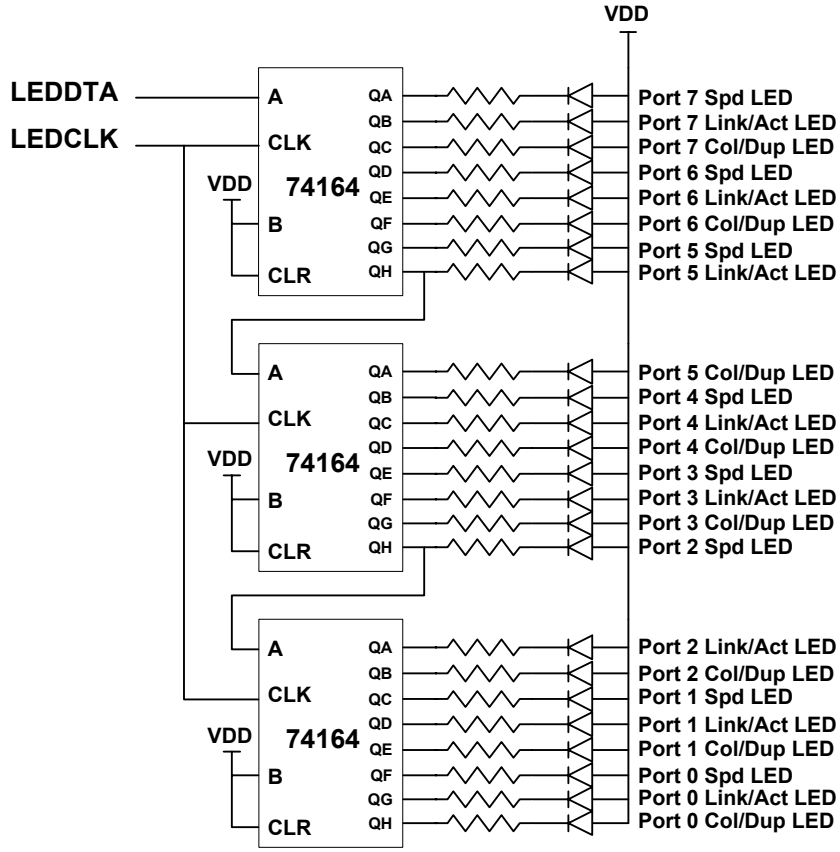


Figure 12. External Circuit for 3-Bit Serial LED Mode

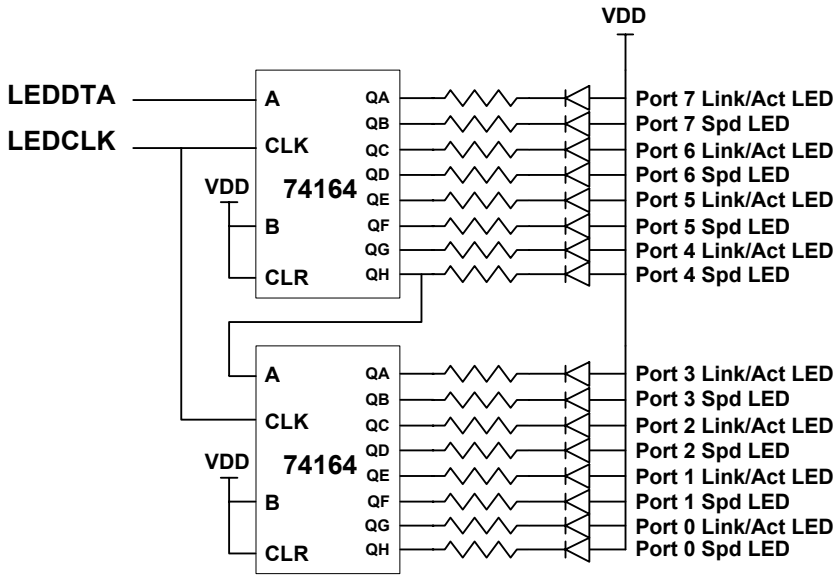


Figure 13. External Circuit for 2-Bit Serial LED Mode

Bi-Color LED

For 3-bit Bi-color LED mode, Link/Act and Spd are used for one Bi-color LED package, which is a single LED package with two LEDs connected in parallel and with opposite polarities.

Table 32. Bi-Color LED

Spd	Link/Act	Indication	Bi-Color State
0	0	No Link	Off
0	1	100Mbps Link up	Green
1	0	10Mbps Link up	Yellow

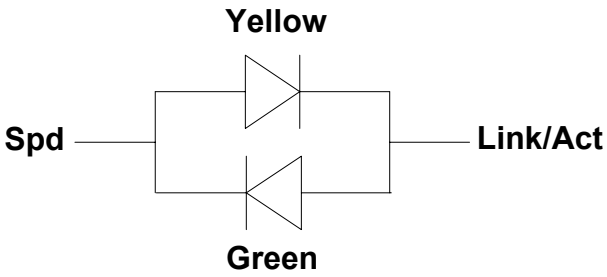


Figure 14. 3-Bit Bi-Color LED

7.9.2. Scan LED

The RTL8208B(F)-LF supports Scan LED display mode. The forms of LED status streams, as shown below, are controlled by LEDMODE[1:0] pins, which are latched upon reset.

Table 33. Scan LED

LEDMODE[1:0]	Mode	SCAN_STATUS[2:0]
00	Mode 0	Col/Fulldup, Link/Act, Spd
01	Mode 1	Rx, Tx, Link
10	Mode 2 for Bi-color LED	NC, Bi-color Link/Act/Spd, NC
11	Reserved	

Table 34. Scan LED Status

LED Status	Description
Link/Act	Link/Activity Indicator. High for link established. Blinks when the corresponding port is transmitting or receiving.
Link	Link Indicator. High for link established.
Spd	Speed Indicator. High for 100Mbps and low for 10Mbps.
Col/Fulldup	Collision/Full duplex Indicator. High for full duplex, low for half duplex. Blinks when collisions occur on the corresponding port.
Bi-Color Link/Act/Spd	Bi-Color LED Link, Activity, and Speed Indicator. Its polarity depends on the Speed status. Blinks when the corresponding port is transmitting or receiving.
RX	High for receive activity.
TX	High for transmit activity.

Scan LED Timing for Mode 0 and Mode 1

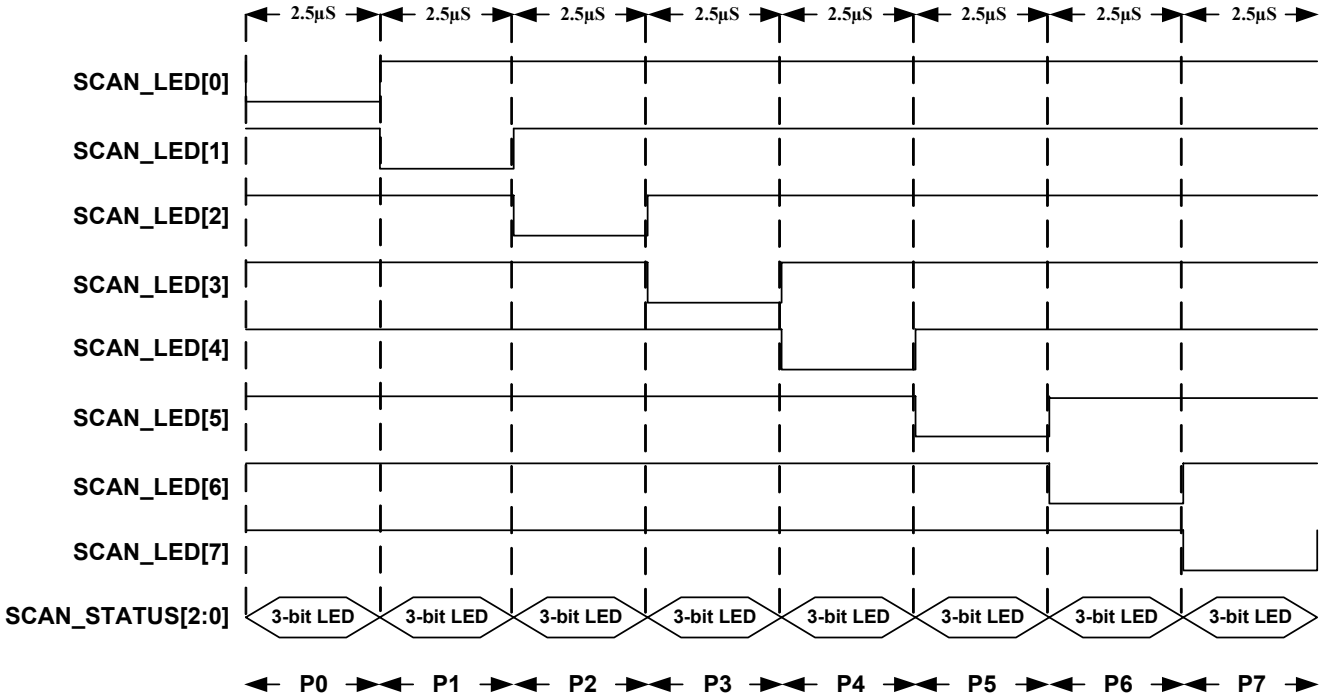


Figure 15. Scan LED Timing for Mode 0 and Mode 1

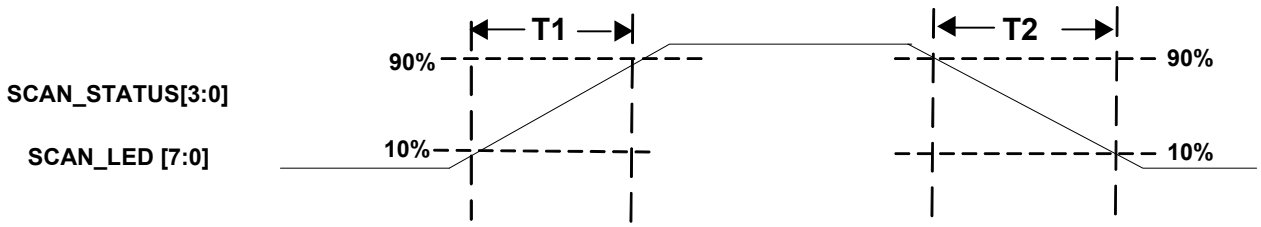


Figure 16. Rise and Fall Timing of the SCAN_STATUS and SCAN_LED Transition

T1: Rise time of all SCAN signals, typically 40ns.

T2: Fall time of all SCAN signals, typically 40ns.

External Circuit for Scan LED Mode 0

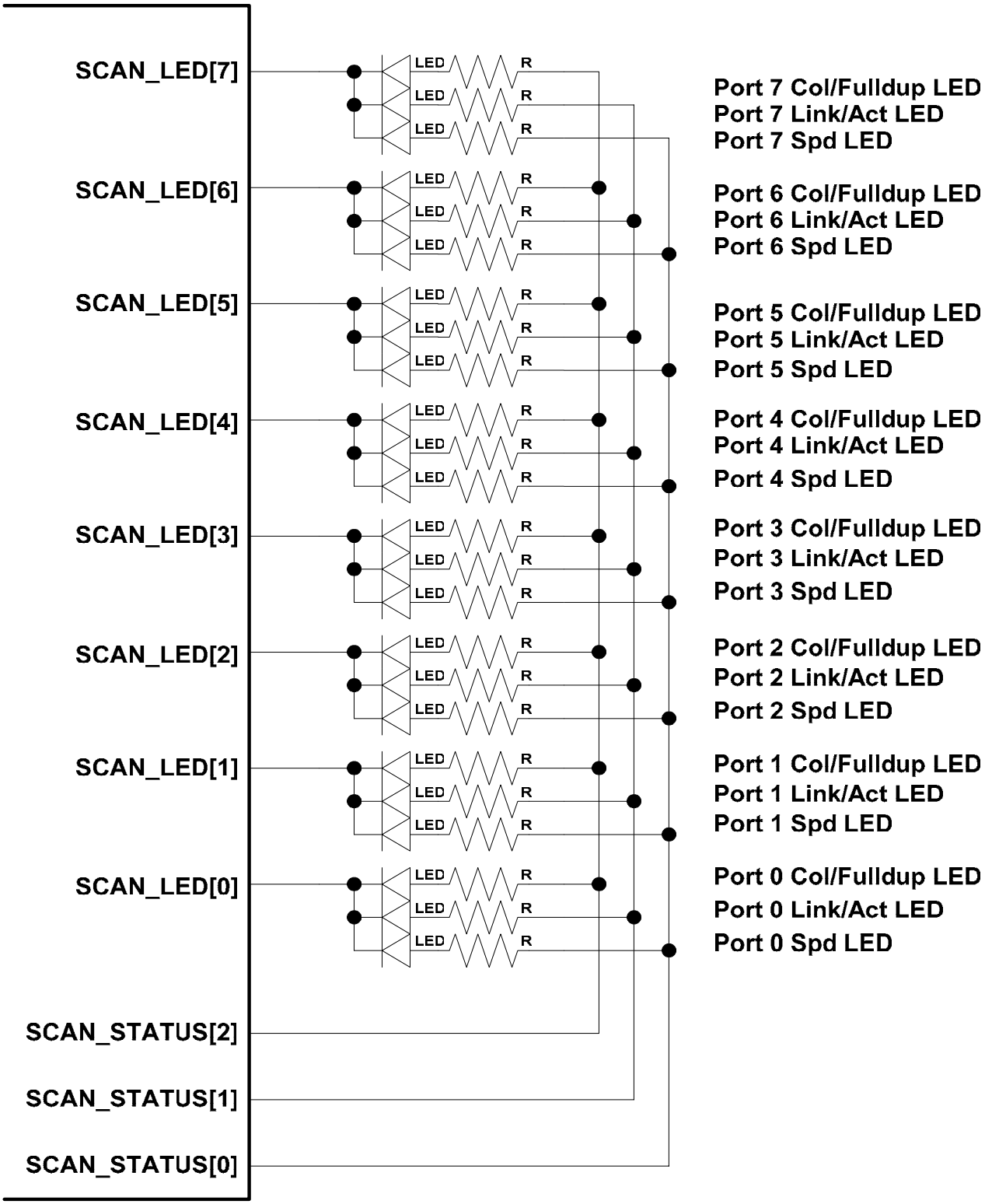


Figure 17. External Circuit for Scan LED Mode 0

External Circuit for Scan LED Mode 1

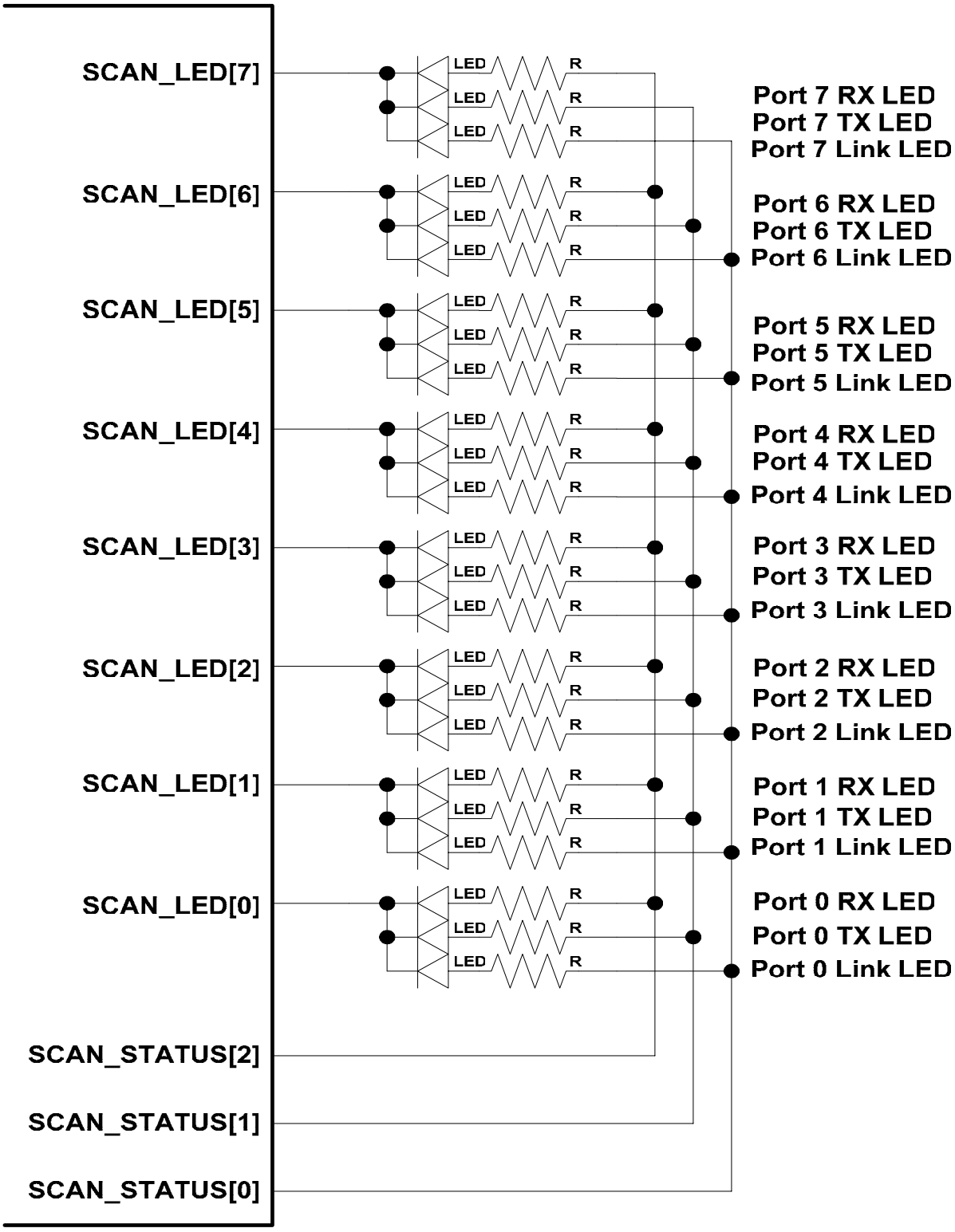


Figure 18. External Circuit for Scan LED Mode 1

External Circuit for Scan LED Mode 2

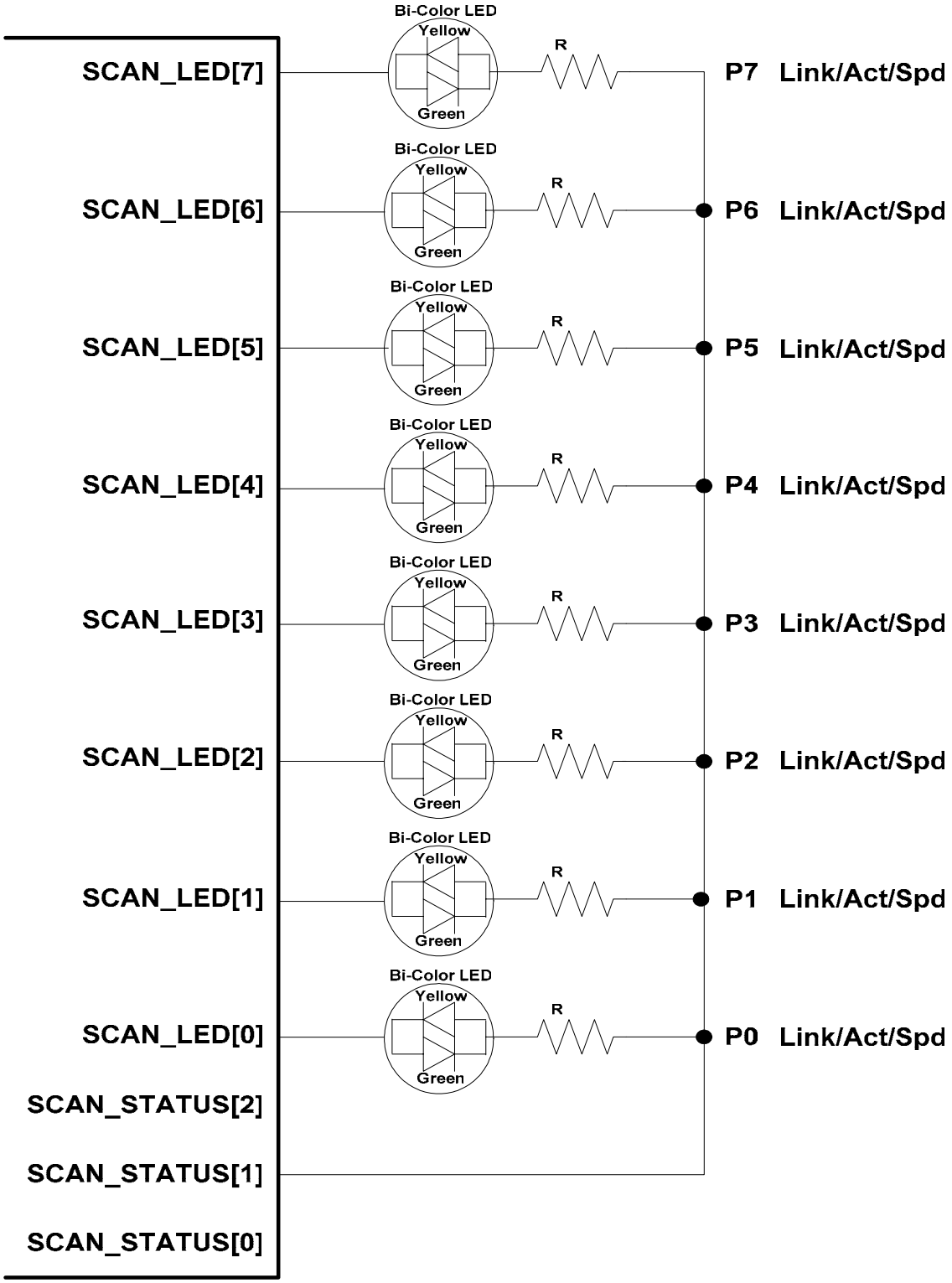


Figure 19. External Circuit for Scan LED Mode 2

7.10. Crossover Detection and Auto Correction

During the link setup phase, the RTL8208B(F)-LF checks whether it receives active signals on each port in order to determine if a connection can be established. In cases where the RTL8208B(F)-LF receiver data pin pair is connected to the receiver data pin pair of the peer device, or vice versa, the RTL8208B(F)-LF will automatically change its configuration to swap receiver data pins with transmitter data pins. If a port is connected to a PC or NIC with MDI-X interface with a crossover cable, the RTL8208B(F)-LF will reconfigure the port to ensure proper connection. This effectively replaces the DIP switch commonly used for reconfiguring a port on a hub or switch.

By pulling-up EN_AUTOXOVER, the RTL8208B(F)-LF identifies the type of connected cable and sets the port to MDI or MDIX. When switching to MDI mode, the RTL8208B(F)-LF uses TXOP/N as transmit pairs; when switching to MDIX mode, the RTL8208B(F)-LF uses RXIP/N as transmit pairs. The same is true for the receive pairs. This function is port-based. Pulling-down EN_AUTOXOVER disables this function and the RTL8208B(F)-LF operates in MDI mode, in which TXOP/N represents transmit pairs, and RXIP/N represents receive pairs.

Note: IEEE 802.3 compliant forced mode 100M ports with Autoxover have link problems with NWAY (Auto-Negotiation) ports. It is recommended to NOT use Autoxover for forced 100M.

7.11. Polarity Detection and Auto Correction

For better noise immunity and lower interference to ambient devices, the Ethernet electrical signal on a twisted pair cable is transmitted in differential form. That is, the signal is transmitted on two wires in each direction with inverse polarities (+/-). If wiring on the connector is faulty, or a faulty transformer is used, the two inputs to a transceiver may carry signals with opposite but incorrect polarities. As a direct consequence, the transceiver will not work properly.

When the RTL8208B(F)-LF operates in 10Base-T mode, it automatically reverses the polarity of its two receiver input pins if it detects that the polarities of the incoming signals on the pins is incorrect. However, this feature is unnecessary when the RTL8208B(F)-LF is operating in 100Base-TX mode.

7.12. 1.8V Power Generation

The RTL8208B(F)-LF uses a PNP power transistor to generate 1.8V from the 3.3V power supply. This 1.8V provides for digital core and analog circuits. The 1.8V power generation circuit also uses an external diode (1N4001) to reduce the voltage drop between the Emitter and Collector of the power transistor. If your system needs more than one RTL8208B(F)-LF chip (greater than 8 ports), do not use one PNP transistor for all of the RTL8208B(F)-LF chips, even if the rating is enough. Instead, use one transistor for each RTL8208B(F)-LF.

Do not connect any beads directly between the collector of the PNP transistor and VDDA. This will affect the stability of the 1.8V power significantly.

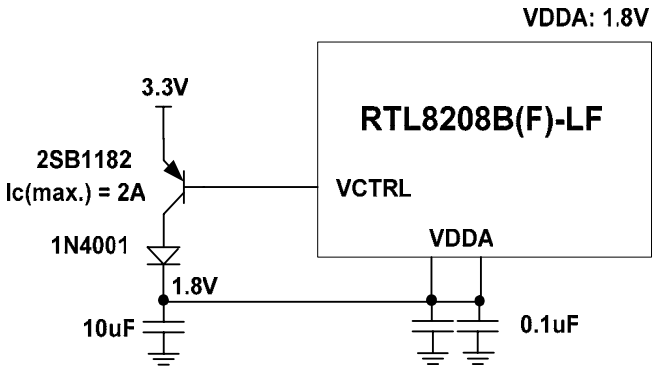


Figure 20. Using a PNP Transistor to Transform 3.3V Into 1.8V

Table 35. An Example Using Power Transistor 2SB1182

Parameter	Symbol	Limits	Unit
Collector-Base Voltage	V_{CBO}	-40	V
Collector-Emitter Voltage	V_{CEO}	-32	V
Emitter-Base Voltage	V_{EBO}	-5	V
Collector Current	I_C	-2	A (DC)
Collector Power Dissipation	P_C	10	W
Junction Temperature	Tj	150	°C
Storage Temperature	Tstg	-55~+150	°C

Note: Absolute maximum ratings (Ta=25°C).
For more information, refer to http://www.rohm.com

7.13. Cable Tester

The cable tester (UTP cable only) determines the quality of the cables, connectors, and terminations. Some of the possible problems that can be diagnosed include open/short faults. The fault location can also be identified.

The RTL8208B(F)-LF's cable tester transmits a signal of known amplitude to one pair of an attached cable. The transmitted signal will continue down the cable until it reflects off a cable imperfection. The magnitude of the reflection and the time it takes for the reflection to come back are shown in registers. Using the information in the registers, the distance to the problem location and the type of problem can be determined.

8. Application Information

8.1. 10Base-T/100Base-TX Application

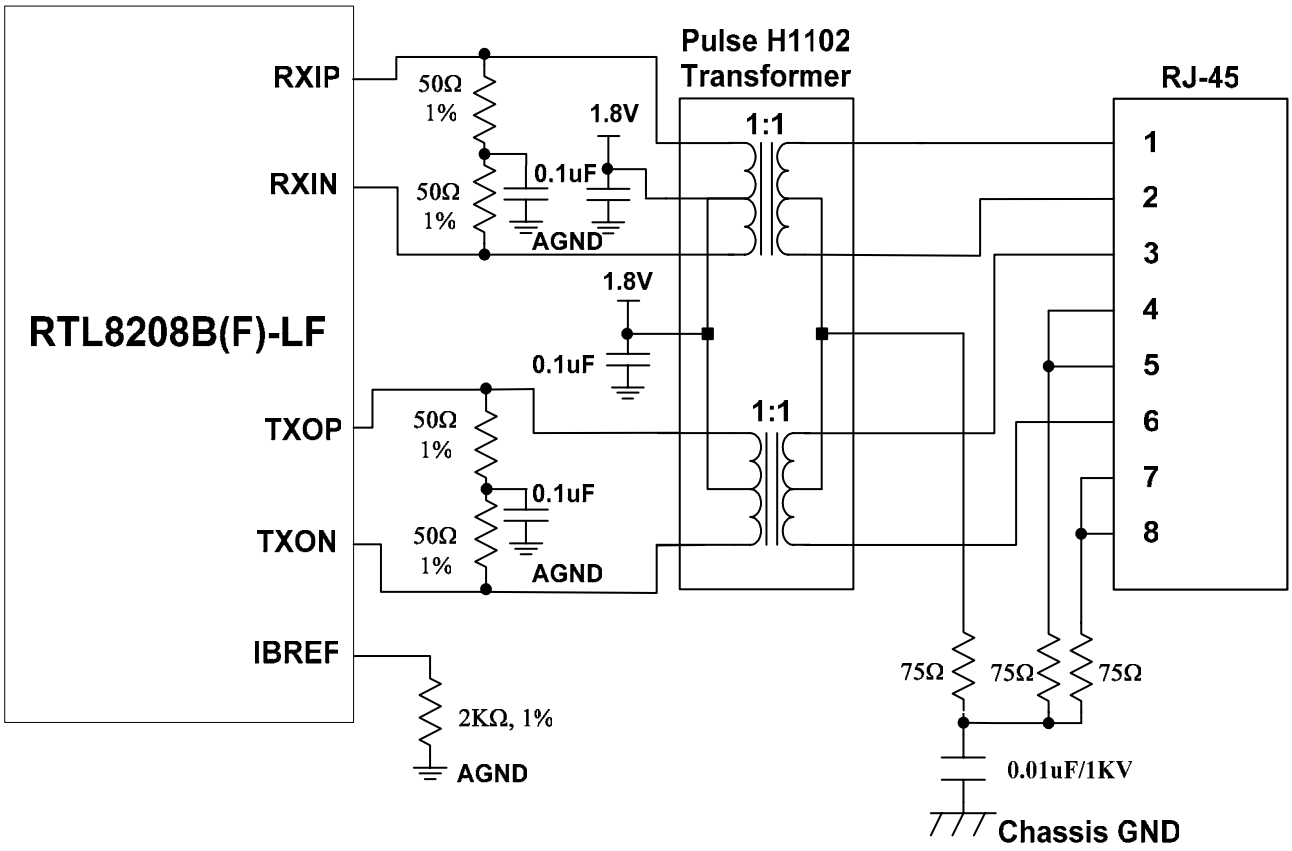


Figure 21. 10Base-T/100Base-TX Application

8.2. 100Base-FX Application (RTL8208BF-LF only)

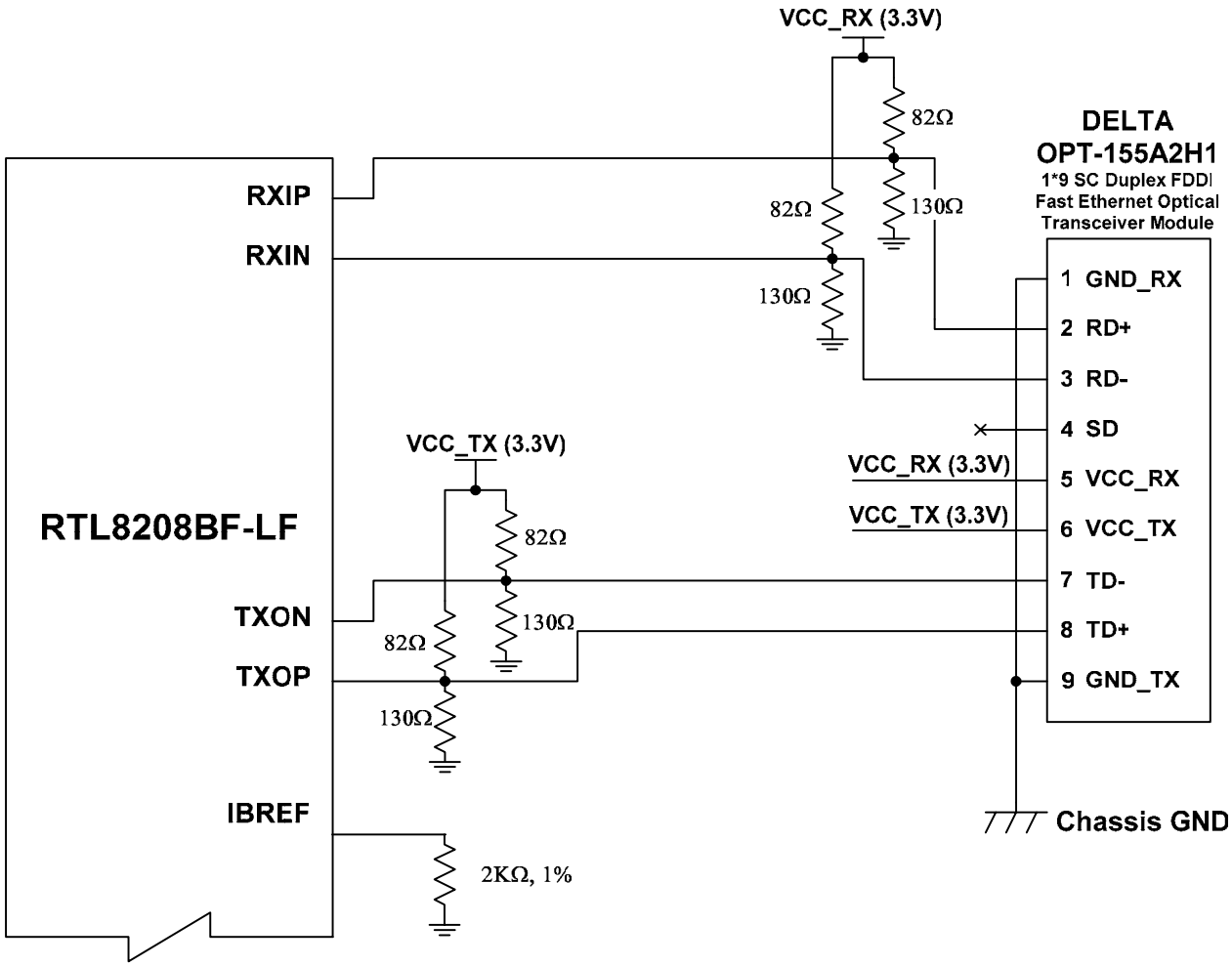


Figure 22. 100Base-FX Application (RTL8208BF-LF only)

9. Characteristics

9.1. Absolute Maximum Ratings

WARNING: Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability will be affected. All voltages are specified reference to GND unless otherwise specified.

Table 36. Absolute Maximum Ratings

Parameter	Min	Max	Units
Storage Temperature	-10	+125	°C
VDDA ,VDD Supply Referenced to GND	GND-0.3	+1.98	V
VDDAH,VDDO Supply Referenced to GND	GND-0.3	+3.63	V
Digital Input Voltage	GND	VDD+0.3	V

9.2. Operating Range

Table 37. Operating Range

Parameter	Min	Typical	Max	Units
Ambient Operating Temperature (Ta)	0	-	+70	°C
3.3V Supply Voltage Range (VDDAH, VDDO)	3.13	3.3	3.46	V
1.8V Supply Voltage Range (VDDA, VDD)	1.74	1.8	1.93	V

9.3. DC Characteristics

Table 38. DC Characteristics

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Power Supply Current for 1.8V	Icc	10Base-T, idle 10Base-T, peak continuous 100% utilization 100Base-TX, idle 100Base-TX, Peak continuous 100% utilization Power saving Power down	TBD	TBD	80 810 760 760 70 60	mA
Power Supply Current for 3.3V	Icc	10Base-T, idle 10Base-T, peak continuous 100% utilization 100Base-TX, idle 100Base-TX, peak continuous 100% utilization Power saving Power down	-	-	42 40 35 37 25 20	mA
Total Power Consumption for all 8 ports	PS	10Base-T, idle 10Base-T, peak continuous 100% utilization 100Base-TX, idle 100Base-TX, peak continuous 100% utilization Power saving Power down	-	-	282 1590 1483 1490 208 174	mW

Parameter	Symbol	Conditions	Min	Typical	Max	Units
TTL Input High Voltage	V_{ih}		2	-	-	V
TTL Input Low Voltage	V_{il}		-	-	0.8	V
TTL Input Current	I_{in}		-10	-	10	uA
TTL Input Capacitance	C_{in}		-	3	-	pF
Output High Voltage	V_{oh}		2.6	-	-	V
Output Low Voltage	V_{ol}		-	-	0.4	V
Output Tristate Leakage Current	|IOZ|		-	-	10	uA
Transmitter, 100Base-TX (1:1 Transformer Ratio)						
TX+/- Output Current High	I_{OH}		-	-	40	mA
TX+/- Output Current Low	I_{OL}		0	-	-	uA
Transmitter, 10Base-T(1:1 Transformer Ratio)						
TX+/- Output Current High	I_{OH}		-	-	100	mA
TX+/- Output Current Low	I_{OL}		0	-	-	uA
Receiver, 100Base-TX						
RX+/- Common-mode Input Voltage	-		-	1.8	-	V
RX+/- Differential Input Resistance	-		-	2.5	-	kΩ
Receiver, 10Base-T						
Differential Input Resistance	-		-	2.5	-	kΩ
Input Squelch Threshold	-		-	340	-	mV

9.4. AC Characteristics

Table 39. AC Characteristics

Parameter	SYM	Conditions	Min	Typical	Max	Units
Transmitter, 100Base-TX						
Differential Output Voltage, Peak-to-Peak	V_{OD}	50Ω from each output to Vcc, Best-fit over 14 bit times	-	2.022	-	V
Differential Output Voltage Symmetry	V_{OS}	50Ω from each output to Vcc, |Vp+|/|Vp-|	-	100.3	-	%
Differential Output Overshoot	V_{OO}	Percent of Vp+ or Vp-	-	2.7	-	%
Rise/Fall Time	t_r ,t_f	10-90% of Vp+ or Vp-	-	4.2/4.3	-	ns
Rise/Fall Time Imbalance	$\|t_r - t_f\|$		-	100	-	ps
Duty Cycle Distortion	-	Deviation from best-fit time-grid, 010101 … Sequence	-	133	-	ps
Timing Jitter	-	Idle pattern	-	650	-	ps
Transmitter, 10Base-TX						
Differential Output Voltage, Peak-to-Peak	V_{OD}	50Ω from each output to Vcc, all pattern	-	4.56	-	V
TP_IDL Silence Duration	-	Period of time from start of TP_IDL to link pulses or period of time between link pulses	10.5	-	15.8	ms
Transmitter Output Jitter	-		-	6	-	ns
Harmonic Content	-	dB below fundamental, 20 cycles of all ones data	-	31.6	-	dB

9.5. Digital Timing Characteristics

Table 40. Digital Timing Characteristics

Parameter	SYM	Conditions	Min	Typical	Max	Units
100Base-TX Transmit System Timing						
Active TX_EN Sampled to first bit of 'J' on MDI output	-		-	11	12	Bits
Inactive TX_EN Sampled to first bit of 'T' on MDI output	-		-	15	16	Bits
TX Propagation Delay	t_{TXpd}	From TXD[1:0] to TXOP/N	-	11	12	Bits
100Base-TX Receive System Timing						
First bit of 'J' on MDI input to CRS_DV assert	-	From RXIP/N to CRS_DV	-	6	8	Bits
First bit of 'T' on MDI input to CRS_DV de-assert	-	From RXIP/N to CRS_DV	-	16	18	Bits
RX Propagation Delay	t_{RXpd}	From RXIP/N to RXD[1:0]	-	15	17	Bits
10Base-TX Transmit System Timing						
TX Propagation Delay	t_{TXpd}	From TXD[1:0] to TXOP/N	-	5	6	Bits
TX_EN to MDI output	-	From TX_EN assert to TXOP/N	-	5	6	Bits

Parameter	SYM	Conditions	Min	Typical	Max	Units
10Base-TX Receive System Timing						
From RXIP/N to CRS_DV	t_{CSON}	Preamble on RXIP/N to CRS_DV asserted	-	12	-	Bits
Carrier Sense Turn-off Delay	t_{CSOFF}	TP_IDL to CRS_DV de-asserted	-	8	9	Bits
RX Propagation Delay	t_{RXpd}	From RXIP/N to RXD[1:0]	9	-	12	Bits
LED Timing						
LED On Time	t_{LEDon}	While LED blinking	43	-	120	ms
LED Off Time	t_{LEDoff}	While LED blinking	43	-	120	ms
Jabber Timing (10Base-T Only)						
Jabber Active	-	From TX_EN=1 to Jabber asserted	60	70	80	ms
Jabber de-assert	-	From TX_EN=0 to Jabber de-asserted	60	-	80	ms
SMI Timing						
MDC	-	MDC clock rate	-	-	2.5	MHz
MDIO Setup Time	-	Write cycle	10	-	-	ns
MDIO Hold Time	-	Write cycle	10	-	-	ns
MDIO output delay relative to rising edge of MDC	-	Read cycle	-	-	10	ns

9.5.1. RMII Receive Timing

Table 41. RMII Receive Timing

Symbol	Description	Minimum	Typical	Maximum	Units
T_opd_rxd_rmii	REFCLK rising edge to RXD/CRS_DV delay.	4	-	9	ns

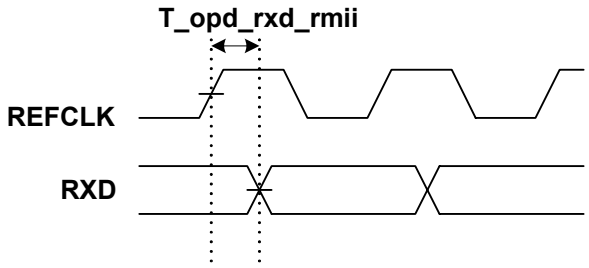


Figure 23. RMII Receive Timing

9.5.2. RMII Transmit Timing

Table 42. RMII Transmit Timing

Symbol	Description	Minimum	Typical	Maximum	Units
T_ipsu_txd_rmii	TXD/TX_EN setup time to REFCLK.	2	-	-	ns
T_iphd_txd_rmii	TXD/TX_EN hold time from REFCLK.	2	-	-	ns

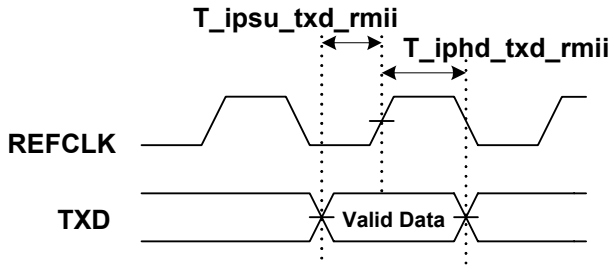


Figure 24. RMII Transmit Timing

9.5.3. SMII Receive Timing

Table 43. SMII Receive Timing

Symbol	Description	Minimum	Typical	Maximum	Units
T_opd_rxd_smii	REFCLK rising edge to RXD delay.	3.5	4	4.5	ns

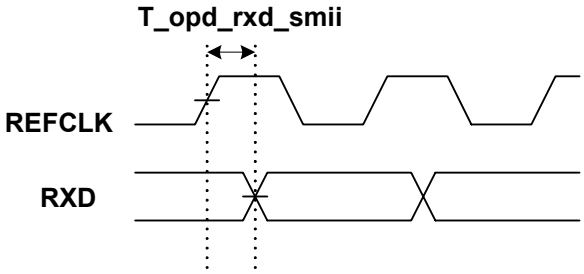


Figure 25. SMII Receive Timing

9.5.4. SMII Transmit Timing

Table 44. SMII Transmit Timing

Symbol	Description	Minimum	Typical	Maximum	Units
T_ipsu_txd_smii	TXD/SYNC setup time to REFCLK.	1	-	-	ns
T_iphd_txd_smii	TXD/SYNC hold time from REFCLK.	1.5	-	-	ns

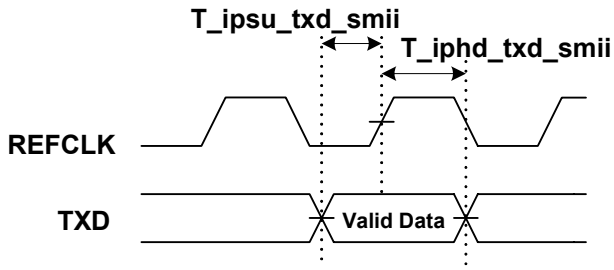


Figure 26. SMII Transmit Timing

9.5.5. SS-SMII Receive Timing

Table 45. SS-SMII Receive Timing

Symbol	Description	Minimum	Typical	Maximum	Units
T_opd_rxd_s3mii	RX_CLK rising edge to RXD/RX_SYNC delay.	1.5	-	3	ns

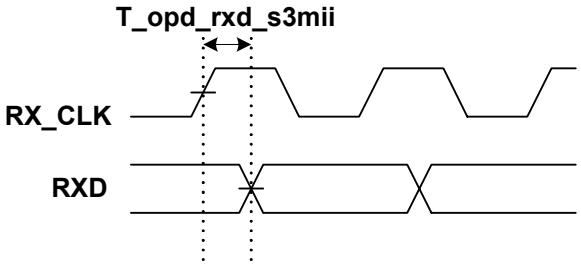


Figure 27. SS-SMII Receive Timing

9.5.6. SS-SMII Transmit Timing

Table 46. SS-SMII Transmit Timing

Symbol	Description	Minimum	Typical	Maximum	Units
T_ipsu_txd_s3mii	TXD/TX_SYNC setup time to TX_CLK.	1.5	-	-	ns
T_iphd_txd_s3mii	TXD/TX_SYNC hold time from TX_CLK.	1	-	-	ns

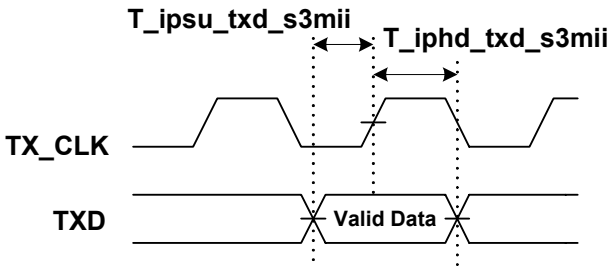


Figure 28. SS-SMII Transmit Timing

9.6. Power Start Up & Internal Reset Sequence

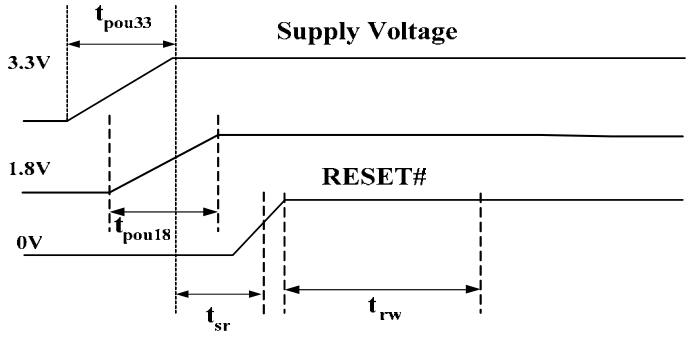


Figure 29. Power Start Up & Internal Reset Sequence

- t_{pou33}: min. 1ms and max. 5ms, 3.3V power on to stable duration requirement.
- t_{pou18}: min. 600µs and max. 2ms, 1.8V power on to stable duration requirement.
- tsr: min. 10ms after 1.8V Power Stable, stable supply voltage to reset high duration.
- trw: max. 50ms, Reset_wait (Start normal PHY after reset deassertion).

9.7. Thermal Characteristics

Heat generated by the chip causes a temperature rise of the package. If the temperature of the chip (Tj, junction temperature) is beyond the design limits, there will be negative effects on operation and the life of the IC package. Heat dissipation, either through a heat sink or electrical fan, is necessary to provide a reasonable environment (Ta, ambient temperature) in a closed case. As power density increases, thermal management becomes more critical. A method to estimate the possible Ta is outlined below.

Thermal parameters are defined according to JEDEC standard JESD 51-2, 51-6:

θja (Thermal resistance from junction to ambient), represents resistance to heat flow from the chip to ambient air. This is an index of heat dissipation capability. A lower θja means better thermal performance.

$$\theta ja = (Tj - Ta) / Ph$$

Where Tj is the junction temperature
Ta is the ambient temperature
Ph is the power dissipation

θjc (Thermal resistance from junction to case), represents resistance to heat flow from the chip to the package top case. θjc is important when an external heat sink is attached on the package top.

$$\theta jc = (Tj - Tc) / Ph$$, where Tj is the junction temperature

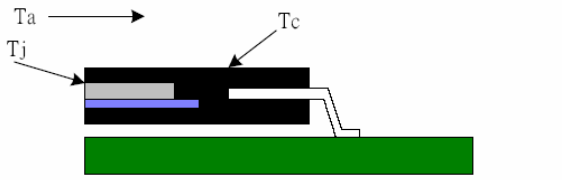


Figure 30. Cross-section of 128-Pin QFP

9.7.1. Thermal Operating Range

Table 47. Thermal Operating Range

Parameter	SYM	Conditions	Min	Typical	Max	Units
Junction operating temperature	Tj		-	25	125	°C
Ambient operating temperature	Ta		-	25	70	°C

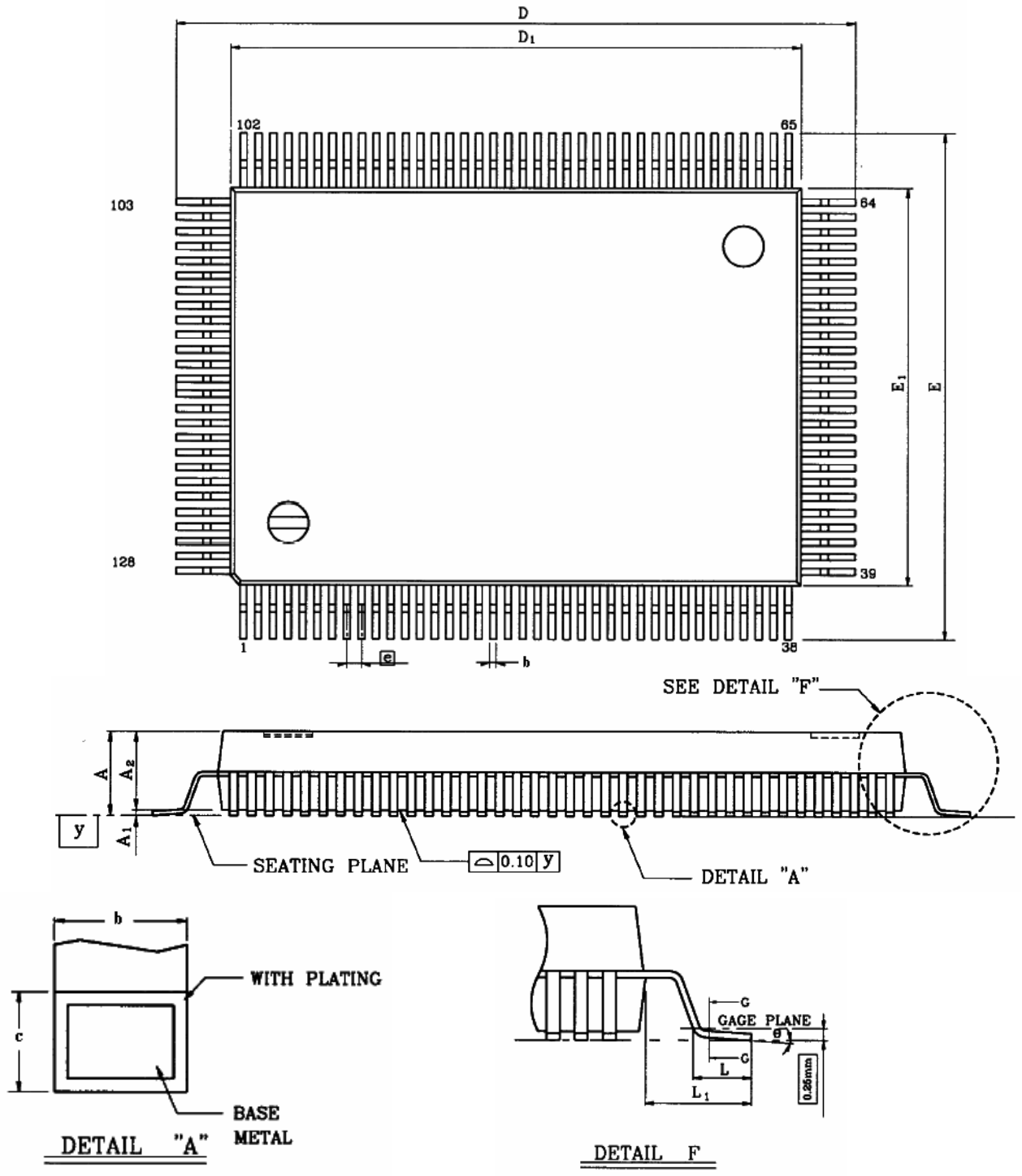
9.7.2. Thermal Resistances

Table 48. Thermal Resistances

Parameter	SYM	Conditions	Min	Typical	Max	Units
Thermal resistance: junction to ambient	θja	2 layer PCB, 0 ft/s airflow	-	28.2	-	°C/W
Thermal resistance: junction to case	θjc	2 layer PCB, 0 ft/s airflow	-	2.0	-	°C/W

Note: PCB conditions (JEDEC JESD51-7)

10. Mechanical Dimensions



See the Mechanical Dimensions notes on the next page.

10.1. Notes for Mechanical Dimensions

Symbol	Dimensions in inches			Dimensions in mm		
	Min	Typical	Max	Min	Typical	Max
A	-	-	0.134	-	-	3.40
A_1	0.010	-	-	0.25	-	-
A_2	0.101	0.107	0.117	2.50	2.72	2.97
b	0.004	0.008	0.012	0.10	0.20	0.30
c	0.004	-	0.008	0.09	-	0.23
D	0.913 BSC			23.2 BSC		
D_1	0.787 BSC			20.00 BSC		
E	0.677 BSC			17.20 BSC		
E_1	0.551 BSC			14.00 BSC		
e	0.20 BSC			0.5 BSC		
L	0.026	0.035	0.041	0.65	0.88	1.03
L_1	0.063 BSC			1.60 BSC		
y	-	-	0.004	-	-	0.10
θ	0°	-	12°	0°	-	12°

Notes:
1. Dimensions D_1 & E_1 do not include mold protrusion.
2. Controlling dimension: Millimeter (mm).
3. General appearance spec. Should be based on final visual inspection.

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		PAGE	
CHECK		DWG NO.	
		DATE	
REALTEK SEMICONDUCTOR CORP.			

11. Ordering Information

Table 49. Ordering Information

Part Number	Package	Status
RTL8208B-LF	128-pin QFP with lead (Pb)-free package	
RTL8208BF-LF	RTL8208B-LF with Fiber support	

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