Single Port 10/100 MII/RMII/TP/Fiber Fast Ethernet Transceiver

(85nm/Extreme Low PW, PWMT® and EMIMT®)

Features

- 10/100Mbps IEEE 802.3/802.3u compliant Fast Ethernet transceiver
- Supports 100Base-TX/FX Media Interface
- Supports MII/ RMII Interface
- Supports Auto MDI/MDIX function
- Power Management Tool
  - APS, auto power saving while Link-off
  - 802.3az, protocol based power saving
  - WOL+, light traffic power saving
  - PWD, force-off power saving
  - Supports MII with LPI for RX and TX
  - Supports RMII with LPI for RX
- Supports Base Line Wander compensation
- Supports Interrupt function
- Built in synchronization FIFO to support jumbo frame size up to 12KB in MII mode (10KB in RMII 100Mbps mode)
- Supports MDC and MDIO to communicate with the MAC
- EMI Management Tool
  - F/W based control
  - 4 levels for mapping the difference layout length on the PCB
- Single 3.3V power supply
- Built-in Vcore regulator
- DSP-based PHY Transceiver technology
- System Debug Assistant Tool
  - 16 bit RX counter
  - 9 bit RXError/CRC counter
  - Isolate MII/RMII
  - RX to TX Loopback
  - Loopback MII/RMII
- Using either 25MHz crystal/oscillator or 50MHz oscillator REF_CLK as clock source
- Built-in 49.9ohm resistors for simplifying BOM
- Flexible LED display
- Process: 85nm

General Description

- Package and operation temperature

IP101G: dice, 0~70℃
IP101GA: 48LQFP, 0~70℃
IP101GR: 32QFN, 0~70℃
IP101GRI: 32QFN, -40~85℃

IP101G is an IEEE 802.3/802.3u compliant single-port Fast Ethernet Transceiver for both 100Mbps and 10Mbps operations. It supports Auto MDI/MDIX function to simplify the network installation and reduce the system maintenance cost. To improve the system performance, IP101G provides a hardware interrupt pin to indicate the link, speed and duplex status change. IP101G provides Media Independent Interface (MII) or Reduced Media Independent Interface (RMII) to connect with different types of 10/100Mbps Media Access Controller (MAC). IP101G is designed to use category 5 unshielded twisted-pair cable or Fiber-Optic cables connecting to other LAN devices. A PECL interface is supported to connect with an external 100Base-FX fiber optical transceiver.
Except good performance, reliability, rich power saving method and extreme low operating current, IP101G provides a serial tool for system designers to complete their projects easily. They are System Debug Assistant Tool and EMI Management Tool.
IP101G is fabricated with advanced CMOS (85nm) technology and design is based on IC Plus's 5th Ethernet-PHY architecture, this feature makes IP101G consumes very low power. Such as in the full load operation (100Mbps_FDX), it only takes below 0.15W.
IP101GA / IP101GR&IP101GRI are available in 48LQFP/32QFN, lead-free package.

* EMIMT: Patent under apply.

Application

- NAS
- Network Printers and Servers
- IP Set-Top Box
- IP/Smart TV
- Game console
- IP and Video Phone
- PoE
- Telecom Fiber device

Table Of Contents

List of Figures

List of Tables

Revision History

Revision #	Change Description
IP101G-DS-R01	Initial release.
IP101G-DS-R01-20120522	1) Correct the typo of Digital IO Pin Control Register. 2) Modify the operation voltage REGOUT and DVDD_REGIN of DC Characteristics.
IP101G-DS-R01-20120611	1) Correct the typo of Linear Regulator Output Control Register. 2) Correct the typo of pin description for pin type PD and PU. 3) Modify the register description for RMII_V12 and RMII_V10. 4) Correct the typo of register default values. 5) Modify the operation voltage DVDD33_IO of DC Characteristics.
IP101G-DS-R01-20120622	Add 30 seconds into the definition for register WOL_PLUS_TIMER_SEL.
IP101G-DS-R01-20120629	Add the symbol SC (Self Clear) for PHY MII register 0.15 Reset and 0.9 Restart Auto-Negotiation.
IP101G-DS-R01-20120709	1) Add LED mode 2 in the pin description and function description. 2) Correct the table of LED Blink Timing. 3) Add more description of PHY Address Configuration and IEEE 802.3az. 4) Add ESD reliability of Absolute Maximum Rating. 5) Correct the typo of function description for Auto Power Saving Mode. 6) Change register P16R16[10] description from HEART_BEAT_EN to Reserved.
IP101G-DS-R01-20120719	Correct the table of Register Map for page selection.
IP101G-DS-R01-20120726	1) Add more description of Register RX2TX_LPBK P1R23[13] for Rx to Tx loopback test. 2) Add more description on Fiber Mode Setting and latched-in pin signals on AC Timing. 3) Add IP101AH into the table of features comparison.
IP101G-DS-R01-20120808	1) Correct the I/O type of IP101GA pin description to O(Ouput) for pin24 RXER. 2) Change the pin name from DVDD33_IO to VDDIO.
IP101G-DS-R01-20120821	1) Change the default value of register P16R27 from 0x0022 to 0x0012. 2) Remove I/O Slew Rate Control Register. 3) Change the register location RMII_WITH_ER from P16R29[0] to P16R29[7].
IP101G-DS-R01-20120927	1) Add more description of low power idle (LPI) state in MII and RMII modes. 2) Correct the typo of Physical Dimensions.
IP101G-DS-R01-20121101	Change the LED blink timing from “On 80ms -> Off (20~40)ms” to “On 26ms -> Off 78ms”.
IP101G-DS-R01-20121113	Add more function description to support Jumbo Frame.
IP101G-DS-R01-20121127	Change the LED mode function as same as IP101A.
IP101G-DS-R01-20121224	Add the notice that does not let these PHY address pins floating for the latched-in settings after the power is ready.

Disclaimer

This document probably contains the inaccurate data or typographic error. In order to keep this document correct, IC Plus reserves the right to change or improve the content of this document.

Features comparison between IP101G and IP101A/IP101AH

Table 1 Features comparison between IP101G and IP101A/IP101AH

Product Name	IP101GR	IP101G	IP101GA	IP101A	IP101AH
Package Type	32pin QFN	Dice	48pin LQFP	48pin LQFP	
REGOUT(1) Output Voltage and location	1.0V, pin28	1.0V, pad5 and pad11	1.0V, pin8	2.5V, pin32	
REGIN Input Voltage and location	NA(2)	1.0V, pad23 and pad26	NA	2.5V, pin8	
RMII mode setting	Pin4	Pad18	Pin1	Pin1 and pin44	
Fiber mode setting: Fiber FXSD signal:	Pin19 Pin1	Pad39 Pad13	Pin22 Pin43	NA	Pin24 and pin48 Pin37
Number of LED	2	4	4	5	
LED mode	1 and 2			1 and 2	
LED Blink Timing	On 26ms -> Off 78ms			On 26ms -> Off 78ms	
PHY address number(3)	Single: 0 ~ 1 Multi: 2 ~ 31	Single: 0 ~ 7 Multi: 8 ~ 31		Single: 0 ~ 31	
Center-tap of transformer	Do not connect to any power			2.5V input power	
Built-in 49.9ohm resistors	Yes			No	
Power consumption	~150mW			~480mW	
Process	85nm			0.25μm	
IEEE 802.3az	Yes			No	
10Base TX amplitude	~1.75V (10Base-Te)			~2.5V (10Base-T)	
WOL+ (Wake On LAN Plus)	Yes			No	
Analog OFF	Yes			No	
16 bit RX counter	Yes			No	
9 bit RXER/CRC counter	Yes			No	
RX to TX Loopback	Yes			No	
Loopback MII/RMII	Yes			Yes	
SNI mode	No			Yes	

Note 1: Regulator voltage output is for internal use only. Do not supply to any other device.
Note 2: Not available for this function. The 1.0V is supplied by the regulator that built-in the chip.
Note 3: Do not let these PHY address pins floating for the latched-in settings after the power is ready.

Transmit and Receive Data Path Block Diagram

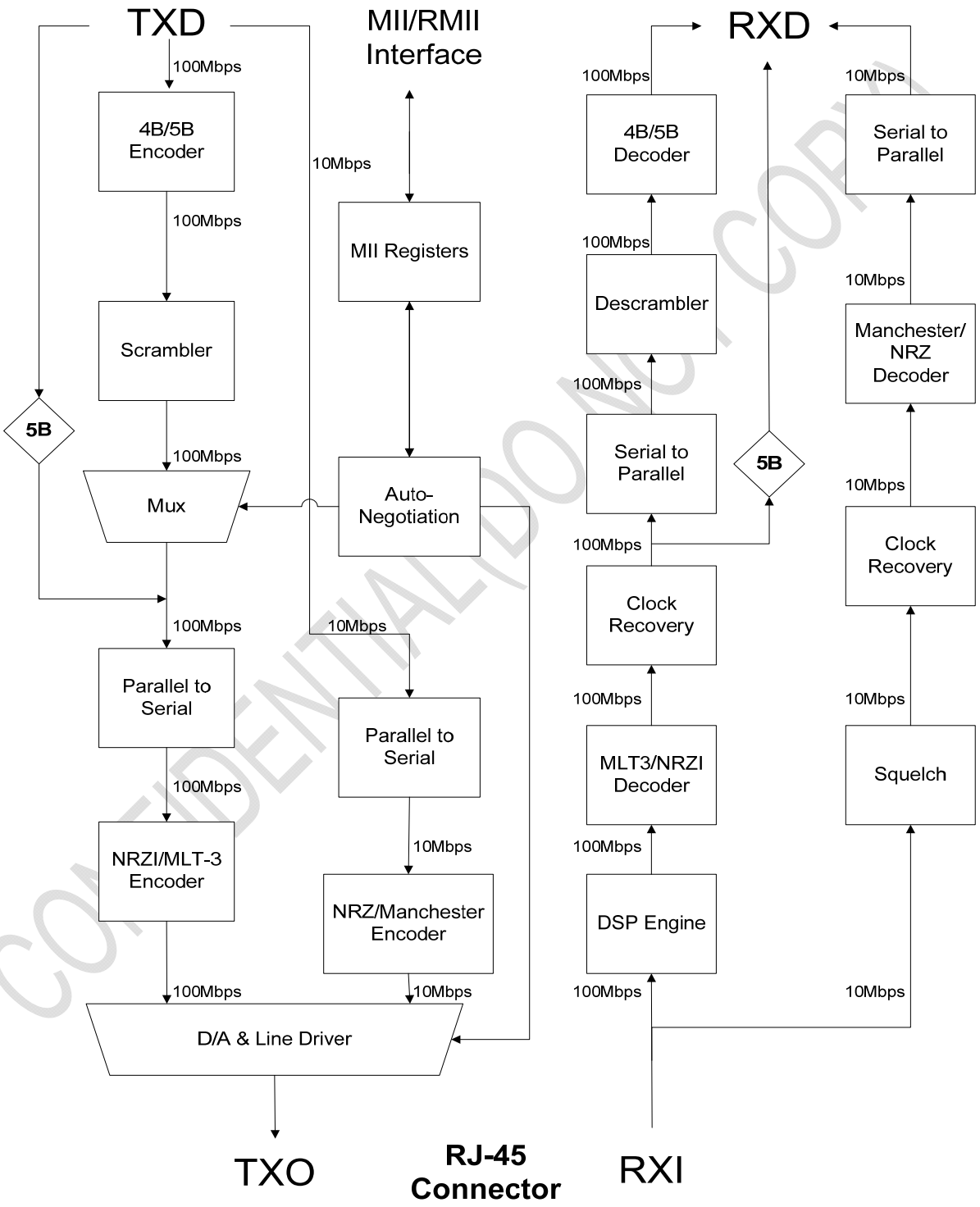


Figure 1 Flow chart of IP101G

1 Pin diagram

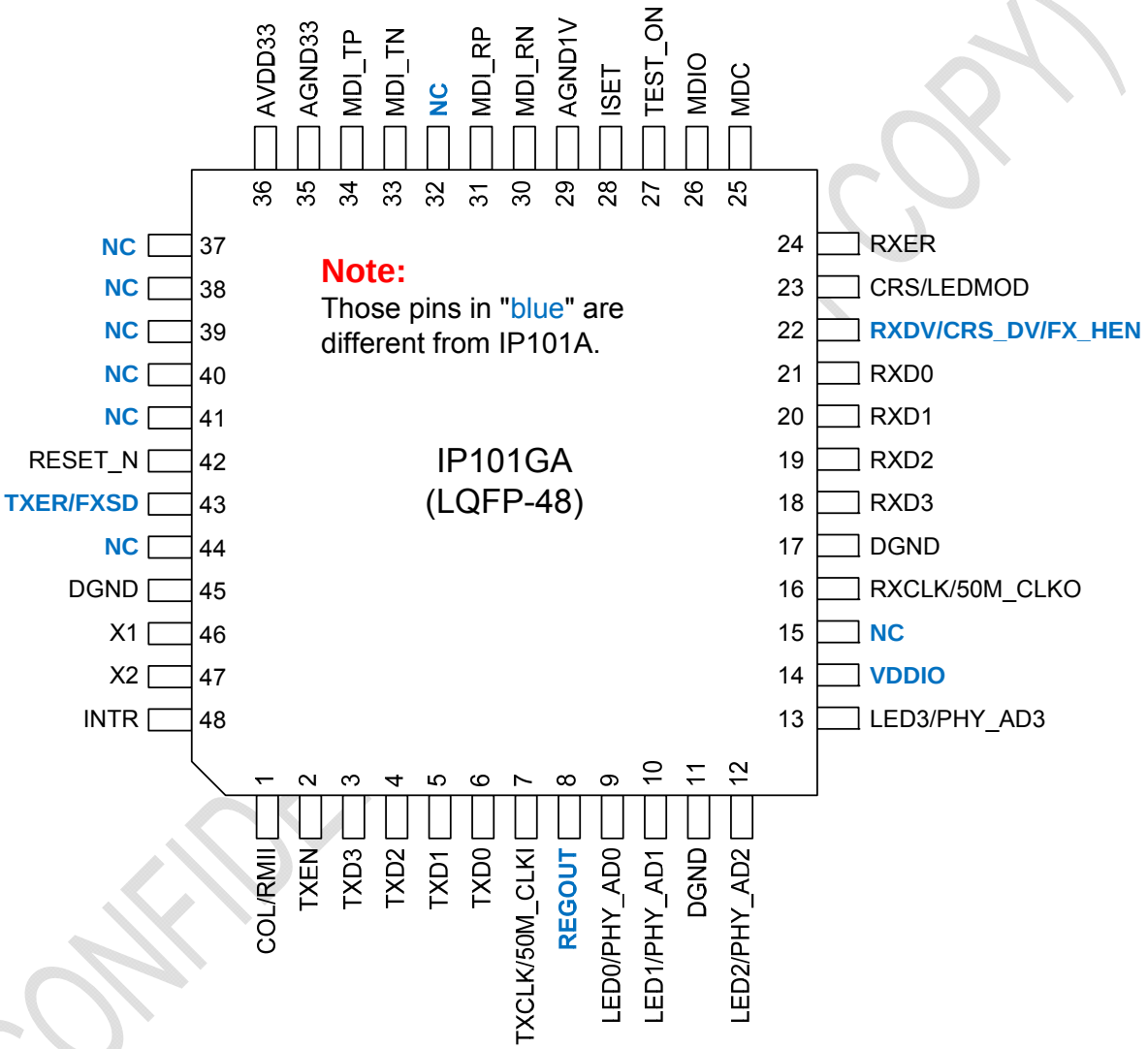


Figure 2 IP101GA 48 Pin Diagram

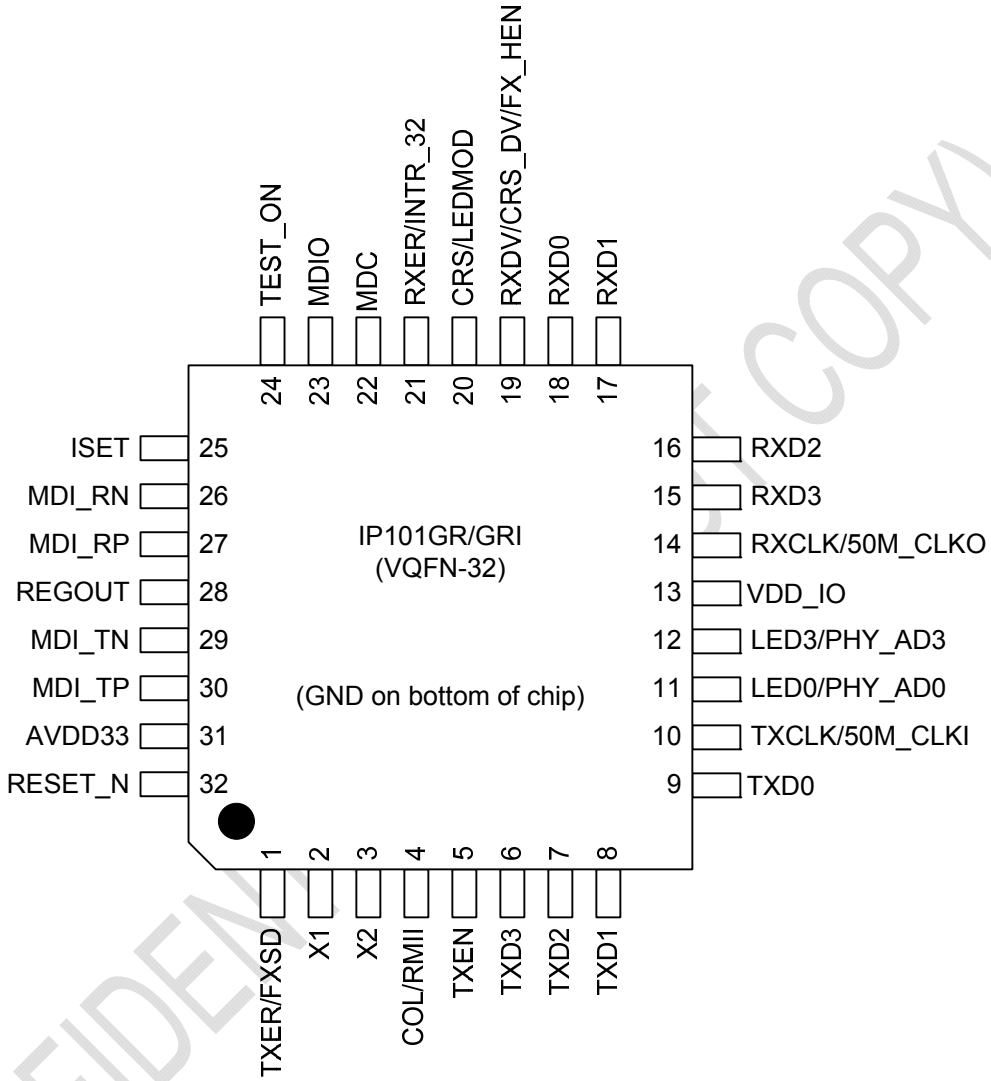
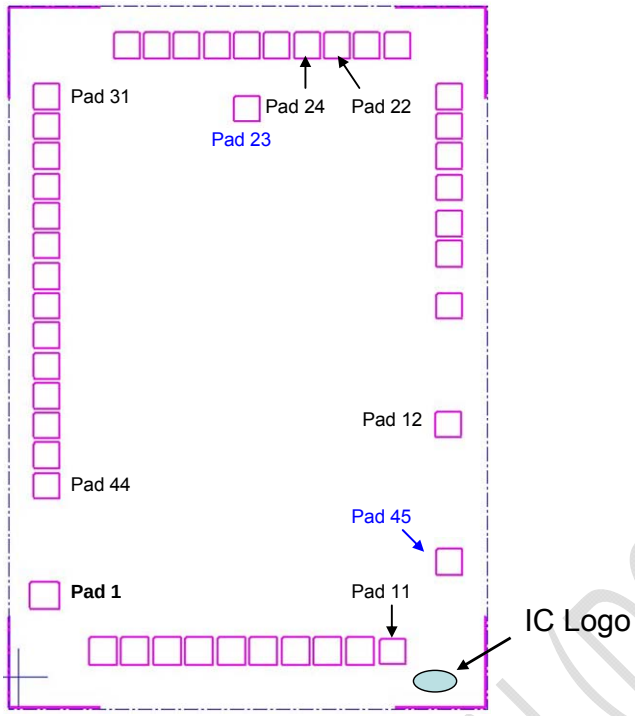


Figure 3 IP101GR/GRI 32 Pin Diagram

2 Dice pad information



Pad No.	Text Name	Pad No.	Text Name
1	ISET	24	TXD[0]
2	AGND_1V	25	TX_CLK
3	MDI_RN	26	REGIN
4	MDI_RP	27	PHYAD_LED0
5	REGOUT	28	PHYAD_LED1
6	MDI_TN	29	VSS
7	MDI_TP	30	PHYAD_LED2
8	AGND_33	31	PHYAD_LED3
9	AGND33	32	VDDIO
10	AVDD33	33	RX_CLK
11	REGOUT	34	VSSIO
12	RESET_N	35	RXD[3]
13	TXER_FXSD	36	RXD[2]
14	VSSIO	37	RXD[1]
15	X1	38	RXD[0]
16	X2	39	RXDV_FIBMOD
17	INTR	40	CRS
18	COL_RMII	41	RXER_INTR
19	TX_EN	42	MDC
20	TXD[3]	43	MDIO
21	TXD[2]	44	TEST_ON
22	TXD[1]	45	AVDD33
23	REGIN		

Figure 4 IP101G dice pad information

3 Pin description

Type	Description		Type	Description
LI	Latched Input in power up or reset		PD	Internal Pull-Down 250KΩ
I/O	Bi-directional input and output		PU	Internal Pull-Up 250KΩ
I	Input		Hi-Z	High impedance
O	Output		P	Power
			OD	Open Drain

3.1 IP101GA pin description

IP101GA

Pin no.	Label	Type	Reset State	Description
Serial Management Interface Pins				
25	MDC	I	Hi-Z	**Management Data Interface Clock:** This pin provides a clock reference to MDIO. The clock rate can be up to 2.5MHz.
26	MDIO	I/O (PU)	I (PU)	**Management Data interface Input/Output:** The function of this pin is to transfer management information between PHY and MAC.
MII/RMII Pins				
2	TXEN	I (PD)	I (PD)	**Transmit Enable or Signal Detect.**
43	TXER/FXSD	I (PD)	I (PD)	**Transmit Error or FXSD:** This is a dual-function pin which is determined by the media type selection. If RXDV/CRS_DV/FX_HEN is latched as "0 (default)" upon reset, the TP interface is selected and its function as TXER. If the fiber interface is selected, this pin's function as FXSD. **FXSD:** 0: Fiber link down; 1: Fiber link up **Transmit Enable:** TXEN / TXER / Description 1 / 1 / Transmission error propagation. 0 / 1 / Combine TXD[3:0] that equal to 0001 for request PHY to enter LPI mode. 1 / 0 / Normal operation 0 / 0 This pin TXER must be either floating or connecting to GND in RMII mode.
7	TXCLK/50M_CLKI	I/O	Hi-Z	**Transmit Clock output or 50M clock input:** In MII mode, this pin provides a continuous 25MHz clock at 100Base-TX and 2.5MHz at 10Base-T. In RMII mode, a 50Mhz clock should input to this pin for the timing reference of the internal circuit.
3,4,5,6	TXD[3:0]	I	Hi-Z	**Transmit Data Input:**

IP101GA				
Pin no.	**Label**	**Type**	**Reset State**	**Description**
				In MII mode, TXD[3:0] is synchronous to TXCLK. In RMII mode, TXD[1:0] is synchronous to 50M_CLKI.
22	RXDV/CRS_DV/ FX_HEN	O/LI (PD)	I (PD)	**Receive Data Valid or Media Type Selection:** **FX_HEN** The input state is latched upon reset to determine whether TP or fiber interface is selected. If it is at logic "0" (default) state upon reset, the TP interface is selected; otherwise the fiber interface is selected. **RXDV/CRS_DV** In MII mode, this pin indicates the Receive Data Valid function. In RMII mode, this pin indicates the Carrier Sense and Receive Data Valid function.
16	RXCLK/ 50M_CLKO	O	Hi-Z	**Receive Clock:** In MII mode, this pin provides 25MHz for 100BT or 2.5MHz for 10BT. In RMII mode, this pin output a 50 MHz clock for the timing reference of MAC side.
18,19, 20,21	RXD[3:0]	O	Hi-Z	**Receive Data:** In MII mode, RXD[3:0] is synchronous to RXCLK. In RMII mode, RXD[1:0] is synchronous to 50M_CLKI.
24	RXER	O	Hi-Z	**Receive error:** RXDV / RXER / Description 1 / 1 / Decoding error of the received signal 0 / 1 / Combine RXD[3:0] equal to 0001 indicates PHY is receiving LPI. 1 / 0 / Normal operation 0 / 0 This pin RXER is an optional input for MAC/CPU device.
1	COL/RMII	O/LI (PD)	I (PD)	**Collision Detected:** During the normal operation, this pin outputs a high status signal it means collision is detected. **RMII Mode Selection:** During the power on reset, this pin status is latched to determine what kind MAC interface will be used. Logic "1" is for RMII mode and logic "0" is for MII mode.
23	CRS/LEDMOD	O/LI (PD)	I (PD)	**Carrier Sense:** When signal output from this pin is high indicates the transmission or reception is in process and at low status means the line is in idle state. **LEDMOD:** During power on reset, this pin status is latched to determine which either LED mode 1 or 2 is selected, please refer to the LED pins description.
Cable Transmission Interface				
34,33	MDI_TP MDI_TN	I/O I/O	Hi-Z	**Transmit Output Pair:** Differential pair shared by 100Base-TX and 10Base-T modes. When configured as 100Base-TX, output is an MLT-3 encoded waveform. When configured as 10Base-T, the output is Manchester

<table>
<tr><th colspan="5">IP101GA</th></tr>
<tr><th>Pin no.</th><th>Label</th><th>Type</th><th>Reset State</th><th>Description</th></tr>
<tr><td></td><td></td><td></td><td></td><td>code.</td></tr>
<tr><td>31,30</td><td>MDI_RP
MDI_RN</td><td>I/O
I/O</td><td>Hi-Z</td><td>Receive Input Pair: Differential pair shared by 100Base-TX and 10Base-T modes.</td></tr>
<tr><td colspan="5">Clock and Miscellaneous Pins</td></tr>
<tr><td>47</td><td>X2</td><td>O</td><td>O</td><td>25MHz Crystal Output: Connects to crystal to provide the 25MHz output. It must be left open when X1 is driven with an external 25MHz oscillator.</td></tr>
<tr><td>46</td><td>X1</td><td>I</td><td>I</td><td>25MHz Crystal Input: Connects to crystal to provide the 25MHz crystal input. If a 25MHz oscillator is used, connect X1 to the oscillator’s output. If a 50MHz clock is applied to pin7 TXCLK/50M_CLKI, X1 must be connected to GND or AGND33.</td></tr>
<tr><td>42</td><td>RESET_N</td><td>I</td><td>I
(PU)</td><td>RESET_N: Enable a low status signal will reset the chip. For a complete reset function. 25MHz clock (x1) must be active for a minimum of 10 clock cycles before the rising edge of RESET_N. Chip will be able to operate after 2.5ms delay of the rising edge of RESET_N. The 2.5ms extension is to ensure the stability of system power.</td></tr>
<tr><td>28</td><td>ISET</td><td>I</td><td>I</td><td>Bandgap Circuit Resistor: This pin should be connected to GND via a 6.19KΩ (1%) resistor to define the standard current of the internal circuit.</td></tr>
<tr><td>48</td><td>INTR</td><td>OD</td><td>Hi-Z</td><td>Interrupt: Programmable Interrupt Output, this is an open drain output, and an external pulled-up resistor is needed for normal mode operation. Another operation mode is Rx to Tx loopback debugging test (reflect on Register P1R23[13] RX2TX_LPBK) when connect INTR pin to GND.</td></tr>
<tr><td>9</td><td>LED0/PHY_AD0</td><td>O/LI</td><td>Hi-Z</td><td>LED 0 and PHY Address [0]
LED 0
<table>
<tr><td></td><td colspan="2">LED mode</td></tr>
<tr><td></td><td>1</td><td>2</td></tr>
<tr><td>LED0</td><td>Link</td><td>Link /ACT(blinking)</td></tr>
</table></td></tr>
<tr><td>10</td><td>LED1/PHY_AD1</td><td>O/LI</td><td>Hi-Z</td><td>LED 1 and PHY Address [1]
LED1
<table>
<tr><td></td><td colspan="2">LED mode</td></tr>
<tr><td></td><td>1</td><td>2</td></tr>
<tr><td>LED1</td><td>Duplex</td><td>Duplex /COL (blinking)</td></tr>
</table></td></tr>
<tr><td>12</td><td>LED2/PHY_AD2</td><td>O/LI</td><td>Hi-Z</td><td>LED 2 and PHY Address [2]
LED2
<table>
<tr><td></td><td colspan="2">LED mode</td></tr>
<tr><td></td><td>1</td><td>2</td></tr>
<tr><td>LED2</td><td>10M Link /ACT</td><td>10M Link</td></tr>
</table></td></tr>
<tr><td>13</td><td>LED3/PHY_AD3</td><td>O/LI
(PD)</td><td>Hi-Z</td><td>LED 3 and PHY Address [3]
LED3
<table>
<tr><td></td><td colspan="2">LED mode</td></tr>
<tr><td></td><td>1</td><td>2</td></tr>
<tr><td>LED3</td><td>100M Link /ACT</td><td>100M Link</td></tr>
</table></td></tr>
<tr><td>27</td><td>TEST_ON</td><td>I</td><td>I</td><td>Test Enable: Set this pin to high to enable Test mode.</td></tr>
</table>

IP101GA				
Pin no.	**Label**	**Type**	**Reset State**	**Description**
		(PD)	(PD)	For normal operation, this pin doesn't need to be connected.
Power and Ground				
32	NC	--	--	**It's a NC pin.**
8	REGOUT	P	P	**Regulator Power Output:** This is a regulator power output. A 10uF and 0.1uF should be connected to this pin to filter the power noise.
14	VDDIO	P	P	**Digital Power input:** Either 3.3V or 2.5V for I/O power supply.
36	AVDD33	P	P	**3.3V Analog power input:** This is a 3.3V power supply for analog circuitry, and it should be decoupled carefully.
35	AGND33	P	P	**Ground**.
29	AGND1V	P	P	**Ground**
45,11,17	DGND	P	P	**Ground**.

3.2 IP101GR/GRI pin description

<table>
<tr><th colspan="5">IP101GR/GRI</th></tr>
<tr><th>Pin no.</th><th>Label</th><th>Type</th><th>Reset State</th><th>Description</th></tr>
<tr><td colspan="5">Serial Management Interface Pins</td></tr>
<tr><td>22</td><td>MDC</td><td>I</td><td>Hi-Z</td><td>Management Data Interface Clock: This pin provides a clock reference to MDIO. The clock rate can be up to 2.5MHz.</td></tr>
<tr><td>23</td><td>MDIO</td><td>I/O (PU)</td><td>I (PU)</td><td>Management Data interface Input/Output: The function of this pin is to transfer management information between PHY and MAC.</td></tr>
<tr><td colspan="5">MII/RMII Pins</td></tr>
<tr><td>5</td><td>TXEN</td><td>I (PD)</td><td>I (PD)</td><td>Transmit Enable or Signal Detect.</td></tr>
<tr><td>1</td><td>TXER/FXSD</td><td>I (PD)</td><td>I (PD)</td><td>Transmit Error or FXSD:
This is a dual-function pin which is determined by the media type selection. If RXDV/CRS_DV/FX_HEN is latched as “0 (default)” upon reset, the TP interface is selected and its function as TXER. If the fiber interface is selected, this pin’s function as FXSD.

FXSD:
0: Fiber link down; 1: Fiber link up

Transmit Enable:
<table>
<tr><th>TXEN</th><th>TXER</th><th>Description</th></tr>
<tr><td>1</td><td>1</td><td>Transmission error propagation.</td></tr>
<tr><td>0</td><td>1</td><td>Combine TXD[3:0] that equal to 0001 for request PHY to enter LPI mode.</td></tr>
<tr><td>1</td><td>0</td><td rowspan="2">Normal operation</td></tr>
<tr><td>0</td><td>0</td></tr>
</table>
This pin TXER must be either floating or connecting to GND in RMII mode.</td></tr>
<tr><td>10</td><td>TXCLK/50M_CLKI</td><td>I/O</td><td>Hi-Z</td><td>Transmit Clock output or 50M clock input:
In MII mode, this pin provides a continuous 25MHz clock at 100Base-TX and 2.5MHz at 10Base-T.
In RMII mode, a 50Mhz clock should input to this pin for the timing reference of the internal circuit.</td></tr>
<tr><td>6,7,8,9</td><td>TXD[3:0]</td><td>I</td><td>Hi-Z</td><td>Transmit Data Input:
In MII mode, TXD[3:0] is synchronous to TXCLK.
In RMII mode, TXD[1:0] is synchronous to 50M_CLKI.</td></tr>
<tr><td>19</td><td>RXDV/CRS_DV/ FX_HEN</td><td>O/LI (PD)</td><td>I (PD)</td><td>Receive Data Valid or Media Type Selection:
FX_HEN
The input state is latched upon reset to determine whether TP or fiber interface is selected. If it is at logic “0” (default) state upon reset, the TP interface is selected; otherwise the fiber interface is selected.
RXDV/CRS_DV
In MII mode, this pin indicates the Receive Data Valid</td></tr>
</table>

IP101GR/GRI				
Pin no.	**Label**	**Type**	**Reset State**	**Description**
				function. In RMII mode, this pin indicates the Carrier Sense and Receive Data Valid function.
14	RXCLK/ 50M_CLKO	O	Hi-Z	**Receive Clock:** In MII mode, this pin provides 25MHz for 100BT or 2.5MHz for 10BT. In RMII mode, this pin output a 50 MHz clock for the timing reference of MAC side.
15,16, 17,18	RXD[3:0]	O	Hi-Z	**Receive Data:** In MII mode, RXD[3:0] is synchronous to RXCLK. In RMII mode, RXD[1:0] is synchronous to 50M_CLKI.
21	RXER/INTR_32	O/OD	Hi-Z	The multiplex function of this pin is set by the register SEL_INTR32, page 16, 29[2]. The default function is RXER. **Receive error:** RXDV / RXER / Description: 1 / 1 / Decoding error of the received signal 0 / 1 / Combine RXD[3:0] equal to 0001 indicates PHY is receiving LPI. 1 / 0 / Normal operation 0 / 0 This pin RXER is an optional input for MAC/CPU device. **Interrupt:** Programmable Interrupt Output, this is an open drain output, and an external pulled-up resistor is needed.
4	COL/RMII	O/LI (PD)	I (PD)	**Collision Detected:** During the normal operation, this pin outputs a high status signal it means collision is detected. **RMII Mode Selection:** During the power on reset, this pin status is latched to determine what kind MAC interface will be used. Logic “1” is for RMII mode and logic “0” is for MII mode.
20	CRS/LEDMOD	O/LI (PD)	I (PD)	**Carrier Sense:** When signal output from this pin is high indicates the transmission or reception is in process and at low status means the line is in idle state. **LEDMOD:** During power on reset, this pin status is latched to determine which either LED mode 1 or 2 is selected, please refer to the LED pins description.
Cable Transmission Interface				
30,29	MDI_TP MDI_TN	I/O I/O	Hi-Z	**Transmit Output Pair:** Differential pair shared by 100Base-TX and 10Base-T modes. When configured as 100Base-TX, output is an MLT-3 encoded waveform. When configured as 10Base-T, the output is Manchester code.
27,26	MDI_RP MDI_RN	I/O I/O	Hi-Z	**Receive Input Pair:** Differential pair shared by 100Base-TX and 10Base-T modes.
Clock and Miscellaneous Pins				

IP101GR/GRI				
Pin no.	**Label**	**Type**	**Reset State**	**Description**
3	X2	O	O	**25MHz Crystal Output:** Connects to crystal to provide the 25MHz output. It must be left open when X1 is driven with an external 25MHz oscillator.
2	X1	I	I	**25MHz Crystal Input:** Connects to crystal to provide the 25MHz crystal input. If a 25MHz oscillator is used, connect X1 to the oscillator's output. If a 50MHz clock is applied to pin10 TXCLK/50M_CLKI, X1 must be connected to GND.
32	RESET_N	I	I (PU)	**RESET_N:** Enable a low status signal will reset the chip. For a complete reset function. 25MHz clock (x1) must be active for a minimum of 10 clock cycles before the rising edge of RESET_N. Chip will be able to operate after 2.5ms delay of the rising edge of RESET_N. The 2.5ms extension is to ensure the stability of system power.
25	ISET	I	I	**Bandgap Circuit Resistor:** This pin should be connected to GND via a 6.19KΩ (1%) resistor to define the standard current of the internal circuit.
11	LED0/PHY_AD0	O/LI	Hi-Z	**LED 0 and PHY Address [0]** **LED 0** LED mode: 1 = Link; 2 = Link /ACT(blinking)
12	LED3/PHY_AD3	O/LI (PD)	Hi-Z	**LED 3 and PHY Address [3]** **LED3** LED mode: 1 = 100M Link /ACT; 2 = 100M Link
24	TEST_ON	I (PD)	I (PD)	**Test Enable:** Set this pin to high to enable Test mode. For normal operation, this pin doesn't need to be connected.
Power and Ground				
28	REGOUT	P	P	**Regulator Power Output:** This is a regulator power output. A 10uF and 0.1uF should be connected to this pin to filter the power noise.
13	VDDIO	P	P	**Digital Power input:** IP101GR: Either 3.3V or 2.5V for I/O power supply. IP101GRI: 3.3V for I/O power supply.
31	AVDD33	P	P	**3.3V Analog power input:** This is a 3.3V power supply for analog circuitry, and it should be decoupled carefully.
Bottom PAD	GND	P	P	**Ground**.

4 Register Descriptions

Table 2 Register Map

Page	Register	Description	Default	Note
X	20	Page Control Register	0x0010	
--	0	Control Register	0x3100	
--	1	Status Register	0x7849	
--	2	PHY Identifier 1 Register	0x0243	
--	3	PHY Identifier 2 Register	0x0C54	
--	4	Auto-Negotiation Advertisement Register	0x01E1	
--	5	Auto-Negotiation Link Partner Ability Register	0x0000	
--	6	Auto-Negotiation Expansion Register	0x0004	
--	7	Auto-Negotiation Next Page Transmit Register	0x2001	
--	8	Auto-Negotiation Link Partner Next Page Register	0x0000	
--	13	MMD Access Control Register	0x0000	
--	14	MMD Access Address Data Register	0x0000	
16	16	PHY Specific Control Register	0x0002	
16	17	PHY Interrupt Ctrl/Status Register	0x0F00	
16	18	PHY Status Monitoring Register	0x0208	
16	26	Digital IO Pin Driving Control Register	0x1249	
16	27	Digital IO Pin Driving Control Register	0x0012	
16	29	Digital I/O Specific Control Register	0x0082	
16	30	PHY MDI/MDIX Control and Specific Status Register	0x0000	
--	MMD 3.0	PCS Control 1 Register	0x0000	
--	MMD 3.1	PCS Status 1 Register	0x0000	
--	MMD 3.20	EEE Capability Register	0x0002	
--	MMD 3.22	EEE Wake Error Count Register	0x0000	
--	MMD 7.60	EEE Advertisement Register	0x0002	
--	MMD 7.61	EEE Link Partner Ability Register	0x0000	
1	17	PHY Specific Control Register	0x0000	
1	18	RX CRC Error Counter Register	0x0000	
1	22	Linear Regulator Output Control Register	0x2020	
1	23	UTP PHY Specific Control Register	0x8000	
2	18	RX Packet Counter Register	0x0000	
3	16	LED Control Register	0x0000	
4	16	WOL+ Control Register	0x5F40	
4	22	Digital IO Pin Driving Control Register	0x4000	
5	16	PHY WOL+ MAC Address Register	0x0000	
8	17	RX Counter Control Register	0x7000	
11	18	UTP PHY Interrupt Control/Status Register	0x0000	

Page	Register	Description	Default	Note
17	17	PHY WOL+ Status Register	0x0000	
18	17	RX Counter Interrupt Control/Status Register	0x0000	

Register descriptions
R/W = Read/Write, SC = Self-Clearing, RO = Read Only, LL = Latching Low, LH = Latching High
(TP): for twisted pair operation. (FX): for fiber operation.
(e-fuse): only available for IP101G (dice).

4.1 Register Page mode Control Register

MII register 20

PHY	MII	ROM	R/W	Description	Default
Page Control Register					
--	20[4:0]	--	R/W	Reg16~31_Page_Sel[4:0] Register Page Select	0x10

The other Registers are reserved registers. User is inhibited to access to these registers. It may introduce abnormal function to write these registers.

4.2 MII Registers

Bit	Name	Description/Usage	Default value (h): 3100
Register 0 : Control Register			
15	Reset	When set, this action will bring both status and control registers of the PHY to default state. This bit is self-clearing. 1 = Software reset 0 = Normal operation	0, RW/SC
14	Loopback	This bit enables loopback of transmit data to the receive data path, i.e., TXD to RXD. 1 = enable loopback 0 = normal operation	0, RW
13	Speed Selection	This bit sets the speed of transmission. 1 = 100Mbps 0 = 10Mbps After completing auto-negotiation, this bit will reflect the speed status.(1: 100Mbps, 0: 10Mbps)	1, RW
12	Auto-Negotiation Enable	This bit determines the auto-negotiation function. 1 = enable auto-negotiation; bits 13 and 8 will be ignored. 0 = disable auto-negotiation; bits 13 and 8 will determine the link speed and the data transfer mode, under this condition.	1, RW (TP) 0, RO (FX)
11	Power Down	This bit will turn down the power of the PHY chip and the internal crystal oscillator circuit if this bit is enabled. The MDC and MDIO are still activated for accessing to the MAC. 1 = power down 0 = normal operation	0, RW
10	Isolate	1=electrically Isolate PHY from MII but not isolate MDC and MDIO	0,RW

Bit	Name	Description/Usage	Default value (h): 3100
Register 0 : Control Register			
		0=normal operation	
9	Restart Auto-Negotiation	This bit allows the auto-negotiation function to be reset. 1 = restart auto-negotiation 0 = normal operation	0, RW/SC
8	Duplex Mode	This bit sets the duplex mode if auto-negotiation is disabled (bit 12=0) 1 = full duplex 0 = half duplex After completing auto-negotiation, this bit will reflect the duplex status.(1: Full duplex, 0: Half duplex)	1, RW
7	Collision Test	1=enable COL signal test 0=disable COL signal test	0,RW
6:0	Reserved		0, RO

Bit	Name	Description/Usage	Default value (h): 7849
Register 1 : Status Register			
15	100Base-T4	1 = enable 100Base-T4 support 0 = suppress 100Base-T4 support	0, RO
14	100Base-TX Full Duplex	1 = enable 100Base-TX full duplex support 0 = suppress 100Base-TX full duplex support	1, RO
13	100BASE-TX Half Duplex	1 = enable 100Base-TX half duplex support 0 = suppress 100Base-TX half duplex support	1, RO
12	10Base-T Full Duplex	1 = enable 10Base-T full duplex support 0 = suppress 10Base-T full duplex support	1, RO
11	10_Base-T Half Duplex	1 = enable 10Base-T half duplex support 0 = suppress 10Base-T half duplex support	1, RO
10:7	Reserved		0, RO
6	MF Preamble Suppression	The IP101G will accept management frames with preamble suppressed. The IP101G accepts management frames without preamble. A Minimum of 32 preamble bits is required for the first SMI read/write transaction after reset. One idle bit is required between any two management transactions as per IEEE802.3u specifications	1, RO
5	Auto- Negotiation Complete	1 = auto-negotiation process completed 0 = auto-negotiation process not completed	0, RO
4	Remote Fault	1 = remote fault condition detected (cleared on read) 0 = no remote fault condition detected	0, RO/LH
3	Auto- Negotiation	1 = able to perform auto-negotiation 0 = unable to perform auto-negotiation	1, RO
2	Link Status	1 = valid link established 0 = no valid link established	0, RO/LL
1	Jabber Detect	1 = jabber condition detected 0 = no jabber condition detected	0, RO/LH
0	Extended Capability	1 = extended register capability 0 = basic register capability only	1, RO

Bit	Name	Description/Usage	Default value (h): 0243
Register 2 : PHY Identifier 1 Register			
15:0	PHYID1	PHY identifier ID for software recognize IP101G	0X0243, RO

Bit	Name	Description/Usage	Default value (h): 0C54
Register 3 : PHY Identifier 2 Register			
15:0	PHYID2	PHY identifier ID for software recognize	0X0C54, RO

Note: Register 2 and register 3 identifier registers altogether consist of Vender model, model revision number and Organizationally Unique identifier (OUI) information. Total of 32 bits allocate in these 2 registers and they can return all zeroes in all bits if desired. Register 2 contains OUI's most significant bits and OUI's least significant bits, Vender model, Model revision number are allocated in register 3.

Register 4 lists the advertised abilities during auto-negotiation for what will be transmitted to IP101G's Link Partner.

Bit	Name	Description/Usage	Default value (h): 01E1
Register 4 : Auto-Negotiation Advertisement Register			
15	NP	Next Page bit. 0 = transmitting the primary capability data page 1 = transmitting the protocol specific data page	0, RO
14	Reserved		0, RO
13	RF	1 = advertise remote fault detection capability 0 = do not advertise remote fault detection capability	0, RW
12	Reserved		0, RO
11	Asymmetric. Pause	1 = asymmetric flow control is supported by local node 0 = asymmetric flow control is NOT supported by local node	0, RW
10	Pause	1 = flow control is supported by local node 0 = flow control is NOT supported by local node	0, RW
9	T4	1 = 100Base-T4 is supported by local node 0 = 100Base-T4 not supported by local node	0, RO
8	TX Full Duplex	1 = 100Base-TX full duplex is supported by local node 0 = 100Base-TX full duplex not supported by local node	1, RW
7	TX	1 = 100Base-TX is supported by local node 0 = 100Base-TX not supported by local node	1, RW
6	10 Full Duplex	1 = 10Base-T full duplex supported by local node 0 = 10Base-T full duplex not supported by local node	1, RW
5	10	1 = 10Base-T is supported by local node 0 = 10Base-T not supported by local node	1, RW
4:0	Selector	Binary encoded selector supported by this node. Currently only CSMA/CD <00001> is specified. No other protocols are supported.	<00001>, RO

This register contains the advertised abilities of the Link Partner as received during Auto-negotiation. The content changes after the successful Auto-negotiation if Next-pages are supported.

Bit	Name	Description/Usage	Default value (h): 0000
Register 5 : Auto-Negotiation Link Partner Ability Register (ANLPAR)			
15	Next Page	Next Page bit. 0 = transmitting the primary capability data page 1 = transmitting the protocol specific data page	0, RO
14	Acknowledge	1 = link partner acknowledges reception of local node's capability data word 0 = no acknowledgement	0, RO
13	Remote Fault	1 = link partner is indicating a remote fault 0 = link partner does not indicate a remote fault	0, RO
12	Reserved		0, RO
11	Asymmetric. Pause	1 = asymmetric flow control is supported link partner 0 = asymmetric flow control is NOT supported by link partner	0, RO
10	Pause	1 = flow control is supported by Link partner 0 = flow control is NOT supported by Link partner	0, RO
9	T4	1 = 100Base-T4 is supported by link partner 0 = 100Base-T4 not supported by link partner	0, RO
8	TXFD	1 = 100Base-TX full duplex is supported by link partner 0 = 100Base-TX full duplex not supported by link partner	0, RO
7	100BASE-TX	1 = 100Base-TX is supported by link partner 0 = 100Base-TX not supported by link partner This bit will also be set after the link in 100Base-TX is established by parallel detection.	0, RO
6	10FD	1 = 10Base-T full duplex is supported by link partner 0 = 10Base-T full duplex not supported by link partner	0, RO
5	10Base-T	1 = 10Base-T is supported by link partner 0 = 10Base-T not supported by link partner This bit will also be set after the link in 10Base-T is established by parallel detection.	0, RO
4:0	Selector	Link Partner's binary encoded node selector Currently only CSMA/CD <00001> is specified	<00000>, RO

Register 6 defines more auto-negotiation registers to meet the requirement.

Bit	Name	Description/Usage	Default value (h): 0004
Register 6 : Auto-Negotiation Expansion Register			
15:5	Reserved	This bit is always set to 0.	0, RO
4	MLF	This status indicates if a multiple link fault has occurred. 1 = fault occurred 0 = no fault occurred	0, RO
3	LP_NP_ABLE	This status indicates if the link partner supports Next Page negotiation. 1 = supported 0 = not supported	0, RO
2	NP_ABLE	This bit indicates if the device is able to send additional Next Pages.	1, RO
1	PAGE_RX	This bit will be set if a new link code word page has been received. It is cleared automatically after the auto-negotiation link partner's ability register (register 5) is read by the management.	0, RO
0	LP_NW_ABLE	1 = link partner supports auto-negotiation.	0, RO

Register 7 defines more auto-negotiation registers to meet the requirement.

Bit	Name	Description/Usage	Default value (h): 2001
Register 7 : Auto-Negotiation Next Page Transmit Register			
15	Next Page	Next Page Transmit Code Word Bit 15	0, RW
14	Reserved	Reserved Transmit Code Word Bit 14	0, RW
13	Message Page	Message Page Transmit Code Word Bit 13	1, RW
12	Acknowledge 2	Acknowledge 2 Transmit Code Word Bit 12	0, RW
11	Toggle	Toggle Transmit Code Word Bit 11	0, RW
[10:0]	Message/Unformatted Field	Message/Unformatted Field Transmit Code Word Bit 10:0	1, RW

Register 8 defines more auto-negotiation registers to meet the requirement.

Bit	Name	Description/Usage	Default value (h): 0000
Register 8 : Auto-Negotiation Link Partner Next Page Register			
15	Next Page	Next Page Received Code Word Bit 15	0, RO
14	Reserved	Acknowledge Received Code Word Bit 14	0, RO
13	Message Page	Message Page Received Code Word Bit 13	0, RO
12	Acknowledge 2	Acknowledge 2 Received Code Word Bit 12	0, RO
11	Toggle	Toggle Received Code Word Bit 11	0, RO
[10:0]	Message/Unformatted Field	Message/Unformatted Field Received Code Word Bit 10:0	0, RO

The other Registers are reserved registers. User is inhibited to access to these registers. It may introduce abnormal function to write these registers.

MII page16 register16

<table>
<tr><th>page</th><th>MII</th><th>ROM</th><th>R/W</th><th>Description</th><th>Default</th></tr>
<tr><td colspan="6">UTP PHY Specific Control Register</td></tr>
<tr><td rowspan="6">16</td><td>16[15:14]</td><td></td><td>RO</td><td>Reserved</td><td>2'b00</td></tr>
<tr><td>16[13]</td><td></td><td>R/W</td><td>RMII_V10
This bit combines with RMII_V12 bit for RMII mode settings.</td><td>0</td></tr>
<tr><td>16[12]</td><td></td><td>R/W</td><td>RMII_V12
<table>
<tr><th>RMII_V10</th><th>RMII_V12</th><th>REPEATER_MODE (P16R16[2])</th><th>Mode</th></tr>
<tr><td>0</td><td>0</td><td>X</td><td>RMII back to back mode</td></tr>
<tr><td>X</td><td>1</td><td>1</td><td>RMII v1.2 CRS_DV will toggle at the end</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>RMII v1.0 CRS_DV will not toggle at the end</td></tr>
</table>
Note 1: "X" indicate don't care (either 1 or 0).
Note 2: When RMII_v10 or RMII_v12 is selected, page16 reg16 bit2 should be also set to 1 to enable repeater mode. Then CRS_DV will be asserted only when receive medium is nonidle.</td><td>0</td></tr>
<tr><td>16[11]</td><td></td><td>R/W</td><td>AUTO_MDIX_DIS
Set high to disable the automatic switch of MDI and MDI-X modes. For details, please refer to section 4 Auto-MDIX function description.</td><td>0</td></tr>
<tr><td>16[10]</td><td></td><td>R/W</td><td>Reserved</td><td>0</td></tr>
<tr><td>16[9]</td><td></td><td>R/W</td><td>JABBER_ENABLE
Jabber function enable at 10Base-T</td><td>0</td></tr>
</table>

MII page16 register16

page	MII	ROM	R/W	Description	Default
	16[8]		R/W	FEF_DISABLE To enable or disable the functionality of Far-End Fault Mode Enable Disable 100Base-TX 1 0	0
	16[7]		R/W	NWAY_PSAVE_DIS Set high to disable the power saving during auto-negotiation	0
	16[6]		RO	Reserved	0
	16[5]		R/W	BYPASS_DSP_RESET Set high to bypass the reset DSP mechanism in PCS sub-layer	0
	16[4:3]		RO	Reserved	2'b00
	16[2]		R/W	REPEATER_MODE Set high to put IP101G into repeater mode	0
	16[1]		R/W	LDPS_ENABLE Set high to enable Auto Power Saving mode	1
	16[0]		R/W	ANALOG_OFF Set high to power down analog transceiver	0

The other Registers are reserved registers. User is inhibited to access to these registers. It may introduce abnormal function to write these registers.

MII page16 register17

page	MII	ROM	R/W	Description	Default
Interrupt Status Register					
16	17[15]		R/W	INTR pin used Interrupt pin used. Set high to enable INTR or INTR_32 as an interrupt pin. Pin INTR or INTR_32 will be high impedance if this bit is set low.	0
	17[14:12]		RO	Reserved	3'b000
	17[11]		R/W	All Mask When this bit is set high, flags to be raised on bit 6, 2, 1 and 0 will not cause an interrupt.	1
	17[10]		R/W	Speed Mask When this bit is set high, changes in speed mode will not cause an interrupt.	1
	17[9]		R/W	Duplex Mask When this bit is set high, changes in duplex mode will not cause an interrupt.	1
	17[8]		R/W	Link Mask When this bit is set high, changes in link status will not cause an interrupt.	1
	17[7:4]		RO	Reserved	0x0
	17[3]		RO (SC)	INTR Status Flag to indicate interrupt status	0
	17[2]		RO (SC)	Speed Change Flag to indicate speed change interrupt	0

MII page16 register17

page	MII	ROM	R/W	Description	Default
	17[1]		RO (SC)	Duplex Change Flag to indicate duplex change interrupt	0
	17[0]		RO (SC)	Link Change Flag to indicate link status change interrupt	0

The other Registers are reserved registers. User is inhibited to access to these registers. It may introduce abnormal function to write these registers.

MII page16 register18

page	MII	ROM	R/W	Description	Default
UTP PHY Interrupt Control/Status Register					
16	18[15]		RO	Reserved	0
	18[14]		RO	Resolved Speed The resolved speed selection after auto negotiation or forced mode	0
	18[13]		RO	Resolved Duplex The resolved duplex selection after auto negotiation or forced mode	0
	18[12]		RO	Reserved	0
	18[11]		RO	Resolved Auto negotiation completed To indicate if auto negotiation is finished	0
	18[10]		RO	LINK_UP To indicate the link status is OK or FAIL	0
	18[9]		RO	MDI/MDIX To indicate which channel is selected by auto-MDIX. 1: MDIX is selected 0: MDI is selected	1
	18[8]		RO	POLARITY To indicate the polarity of twist pair N/P is reversed	0
	18[7]		RO	JABBER To indicate if jabber packet is received or not, when bit 16:<9> is set high	0
	18[6:4]		RO	Reserved	0
	18[3:0]		RO	AN_ARBIT_STATE To monitor the current value of N-WAY arbiter state machine 8: AUTO NEGOTIATION ENABLE 0: TRANSMIT DISABLE 1: ABILITY DETECT 5: ACKNOWLEDGE DETECT 4: COMPLETE ACKNOWLEDGE 12: NEXT PAGE WAIT 3: LINK STATUS CHECK 9: PARALLEL DETECTION FAULT 2: FLP LINK GOOD CHECK 10: FLP LINK GOOD	0x8

The other Registers are reserved registers. User is inhibited to access to these registers. It may introduce abnormal function to write these registers.

MII page16 register29

page	MII	ROM	R/W	Description	Default
Digital I/O Specific Control Register					
16	29[15:8]		R/W	Reserved	0x00
	29[7]		R/W	RMII_WITH_ER 1: enable TXER/RXER function in RMII mode. 0: disable TXER/RXER function in RMII mode.	1
	29[6:3]		R/W	Reserved	4'b0000
	29[2]		R/W	SEL_INTR32 The multiplex function is for 32pin package at pin21 RXER/INTR_32. 1: INTR function 0: RXER function	0
	29[1:0]		R/W	Reserved	2'b10

The other Registers are reserved registers. User is inhibited to access to these registers. It may introduce abnormal function to write these registers.

MII page16 register30

page	MII	ROM	R/W	Description	Default
PHY MDI/MDIX Control and Specific Status Register					
16	30[15:9]		RO	Reserved	0
	30[8]		RO	LINK_UP To indicate the link status is OK or FAIL	0
	30[7:4]		RO	Reserved	0
	30[3]		R/W	FORCE_MDIX Set high to force the MDIX channel to be selected. 1: Force the MDIX channel to be selected. 0: MDI channel is selected when auto-MDIX is turned off. When IP101G operates in Force 10Mbps mode or APS mode, this bit is not able to write.	0
	30[2:0]		RO	OP_MODE_IND Operation Mode Idicator 000= Link off 001= 10M Half 010= 100M Half 011= Reserved 100= Reserved 101= 10M Full 110= 100M Full 111= Reserved	3'b000

The other Registers are reserved registers. User is inhibited to access to these registers. It may introduce abnormal function to write these registers.

MII page1 register17

page	MII	ROM	R/W	Description	Default

MII page1 register17

page	MII	ROM	R/W	Description	Default
PHY Spec. Control Register					
1	17[15:9]		R/W	Reserved	0
	17[8]		R/W	FORCE_LINK_10	0
	17[7]		R/W	FORCE_LINK_100	0
	17[6:0]		R/W	Reserved	0

The other Registers are reserved registers. User is inhibited to access to these registers. It may introduce abnormal function to write these registers.

4.3 MMD Control Register

MII register 13

page	MII	ROM	R/W	Description	Default
MMD Access Control Register					
--	13[15:14]	--	R/W	Function 00 = address 01 = data, no post increment 10 = data, post increment on reads and writes 11 = data, post increment on writes only	0
--	13[13:5]	--	R/W	Reserved Write as 0, ignore on read	0
--	13[4:0]	--	R/W	DEVAD Device Address	0

MII register 14

page	MII	ROM	R/W	Description	Default
MMD Access Address Data Register					
--	14[15:0]	--	R/W	Address Data If 13.15:14 = 00, MMD DEVAD's address register. Otherwise, MMD DEVAD's data register as indicated by the contents of its address register	0

Example 1, Read 0.3.20 (Read Data from MMD register 3.20 of PHY address 0):

1. Write 0.13 = 0x0003 //MMD DEVAD 3
2. Write 0.14 = 0x0014 //MMD Address 20
3. Write 0.13 = 0x4003 //MMD Data command for MMD DEVAD 3
4. Read 0.14 //Read MMD Data from 0.3.20

Example 2, Write 1.7.60 = 0x3210 (Write 0x3210 Data to MMD register 7.60 of PHY address 1):

1. Write 1.13 = 0x0007 //MMD DEVAD 7
2. Write 1.14 = 0x003C //MMD Address 60
3. Write 1.13 = 0x4007 //MMD Data command for MMD DEVAD 7
4. Write 1.14 = 0x3210 //Write MMD Data 0x3210 to 1.7.60

4.4 MMD Data Register

MMD register 3.0

Page	MII	ROM	R/W	Description	Default
PCS Control 1 Register					
--	3.0[15:11]		RO	Reserved Ignore when read	0
--	3.0.10		R/W	Clock stop enable 1 = IP101G may stop xMII Rx clock during LPI 0 = Clock not stoppable	0
--	3.0[9:0]		RO	Reserved Ignore when read	0

MMD register 3.1

page	MII	ROM	R/W	Description	Default
PCS Status 1 Register					
--	3.1[15:12]		RO	Reserved Ignore when read	0
--	3.1.11		RO/LH	Tx LPI received 1 = Tx PCS has received LPI 0 = LPI not received	0
--	3.1.10		RO/LH	Rx LPI received 1 = Rx PCS has received LPI 0 = LPI not received	0
--	3.1.9		RO	Tx LPI indication 1 = Tx PCS is currently receiving LPI 0 = PCS is not currently receiving LPI	0
--	3.1.8		RO	Rx LPI indication 1 = Rx PCS is currently receiving LPI 0 = PCS is not currently receiving LPI	0
--	3.1.7		RO	Reserved Ignore on read	0
--	3.1.6		RO	Clock stop capable 1 = The MAC may stop the clock during LPI 0 = Clock not stoppable	0
--	3.1[5:0]		RO	Reserved Ignore when read	0

MMD register 3.20

page	MII	ROM	R/W	Description	Default
EEE Capability Register					
--	3.20[15:7]		RO	Reserved Ignore when read	0

MMD register 3.20

page	MII	ROM	R/W	Description	Default
--	3.20.6		RO	10GBASE-KR EEE 1 = EEE is supported for 10GBASE-KR 0 = EEE is not supported for 10GBASE-KR	0
--	3.20.5		RO	10GBASE-KX4 EEE 1 = EEE is supported for 10GBASE-KX4 0 = EEE is not supported for 10GBASE-KX4	0
--	3.20.4		RO	1000BASE-KX EEE 1 = EEE is supported for 1000BASE-KX 0 = EEE is not supported for 1000BASE-KX	0
--	3.20.3		RO	10GBASE-T EEE 1 = EEE is supported for 10GBASE-T 0 = EEE is not supported for 10GBASE-T	0
--	3.20.2		RO	1000BASE-T EEE 1 = EEE is supported for 1000BASE-T 0 = EEE is not supported for 1000BASE-T	0
--	3.20.1		RO	100BASE-TX EEE 1 = EEE is supported for 100BASE-TX 0 = EEE is not supported for 100BASE-TX	1
--	3.20.0		RO	Reserved Ignore when read	0

MMD register 3.22

page	MII	ROM	R/W	Description	Default
EEE Wake Error Count Register					
--	3.22[15:0]		RO (SC)	EEE wake error count Count wake time faults where IP101G fails to complete its normal wake sequence within the time required for the specific PHY type.	0x0000

MMD register 7.60

page	MII	ROM	R/W	Description	Default
EEE Advertisement Register					
--	7.60[15:7]		RO	Reserved Ignore when read	0
--	7.60.6		RO	10GBASE-KR EEE 1 = Advertise that the 10GBASE-KR has EEE capability 0 = Do not advertise that the 10GBASE-KR has EEE capability	0
--	7.60.5		RO	10GBASE-KX4 EEE 1 = Advertise that the 10GBASE-KX4 has EEE capability 0 = Do not advertise that the 10GBASE-KX4 has EEE capability	0
--	7.60.4		RO	1000BASE-KX EEE 1 = Advertise that the 1000BASE-KX has EEE capability 0 = Do not advertise that the 1000BASE-KX has EEE capability	0

MMD register 7.60

page	MII	ROM	R/W	Description	Default
--	7.60.3		RO	10GBASE-T EEE 1 = Advertise that the 10GBASE-T has EEE capability 0 = Do not advertise that the 10GBASE-T has EEE capability	0
--	7.60.2		RO	1000BASE-T EEE 1 = Advertise that the 1000BASE-T has EEE capability 0 = Do not advertise that the 1000BASE-T has EEE capability	0
--	7.60.1		R/W	100BASE-TX EEE 1 = Advertise that the 100BASE-TX has EEE capability 0 = Do not advertise that the 100BASE-TX has EEE capability	1
--	7.60.0		RO	Reserved Ignore when read	0

MMD register 7.61

page	MII	ROM	R/W	Description	Default
EEE Link Partner Ability Register					
--	7.61[15:7]		RO	Reserved Ignore when read	0
--	7.61.6		RO	10GBASE-KR EEE 1 = Link partner is advertising EEE capability for 10GBASE-KR 0 = Link partner is not advertising EEE capability for 10GBASE-KR	0
--	7.61.5		RO	10GBASE-KX4 EEE 1 = Link partner is advertising EEE capability for 10GBASE-KX4 0 = Link partner is not advertising EEE capability for 10GBASE-KX4	0
--	7.61.4		RO	1000BASE-KX EEE 1 = Link partner is advertising EEE capability for 1000BASE-KX 0 = Link partner is not advertising EEE capability for 1000BASE-KX	0
--	7.61.3		RO	10GBASE-T EEE 1 = Link partner is advertising EEE capability for 10GBASE-T 0 = Link partner is not advertising EEE capability for 10GBASE-T	0
--	7.61.2		RO	1000BASE-T EEE 1 = Link partner is advertising EEE capability for 1000BASE-T 0 = Link partner is not advertising EEE capability for 1000BASE-T	0
--	7.61.1		RO	100BASE-TX EEE 1 = Link partner is advertising EEE capability for 100BASE-TX 0 = Link partner is not advertising EEE capability for 100BASE-TX	0
--	7.61.0		RO	Reserved Ignore when read	0

The other Registers are reserved registers. User is inhibited to access to these registers. It may introduce abnormal function to write these registers.

4.5 RX Counter Register

MII page1 register17

page	MII	ROM	R/W	Description	Default
RX Counter Control Register					
1	17[13]		R/W	RX Counter Enable 0= RX Counter Disable 1= RX Counter Enable for CRC_ERR_CNT(P1R18[15:0]), PKT_STS_CNT(P2R18[15:0]) and SYMB_ERR_CNT(P11R18[15:0]).	0

The other Registers are reserved registers. User is inhibited to access to these registers. It may introduce abnormal function to write these registers.

MII page1 register18

page	MII	ROM	R/W	Description	Default
RX CRC Error Counter Register					
1	18[15:0]		RO	CRC_ERR_CNT RX CRC error counter	0x0000

MII page2 register18

page	MII	ROM	R/W	Description	Default
RX Packet Counter Register					
2	18[15:0]		RO	PKT_STS_CNT RX packet status counter (include CRC good and error packet)	0x0000

MII page8 register17

page	MII	ROM	R/W	Description	Default
RX Counter Control Register					
8	17[15]		R/W	RXERR_CNT_RDCLR_EN Set 1 to clear RX error counter after reading	0
	17[14]		R/W	RXERR_CNT_REPEAT This bit is set to 0 when RXERR_INTR_EN = 1	1
	17[13:12]		R/W	RXERR_CNTDOWN_SEL Select the RX error countdown value 2'b00: 1 2'b01: 255 2'b10: 1023 2'b11: 65535	2'b11
	17[11:0]		RO	Reserved	0x000

MII page11 register18

page	MII	ROM	R/W	Description	Default
UTP PHY Interrupt Control/Status Register					

MII page11 register18

page	MII	ROM	R/W	Description	Default
11	18[15:0]		RO	SYMB_ERR_CNT RX symbol error counter Each symbol error of idle will add the counter by 1. Several symbol errors of one data frame will add the counter by 1.	0x0000

MII page18 register17

page	MII	ROM	R/W	Description	Default
RX Counter Interrupt Control/Status Register					
18	17[15]		R/W	RXERR_INTR_EN Set 1 to enable RXERR interrupt function	0
	17[14]		R/W	RXERR_INTR_SEL Select RXERR interrupt type 0= RX CRC error 1= RX Symbol error	0
	17[13:1]		RO	Reserved	0x000
	17[0]		RO/ LH	INTR_RXERR_CNTDOWN Flag to indicate RX error countdown interrupt	0

The other Registers are reserved registers. User is inhibited to access to these registers. It may introduce abnormal function to write these registers.

4.6 LED Mode Control Register

MII page3 register16

page	MII	ROM	R/W	Description	Default
LED Control Register					
3	16[14]		R/W	LED_SEL LED output mode selection. 1'b0= LED Mode 1 1'b1= LED Mode 2	{pin CRS/LEDMOD}

	Mode 1	Mode 2
LED0	Link	Link/ACT
LED1	Duplex	Duplex/COL
LED2	10M Link/ACT	10M Link
LED3	100M Link/ACT	100M Link

The other Registers are reserved registers. User is inhibited to access to these registers. It may introduce abnormal function to write these registers.

4.7 WOL+ Control Register

MII page4 register16

page	MII	ROM	R/W	Description	Default
PHY WOL+ Control Register					

MII page4 register16

page	MII	ROM	R/W	Description	Default
4	16[15]		R/W	WOL_PLUS_EN WOL+ enable function. Set high to enable WOL+ function. 1=Enable 0=Disable	0
	16[14]		R/W	WOL_PLUS_MASTER WOL+ master mode setting. This bit is used to select WOL+ either master mode or slave mode. 1=WOL+ Master mode 0=WOL+ Slave mode	1
	16[13]		R/W	INTR_ACT_HIGH Interrupt active high. This bit is used to select the active level either high or low of interrupt pin. 1=Pin "INTR" is set to output type and active high. 0=Pin "INTR" is set to open drain type and active low.	0
	16[12]		R/W	Reserved	1
	16[11]		R/W	SENSE_MAGIC_PKT Sense Magic Packet. Set high to enable WOL+ interrupt when magic packet is receiving. 1=Enable 0=Disable	1
	16[10]		R/W	SENSE_ANY_PKT Sense Any Packet. Set high to enable WOL+ interrupt when any good CRC packet is receiving. 1=Enable 0=Disable	1
	16[9]		R/W	SENSE_DUT Sense DUT. Set high to enable wake up event detection (magic packet, any packet) of corresponding port. 1=Enable 0=Disable	1
	16[8]		R/W	WOL_PLUS_DNSPD_EN WOL+ Down Speed Enable. Set high to enable WOL+ down speed function 1=Enable 0=Disable	1
	16[7:6]		R/W	WOL_PLUS_TIMER_SEL WOL+ Timer Select, 2'b00 = 30 seconds. 2'b01 = 3 minutes. 2'b10 = Reserved for internal test used. 2'b11 = 10 minutes.	2'b01

MII page4 register16

page	MII	ROM	R/W	Description	Default
	16[5]		R/W (SC)	WOL_PLUS_MANUAL_SET WOL+ Manual Set. CPU/MAC can set high to sleep mode or wake up in slave mode. 1=Manual set sleep/wake in WOL+ slave mode. 0=Disable.	0
	16[4:0]		RO	Reserved	0x00

MII page5 register16

page	MII	ROM	R/W	Description	Default
PHY WOL+ MAC Address Register					
5	16[15:0]		R/W	WOL_PLUS_MAC_ADDR WOL+ MAC address table. Continuously write/read this register 3 times to set/obtain WOL+ Magic packet MAC address. The sequence of MAC address is [47~32], [31~16] then [15~0].	0x0000

MII page17 register17

page	MII	ROM	R/W	Description	Default
PHY WOL+ Status Register					
17	17[15]		R/W	WOL_PLUS_INTR_PIN_DIS WOL+ interrupt pin disable. Interrupt pin INTR is served to WOL+ event only, when this bit set to 0 and not only enable WOL_PLUS_EN (Page4 Reg16[15]=1) but also INTR pin used (Page16 Reg17[15]=1).	0
17	17[14:4]		RO	Reserved	0x000
17	17[3]		RO (SC)	WOL_PLUS_INTR_STATUS WOL+ interrupt status. 1=Interrupt event. 0=Normal (no any interrupt event).	0
17	17[2]		RO	WOL_PLUS_SLEEPING WOL+ sleeping status. This bit is a real-time status in WOL+ sleep mode. 1=IP101G is in WOL+ sleeping mode.	0

INTR pin used (P16R17[15])	WOL_PLUS_EN (P4R16[15])	WOL_PLUS_INT_PIN_DIS (P17R17[15])	INTR pin function
0	X	X	Disable
1	0	0	Not including WOL+ interrupt status
1	X	1	
1	1	0	Only for WOL+ interrupt status

MII page17 register17

page	MII	ROM	R/W	Description	Default
17	17[1]		RO/ LH	WOL_PLUS_SLEEP WOL+ sleep status. This bit is a latched high signal that provide a previous status for WOL+ sleep mode. Master mode: 1=IP101G has entered WOL+ sleep mode. Slave mode: 1=IP101G is ready for entering WOL+ sleep mode.	0
17	17[0]		RO/ LH	WOL_PLUS_WAKE WOL+ wake status. This bit is a latched high signal that provide a previous status for WOL+ wake up. Master mode: 1=IP101G has left WOL+ sleep mode. Slave mode: 1=IP101G is ready for wake up.	0

The other Registers are reserved registers. User is inhibited to access to these registers. It may introduce abnormal function to write these registers.

Example 1, Read page3 register16 (Read Data from page3 register16 of PHY address 0):

1. Write 0.20 = 0x0003 //page3
2. Read 0.16 //Read Data from page3 register16
3. Write 0.20 = 0x0000 //restore to page0

Example 2, Write page3 register16 = 0x3400 (Write Data 0x3400 to page3 register16 of PHY address 0):

1. Write 0.20 = 0x0003 //page3
2. Write 0.16 = 0x3400 //Write Data 0x3400 to page3 register16
3. Write 0.20 = 0x0000 //restore to page0

4.8 UTP PHY Specific Control Register

MII page1 register22

page	MII	ROM	R/W	Description	Default
Linear Regulator Output Control Register					
1	22[15]		R/W	LDO Output Disable 1: LDO Output Disable 0: LDO Output Enable	0 (e-fuse)
	22[14:0]		R/W	Reserved	0x2020

The other Registers are reserved registers. User is inhibited to access to these registers. It may introduce abnormal function to write these registers.

MII page1 register23

page	MII	ROM	R/W	Description	Default
UTP PHY Specific Control Register					
1	23[15:14]		R/W	Reserved	2'b10

MII page1 register23

page	MII	ROM	R/W	Description	Default
	23[13]		R/W	RX2TX_LPBK 1= Rx to Tx loopback mode for debugging 0= Normal mode (INTR pin of IP101G/IP101GA should pull 5.1K resistor to DVDD33_IO for normal mode operation. We can connect INTR pin to GND for Rx to Tx loopback test.)	0
	23[12]		R/W	Reserved	0
	23[11]		R/W	FIX_TXD_EN 1= Fix TXD pattern 0= Normal mode	0
	23[10]		R/W	FIX_TXD_SEL 1= Long pulse 0= Short pulse	0
	23[9]		R/W	FORCE_TX_LPI 1= Force TX LPI 0= TX respond to MII	0
	23[8:0]		R/W	Reserved	0

The other Registers are reserved registers. User is inhibited to access to these registers. It may introduce abnormal function to write these registers.

4.9 Digital IO Pin Control Register

MII page4 Register22

page	MII	ROM	R/W	Description	Default
Digital IO Pin Driving Control Register					
4	22[15:13]		R/W	RXC_DRIVE RXC PAD Driving Current 3'b000: 1.62mA 3'b001: 3.24mA 3'b010: 4.86mA 3'b011: 6.48mA 3'b100: 8.10mA 3'b101: 12.96mA 3'b110: 17.82mA 3'b111: 22.68mA	3'b010 (e-fuse)
	22[12:11]		RO	Reserved	2'b00
	22[10:0]		R/W	Reserved	0x000

The other Registers are reserved registers. User is inhibited to access to these registers. It may introduce abnormal function to write these registers.

MII page16 Register26~27

page	MII	ROM	R/W	Description	Default
Digital IO Pin Driving Control Register					
16	26[15]		RO	Reserved	0

MII page16 Register26~27

page	MII	ROM	R/W	Description	Default
	26[14:12]		R/W	RXDV_DRIVE RXDV PAD Driving Current is defined as same as RXC.	3'b001
	26[11:9]		R/W	RXD3_DRIVE RXD3 PAD Driving Current is defined as same as RXC.	3'b001
	26[8:6]		R/W	RXD2_DRIVE RXD2 PAD Driving Current is defined as same as RXC.	3'b001
	26[5:3]		R/W	RXD1_DRIVE RXD1 PAD Driving Current is defined as same as RXC.	3'b001
	26[2:0]		R/W	RXD0_DRIVE RXD0 PAD Driving Current is defined as same as RXC.	3'b001
	27[15]		RO	Reserved	0
	27[14:12]		R/W	MDIO_DRIVE MDIO PAD Driving Current is defined as same as RXC.	3'b000
	27[11:9]		R/W	COL_DRIVE COL PAD Driving Current is defined as same as RXC.	3'b000
	27[8:6]		R/W	CRS_DRIVE CRS PAD Driving Current is defined as same as RXC.	3'b000
	27[5:3]		R/W	Reserved	3'b010
	27[2:0]		R/W	TXC_DRIVE TXC PAD Driving Current is defined as same as RXC.	3'b010

The other Registers are reserved registers. User is inhibited to access to these registers. It may introduce abnormal function to write these registers.

5 Function Description

IP101G 10/100Mbps Ethernet PHY Transceiver integrates 100 Base-TX and 10 Base-T modules into a single chip. IP101G acts as an interface between physical signaling and Media Access Controller (MAC).

IP101G has several major functions:

1. **PCS layer (Physical Coding Sub-Layer)**: This function contains transmit, receive and carrier sense functional circuitries.
2. **Management interface**: Media Independent Interface (MII) or Reduced Management Interface (RMII) registers contains information for communication with other MAC.
3. **Auto-Negotiation**: Communication conditions between 2 PHY transceivers. IP101G advertise its own ability and also detects corresponding operational mode from the other party, eventually both sides will come to an agreement for their optimized transmission mode.

5.1 Major Functional Block Description

The functional blocks diagram is referred to Figure 1:

a. 4B/5B encoder: 100 Base-X transmissions require converting 4-bit nibble data into 5-bit wide data code-word format. Transmitting data is packaged by J/K codes at the start of packet and by T/R codes at the end of packet in the 4B/5B block. When transmit error has occurred during a transmitting process, the H error code will be sent. The idle code is sent between two packets.

b. 4B/5B Decoder: The decoder performs the 5B/4B decoding from the received code-groups. The 5 bits (5B) data is decoded into four bits nibble data. The decoded 4 bit (4B) data is then forwarded through MII to the repeater, switch or MAC device. The SSD is then converted into 4B 5 nibbles and the ESD and IDLE Codes are replaced by 4B 0 nibbles data. The decoded data is driven onto the corresponding MII port or shared MII port. Receiving an invalid code group will cause PHY to assert the MII RXER signal.

c. Scrambler/Descrambler: Repetitive patterns exist in 4B/5B encoded data which result in large RF spectrum peaks and keep the system from being approved by regulatory agencies. The peak in the radiated signal is reduced significantly by scrambling the transmitted signal. Scrambler adds a random generator to the data signal output. The resulting signal is with fewer repetitive data patterns. The scrambled data stream is descrambled at the receiver by adding another random generator to the output. The receiver's random generator has the same function as the transmitter's random generator. Scrambler operation is dictated by the 100Base-TX and TP_FDDI standards.

d. NRZI/MLT-3(Manchester) Encoder and Decoder: 100Base-TX Transmission requires encoding the data into NRZ format and again converted into MLT-3 signal, while 10 Base-T will convert into Manchester form after NRZ coding. This helps to remove the high frequency noise generated by the twisted pair cables. At receiving end, the coding is reversed from MLT-3 (Manchester) signal back to NRZ format.

e. **Clock Recovery:** The receiver circuit recovers data from the input stream by regenerating clocking information embedded in the serial stream. The clock recovery block extracts the RXCLK from the transition of received

f. **DSP Engine:** This block includes Adaptive equalizer and Base Line Wander correction function.

5.1.1 Transmission Description

10Mbps Transmit flow path:

TXD ➔ Parallel to Serial ➔ NRZI/Manchester Encoder ➔ D/A & line driver ➔ TXO

After MAC passes data to PHY via 4 bits nibbles, the data are serialized in the parallel to serial converter. The converter outputs NRZI coded data which the data are then mapped to Manchester code within the Manchester Encoder. Before transmitting to the physical medium, the Manchester coded data are shaped by D/A converter to fit the physical medium.

10Mbps Receive:

RXI ➔ Squelch ➔ Clock Recovery ➔ Manchester/NRZ Decoder ➔ Serial to Parallel ➔ RXD

The squelch block determines valid data from both AC timing and DC amplitude measurement. When a valid data is present in the medium, squelch block will generate a signal to indicate the data has received. The data receive are coded in Manchester form, and are decoded in the Manchester to NRZ Decoder. Then the data are mapped to 4 bits nibbles and transmitted onto MAC interface.

100Mbps TX Transmit:

TXD ➔ 4B/5B Encoder ➔ Scrambler ➔ Mux ➔ Parallel to Serial ➔ NRZI/MLT-3 Encoder ➔ D/A & line driver ➔ TXO

The major differences between 10Mbps transmission and 100Mbps transmission are that 100Mbps transmission requires to be coded from 4-bit wide nibbles to 5 bits wide data coding, and after that the data are scrambled through scrambler to reduce the radiated energy generated by the 4B/5B conversion.
Then the data is converted into NRZI form and again from NRZI coded form into MLT-3 form. The MLT-3 data form is fed into D/A converter and shaped to fit the physical medium transmission.

100Mbps RX Receive:

RXI ➔ DSP ➔ MLT-3/NRZI Decoder ➔ Clock Recovery ➔ Serial to Parallel ➔ Descrambler ➔ 4B/5B Decoder ➔ RXD

The received data first go through DSP engines which includes adaptive equalizer and base-line wander correction mechanism. The adaptive equalizer will compensate the loss of signals during the transmission, while base-line wander monitors and corrects the equalization process. If a valid data is detected then the data are parallelized in Serial to Parallel block, which it converts NRZI coded data form back to scrambled data. The scrambled data are descrambled and converted back to 4 bits–wide format data and then feed into MAC.

5.1.2 MII and Management Control Interface

Media Independent Interface (MII) is described in clause 22 in the IEEE 802.3u standard. The main function of this interface is to provide a communication path between PHY and MAC/Repeater. It can operate either in 10Mbps or 100Mbps environment, and operate at 2.5MHz frequency for 10Mbps clock data rate or 25MHz frequency for 100Mbps data rate transmission. MII consists of 4 bit wide data path for both transmit and receive. The transmission pins consists of TXD[3:0], TX_EN and TXC, and at receiving MII pins have RXD[3:0], RXER, RX_DV and RXC. The Management control pins include MDC and MDIO. MDC, Management Data Clock, provides management data clock at maximum of 2.5MHz as a reference for MDIO, Management Data Input/Output. CRS, Carrier Sense, is used for signaling data transmission is in process while COL, Collision, is used for signaling the occurrence of collision during transmission.

Transmitting a packet, MAC will first assert TX_EN and convert the information into 4 bits wide data and then pass the data to IP101G. IP101G will sample the data according to TX_CLK until TX_EN is low.
While receiving a packet, IP101G asserts RX_DV high when data present in the medium through RXD[3:0] bus lines. IP101G samples received data according to RX_CLK until the medium is back to idle state.

The MDI transmitter of IP101G can enter low power idle (LPI) state via TX_ER, TXD[3:0] and TX_EN as the following behavior.

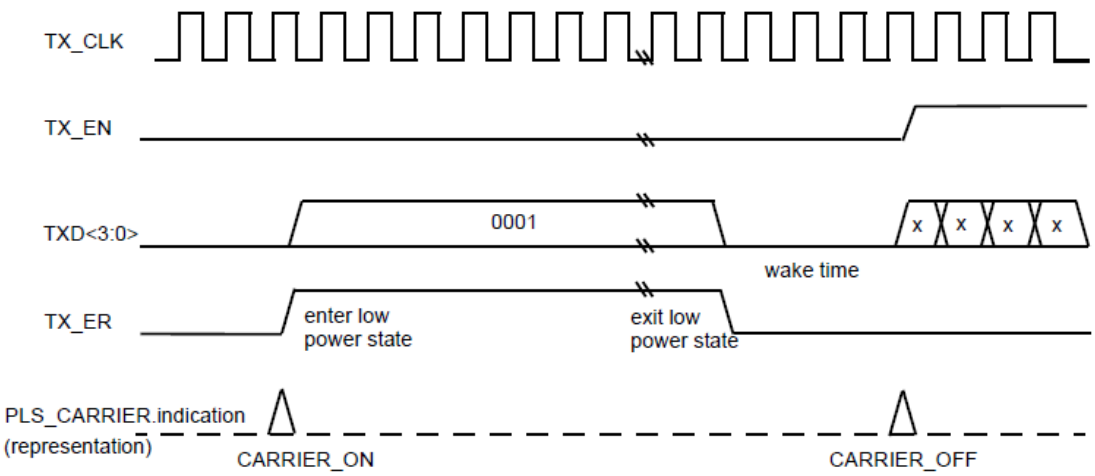


Figure 5 LPI transition

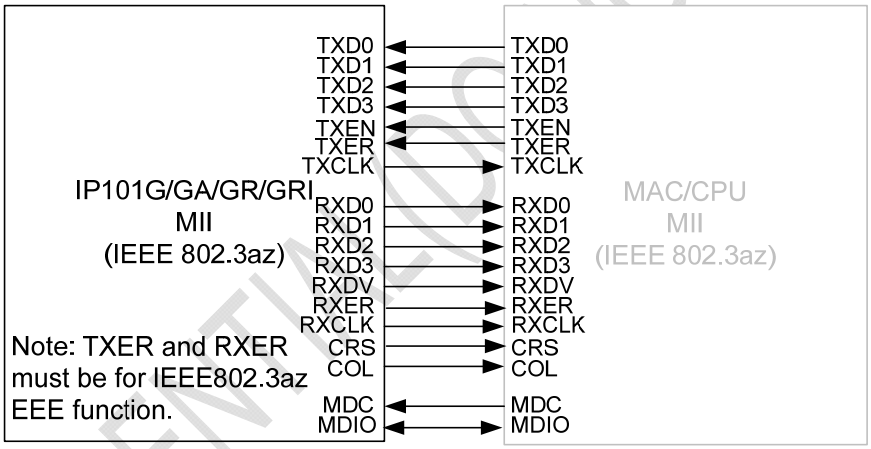


Figure 6 IP101G/GA/GR/GRI MII Mode with LPI transition Block Diagram

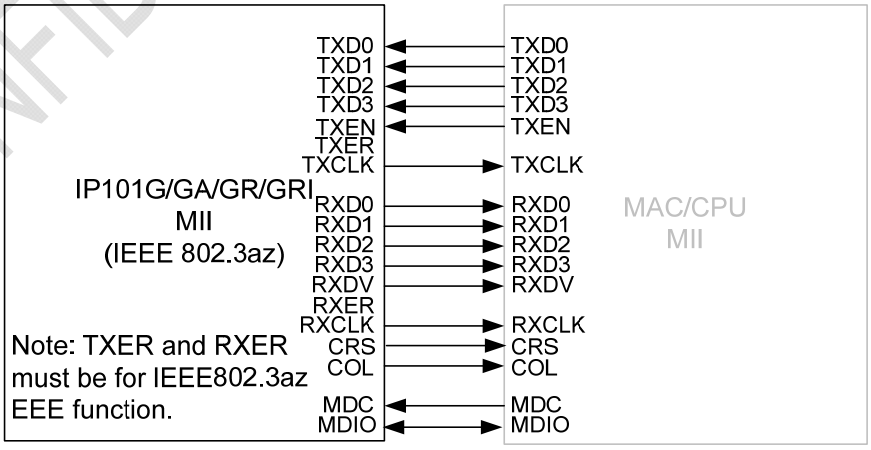


Figure 7 IP101G/GA/GR/GRI MII Mode without LPI transition Block Diagram

5.1.3 RMII Interface

Reduced Media Independent Interface (RMII) is defined to provide a fewer pins data transmission condition. The management interface, MDC and MDIO, are identical to the MII defined in IEEE 802.3. RMII supports 10/100Mb data rates and the clock source are provided by a single 50MHz clock from either external or within IP101G. This clock is used as reference for transmit, receive and control. RMII provides independent 2 bit wide transmit and receive data path, i.e., TXD[1:0] and RXD[1:0]. CRS_DV is asserted when the receive medium is not idle and de-asserted when the medium is idle.

Before any transmission occurs, CRS_DV should be de-asserted and value “00” should be present in both TXD[1:0] and RXD[1:0]. When transmission begins, IP101G will send “01” (TXD[1:0] = 01) for preamble to indicate SFD, and also assert TX_EN synchronous with first nibble of the preamble. TX_EN should be de-asserted until the end of the data transmission. At receiving mechanism, by receiving “01” means a valid data is available. If the False carrier is detected, RXD[1:0] shall be “10” until the end of the transmission. The MDI transmitter of IP101G can not enter low power idle (LPI) state, but can receive the LPI signal from MDI path.

At 10Mbps mode, every 10th cycle of REF_CLK will be sampled in RXD[1:0] and TXD[1:0], because the REF_CLK frequency is 10 times faster than the data rate of the 10Mbps.

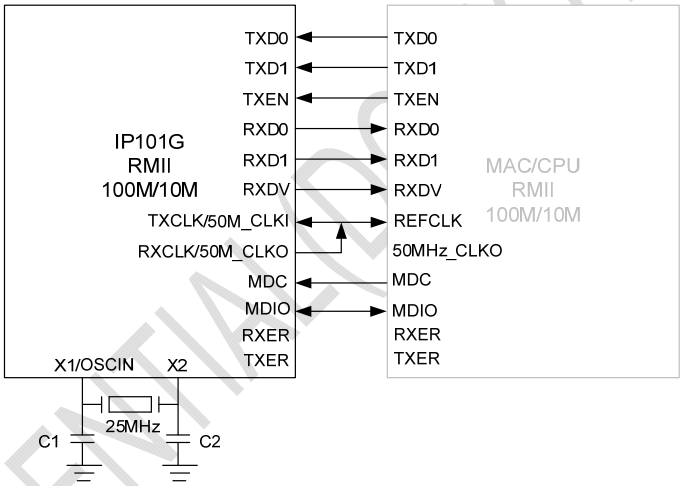


Figure 8 IP101G RMII Mode with internal clock Block Diagram

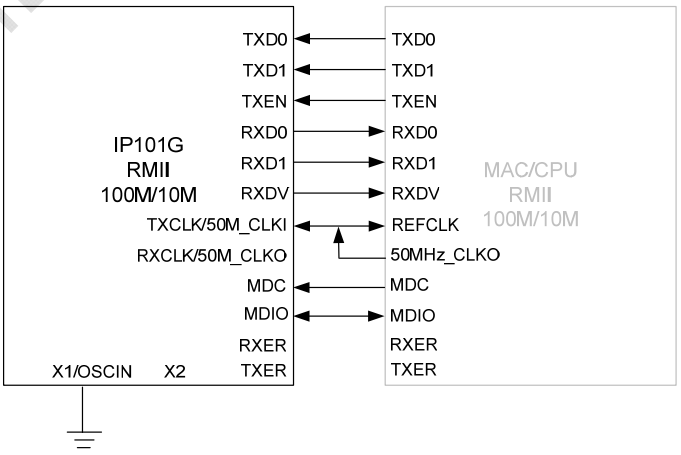


Figure 9 IP101G RMII Mode with external clock Block Diagram

5.1.4 Flexible Clock Source

While set COL/RMII pin to logic 1, 50MHz reference clock will be provided by IP101G in RMII mode. For this configuration, RMII reference clock output for IP101G is from RXCLK/50M_CLKO. Clock skew could be eliminated by adding an external buffer and placing equal trace lengths between buffer outputs and each chip.

The flexible clock source is list as the following table.

Table 3 Flexible Clock Source Setting

Pin name COL/RMII	Mode	Clock Source	Function
1	RMII	Crystal 25MHz	Provides a crystal 25MHz into pin X1 and X2.
		Clock 25MHz	Provides a clock source 25MHz into pin X1.
		Clock 50MHz	Provides a clock source 50MHz into pin TXCLK/50M_CLKI and connect pin X1 to GND or AGND33.
0	MII	Crystal 25MHz	Provides a crystal 25MHz into pin X1 and X2.
		Clock 25MHz	Provides a clock source 25MHz into pin X1.

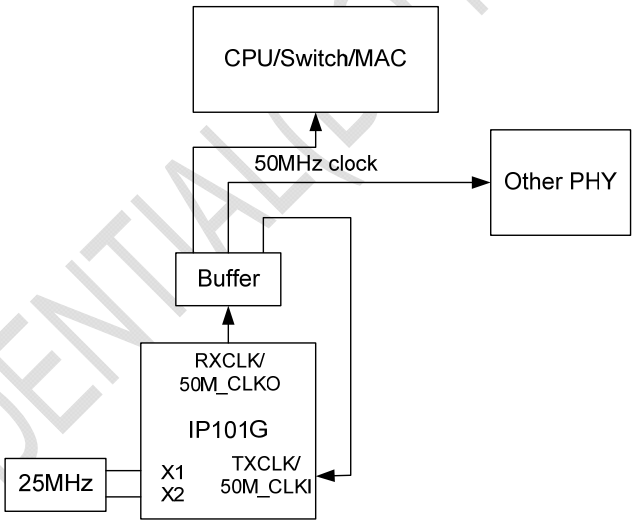


Figure 10 IP101G RMII Clock Application Circuit

5.1.5 Auto-Negotiation and Related Information

IP101G supports clause 28 in the IEEE 802.3u standard. IP101G can be operated either in 10Mbps/100Mbps or half/full duplex transmission mode. IP101G also supports flow control mechanism to prevent any collision in the network. If the other end does not support Auto-Negotiation function, IP101G will link at half duplex mode and enter parallel detection.

At beginning of auto-negotiation, IP101G will advertise its own ability by sending FLP waveform out to the other end and also listening signals from the other end. IP101G will place itself into correct connection speed depends on the received signals. If NLP signal is replied from the other end, IP101G will enter 10Mbps, while active idle pulses (unique 100Mbps pattern) IP101G will go to 100Mbps mode instead.

Once the negotiation has completed with the other party, IP101G will configure itself to the desired connection mode, i.e., 10/100Mbps or Half/Full duplex modes. If there is no detection of link pulses within 1200~1500ms, IP101G will enter Link Fail State and restart auto-negotiation procedure.

The auto-negotiation information is stored in the IP101G's MII registers. These registers can be modified and monitor the IP101G's Auto-Negotiation status. The reset auto-negotiation in register 0 of MII registers can be set at any time to restart auto-negotiation.

The flow control ability is also included in the IP101G chip. If MAC supports flow control condition, then flow control will be enabled by setting bit 10 (Pause) of the Register 4.

We can determine the link speed and EEE ability from IP101G's MII registers. There is an example as following figure.

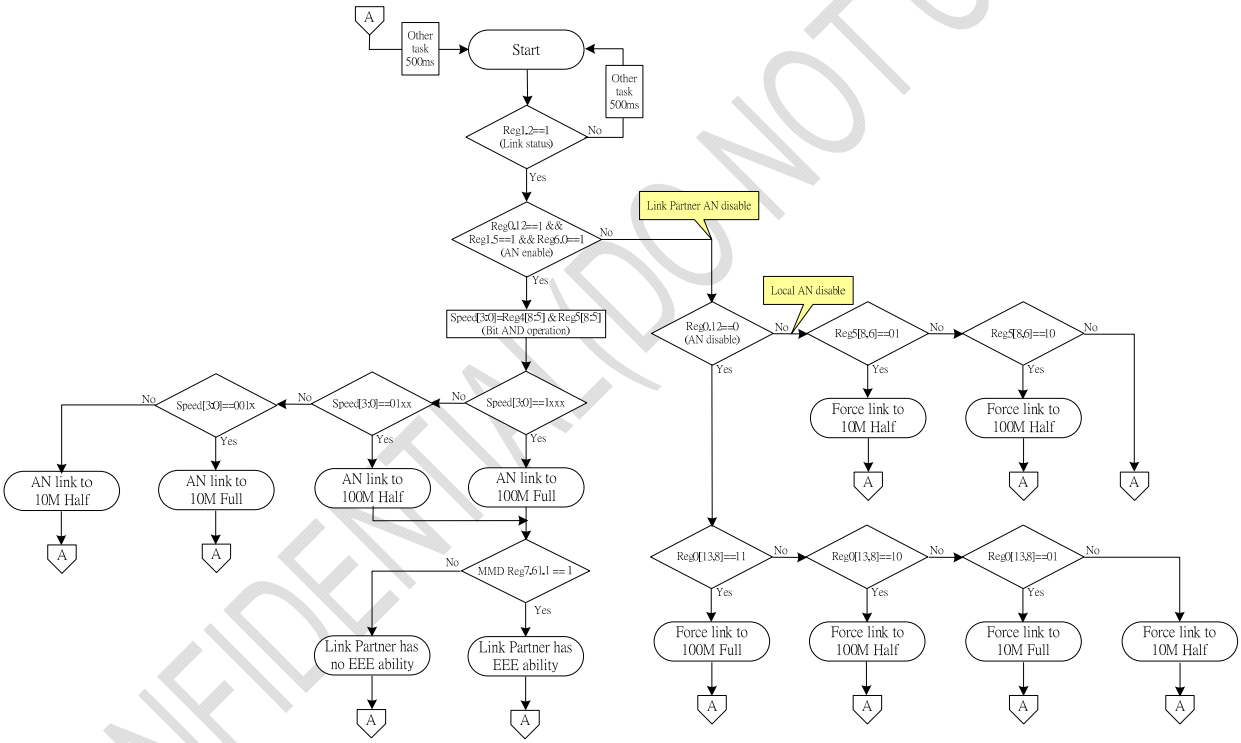


Figure 11 IP101G link speed and EEE ability programming guide

5.1.6 Auto-MDIX function

IP101G will keep sensing incoming signal in MDI RX pair, if no incoming signal is detected, IP101G will switch TX and RX pairs automatically trying to establish connection. IP101G supports this function both in Auto-Negotiation mode and force mode.

5.2 PHY Address Configuration

IP101GR/IP101GRI PHY Address can be configured to 5'd0, 5'd1 or response any one PHY address from 5'd2 to 5'd31. IP101G/IP101GA PHY Address can be configured to 5'd0, 5'd1,…, 5'd7 or response any one PHY address from 5'd8 to 5'd31. This PHY Address configuration is the following table.

Table 4 PHY Address Configuration

Package	Pin name				PHY Address setting
	LED3/PHY_AD3	LED2/PHY_AD2	LED1/PHY_AD1	LED0/PHY_AD0	
32 pin	0	X	X	0	5'd0
	X	X	X	1	5'd1
	1	X	X	0	5'd2 ~ 5'd31
48 pin	0	0	0	0	5'd0
	X	0	0	1	5'd1
	X	0	1	0	5'd2
	X	0	1	1	5'd3
	X	1	0	0	5'd4
	X	1	0	1	5'd5
	X	1	1	0	5'd6
	X	1	1	1	5'd7
	1	0	0	0	5'd8 ~ 5'd31

Note: "X" indicate don't care (either 1 or 0). Do not let these PHY address pins floating for the latched-in settings after the power is ready.

LED pins also include the information of PHY address. The PHY address can be modified by changing the LED circuitry. The modification can be arranged as follows.

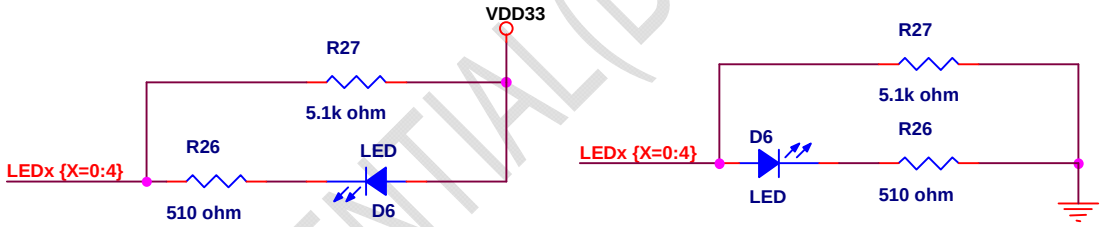


Figure 12 PHY Address Configuration

The left diagram will enable the specific PHY address to 1, if it is connected to VDD33. The diagram on the right shows the configuration for setting PHY address to 0, when the circuit is connected to ground. By setting either one of the bits according to the diagram will allow one to modify PHY addresses from PHY_AD0 to PHY_AD3.

5.3 Power Management Tool

IP101G provides rich power management tool to save the power consumption. They are

- APS, auto power saving while Link-off
- 802.3az, protocol based power saving
- PWD, force power down
- WOL+, light traffic power saving

5.3.1 Auto Power Saving Mode

APS mode in bit 1 of Register 16: Set high to this bit will set PHY into power saving mode (APS sleeping mode) while link is down, MDC and MDIO are kept activated. IP101G will send NLP every 256ms or (256*N)ms during APS sleeping mode, and the symbol N is an integer such as 2,3,4… random seed for power saving.

5.3.2 IEEE802.3az EEE (Energy Efficient Ethernet)

In order to enter this mode, the PHY part should declare the EEE capability during the auto-negotiation phase, and then send a LLDP to the link partner to indicate the wakeup time.

If both ends of the cable support EEE, IP101G can enter Low Power Idle mode per the request from the higher layer (such as the command from CPU or MAC layer). There are 2 methods to activate Low Power Idle Mode: the MII/RMII bus coming from MAC layer and the MII register control coming from MDC/MDIO serial bus.

For legacy Ethernet MAC, the MII/RMII does not provide any command regarding EEE. When used in conjunction with these MACs, IP101G provides a MII register that allows the designer to activate the Low Power Idle mode.

It's the higher layer's responsibility to memorize the link partner's wakeup time and wakeup the link partner before sending data. The higher layer means a mechanism that can evaluate the packet buffer utilization and wake the link partner before sending the data. In general speaking, this mechanism probably consists of at least one of the following items: the packet buffer manager, the application program and OS.

The EEE module works well at LPI (Low Power Idle) mode when

1. Link at full-duplex and
2. Auto-negotiation is enabled in both local and remote PHYs and
3. 100Mbps and
4. EEE ability is supported in both local & remote PHYs and
5. EEE_EN (MMD register 7.60[1]) is enabled for EEE function via default value.

In general applications, the energy-saving mechanism is activated by the real-time OS or the higher layer hardware. When the OS or higher layer hardware knows that it's the time to force the unused function to enter standby mode or sleeping mode, it can force the MAC to send IEEE 802.3az compliant command to set IP101G to "low power idle" mode. Once entering the "low power idle" mode, IP101G will stay at a low power consumption level without losing the link capability. After awaken, it can generate a INTR signal, hardware pin from IP101G, to notify the CPU or external circuitry.

IP101G supports not only EEE ability at 100Mbps but also smaller transmit amplitude requirement at 10Mbps. That complies with 10Base-T PHY interoperability over 100 meters of Category 5 or better cable types.

5.3.3 Force power down

IP101G can be power-down by 2 methods. These 2 methods are as follows.

Power Down in bit 11 of Register 0: Enable this bit will disconnect the power to IP101G and also internal clock, but MDC and MDIO are still activated.

Analog off in bit 0 of Register 16: Enable this bit will put IP101G in analog off state. This will power down all analog functions but internal 25MHz operating clock is active, and MDC and MDIO are also activated.

5.3.4 WOL+ operation mode

The huge amount of legacy Ethernet devices will make an Ethernet device which supports 802.3az lost his energy saving capability, because they can not talk to each other for settling down the idle schedule. IP101G to be a full-range-green Ethernet PHY, not only consumes very low power and with 802.3az capability, but also supports a WOL+ function for solving this issue.

IP101G supports WOL+ either master mode or slave mode. In master mode, the WOL+ function will be active if all ports are in idle state has been continuously held for a period time. This period time can be configured by WOL+ timer register (Page4 Reg16[7:6]).

In slave mode, a WOL+ interrupt will take place if no any frame for a period time and the WOL+ function only be asserted by CPU through SMI interface to write WOL+ control register (Page4 Reg16[5]).

Table 5 WOL+ operation mode

Register Page17			Description
Sleeping (Reg17.2)	Sleep (Reg17.1)	Wake (Reg17.0)	
0	0	0	IP101G is in normal mode.
0	x	1	IP101G has been changed to normal mode.
0	1	0	IP101G is in normal mode and it's ready for sleeping in WOL+ slave mode. CPU may set Page4 Reg16[5] as 1 to force sleep.
1	x	0	IP101G is in WOL+ sleep mode.
1	0	1	IP101G is in WOL+ sleep mode and it's ready for wake up in WOL+ slave mode. CPU may set Page4 Reg16[5] as 1 to force wake up.
1	1	1	IP101G is in WOL+ sleep mode.

Once IP101G enters to power-saving mode (speed down to 10Mbps when sleep), it shall wake up if

a) Disable WOL+ function (Page4 Reg16.15);
b) Sense magic packet;
c) Sense link change;
d) Sense any packet;

The packet format of Magic packet is showing as follows, source address=0x112233445566 for example, repeat this source address 16 times at least.

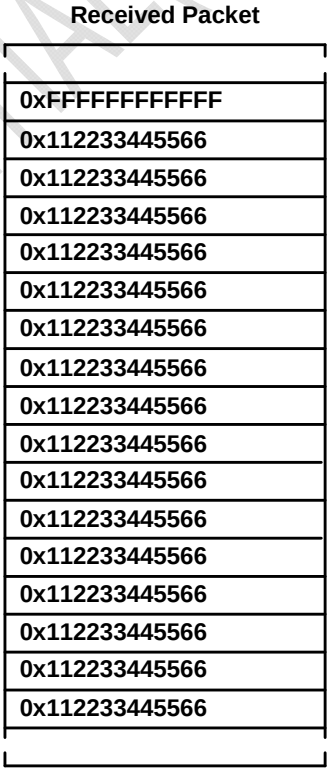


Figure 13 Magic Packet Format

IP101G can sleep or wake up automatically in WOL+ master mode. There is an example as the following figure. Setting to wake up by any packets or the link status changed, and use an active-high INTR (interrupt) to notify the MAC when sense any WOL+ events.

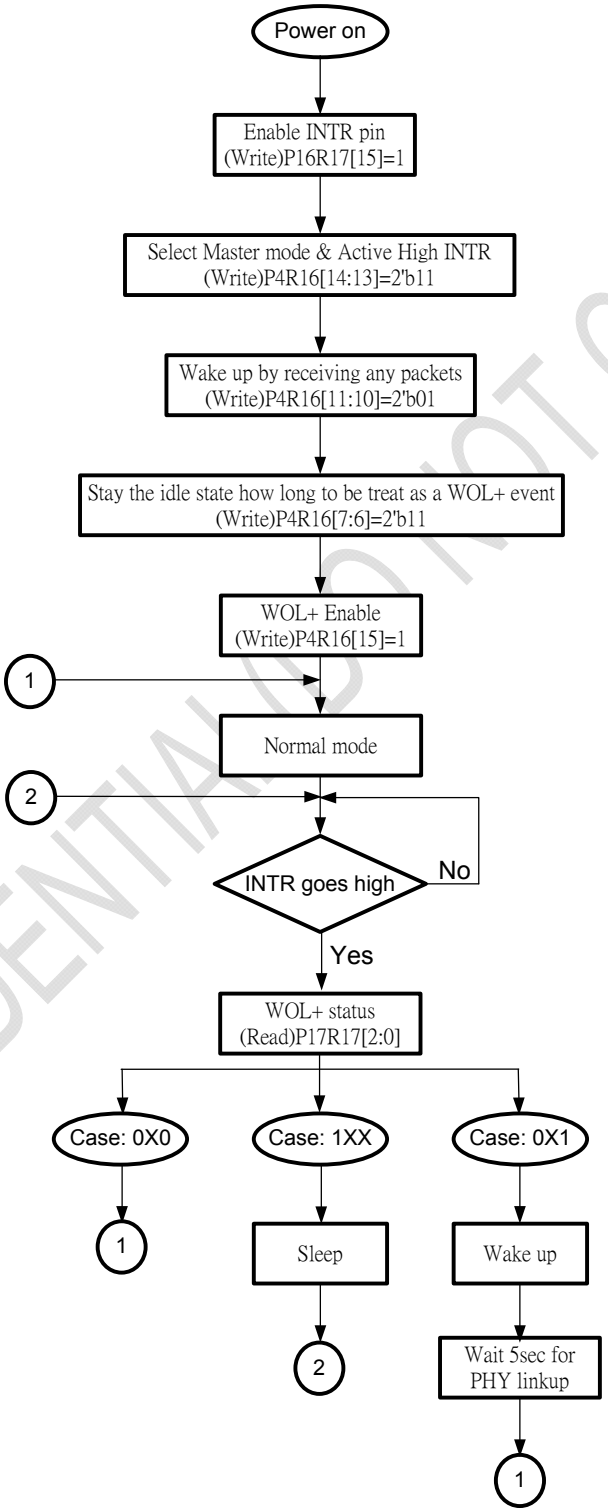


Figure 14 Sleep or wake up automatically programming guide

IP101G can sleep or wake up by MAC manual set in WOL+ slave mode. There is an example as the following figure. Setting to wake up by magic packets or the link status changed, and use an active-low INTR (interrupt) to notify the MAC when sense any WOL+ events.

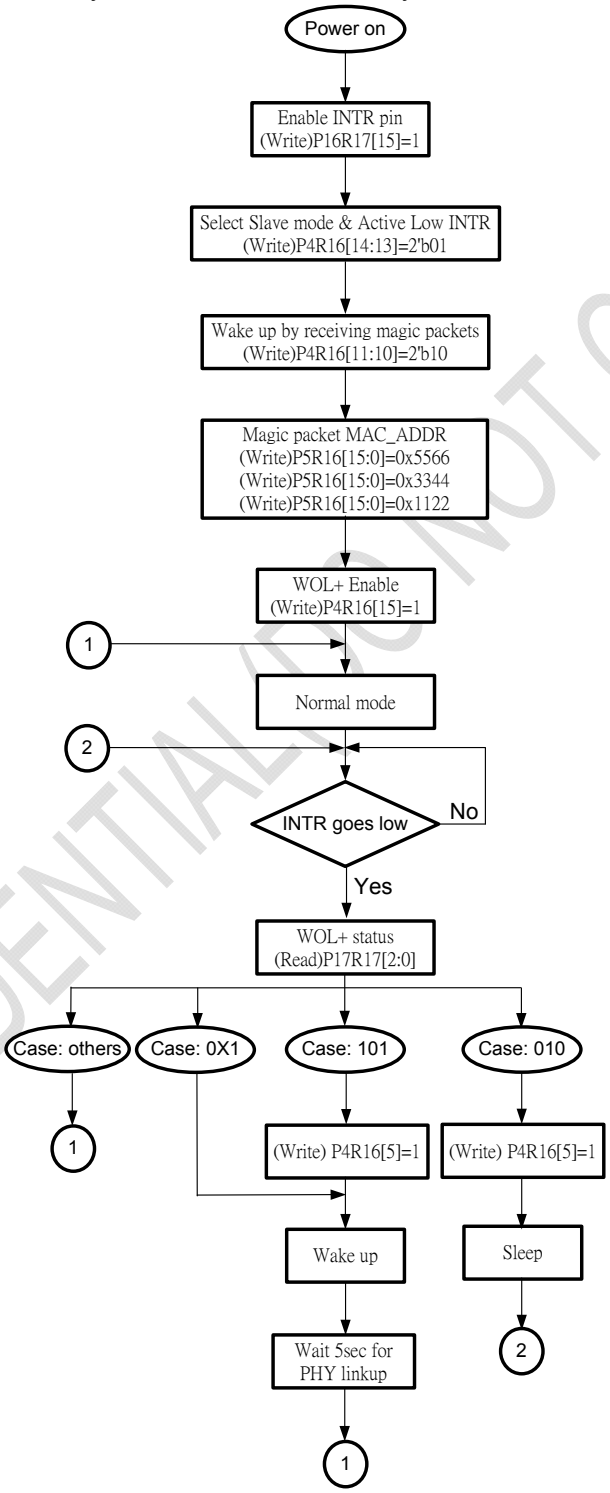


Figure 15 MAC control sleep or wake up programming guide

5.4 LED Mode Configuration

IP101G provides 2 LED operation modes,

LED Mode 1 (default):

Table 6 LED Mode 1 Function

LED	Function
LED0	Link status: Active indicates the link has established
LED1	Duplex operation: Active indicates full duplex
LED2	10BT/ACT: Active indicates 10Mbps connection has established, and blinking while TX/RX events occur.
LED3	100BT/ACT: Active indicates 100Mbps connection has established, and blinking while TX/RX events occur.

LED Mode 2 (could be set by pulling up pin CRS/LEDMOD with a 4.7K resistor):

Table 7 LED Mode 2 Function

LED	Function
LED0	Link/ACT: Active indicates the link has established, and blinking while TX/RX events occur.
LED1	Duplex/COL: Active indicates full duplex, and blinking while collision events occur.
LED2	10BT: Active indicates 10Mbps connection has established
LED3	100BT: Active indicates 100Mbps connection has established

5.5 LED Blink Timing

Table 8 LED Blink Timing

LED mode	Blinking speed
Active LED blink	On 26ms -> Off 78ms -> On 26ms -> Off 78ms …
Collision LED blink	On 26ms -> Off 78ms -> On 26ms -> Off 78ms …

5.6 Repeater Mode

To enter Repeater mode, one can set 1 to bit 2 of Register 16 will allow IP101G to enter Repeater mode. If IP101G is used in repeater, CRS will be high if IP101G is in a process of receiving packets. While IP101G is used in a network interface card, CRS will be generated in both transmitting and receiving packets.

5.7 Interrupt

IP101G provides 4 kinds of interrupt function: speed change, duplex change, link change and arbiter state change. Interrupt masks could be selected by Reg 17, and an active low interrupt will be sent from INTR or INTR_32 pin when event occurs.

5.8 Miscellaneous

ISET pin should be connected to GND via a 6.19K ohm resistor with 1% accuracy to ensure a correct driving current for transmit DAC.

Set low to RESET_N pin, for at least 10ms will reset all functions available in IP101G. The bit 15 of Register 0 will put PHY into its default status.

5.9 Serial Management Interface

IP101G supports one serial management interface (SMI). User can access IP101G's MII registers through MDC and MDIO. Its format is shown in the following table. To access MII register in IP101G, MDC should be at least one more cycle than MDIO. That is, a complete command consists of 32 bits MDIO data and at least 33 MDC clocks. When the SMI is idle, MDIO is in high impedance.

Table 9 SMI Format

Frame format	<Idle><start><op code><PHY address><Registers address><turnaround><data><idle>
Read Operation	<Idle><01><10><$A_4A_3A_2A_1A_0$><$R_4R_3R_2R_1R_0$><Z0><b_{15} b_{14} b_{13} b_{12} b_{11} b_{10} b_9 b_8 b_7 b_6 b_5 b_4 b_3 b_2 b_1b_0><Idle>
Write Operation	<Idle><01><01><$A_4A_3A_2A_1A_0$><$R_4R_3R_2R_1R_0$><10><b_{15} b_{14} b_{13} b_{12} b_{11} b_{10} b_9 b_8 b_7 b_6 b_5 b_4 b_3 b_2 b_1b_0><Idle>

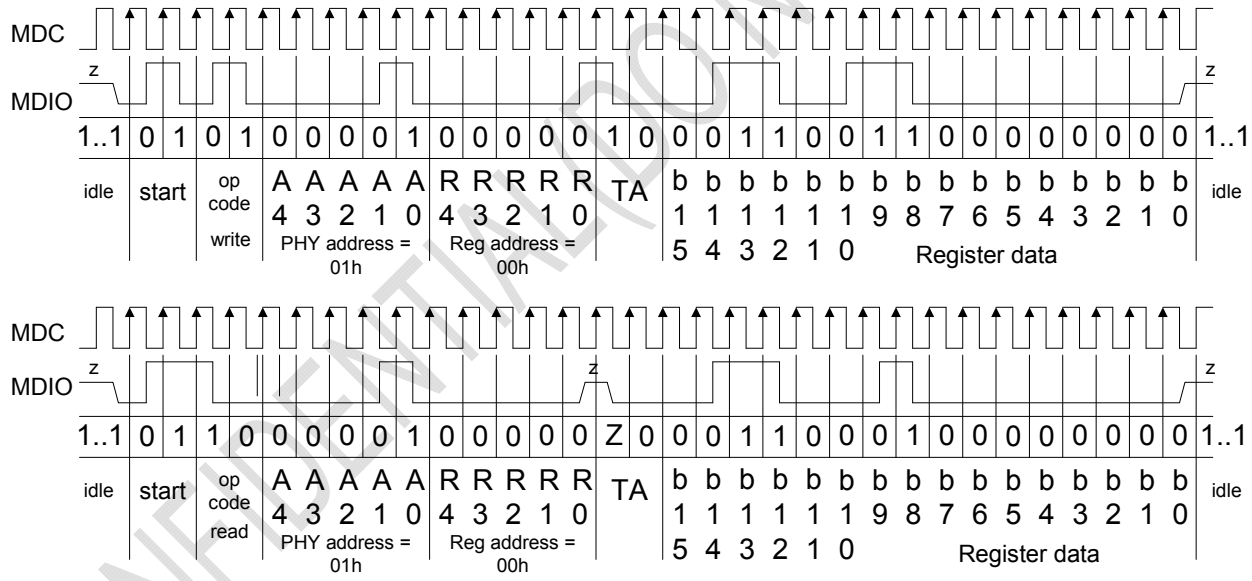


Figure 16 MDC/MDIO Format

5.10 Fiber Mode Setting

IP101G supports either TP mode or Fiber mode. User should pull high voltage on pin RXDV/CRS_DV/FX_HEN of IP101G when reset signal is completed for Fiber mode operation. Fiber MAU provides high voltage to pin TXER/FXSD of IP101G when Fiber MAU is active to transmit or receive packet frames.

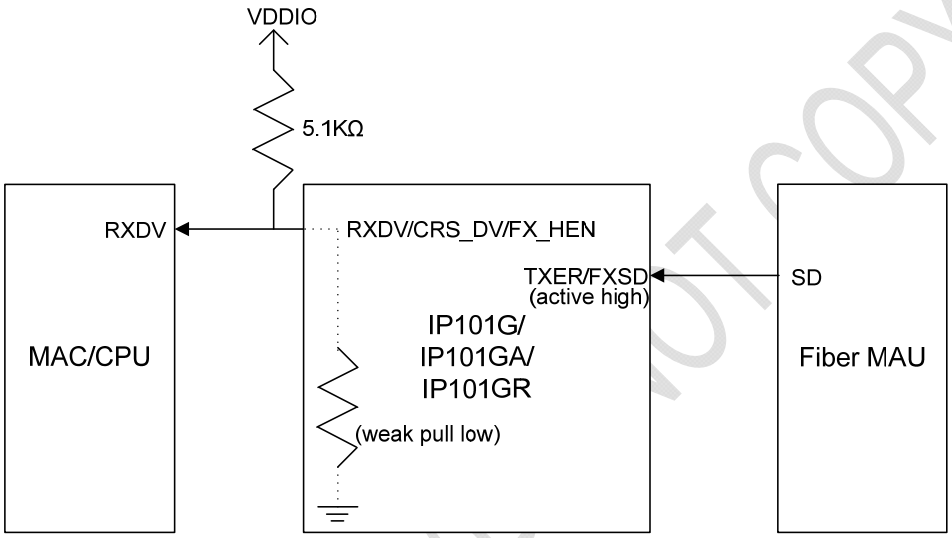


Figure 17 IP101G Fiber Mode Setting

5.11 Jumbo Frame

IP101G supports jumbo frame size up to 12K Bytes in MII mode. In the other mode RMII, IP101G supports jumbo frame size up to 10K Bytes that is auto-negotiation at 100Mbps full duplex.

6 Layout Guideline

6.1 General Layout Guideline

Best performance depends on a good PCB layout. The following recommendation steps will help customer to gain maximum performance.

- Create a good power source to minimize noise from switching power source.
- All components are qualified, especially high noise component, such as clock component.
- Use bulk capacitors between power plane and ground plane for 4 layers board, signals trace on component and bottom side, power plane on third layer, and ground layer on second layer.
- Use decoupling capacitors to decouple high frequency noise between chip's power and ground, must be as close as possible to IP101G.
- The clock trace length to IP101G must be equal the clock trace length to MAC.
- Use guard traces to protect clock traces if possible.
- Avoid signals path parallel to clock signals path, because clock signals will interference with other parallel signals, degrading signal quality, such as MDC and X1 signals.
- The clock must be low jitter for 25/50/125MHz PLL requirement with less than the 500ps Peak-to-Peak, or 83ps RMS for normal distribution.
- Avoid highly speed signal across ground gap to prevent large EMI effect.
- Keep ground region as one continuous and unbroken plane.
- Place a gap between the system and chassis grounds.
- No any ground loop exists on the chassis ground.

6.2 Twisted Pair recommendation

When routing the MDI_TP/MDI_TN signal traces from IP101G to transformer, the traces should be as short as possible, the termination resistors should be as close as possible to the output of the MDI_TP/MDI_TN pair of IP101G. Center tap of primary winding of these transformers must be connected to decoupling capacitors respectively. It is recommended that MDI_RP/MDI_RN trace pair be route such that the space between it and others is three times space, which can separate individual traces from one another.

It is recommended that offers chassis ground in the area between transformer and media connector (RJ-45 port), this isolates the analog signals from external noise sources and reduces EMI effect. Note the usage of the vias, it is best not use via to place anywhere other than in close proximity to device, in order to minimize impedance variations in a given signal trace.

7 Electrical Characteristics

7.1 Absolute Maximum Rating

Stresses exceed those values listed under Absolute Maximum Ratings may cause permanent damage to the device. Functional performance and device reliability are not guaranteed under these conditions. All voltages are specified with respect to GND.

Supply Voltage…….....	-0.3V to 3.63V
Input Voltage……...	-0.3V to 3.63V
Output Voltage……	-0.3V to 3.63V
Storage Temperature……	-65°C to 150°C
Ambient Operating Temperature (Ta) for IP101G/GR/GA……	0°C to 70°C
Ambient Operating Temperature (Ta) for IP101GRI……..	-40°C to 85°C
IC Junction Temperature (Tj)……	0°C to 125°C
IEC 61000-4-2 Contact Discharge ESD Reliability…….	±12KV
IEC 61000-4-2 Air Discharge ESD Reliability……..	±15KV

7.2 DC Characteristics

Table 10 DC Characteristics

Symbol	Specific Name	Minimum	Typical	Maximum	Condition
REGOUT	Linear regulator output voltage	1.07V	1.10V	1.18V	
DVDD_REGIN	Digital core supply voltage	1.07V	1.10V	1.18V	
VDDIO	I/O pad supply voltage for LED, RESETB and MII/RMII	3.135V	3.30V	3.465V	MAC uses 3.3V I/O supply voltage.
		2.375V	2.50V	2.625V	MAC uses 2.5V I/O supply voltage. Both MAC and IP101G sides use the same I/O supply voltage for MII/RMII. IP101GRI only supports 3.3V I/O.
AVDD33	Analog core supply voltage	3.135V	3.30V	3.465V	

Table 11 I/O Electrical Characteristics

Symbol	Specific Name	Minimum	Typical	Maximum	Condition
V_{IH}	Input High Voltage	0.8*VDDIO		3.3V +0.5V	
V_{IL}	Input Low Voltage	-0.5V		0.2*VDDIO	
V_{OH}	Output High Voltage	0.9* VDDIO		VDDIO	
V_{OL}	Output Low Voltage			0.1*VDDIO	
V_{IH}	X1 Input High Voltage	0.8* AVDD33		AVDD33 +0.5V	
V_{IL}	X1 Input Low Voltage	-0.5V		0.2*AVDD33	
V_{RST}	RESETB Threshold Voltage	0.4* VDDIO		0.6*VDDIO	
V_{FRC}	Fiber Rx common mode Voltage		1.8V		
V_{FRD}	Fiber Rx differential mode Voltage	0.4V			
V_{FXSD}	Fiber signal detect on when plug	2.0V	2.2V	3.3V +0.5V	
V_{FXSD}	Fiber signal detect on when unplug	1.3V		1.7V	
t_{jitter}	Jitter on TXOP, TXOM			800ps	

Symbol	Specific Name	Minimum	Typical	Maximum	Condition
t_r / t_f	Rise time & Fall time on TXOP, TXOM			6ns	

Table 12 Pin Latched-in Configuration Resistor

I/O Voltage	Pull-up/ Pull-down Resistor	Condition
VDDIO	5.1KΩ	

7.3 Crystal Specifications

Table 13 Crystal Specifications

Item	Parameter	Range
1	Nominal Frequency	25.000 MHz
2	Oscillation Mode	Fundamental Mode
3	Frequency Tolerance at 25℃	+/- 50 ppm
4	Temperature Characteristics	+/- 50 ppm
5	Operating Temperature Range	-10℃ ~ +70℃
6	Load Capacitance	20 pF, or Specify
7	Shunt Capacitance	7 pF Max
8	Insulation Resistance	Mega ohm Min./DC 100V
9	Aging Rate A Year	+/- 5 ppm/year

7.4 AC Timing

7.4.1 Reset, Pin Latched-in, Clock and Power Source

Table 14 Reset, Pin Latched-in, Clock and Power Source Timing Requirements

Symbol	Description	Min.	Typ.	Max.	Unit
T_{clk_lead}	X1 input clock valid period before reset released	10	-	-	ms
T_{rst}	Reset period	10	-	-	ms
$T_{clk\_MII\_rdy}$	MII/RMII clock output ready after reset released (Pins settings are latched into IP101G this moment.)	10	-	-	ms
T_{diff}	Time difference between AVDD33 and VDDIO, DVDD_REGIN			30	ms
T_{pwr_lead}	All power source ready before reset released	11			ms
T_{lat_s}	Latched-in pin signal setup time	10	-	-	µs
T_{lat_h}	Latched-in pin signal hold time	2.63	-	-	ms

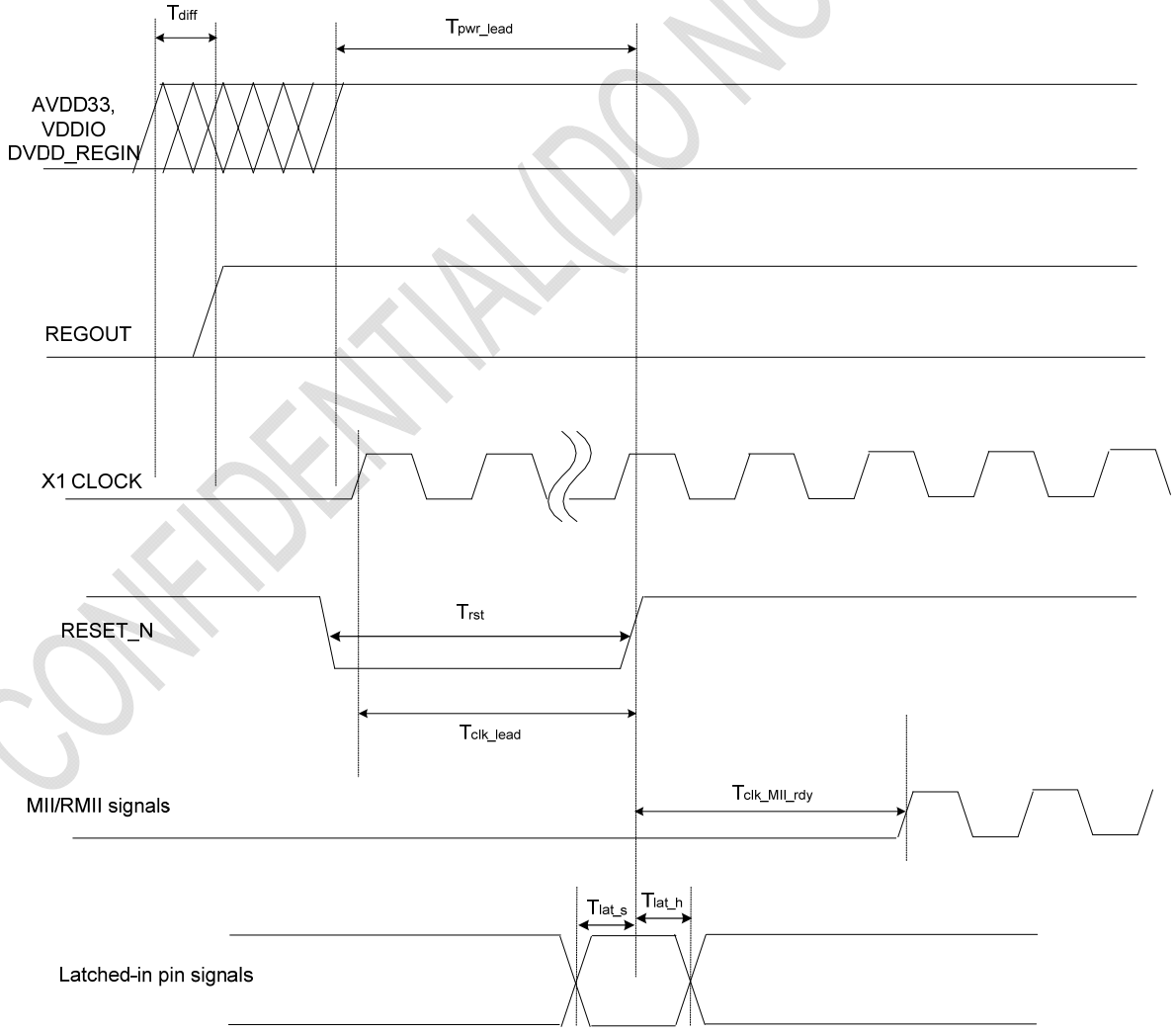


Figure 18 Reset, Pin Latched-In, Clock and Power Source Timing Requirements

7.4.2 MII Timing

a. Transmit Timing Requirements

Table 15 MII Transmit Timing Requirements

Symbol	Description	Min.	Typ.	Max.	Unit
T_{Tclk1}	Period of transmit clock in 100M mode	-	40	-	ns
T_{Tclk1}	Period of transmit clock in 10M mode	-	400	-	ns
T_{s1}	TXEN, TXD to TX_CLK setup time	10			ns
T_{h1}	TXEN, TXD to TX_CLK hold time	0			ns

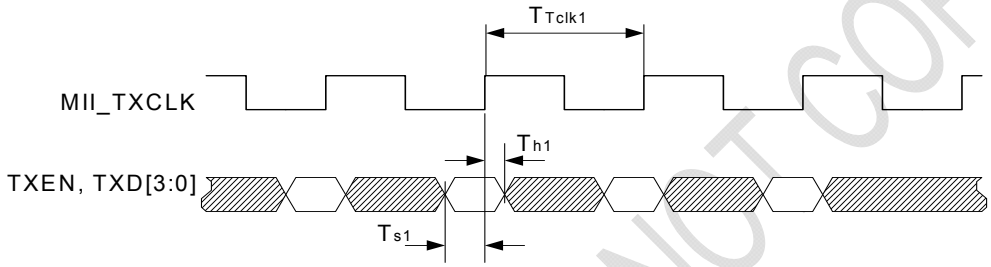


Figure 19 MII Transmit Timing Requirements

b. Receive Timing

Table 16 MII Receive Timing Specifications

Symbol	Description	Min.	Typ.	Max.	Unit
T_{Rclk1}	Period of receive clock in 100M mode	-	40	-	ns
T_{Rclk1}	Period of receive clock in 10M mode	-	400	-	ns
T_{d1} 100Mbps	MII_RXCLK rising edge to RXDV, RXD	-	22	26	ns
T_{d1} 10Mbps		-	202	206	ns
T_{d1} 100Mbps	MII_RXCLK falling edge to RXDV, RXD	-	2	6	ns
T_{d1} 10Mbps		-	2	6	ns

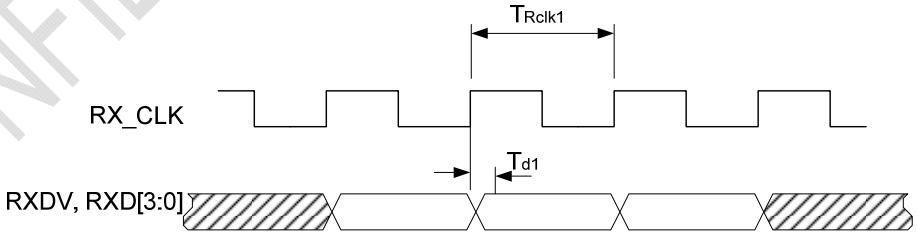


Figure 20 MII Receive Timing Specifications

7.4.3 RMII Timing

a. Transmit Timing Requirements

Table 17 RMII Transmit Timing Requirements

Symbol	Description	Min.	Typ.	Max.	Unit
$T_{RMII\_CLK\_IN}$	Period of RMII clock input	-	20	-	ns
T_s	TXEN, TXD to RMII_CLK_IN setup time	4			ns
T_h	TXEN, TXD to RMII_CLK_IN hold time	2			ns

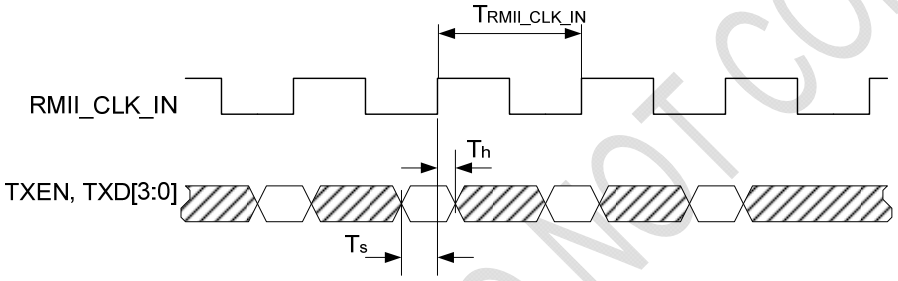


Figure 21 RMII Transmit Timing Requirements

b. Receive Timing

Table 18 RMII Receive Timing Specifications

Symbol	Description	Min.	Typ.	Max.	Unit
$T_{RMII\_CLK\_IN}$	Period of RMII clock input	-	20	-	ns
T_d	RMII_CLK_IN rising edge to RXDV, RXD	-	10	12	ns

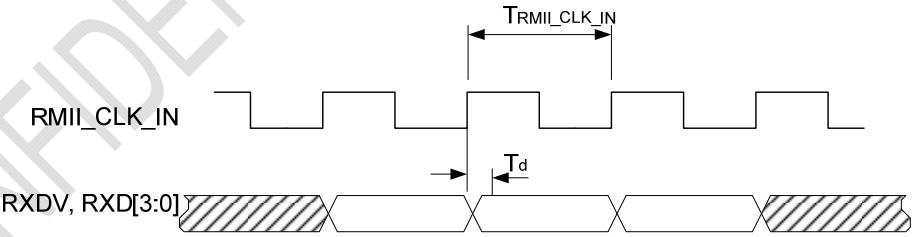


Figure 22 RMII Receive Timing Specifications

7.4.4 SMI Timing

MDC/MDIO Timing Requirements

Table 19 SMI Timing Requirements

Symbol	Description	Min.	Typ.	Max.	Unit
T_{ch}	MDC High Time	200	-	-	ns
T_{cl}	MDC Low Time	200	-	-	ns
T_{cm}	MDC period	400	-	-	ns
T_{md}	MDIO output delay	-	-	15	ns
T_{mh}	MDIO setup time	10	-	-	ns
T_{ms}	MDIO hold time	10	-	-	ns

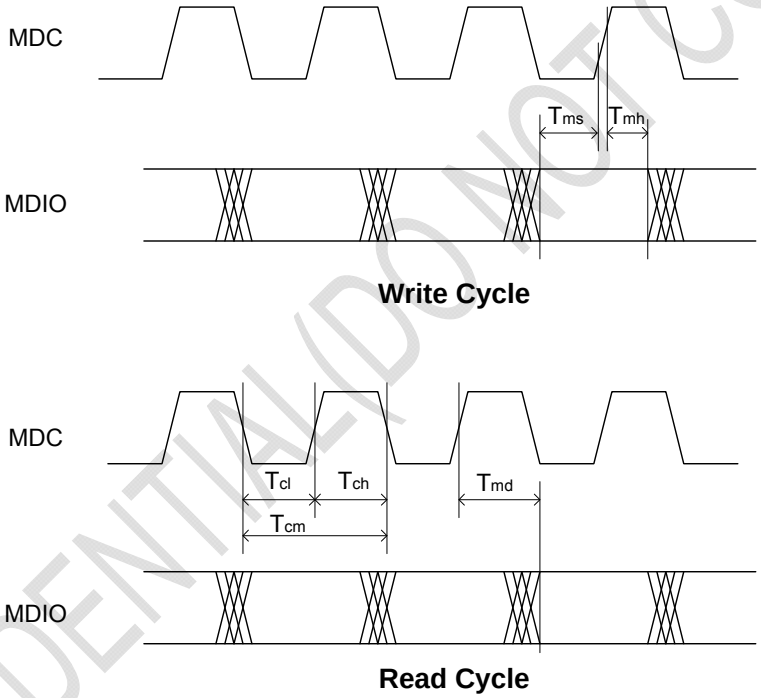


Figure 23 SMI Timing Requirements

7.5 Thermal Data

Table 20 Thermal Data

Theta Ja	Theta Jc	Conditions	Units
TBD	--	2 Layer PCB	°C/W

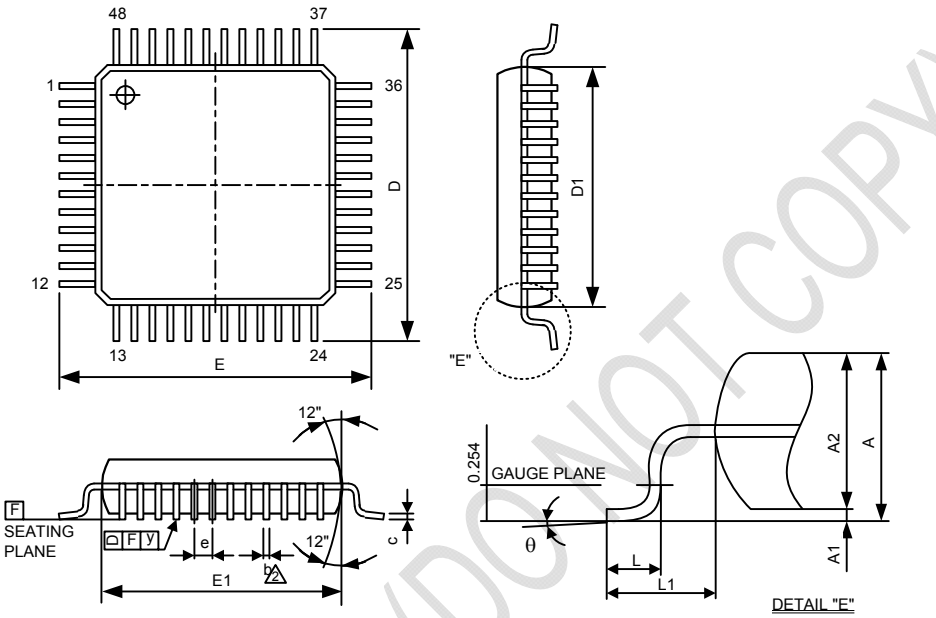
8 Order Information

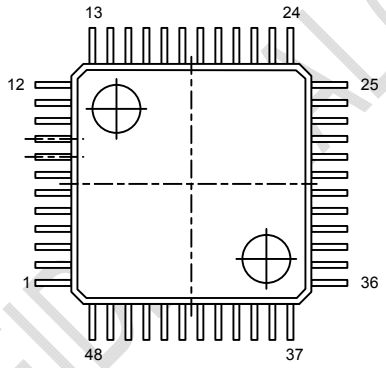
Table 21 Part Number and Package

Part No.	Package	Notice
IP101G	IP101G dice	
IP101GA	48-PIN LQFP	
IP101GR	32-PIN QFN	
IP101GRI	32-PIN QFN	

9 Physical Dimensions

9.1 48-PIN LQFP



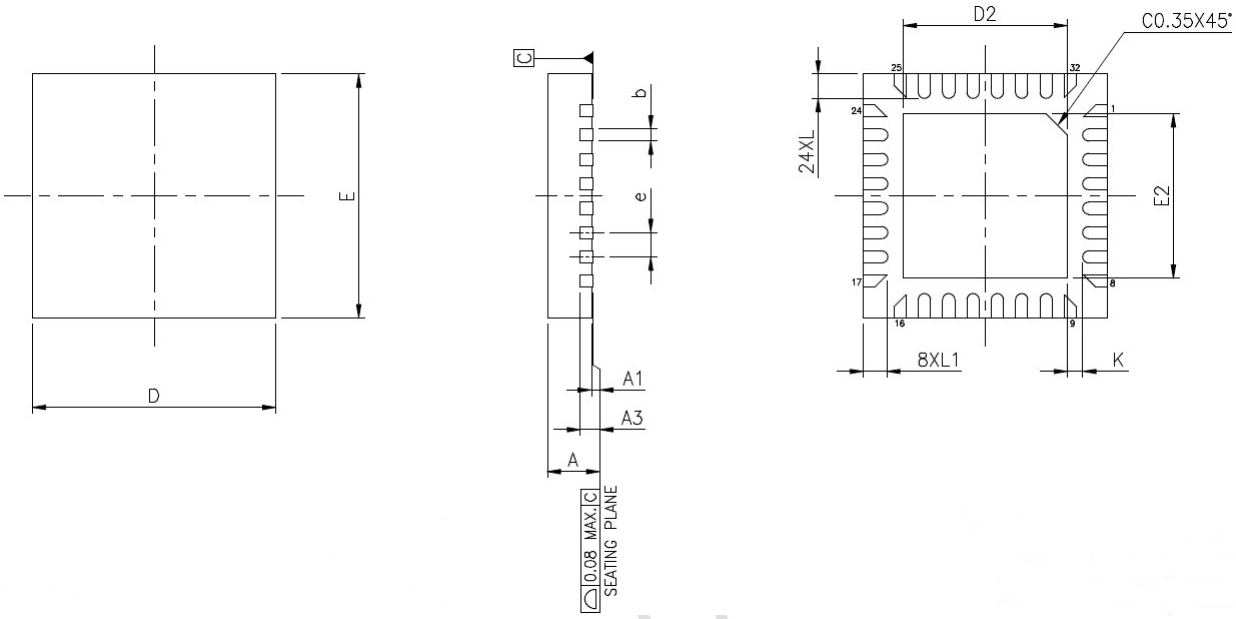


Symbols \ Unit	mm	inch
A	1.600MAX.	0.0630MAX.
A1	0.050~0.150	0.0020~0.0059
A2	1.400 ± 0.05	0.0551 ± 0.0020
b	0.200TYP	0.0078TYP
c	0.127TYP	0.0050TYP
D1	7.000 ± 0.100	0.2756 ± 0.0039
E1	7.000 ± 0.100	0.2756 ± 0.0039
e	0.500TYP	0.0196TYP
D	9.000 ± 0.250	0.3543 ± 0.0098
E	9.000 ± 0.250	0.3543 ± 0.0098
L	0.600 ± 0.150	0.0236 ± 0.006
L1	1.000REF	0.0393REF
y	0.100MAX.	0.0039MAX.
θ	0"~7"	0"~7"

Notes:
1. DIMENSION D1 & E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSION.
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.
3. MAX. END FLASH IS 0.15mm.
4. MAX. DAMBAR PROTRUSION IS 0.13mm.
GENERAL APPEARANCE SPEC SHOULD BE BASED ON FINAL VISUAL INSPECTION SPEC.

Figure 24 48-PIN LQFP Dimension

9.2 32-PIN QFN



JEDEC OUTLINE	PACKAGE TYPE		
SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.20 REF.	
b	0.15	0.20	0.25
D		4.00 RSC	
E		4.00 BSC	
e		0.40 BSC	
L	0.35	0.40	0.45
L1	0.332	0.382	0.432
K	0.20	--	--

	E2			D2			LEAD FINISH		JEDEC CODE
PAD SIZE	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
114X114 MIL	2.60	2.70	2.75	2.60	2.70	2.75	V	X	N/A

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO MATALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

Figure 25 32-PIN QFN Dimension

IC Plus Corp.

Headquarters
10F, No.47, Lane 2, Kwang-Fu Road, Sec. 2,
Hsin-Chu City, Taiwan 30071, R.O.C.
TEL : 886-3-575-0275 FAX : 886-3-575-0475
Website: www.icplus.com.tw

Sales Office
4F, No. 106, Hsin-Tai-Wu Road, Sec.1,
Hsi-Chih, New Taipei City, Taiwan 22102, R.O.C.
TEL : 886-2-2696-1669 FAX : 886-2-2696-2220