5V/12V Synchronous Buck PWM DC/DC Controller

General Description

The RT8105 is a high efficiency synchronous buck PWM controllers that generate logic-supply voltages in PC based systems. These high performance , single output devices include internal soft-start, frequency compensation networks and integrates all of the control, output adjustment, monitoring and protection functions into a single package.

The device operating at fixed 300kHz frequency provides an optimum compromise between efficiency, external component size, and cost.

Adjustable over-current protection (OCP) monitors the voltage drop across the $R_{DS(ON)}$ of the lower MOSFET for synchronous buck PWM DC/DC controller. The over-current function cycles the soft-start in 4-times hiccup mode to provide fault protection, and in an always hiccup mode for under-voltage protection.

Ordering Information

RT8105 □□

- Package Type
  S : SOP-8
- Lead Plating System
  G : Green (Halogen Free and Pb Free)
  Z : ECO (Ecological Element with Halogen Free and Pb free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

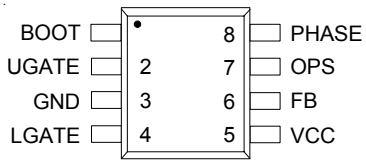
- **Operating with 5V or 12V Supply Voltage**
- **Drives All Low Cost N-MOSFETs**
- **Voltage Mode PWM Control**
- **300kHz Fixed Frequency Oscillator**
- **Fast Transient Response :**
  - **High-Speed GM Amplifier**
  - **Full 0 to 100% Duty Ratio**
- **Internal Soft-Start**
- **Adaptive Non-Overlapping Gate Driver**
- **Over-Current Fault Monitor on MOSFET, No Current Sense Resistor Required**
- **Full-Time Over Voltage Protection**
- **RoHS Compliant and Halogen Free**

Applications

- Graphic Card
- Motherboard, Desktop Servers
- IA Equipments
- Telecomm Equipments
- High Power DC/DC Regulators

Pin Configurations

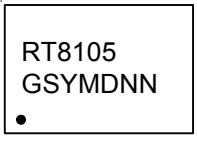
(TOP VIEW)



SOP-8

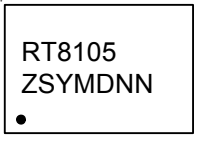
Marking Information

RT8105GS



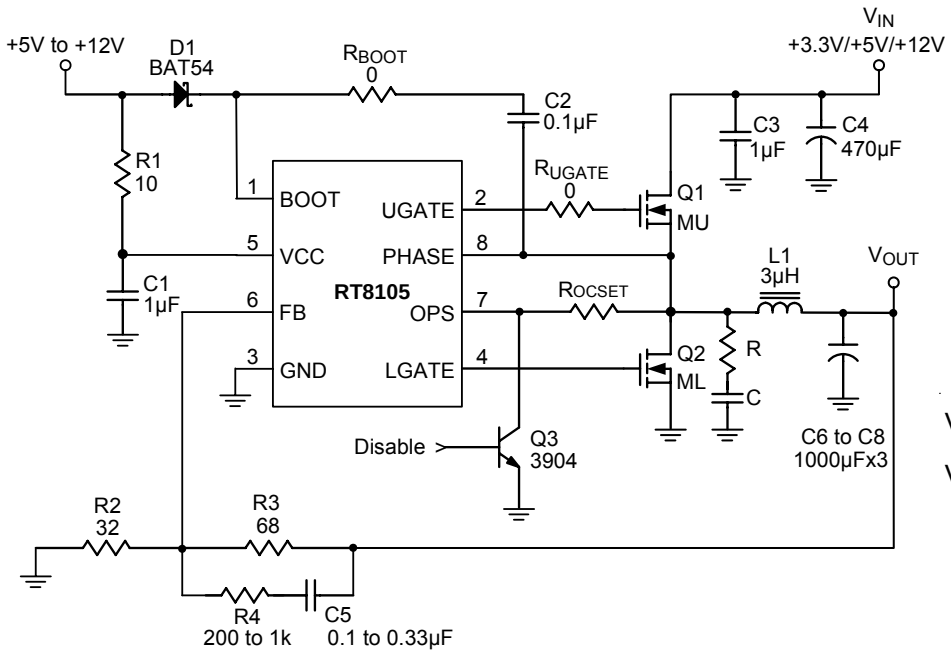
RT8105GS : Product Number
YMDNN : Date Code

RT8105ZS



RT8105ZS : Product Number
YMDNN : Date Code

Typical Application Circuit



$$V_{OUT} = V_{REF} \times (1 + \frac{R3}{R2})$$

V_{REF} : Internal reference voltage (0.8V ± 2%)

Functional Pin Description

BOOT (Pin 1)

Bootstrap supply pin for the upper gate driver. Connect the bootstrap capacitor between BOOT pin and the PHASE pin. The bootstrap capacitor provides the charge to turn on the upper MOSFET.

UGATE (Pin 2)

Upper gate driver output. Connect to the gate of high side power N-MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off.

GND (Pin 3)

Both signal and power ground for the IC. All voltage levels are measured with respect to this pin. Ties the pin directly to the low side MOSFET source and ground plane with the lowest impedance.

LGATE (Pin 4)

Lower gate drive output. Connect to the gate of low side power N-MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the lower MOSFET has turned off.

VCC (Pin 5)

Connect this pin to a well-decoupled 5V or 12V bias supply. It is also the positive supply for the lower gate driver, LGATE.

FB (Pin 6)

Switcher feedback voltage. This pin is the inverting input of the error amplifier. FB senses the switcher output through an external resistor divider network.

OPS (OCSET, POR and Shut-Down) (Pin 7)

This pin provides multi-function of the over-current setting, UGATE turn-on POR sensing, and shut-down features. Connecting a resistor (R_{OCSET}) between OPS and PHASE pins sets the over-current trip point.

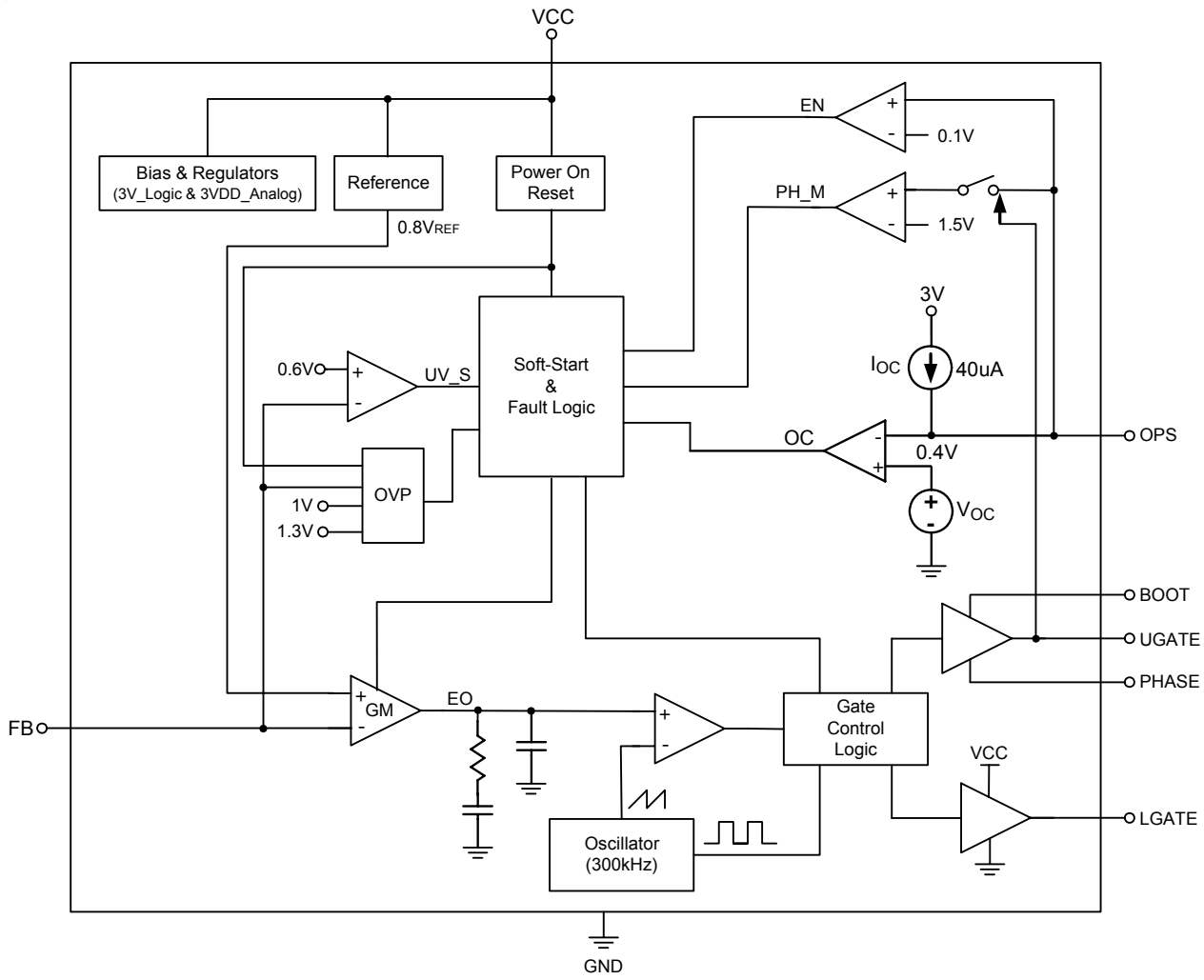
Pulling the pin to ground resets the device and all external MOSFETs are turned off allowing the output voltage power rails to float.

This pin is also used to detect V_{IN} in power on stage and issues an internal POR signal.

PHASE (Pin 8)

Connect this pin to the source of the upper MOSFET and the drain of the lower MOSFET.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Voltage, V_{CC} ---------- 16V
- BOOT to PHASE ---------- 15V
- UGATE to PHASE
  - DC ---------- –0.3V to ($V_{BOOT-PHASE}$ + 0.3V)
  - <20ns ---------- –5V to ($V_{BOOT-PHASE}$ + 5V)
- PHASE to GND
  - DC ---------- –0.5V to 15V
  - <20ns ---------- –5V to 25V
- LGATE to GND
  - DC ---------- –0.3V to (V_{CC} + 0.3V)
  - <20ns ---------- –5V to (V_{CC} + 5V)
- Input, Output or I/O Voltage ---------- GND-0.3V to 7V
- Power Dissipation, P_D @ T_A = 25°C (Note 2)
  - SOP-8 ---------- 0.625W
- Package Thermal Resistance
  - SOP-8, θ_{JA} ---------- 160°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Mode) ---------- 2kV
  - MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Voltage, V_{CC} ---------- 5V ± 5%,12V ± 10%
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –20°C to 85°C

Electrical Characteristics

(V_{CC} = 5V/12V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
IC Supply Voltage	V_{CC}		4.75	--	13.2	V
Nominal Supply Current	I_{CC}	UGATE and LGATE Open	--	6	15	mA
Power-On Reset						
POR Threshold	V_{CCRTH}	V_{CC} Rising	3.8	4.1	4.35	V
Hysteresis	V_{CCHYS}		0.35	0.5	--	V
Switcher Reference						
Reference Voltage	V_{REF}	V_{CC} = 12V	0.784	0.8	0.816	V
Oscillator						
Free Running Frequency	f_{OSC}	V_{CC} = 12V	250	300	350	kHz
Ramp Amplitude	ΔV_{OSC}	V_{CC} = 12V	--	1.5	--	V_{P-P}

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Error Amplifier (GM)						
E/A Transconductance	g_m		--	0.2	--	ms
Open Loop DC Gain	A_O		--	90	--	dB
PWM Controller Gate Drivers (V_{CC} = 12V)						
Upper Gate Source	I_{UGATE}	$V_{BOOT} - V_{PHASE}$ = 12V, $V_{UGATE} - V_{PHASE}$ = 6V	0.6	1	--	A
Upper Gate Sink	R_{UGATE}	$V_{BOOT} - V_{PHASE}$ = 12V, $V_{UGATE} - V_{PHASE}$ = 1V	--	4	8	Ω
Lower Gate Source	I_{LGATE}	V_{CC} = 12V, V_{LGATE} = 6V	0.6	1	--	A
Lower Gate Sink	R_{LGATE}	V_{CC} = 12V, V_{LGATE} = 1V	--	3	5	Ω
Protection						
FB Under-Voltage Trip	Δ_{FBUVT}	FB Falling	70	75	80	%
OC Current Source	I_{OC}	V_{PHASE} = 0V	35	40	45	μA
Pre-OVP Threshold (Before POR)	V_{OVP1}	V_{CC} = 3V, Sweep V_{FB}	--	1.1	1.3	V
OVP Threshold (After POR)	V_{OVP2}	V_{CC} = 5V, Sweep V_{FB}	1	1.3	1.5	V
Soft-Start Interval	T_{SS}		--	3.5	--	ms

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

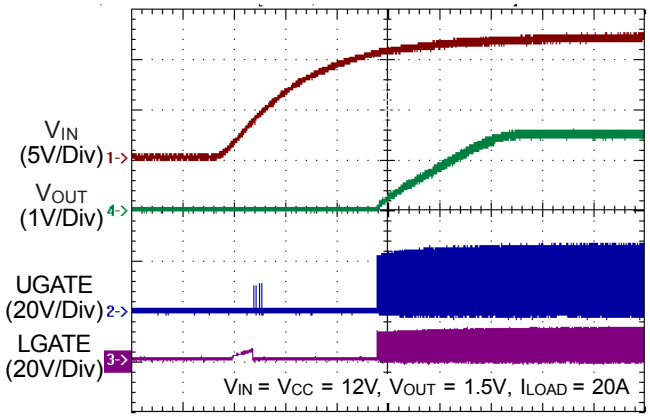
Note 2. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

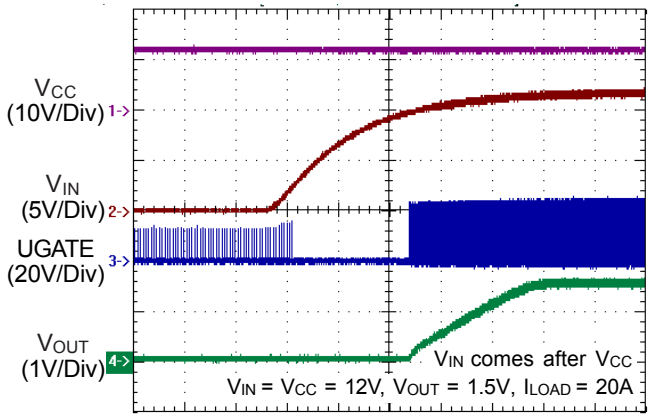
Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Operating Characteristics

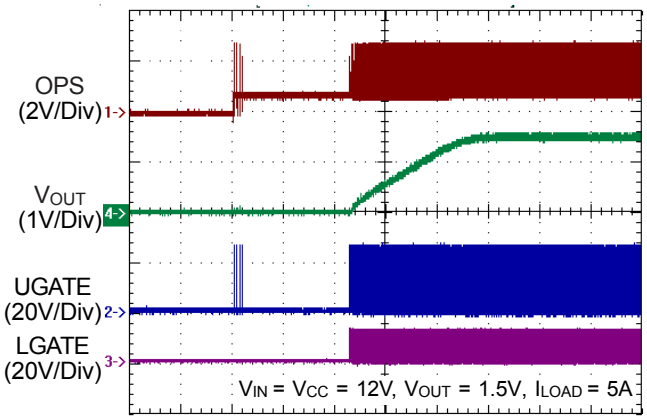
Power On from V_{IN}



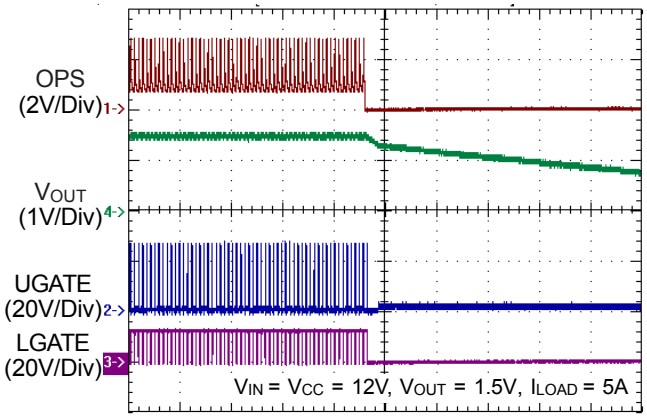
V_{IN} and V_{CC} Power Sequence



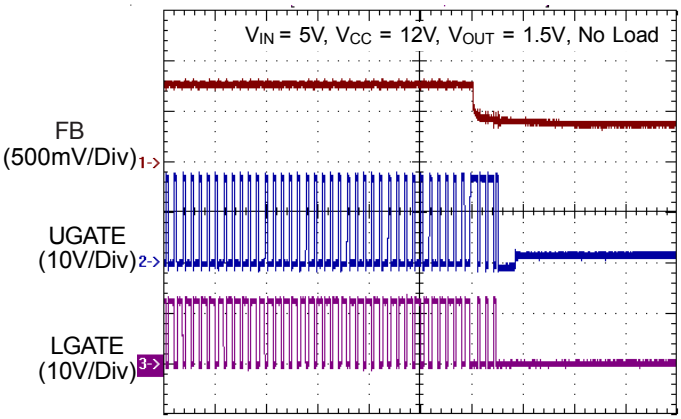
Enable from OPS



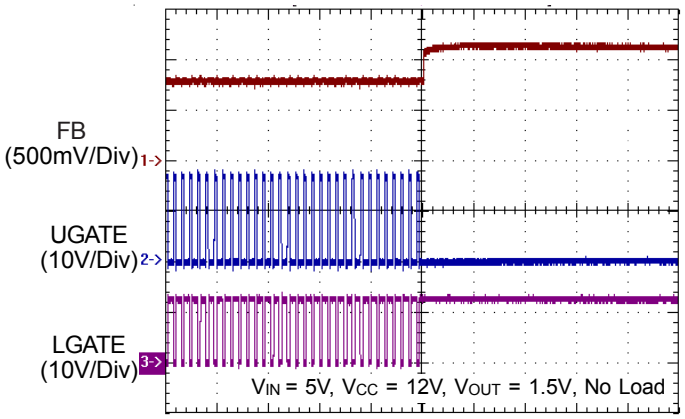
Disable from OPS



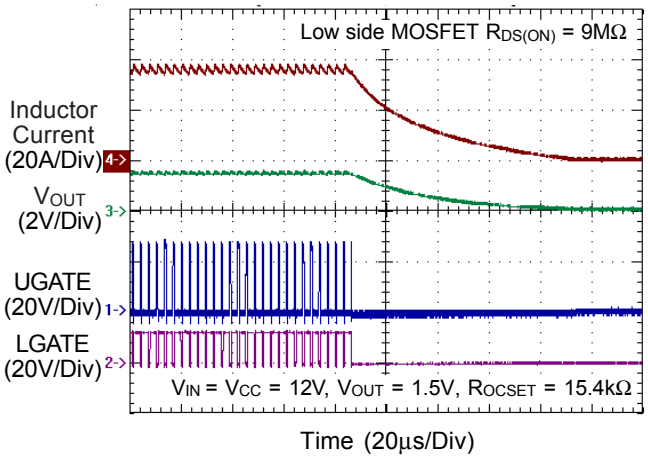
Under Voltage Protection



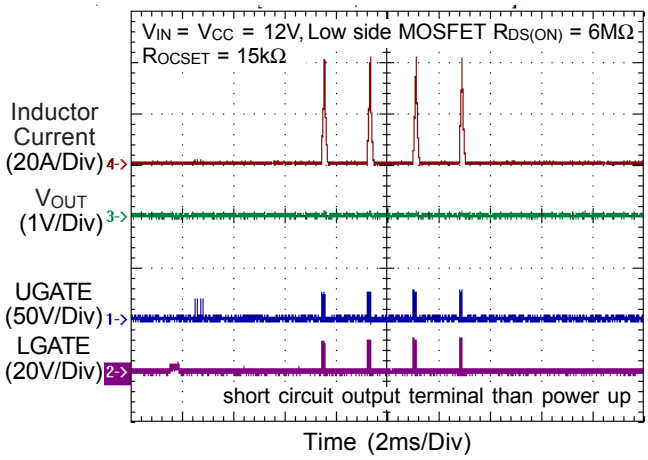
Over Voltage Protection



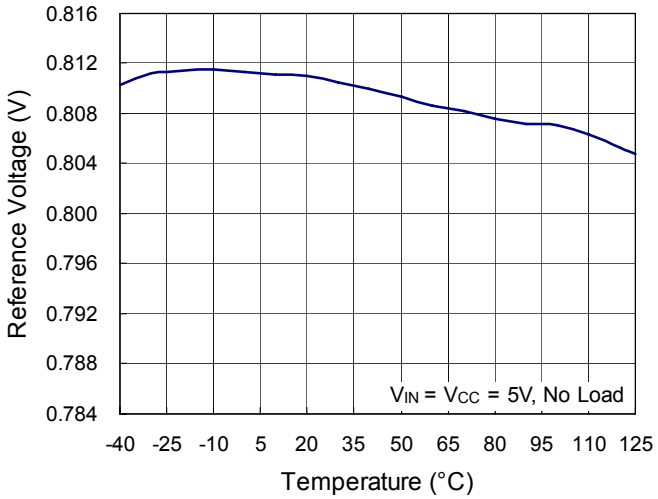
Over Current Protection



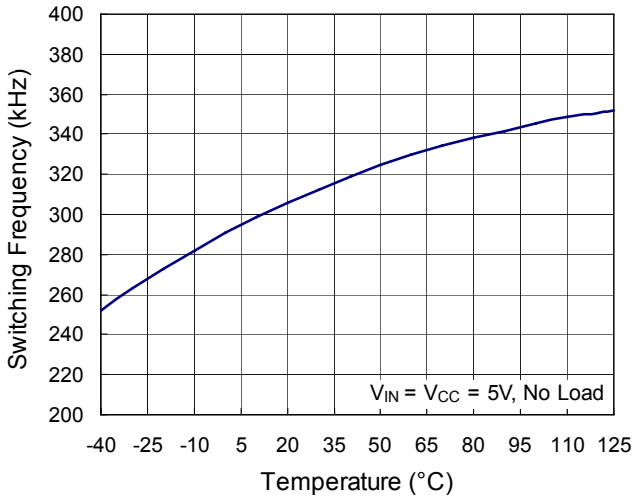
Short Circuit Over Current Protection



Reference Voltage vs. Temperature



Switching Frequency vs. Temperature



Application Information

RT8105 is a voltage-mode single phase synchronous buck controller with embedded MOSFET drivers. This part provides complete protection functions such as over voltage protection, under voltage protection and over current protection. Inductor current information is sensed by the $R_{DS(ON)}$ of the low side MOSFET. The over current protection threshold can be simply programmed by a resistor. In addition, the compensation circuit is implemented internally to minimize the external component count.

VCC Power on Reset and V_{IN} Detection

Once VCC exceeds its power on reset rising threshold V_{CCRTH}, UGATE will output continuous pulses (~10kHz, 1% duty cycle) for converter input voltage V_{IN} detection. Figure 1 and figure 2 illustrate the operation of V_{IN} detection for RT8105. V_{IN} is recognized ready by detecting the voltage pulses at VOS pin exceed 1.5V for four times (both rising edge + falling edge for counter increment = 1). Once V_{IN} is recognized ready, controller will initiates the soft start operation. Since a 40μA current will continuously flow through R_{OCSET}, R_{OCSET} must be lower than 37.5kΩ for the correct V_{IN} detection function. Controller will not initiate soft start if R_{OCSET} is higher than this value because V_{IN} will not be recognized ready.

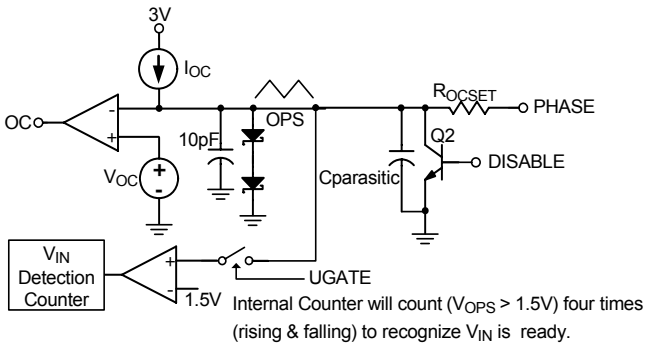


Figure 1. V_{IN} Detection Function

Soft Start

Once V_{IN} is recognized ready, LGATE will go high for a short period of time to discharge the pre-biased voltage at the output capacitor. After that, controller will initiate the soft start operation. RT8105 provides soft start function internally. The soft start function is used to prevent the large inrush current while converter is powered up. The FB signal will track the internal soft start signal, which is controlled by an internal digital counter and ramps up from zero in a monotone during soft start period. Therefore the duty cycle of UGATE signal will increase gradually and so does the input current. The typical soft-start duration is 3ms.

Over Current Protection (OCP)

Figure 2 shows the over current protection (OCP) scheme of RT8105. A resistor R_{OCSET} connected from PHASE pin to OPS pin sets the threshold. An internal current source, I_{OC} (40μA typically), flowing through R_{OCSET} determines the OCP trip point I_{OCSET}, which can be calculated using the following Equation :

$$I_{OCSET} \approx \frac{40uA \times R_{OCSET} - 0.4}{R_{DS(ON)} \text{ of the low side MOSFET}}$$

Because the $R_{DS(ON)}$ of MOSFET increases with temperature, it is necessary to take this thermal effect into consideration in calculating OCP point.

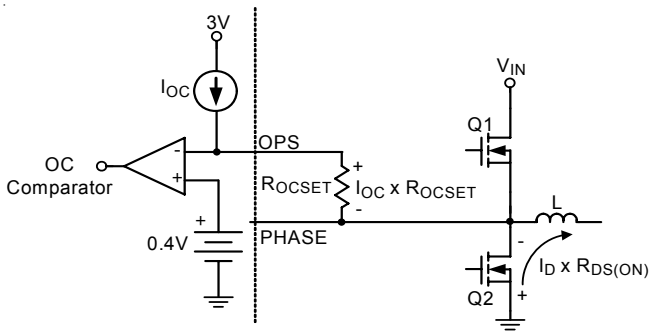


Figure 2. Over Current Protection Scheme

In addition, note that the OCP threshold is very sensitive to the parasitic capacitance at OPS pin. Parasitic capacitance or the drain-to-source capacitance of the small MOSFET (for shutdown function) will have influence on the OCP threshold. It is recommended to use small signal BJT for shutdown function. In addition, it is also recommended to place R_{OCSET} close to IC to minimize the trace parasitic.

When OCP is tripped, both UGATE and LGATE will go low to stop the energy transfer to the load. Controller will

try to restart in a hiccupped way. Figure 3 shows the hiccupped over current protection. Only four times of hiccup is allowed in over current protection. If over current condition still exist after four times of hiccup, controller will be latched.

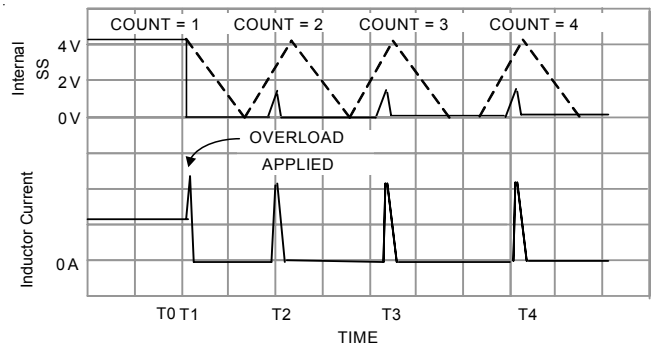


Figure 3. Hiccupped Over Current Protection

Over Voltage Protection (OVP)

The feedback voltage is continuously monitored for over voltage protection. When OVP is tripped, LGATE will go high and UGATE will go low to discharge the output capacitor.

RT8105 provides full-time over voltage protection whenever soft start completes or not.

Over voltage protection has two operating conditions: before soft start completes and after soft start completes. Each condition is described as follows.

Before soft start completes, the typical OVP threshold is 137.5% of the internal reference voltage V_{REF}. RT8105 provides non-latched OVP before soft start completes. The controller will return to normal operation if over voltage condition is removed.

After soft start completes, however, the OVP threshold is typically 162.5% of V_{REF}. RT8105 provides latched OVP after soft start completes. The controller can only be reset if VCC POR is exceeded again.

Under Voltage Protection (UVP)

The feedback voltage is also monitored for under voltage protection. The under voltage protection has 15us triggered delay. When UVP is tripped, both UGATE and LGATE will go low. Unlike OCP, UVP is not a latched protection; controller will always try to restart in a hiccupped way.

Enable/Disable

The controller can be disabled by pulling OPS pin to ground. The enable/disable function can be implemented by connecting a MOSFET or BJT to OPS pin. It is recommended to use small signal MOSFET/BJT to implement the enable/disable function.

Output Inductor Selection

The selection of output inductor depends on the efficiency, output current and operating frequency. Low inductance value can have fast transient response, but the associated large current ripple will cause large output ripple voltage and decrease the efficiency.

In general, a 20% to 40% of inductor ripple current percentage ($\Delta I_L / I_{OUT}$) is preferred in practical application. The minimum inductance can be determined as follows :

$$L = (V_{IN} - V_{OUT}) \times \frac{V_{OUT}}{V_{IN} \times f_S \times \Delta I_L}$$

Where :

V_{IN} = Input voltage

V_{OUT} = Output voltage

ΔI_L = Inductor current ripple

f_S = Switching frequency

Output Capacitor Selection

The selection of output capacitor depends on the inductor ripple current, the output ripple voltage and the amount of voltage under shoot during transient. The output ripple voltage is a function of both the capacitance and the equivalent series resistance (ESR) r_C. The output ripple voltage can be expressed as follows :

$$\Delta V_{OUT} = \Delta V_{OR} + \Delta V_{OC}$$

$$\Delta V_{OUT} = \Delta I_L \times rc + \frac{1}{C_O} \int_{t1}^{t2} ic\, dt$$

$$\Delta V_{OUT} = \Delta I_L \times \Delta I_L \times rc + \frac{1}{8} \frac{V_{OUT}}{C_{OL}} (1-D) T_S^2$$

where ΔV_{OR} is caused by ESR, and ΔV_{OC} is related to the capacitance value.

For electrolytic capacitor application, major of the output voltage ripple is typically contributed by the ESR. Therefore, the output voltage ripple can be simplified as follows :

$\Delta V_{OUT} = \Delta I_L \times r_C$

Therefore the ESR can be determined for a given output voltage ripple requirement.

Input Capacitor Selection

The selection of input capacitor depends on the maximum ripple current capability. Referred to Figure 1, the buck converter draws pulsed current from the input capacitor during S1 is turned on. RMS value of the ripple current flowing through the input capacitor can be expressed as follows :

$$Irms = I_{OUT}\sqrt{D(1-D)} \quad (A)$$

The input capacitor must be able to handle this RMS current. It is recommended to add ceramic capacitor and placed physically close to the drain of the high side MOSFET. This can effectively reduce the input ripple voltage.

Control Loop Stability

RT8105 utilizes operational transconductance amplifier (OTA) as the error amplifier and implements the compensation network internally. Figure 4 shows the internal Type II compensator, which provides two poles and one zero to the control loop.

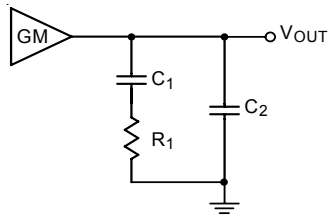


Figure 4. Internal Type II Compensator

One of the poles is located at low frequency to increase the low frequency gain to improve the DC regulation accuracy. The location of the other pole and the single zero can be calculated as follows :

$$F_Z = \frac{1}{2\pi \times R1 \times C2};\ F_P = \frac{1}{2\pi \times R1 \times \left(\frac{C1 \times C2}{C1 + C2}\right)}$$

The transconductance and the internal compensation values are : GM = 0.2mA/V, R1 ≈ 75kΩ, C1 ≈ 2.5nF, C2 ≈ 10pF.

The gain of the internal compensator at middle frequency can be calculated as follows :

$G_{mid\text{-}freq.}$ = GM x R1

Figure 5 illustrates the system Bode plot. The close loop gain is the sum of the modulation gain and the compensation gain. The goal is to obtain the required crossover frequency with sufficient phase margin. The crossover frequency is preferred to be 1/10 to 1/5 of the switching frequency. The preferred phase margin is greater than 45°.

Because RT8105 utilizes internal compensation, the location of F_Z, F_P and the gain at mid-frequency provided by the compensator are fixed. Therefore the inductance, output capacitance and especially the ESR of the output capacitor should be carefully selected to avoid stability issue. The ESR can not be too small, or the system will have stability problem. If the location of the zero contributed by ESR is far away from that of the LC double pole, the system will not have sufficient phase margin. It is recommended to choose output capacitor with proper ESR value to meet the stability requirement.

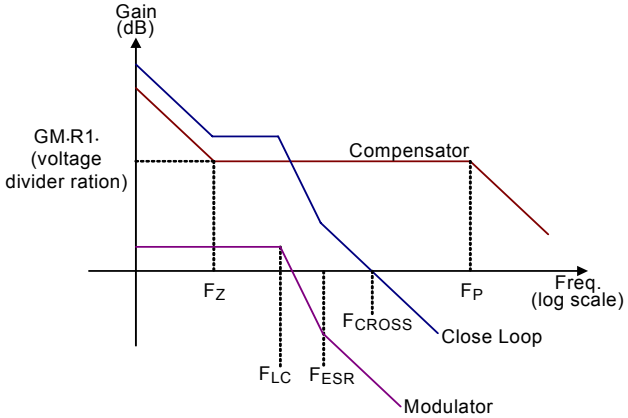


Figure 5. System Bode Plot

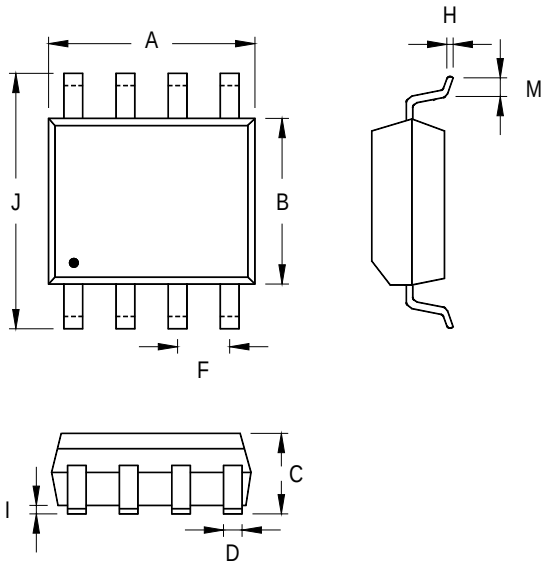
PCB Layout Considerations

PCB layout is critical to high-current high-frequency switching converter design. A good layout can help the controller to function properly and obtain better performance. On the other hand, the circuit may have more power loss, pool performance and even malfunction if without a carefully layout. In order to obtain better performance, the general guidelines of PCB layout are listed as follows.

- Power stage components should be placed first. Place the input bulk capacitors close to the high side power MOSFETs, and then locate the output inductor then finally the output capacitors.

- Placing the ceramic capacitors physically close to the drain of the high side MOSFET. This can reduce the input voltage drop when high side MOSFET is turned on.
- Keep the high-current loops as short as possible. The current transition between MOSFETs usually causes di/dt voltage spike due to the parasitic components on PCB trace and component lead. Therefore, making the trace length between power MOSFETs and inductors wide and short can reduce the voltage spike and also reduce EMI.
- Make MOSFET gate driver path as short as possible. Since the gate driver uses high-current pulses to switch on/off power MOSFET, the driver path must be short to reduce the trace inductance. This is especially important for low side MOSFET because this can reduce the possibility of shoot-through. Besides, also make the width of gate driving path as wide as possible to reduce the trace resistance.
- Provide enough copper area around power MOSFETs to help heat dissipation. Using thick copper also reduces the trace resistance and inductance to have better performance.
- The output capacitors should be placed physically close to the load. This can minimize the trace parasitic components and improve transient response.
- The feedback voltage divider resistor must be placed close to FB pin because it is noise-sensitive.
- R_{OCSET} should be placed close to IC.
- The small signal MOSFET/BJT used to shutdown the controller should be placed close to IC to minimize the trace parasitic components.
- Voltage feedback path must away from switching nodes. The switching nodes, such as the interconnection between high side MOSFET, low side MOSFET and inductor, is extremely noisy. Feedback path must away from this kind of noisy node to avoid noise pick-up.
- A multi-layer PCB design is recommended. Use one single layer as the ground and have separate layers for power rail or signal.

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.170	0.254	0.007	0.010
I	0.050	0.254	0.002	0.010
J	5.791	6.200	0.228	0.244
M	0.400	1.270	0.016	0.050

8-Lead SOP Plastic Package

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