μPD4164
65,536 x 1-BIT
DYNAMIC NMOS RAM

Revision 4

Description

The NEC μPD4164 is a 65,536-word by 1-bit dynamic N-channel MOS Random-access Memory (RAM) designed to operate from a single +5V power supply. The negative-voltage substrate bias is internally generated providing both automatic and transparent operation.

The μPD4164 utilizes a three-poly, N-channel, silicon-gate process which provides high storage cell density, high performance, and high reliability.

The μPD4164 uses a single transistor dynamic storage cell and advanced dynamic circuitry throughout, including the 512 sense amplifiers, which assure that power dissipation is minimized. Refresh characteristics have been chosen to maximize yield at a low cost to the user while maintaining compatibility between dynamic RAM generations.

The μPD4164 three-state output is controlled by $\overline{CAS}$, independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the output by holding $\overline{CAS}$ low. The data-out pin is returned to the high impedance state by returning $\overline{CAS}$ to a high state. The μPD4164 hidden refresh feature allows $\overline{CAS}$ to be held low to maintain output data while $\overline{RAS}$ is used to execute $\overline{RAS}$-only refresh cycles.

Refresh is accomplished by performing $\overline{RAS}$-only refresh cycles, hidden refresh cycles, or normal read or write cycles on the 128-address combinations of A_0 through A_6 during a 2ms period.

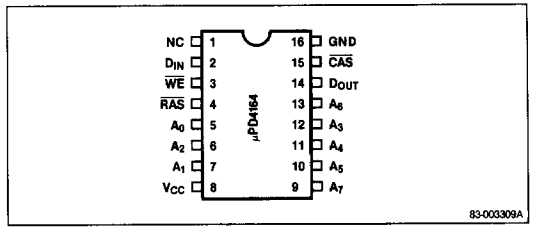
Multiplexed address inputs permit the μPD4164 to be packaged in the standard 16-pin dual-in-line package. The 16-pin package provides the highest system bit densities and is compatible with widely available automated handling equipment.

Features

- ☐ 65,536 x 1-bit organization
- ☐ High memory density
- ☐ Multiplexed address inputs
- ☐ Single +5V power supply
- ☐ On-chip substrate bias generator
- ☐ Low power dissipation: 27.5mW max (standby) (μPD4164-10); 330mW (active); 27.5mW (standby)
- ☐ Three-state, TTL-compatible, nonlatched output
- ☐ Read, write, read-write, read-modify-write, $\overline{RAS}$-only refresh, and page mode capability
- ☐ All inputs TTL-compatible, and low input capacitance
- ☐ 128 refresh cycles (A_0–A_6 pins for refresh address)
- ☐ $\overline{CAS}$-controlled output allows hidden refresh
- ☐ Available in a plastic 16-pin package
- ☐ 4 performance ranges:

Device	Access Time	R/W Cycle	RMW Cycle
μPD4164-10	100ns	200ns	230ns
μPD4164-12	120ns	230ns	245ns
μPD4164-15	150ns	260ns	280ns
μPD4164-20	200ns	330ns	345ns

Pin Configuration



Pin Identification

Pin No.	Symbol	Function
1	NC	No connection
2	D_{IN}	Data input
3	$\overline{WE}$	Write enable
4	$\overline{RAS}$	Row address strobe
5–7, 9–13	A_0–A_7	Address inputs
8	V_{CC}	+5V power supply
14	D_{OUT}	Data output
15	$\overline{CAS}$	Column address strobe
16	GND	Ground

Absolute Maximum Ratings*

Operating Temperature, T_{OPR}	0°C to +70°C
Storage Temperature, T_{STG} (Plastic Package)	−55°C to +125°C
Supply Voltages On Any Pin except V_{CC}	−1V to +7V①
Supply Voltage, V_{CC}	−0.5V to +7V①
Short-circuit Output Current	50mA
Power Dissipation, P_D	1W

Note: ① Relative to GND.

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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DC Characteristics

T_A = 0°C to +70°C ①; V_{CC} = +5V ± 10%; GND = 0V

Parameter	Symbol		Limits Min	Typ	Max	Unit	Test Conditions
Supply Voltage	V_{CC}		4.5	5.0	5.5	V	All voltages referenced to GND
	GND		0	0	0	V	
High-level Input Voltage, ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	V_{IHC}		2.4		5.5	V	
High-level Input Voltage, All Inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	V_{IH}		2.4		5.5	V	
Low-level Input Voltage, All Inputs	V_{IL}		−1.0		0.8	V	
Operating Current Average Power Supply Operating Current $\overline{RAS}$, $\overline{CAS}$ Cycling; t_{RC} = t_{RC} (min)	I_{CC1}	μPD4164-20			45		②
		μPD4164-15			50		
		μPD4164-12			55		
		μPD4164-10			60		
Standby Current Power Supply Standby Current ($\overline{RAS}$ = V_{IHC}, D_{OUT} = High-impedance)	I_{CC2}				5.0	mA	
Refresh Current Average Power Supply Current, Refresh Mode; $\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IHC}, t_{RC} = t_{RC} (min)	I_{CC3}	μPD4164-20			35	mA	②
		μPD4164-15			40		
		μPD4164-12			45		
		μPD4164-10			45		
Page Mode Current Average Power Supply Current, Page Mode Operation $\overline{RAS}$ = V_{IL}; $\overline{CAS}$ Cycling t_{PC} = t_{PC} (min)	I_{CC4}	μPD4164-20			35	mA	②
		μPD4164-15			40		
		μPD4164-12			45		
		μPD4164-10			45		
Input Leakage Current (any input); V_{IN} = 0V to +5.5V; All Other Pins Not Under Test = 0V	$I_{I(L)}$		−10		10	μA	
Output Leakage Current D_{OUT} is Disabled, V_{OUT} = 0V to +5.5V	$I_{O(L)}$		−10		10	μA	
Output Levels High-level Output Voltage (I_{OUT} = 5mA)	V_{OH}		2.4		V_{CC}	V	
Low-level Output Voltage (I_{OUT} = 4.2mA)	V_{OL}		0		0.4	V	

Notes: ① T_A is specified here for operation at frequencies to $t_{RC} \geq t_{RC}$ (min). Operation at higher cycle rates with reduced ambient temperatures and high power dissipation is permissible, however, provided AC operating parameters are met.

② I_{CC1}, I_{CC3} and I_{CC4} depend on output loading and cycle rates. Specified rates are obtained with the output open.

Capacitance

T_A = 0°C to +70°C; V_{CC} = +5V ± 10%; GND = 0V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Capacitance (A_0–A_7), D_{IN}	C_{I1}			5	pF	
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}			8	pF	
Output Capacitance $D_{(OUT)}$	C_O			7	pF	

AC Characteristics

T_A = 0°C to +70°C ①; V_{CC} = +5V ± 10%; GND = 0V ② ③ ④

Parameter	Symbol	Limits 4164-20 Min	4164-20 Max	4164-15 Min	4164-15 Max	4164-12 Min	4164-12 Max	4164-10 Min	4164-10 Max	Unit	Notes
Random Read or Write Cycle Time	t_{RC}	330		260		230		200		ns	⑤
Read-write Cycle Time	t_{RWC}	345		280		245		230		ns	⑤
Page Mode Cycle Time	t_{PC}	190		145		130		110		ns	⑤
Access Time from $\overline{RAS}$	t_{RAC}		200		150		120		100	ns	⑥ ⑦
Access Time from $\overline{CAS}$	t_{CAC}		100		75		60		50	ns	⑦ ⑧
Output Buffer Turn-off Delay	t_{OFF}	0	50	0	40	0	35	0	30	ns	⑨
Transition Times (rise and fall)	t_T	3	50	3	50	3	35	3	35	ns	④
$\overline{RAS}$ Precharge Time	t_{RP}	120		100		90		90		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	.2	10	.15	10	.12	10	.1	10	μs	
$\overline{RAS}$ Hold Time	t_{RSH}	100		75		60		50		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	.1	10	.075	10	.06	10	.05	10	μs	
$\overline{CAS}$ Hold Time	t_{CSH}	200		150		120		100		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	30	100	25	75	25	60	20	50	ns	⑩
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	0		0		0		0		ns	
$\overline{CAS}$ Precharge Time	t_{CPN}	30		25		25		20		ns	
$\overline{CAS}$ Precharge Time (for page mode cycle only)	t_{CP}	80		60		60		50		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	0		0		0		0		ns	
Row Address Set-up Time	t_{ASR}	0		0		0		0		ns	
Row Address Hold Time	t_{RAH}	20		15		15		10		ns	
Column Address Set-up Time	t_{ASC}	0		0		0		0		ns	
Column Address Hold Time	t_{CAH}	30		25		20		15		ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{AR}	130		100		80		65		ns	
Read Command Set-up Time	t_{RCS}	0		0		0		0		ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	25		20		20		20		ns	⑪

AC Characteristics (Cont.)

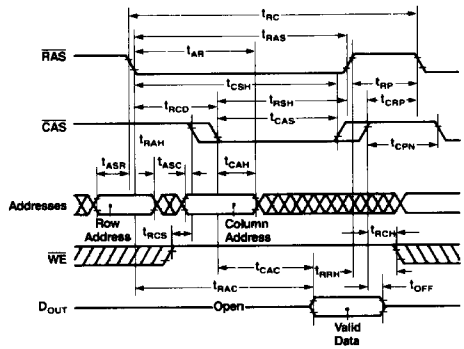
T_A = 0°C to +70°C ①; V_{CC} = +5V ± 10%; GND = 0V ② ③ ④

Parameter	Symbol	Limits 4164-20 Min	4164-20 Max	4164-15 Min	4164-15 Max	4164-12 Min	4164-12 Max	4164-10 Min	4164-10 Max	Unit	Notes
Read Command Hold Time	t_{RCH}	0		0		0		0		ns	⑪
Write Command Hold Time	t_{WCH}	55		45		35		30		ns	
Write Command Hold Time Referenced to $\overline{RAS}$	t_{WCR}	155		120		95		80		ns	
Write Command Pulse Width	t_{WP}	55		45		35		30		ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	55		45		40		35		ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	55		45		40		35		ns	
Data-in Set-up Time	t_{DS}	0		0		0		0		ns	⑫
Data-in Hold Time	t_{DH}	55		45		35		30		ns	⑫
Data-in Hold Time Referenced to $\overline{RAS}$	t_{DHR}	155		120		95		80		ns	
Refresh Period	t_{REF}		2		2		2		2	ms	
Write Command Set-up Time	t_{WCS}	−10		−10		−10		0		ns	⑬
$\overline{CAS}$ to $\overline{WE}$ Delay	t_{CWD}	55		45		40		40		ns	⑬
$\overline{RAS}$ to $\overline{WE}$ Delay	t_{RWD}	130		120		100		90		ns	⑬

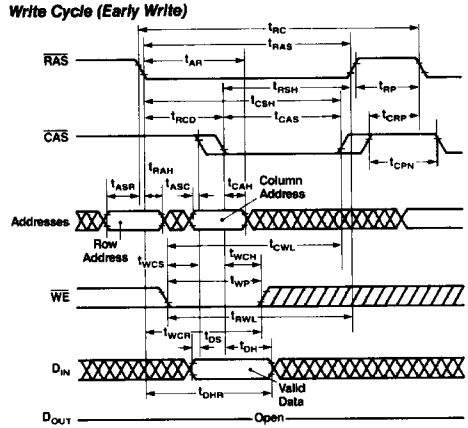
Notes:
① T_A is specified here for operation at frequencies to $t_{RC} \geq t_{RC}$ (min). Operation at higher cycle rates with reduced ambient temperatures and higher power dissipation is permissible, however, provided AC operating parameters are met.
② An initial pause of 100μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
③ AC measurements assume t_T = 5ns.
④ V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.
⑤ The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle times at which proper operation over the full temperature range (T_A = 0°C to +70°C) is assured.
⑥ Assumes that $t_{RCS} \leq t_{RCD}$ (max). If t_{RCS} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the values shown.
⑦ Measured with a load equivalent to 2 TTL loads and 100pF.
⑧ Assumes that $t_{RCD} \geq t_{RCD}$ (max).
⑨ t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to output voltage levels.
⑩ Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC}.
⑪ Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
⑫ These parameters are referenced to CAS leading edge in early write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.
⑬ t_{WCS}, t_{CWD} and t_{RWD} are restrictive operating parameters in read-write, and read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write and the data output will contain data read from the selected cell. If neither of the above conditions is met the condition of the data-out (at access time and until CAS goes back to V_{IH}) is indeterminate.

Timing Waveforms

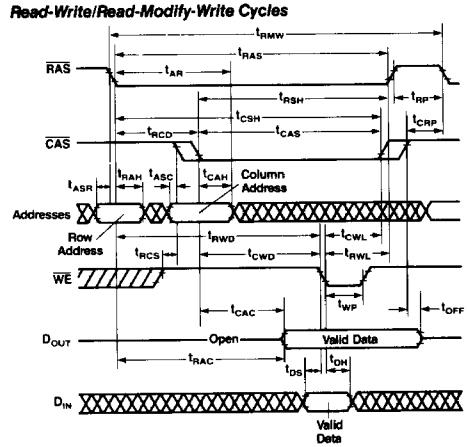
Read Cycle



Write Cycle (Early Write)



Read-Write/Read-Modify-Write Cycles



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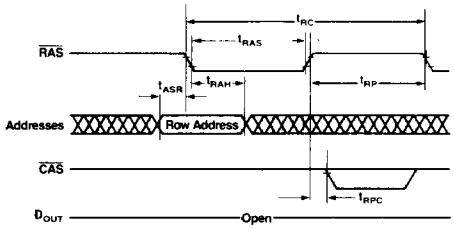
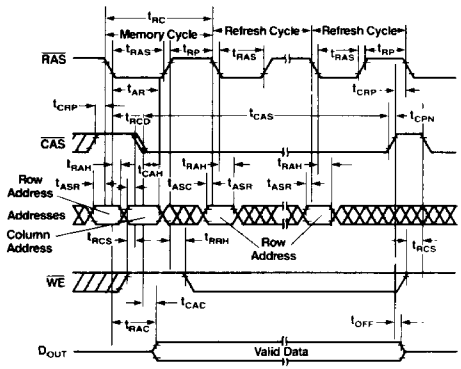
Timing Waveforms (Cont.)

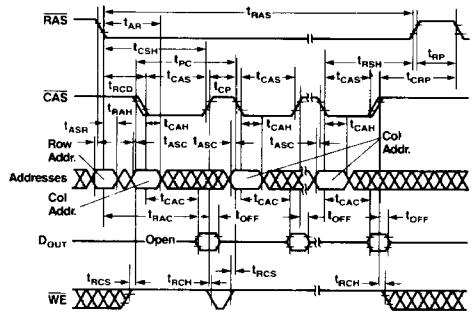
RAS-only Refresh Cycle



Hidden Refresh Cycle



Page Mode Read Cycle



Page Mode Write Cycle