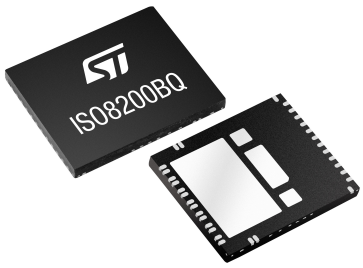
life.augmented

ISO8200BQ

Datasheet

Galvanic isolated octal high-side smart power solid state-relay



Product status link

ISO8200BQ

Product label

SUSTAINABLE TECHNOLOGY

Features

- $V_{CC(AMR)}$ = 45 V
- Process side op. range V_{CC} = 10.5 to 36 V
- $R_{DS(on)}$ = 0.12 Ω per channel (TYP)
- Fast demagnetization of inductive loads $V_{DEMAG(TYP)}$ = V_{CC} - 50 V
- Per channel process side op. current: I_{OUT} < 0.7 A
- Very low process and logic sides supply current
- Under-voltage shut down with auto restart and hysteresis
- Logic side 5 V and 3.3 V TTL/CMOS and MCU compatible I/Os
- Common output enable/disable pin
- Reset function for IC outputs disable
- High common mode transient immunity
- Short circuit protection on output channels: $I_{LIM(MIN)}$ = 0.7 A
- Per channel over-temperature protection with thermal independence of separate channels
- Case over-temperature protection
- ESD protection
- Over-voltage protection (V_{CC} clamping)
- Loss of GND_{CC} and V_{CC} protection
- Common fault open-drain diagnostic
- Designed to meet IEC 61000-4-2, IEC 61000-4-4, IEC 61000-4-5 and IEC 61000-4-8
- UL1577 and UL508 certified
- Safety Limits as per VDE0884-11

Applications

- Programmable logic control
- Industrial PC peripheral input/output
- Numerical control machines
- Drivers for all types of loads (resistive, capacitive, inductive)

Description

The ISO8200BQ is a galvanic isolated 8-channel driver featuring a very low supply current. It contains 2 independent galvanic isolated voltage domains (V_{CC} for the power stage and V_{DD} for the digital stage).

The IC is intended to drive any kind of load with one side connected to ground. Active channel current limitation (OVL) combined with thermal shutdown (OVT) and automatic restart (independent for each channel) , protects the device against overload and short-circuit.

Built-in thermal shutdown protects each channel from over-temperature and overload: each overheated channel automatically turns OFF after its junction temperature triggers the protection threshold (T_{JSD}). The channel turns back ON if its junction temperature decreases lower than restart threshold (T_{JR}).

An additional case temperature sensor protects the whole chip against over-temperature (OVC event): if the case temperature triggers the T_{CSD} threshold then overloaded channels are turned OFF and restart only when case temperature decreased down to the reset threshold (T_{CR}). Non overloaded channels continue to operate normally.

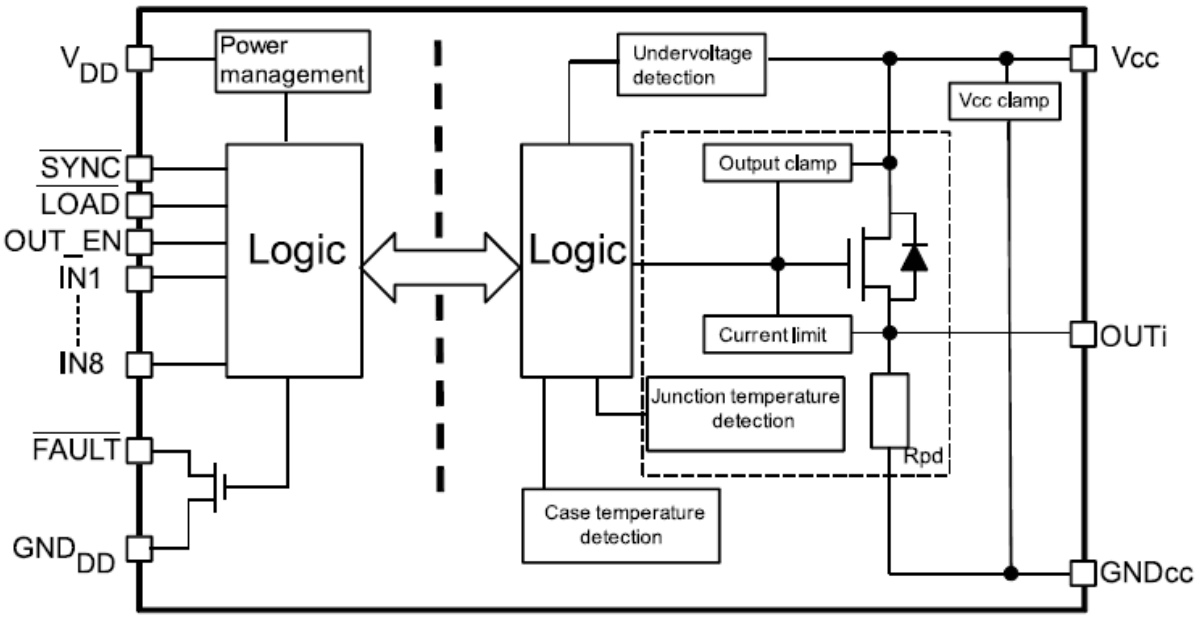
Other embedded functions are loss of ground protection, V_{CC} and V_{DD} UVLOs (with hysteresis), reset function for immediate power output shutdown and watchdog.

An internal circuit provides an OR-wired not latched OVT that is reported on the common $\overline{\text{FAULT}}$ indicator pin. $\overline{\text{FAULT}}$ is an open drain, active low, fault indication pin.

The Synchronous Control Mode (by driving $\overline{\text{SYNC}}$ and $\overline{\text{LOAD}}$ pins independently) is used to reduce the jittering of the outputs and to drive at the same time the outputs of different devices.

1 Block diagram

Figure 1. **Block diagram**



2 Pin connection

Figure 2. **Pin connection (top through view)**

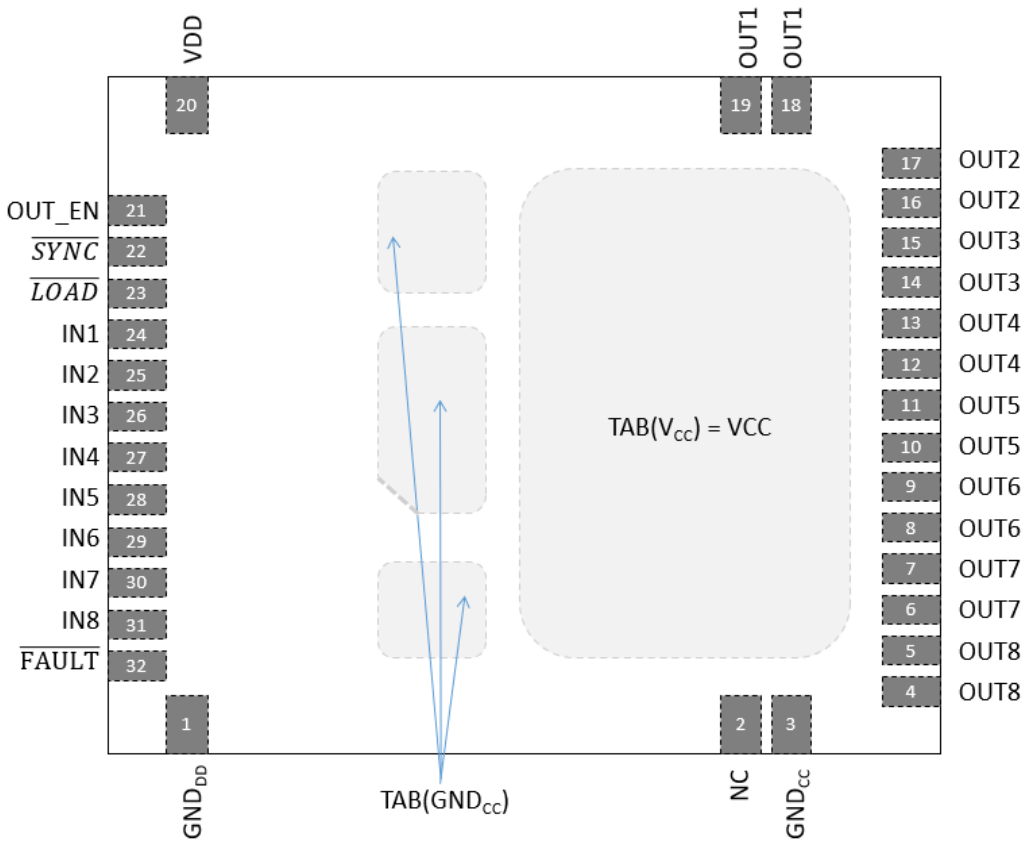


Table 1. Pin description

Pin	Name	Description
1	GND_{DD}	Input logic ground, negative logic supply
2	NC	Not connected
3	GND_{CC}	Output (process side) power ground
4	OUT8	Channel 8 power output(1)
5		
6	OUT7	Channel 7 power output(1)
7		
8	OUT6	Channel 6 power output(1)
9		
10	OUT5	Channel 5 power output(1)
11		
12	OUT4	Channel 4 power output(1)
13		
14	OUT3	Channel 3 power output(1)
15		
16	OUT2	Channel 2 power output(1)
17		
18	OUT1	Channel 1 power output(1)
19		
20	V_{DD}	Positive Control Logic Stage supply
21	OUT_EN	Output enable
22	$\overline{SYNC}$	Input-to-output synchronization signal, active low
23	$\overline{LOAD}$	Load input data signal, active low
24	IN1	Channel 1 input
25	IN2	Channel 2 input
26	IN3	Channel 3 input
27	IN4	Channel 4 input
28	IN5	Channel 5 input
29	IN6	Channel 6 input
30	IN7	Channel 7 input
31	IN8	Channel 8 input
32	$\overline{FAULT}$	Common fault indication, active low
TAB(V_{CC})	V_{CC}	Exposed tab internally connected to V_{CC}, positive power supply voltage
TAB(GND_{CC})	TAB(GND_{CC})	Exposed tab to be connected to GND_{CC} (= ground of Process Stage)

1. *Connect the two pins on the same net of the application board*

3 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Process Stage supply voltage	-0.3	+45	V
V_{DD}	Control Logic Stage supply voltage	-0.3	+6	V
V_{IN}	DC input pins voltage (IN_X, $\overline{LOAD}$, $\overline{SYNC}$ and OUT_EN)	-0.3	+6	V
V_{FAULT}	$\overline{FAULT}$ pin voltage	-0.3	+6	V
$I_{GND_{DD}}$	DC digital ground reverse current		-25	mA
I_{OUT}	Channel output current (continuous)		Internally limited	A
$I_{GND_{CC}}$	DC power ground reverse current		-250	mA
I_{RX}	Reverse output current (from OUT_X pins to V_{CC})		-5(1)	A
I_{IN}	DC input pins current (IN_X, $\overline{LOAD}$, $\overline{SYNC}$ and OUT_EN)	-10	+ 10	mA
I_{FAULT}	$\overline{FAULT}$ pin current	-10	+ 10	mA
V_{ESD}	Electrostatic discharge with human body model (R = 1.5 kΩ; C = 100 pF)		2000	V
E_{AS}	Single pulse avalanche energy per channel not simultaneously @T_{amb}= 125 °C, I_{OUT} = 0.5 A		1.8	J
	Single pulse avalanche energy per channel, all channels driven simultaneously @T_{amb}= 125 °C, I_{OUT} = 0.5 A		0.35	
P_{TOT}	Power dissipation at T_c = 25 °C		Internally limited (2)	W
T_J	Junction operating temperature		Internally limited(2)	°C
T_{STG}	Storage temperature		-55 to 150	°C

1. *this value is intended with each couple of OUT_X pins shorted on the application board*
2. *Protection functions are intended to avoid IC damage in fault conditions and are not intended for continuous operation. Continuous or repetitive operations of protection functions may reduce the IC lifetime.*

4 Thermal data

Table 3. Thermal data

Symbol	Parameter	Max. value	Unit
$R_{thj\text{-}case}$	Thermal resistance, junction-case(1)	2	°C/W
$R_{thj\text{-}amb}$	Thermal resistance, junction-ambient(2)	15(3)	°C/W

1. *For each channel.*
2. *TFQFPN32 mounted on the product evaluation board (FR4, 4 layers, 8 cm^2 for each layer, copper thickness 35 mm).*
3. *Maximum power dissipation = 4.3W (@T_{amb} = 85°C, T_J < 150°C)*

5 Electrical characteristics

(10.5 V < V_{CC} < 36 V; -40 °C < T_J < 125 °C, unless otherwise specified)

Table 4. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{CC(THON)}$	V_{CC} under-voltage turn-ON threshold	V_{DD} = 3.3 V, V_{CC} increasing		9.5	10.5	V
$V_{CC(THOFF)}$	V_{CC} under-voltage turn-OFF threshold	V_{DD} = 3.3 V, V_{CC} decreasing	8	9		V
$V_{CC(HYS)}$	V_{CC} under-voltage hysteresis		0.25	0.5		V
$V_{CCclamp}$	Clamp on V_{CC} pin	I_{clamp} = 20 mA	45	50	52	V
$R_{DS(on)}$	On-state resistance (see Figure 3)	I_{OUT} = 0.5 A, T_J = 25 °C				Ω
		I_{OUT} = 0.5 A T_J = 125 °C		0.12	0.24	
R_{PD}	Output pull-down resistor			210		kΩ
I_{CC}	Power supply current	All channels in OFF-state, V_{CC} = 36 V		5		mA
		All channels in ON-state, V_{CC} = 36 V		9		
I_{LGND}	Ground disconnection output current	V_{CC} = V_{GND} = 0 V, V_{OUT} = -24 V			500	µA
$V_{OUT(OFF)}$	OFF-state output voltage	Channel OFF and I_{OUT} = 0 A			1	V
$I_{OUT(OFF)}$	OFF-state output current	Channel OFF and V_{OUT} = 0 V			5	µA

Table 5. Digital supply voltage

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operating voltage		2.75		5.5	V
$V_{DD(THON)}$	V_{DD} under-voltage turn-ON threshold	V_{CC} = 24 V, V_{DD} increasing	2.55		2.75	V
$V_{DD(THON)}$	V_{DD} under-voltage turn-OFF threshold	V_{CC} = 24 V, V_{DD} decreasing	2.45		2.65	V
$V_{DD(HYS)}$	V_{DD} under-voltage hysteresis		0.04	0.1		V
I_{DD}	I_{DD} supply current	V_{DD} = 5 V and input channel with a steady logic level		4.5	6	mA
		V_{DD} = 3.3 V and input channel with a steady logic level		4.4	5.9	mA

Table 6. Diagnostic pin and output protection function

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{FAULT}	$\overline{FAULT}$ pin open-drain voltage output low	I_{FAULT} = 10 mA			0.4	V
I_{LFAULT}	$\overline{FAULT}$ output leakage current	V_{FAULT} = 5 V			1	µA
I_{PEAK}	Maximum DC output current before limitation	V_{CC} = 24 V R_{LOAD} = 0 Ω		1.6		A
I_{LIM}	Short-circuit current limitation		0.7	1.3	1.9	A
H_{yst}	I_{LIM} tracking limits			0.3		A
T_{JSD}	Junction shutdown temperature		150	170		°C
$T_{J\ R}$	Junction reset temperature			150		°C
T_{HIST}	Junction thermal hysteresis			20		°C
T_{CSD}	Case shutdown temperature		115	130	145	°C
T_{CR}	Case reset temperature			110		°C
T_{CHYST}	Case thermal hysteresis			20		°C
V_{DEMAG}	Output voltage at turn-OFF	I_{OUT} = 0.5 A I_{LOAD} > = 1 mH	V_{CC}-45	V_{CC}-50	V_{CC}-52	V

Table 7. Power switching characteristics (V_{CC} = 24 V; R_{LOAD} = 48 Ω; -40 °C < T_J < 125 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
dV/dt(ON)	Turn-ON voltage slope	(see Figure 4)		5.6		V/µs
t_r	Rise time			5		µs
dV/dt(OFF)	Turn-OFF voltage slope			2.81		V/µs
t_f	Fall time			5		µs
t_d(ON)	Turn-ON delay time	(see Figure 5, Figure 6)		17	22	µs
t_d(OFF)	Turn-OFF delay time (1)			22	40	µs

Figure 3. $R_{DS(on)}$ measurement

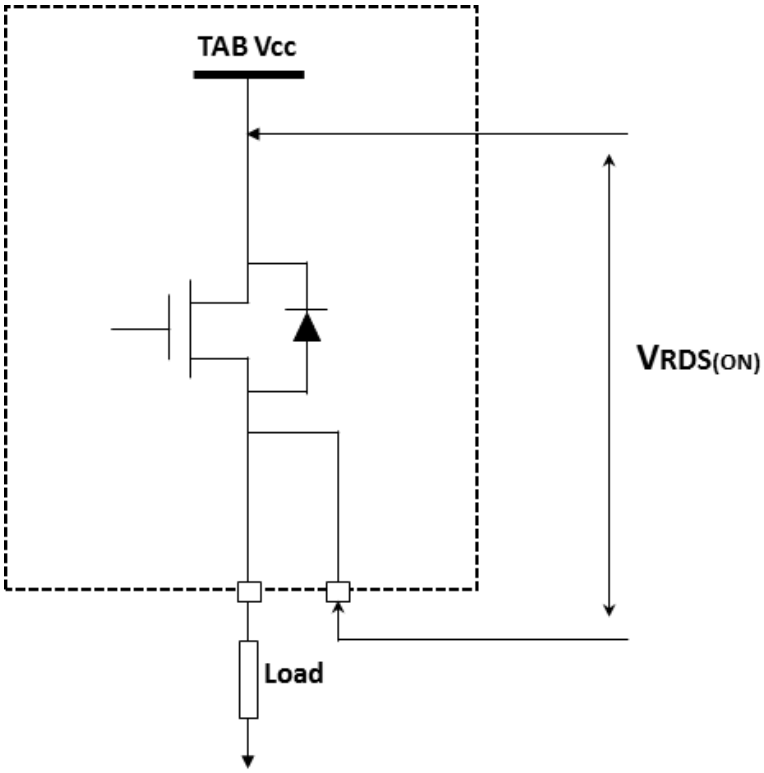


Figure 4. dV/dT

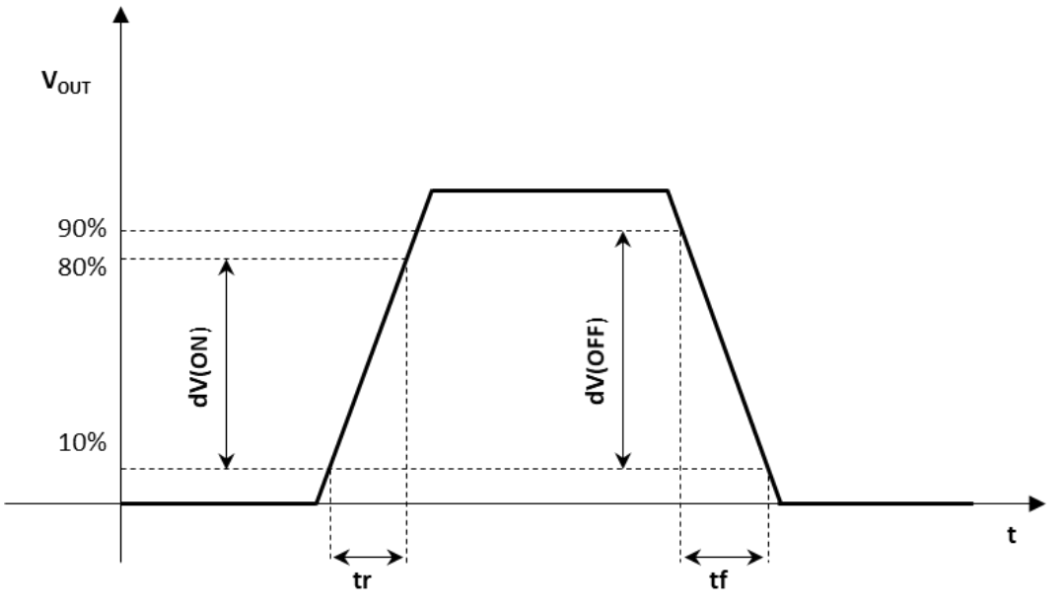


Figure 5. td(ON)-td(OFF) synchronous mode

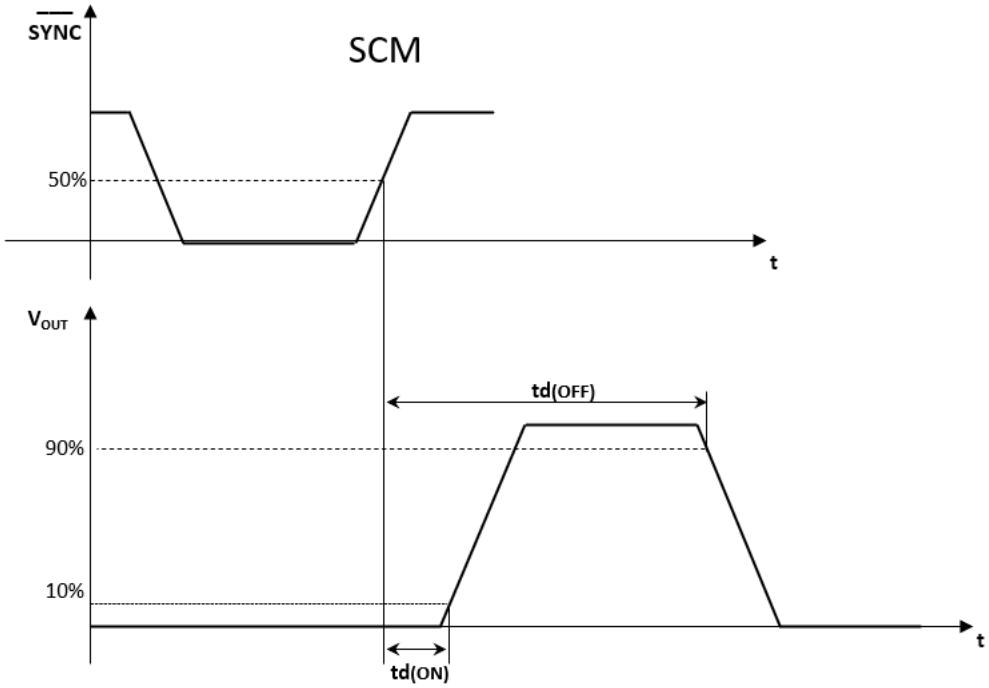


Figure 6. td(ON)-td(OFF) direct control mode

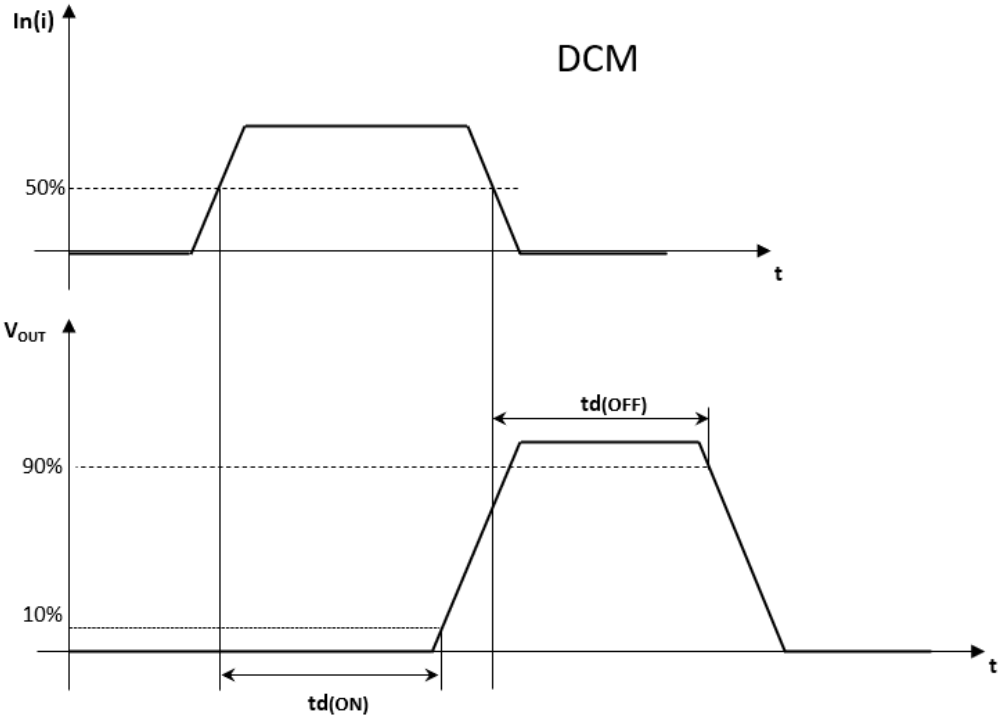


Table 8. Logic input and output

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Logic input pin low level voltage (IN_X, OUT_EN, $\overline{LOAD}$, $\overline{SYNC}$)		-0.3		0.3 x V_{DD}	V
V_{IH}	Logic input pin high level voltage (IN_X, OUT_EN, $\overline{LOAD}$, $\overline{SYNC}$)		0.7 x V_{DD}		V_{DD} + 0.3	V
$V_{I(HYST)}$	Logic input hysteresis voltage (IN_X, OUT_EN, $\overline{LOAD}$, $\overline{SYNC}$)	V_{DD} = 5 V		100		mV
I_{IN}	Logic input pin current (IN_X, OUT_EN, $\overline{LOAD}$, $\overline{SYNC}$)	V_{IN} = 5 V	10			µA

Table 9. Parallel interface timings (V_{DD} = 5 V; V_{CC} = 24 V; -40 °C < T_J < 125 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{dis(SYNC)}$	$\overline{SYNC}$ disable time	Sync. control mode	10			µs
$t_{dis(DCM)}$	$\overline{SYNC}$, $\overline{LOAD}$ disable time	Direct control mode	80			ns
$t_{w(SYNC)}$	$\overline{SYNC}$ negative pulse width	Sync. control mode	20		195	µs
$t_{su(LOAD)}$	$\overline{LOAD}$ setup time	Sync. control mode	80			ns
$t_{h(LOAD)}$	$\overline{LOAD}$ hold time	Sync. control mode	400			ns
$t_{w(LOAD)}$	$\overline{LOAD}$ pulse width	Sync. control mode	240			ns
$t_{su(IN)}$	Input setup time		80			ns
$t_{h(IN)}$	Input hold time		10			ns
$t_{w(IN)}$	Input pulse width	Sync. control mode	160			ns
		Direct control mode	20			µs
t_{INLD}	IN to $\overline{LOAD}$ time	Direct control mode from IN variation to $\overline{LOAD}$ falling edge	80			ns
t_{LDIN}	$\overline{LOAD}$ to IN time	Direct control mode from $\overline{LOAD}$ falling edge to IN variation	400			ns
$t_{w(OUT\_EN)}$	OUT_EN pulse width	(see Figure 8, Figure 9)	150			ns
$t_{p(OUT\_EN)}$	OUT_EN propagation delay			22	40	µs
$t_{jitter(SCM)}$	Jitter on single channel	Sync. mode			6	µs
$t_{jitter(DCM)}$		Direct mode			20	

Table 10. Internal communication timings (V_{DD} = 5 V; V_{CC} = 24 V; -40 °C < T_J < 125 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$f_{refresh}$	Refresh delay			15		kHz
t_{WM}	Power side watchdog time		272	320	400	µs

Table 11. Insulation and safety-related specifications

Symbol	Parameter	Test conditions	Value	Unit
CLR(1)	Clearance (minimum external air gap)	Measured from input terminals to output terminals, the shortest distance through air	3.3	mm
CPG(1)	Creepage (minimum external tracking)	Measured from input terminals to output terminals, the shortest distance path analog body	3.3	mm
CTI(2)	Comparative tracking index (tracking resistance)	DIN IEC 112/VDE 0303 part 1	≥ 600	V
	Isolation group	Material group (DIN VDE 0110, 1/89), table 1	I	-

1. *Creepage and clearance requirements should be applied according to the specific equipment isolation standard of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the PCB do not reduce this distance.*
2. *When high voltage is applied across the isolator, electric discharges on or close to the surface of the package, can cause localized deterioration in the mold compound, resulting in a partially conducting path from one side of the isolator to the other. This phenomenon is called tracking. The ability of a material to withstand tracking is quantified by a comparative tracking index (CTI). Using a mold compound with a higher CTI allows the use of smaller packages and saves board space.*

Table 12. Insulation characteristics

Symbol	Parameter	Test condition	Value	Unit
In accordance with IEC 60747-17				
V_{PR}	Input-to-output test voltage	Method a, type test, tm = 10 s partial discharge < 5 pC	1500	V_{PEAK}
		Method b, 100% production test, tm = 1 s partial discharge < 5 pC	1758	V_{PEAK}
V_{IOTM}	Transient over-voltage	Type test; t_{ini} = 60 s	4245	V_{PEAK}
V_{IOSM}	Maximum surge insulation voltage	Type test	4245	V_{PEAK}
R_{IO}	Insulation resistance	Type test V_{IO} = 500 V, T_{STG} = 60 s	$>10^9$	Ω
UL1577				
V_{ISO}	Insulation withstand voltage	1 min. type test	2500/3536	V_{RMS}/V_{PEAK}
V_{ISO} test	Insulation withstand test	1 s 100% production	3000/4245	V_{RMS}/V_{PEAK}

Table 13. Safety limits

Symbol	Parameter	Test conditions	Value	Unit
Input safety, Logic side				
T_{SI}	Safety temperature of Logic side	-	150	°C
P_{SI}	Safety power of Logic side(1)	V_{DD} ≤ 6.0 V, $V_{LOGIC(x)}$ ≤ 6.0 V, $I_{LOGIC(x)}$ ≤ 10 mA, T_J ≤ T_{SI}	0.9	W
Output safety, Process side				
T_{SO}	Safety temperature of Process side	-	150	°C
P_{SO}	Safety power of Process side(1)	V_{CC} ≤ 36 V, $I_{OUT(x)}$ ≤ 1.5 A, T_J ≤ T_{SO}	4.5	W

1. *The above limits are measured according to VDE 0884-11. Respecting the above limits prevents potential damage to the isolation barrier upon failure on logic or process side circuitry. The user should apply these values to protect the IC and ensure the safety of the embedded isolation barrier. LOGIC(x) stands for any pin on the logic side; OUT(x) stands for any of the 8 output pins on the process side.*

6 Functional description

6.1 Parallel interface

Smart parallel interface built-in ISO8200BQ offers three interfacing signals easily managed by a micro-controller.

The $\overline{\text{LOAD}}$ signal enables the input buffer storing the value of the channel inputs.

The $\overline{\text{SYNC}}$ signal copies the input buffer value into the transmission buffer and manages the synchronization between low voltage side and the channel outputs on the isolated side.

The OUT_EN signal enables the channel outputs.

An internal refresh signal updates the configuration of the channel outputs with a $f_{refresh}$ frequency. This signal can be disabled forcing low the $\overline{\text{SYNC}}$ input when $\overline{\text{LOAD}}$ is high.

$\overline{\text{SYNC}}$ and $\overline{\text{LOAD}}$ pins can be in direct control mode (DCM) or synchronous control mode (SCM).

6.1.1 Input signals (IN1 to IN8)

Inputs from IN1 to IN8 are the driving signals of the corresponding OUT1 to OUT8 outputs. Data are direct loaded on related outputs if $\overline{\text{SYNC}}$ and $\overline{\text{LOAD}}$ inputs are low (DCM operation) or stored into input buffer when $\overline{\text{LOAD}}$ is low and $\overline{\text{SYNC}}$ is high.

6.1.2 Load input data ($\overline{\text{LOAD}}$)

The input is active low; it stores the data from IN1 to IN8 into the input buffer.

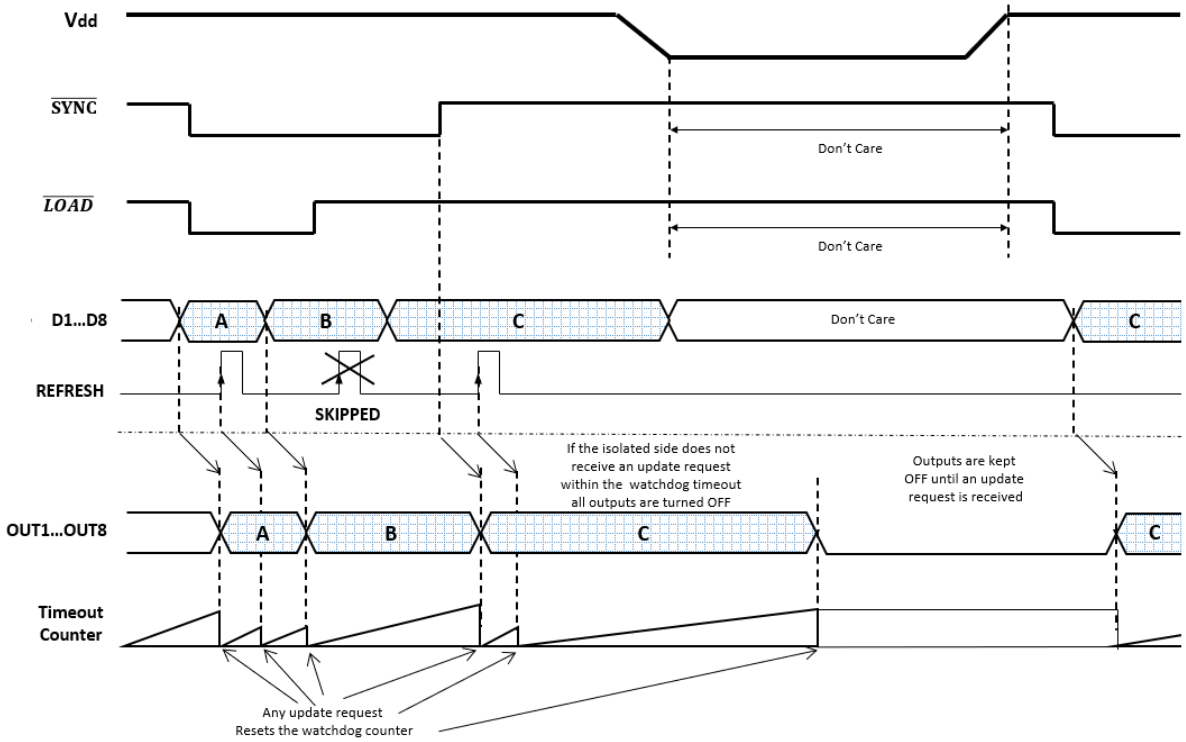
6.1.3 Output synchronization ($\overline{\text{SYNC}}$)

The input is active low; it enables the ISO8200BQ transmission buffer loading input buffer data and manages the transmission between the two isolated sides of the device.

6.1.4 Watchdog

The IC is composed by two chips (Logic Stage and Process Stage) supplied by two independent and galvanic isolated sources (V_{DD}/GND_{DD} and V_{CC}/GND_{CC} pins, respectively). The IC provides a watchdog function in order to guarantee a safe condition for the Process Stage when V_{DD} (or GND_{DD}) supply voltage is missing. If the Logic Stage does not update the output status within t_{WD}, all the outputs of the Process Stage are disabled until a new update request is received. The Logic Stage chip periodically sends a refresh signal to the Process Stage chip. The refresh signal is also considered a valid update signal to reset the timeout counter on the Process Stage, so the isolated side watchdog does not protect the system from a failure of the host controller (e.g., MCU freezing).

Figure 7. Watchdog behavior



6.1.5 Output enable (OUT_EN)

This pin provides a fast way to disable all outputs simultaneously. When the OUT_EN pin is driven low the outputs are disabled. To enable the output stage, the OUT_EN pin has to be raised. This timing execution is compatible with an external reset push, safety requirement, and allows, in a PLC system, the micro-controller polling to obtain all internal information during a reset procedure.

Figure 8. OUT_EN without effect on output

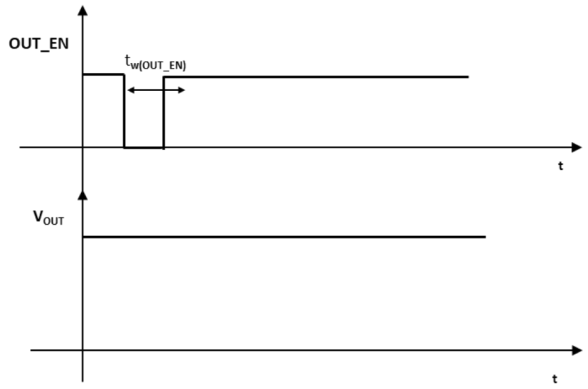
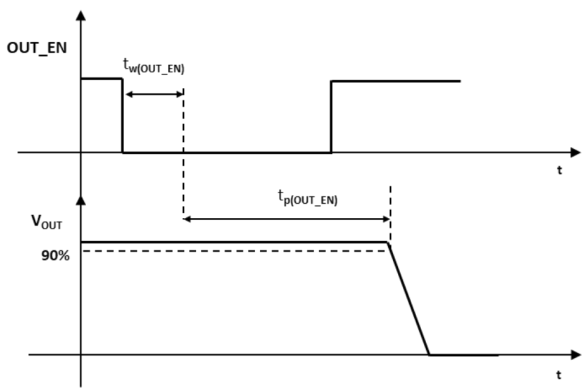


Figure 9. OUT_EN effective on output channel



6.2 Direct control mode (DCM)

When $\overline{\text{SYNC}}$ and $\overline{\text{LOAD}}$ inputs are driven by the same signal, the device operates in direct control mode (DCM).

In DCM the $\overline{\text{SYNC}}$/ $\overline{\text{LOAD}}$ signal operates as an active low input enable:

- when the signal is high, the current output configuration is kept regardless the input values
- when the signal is low, each channel input directly drives the respective output

This operation mode can also be set shorting both signals to the digital ground; in this case the channel outputs are always directly driven by the inputs except when OUT_EN is low (outputs disabled).

Table 14. Interface signal operation in direct control mode

$\overline{\text{SYNC}}$/ $\overline{\text{LOAD}}$	OUT_EN	Device behavior
Don't care	Low (1)	The outputs are disabled (turned off)
High	High	The outputs are left unchanged
Low	High	The channel inputs drive the outputs

1. *The outputs are turned off on OUT_EN falling edge and they are kept disabled as long as it is low.*

Figure 10. Direct control mode IC configuration

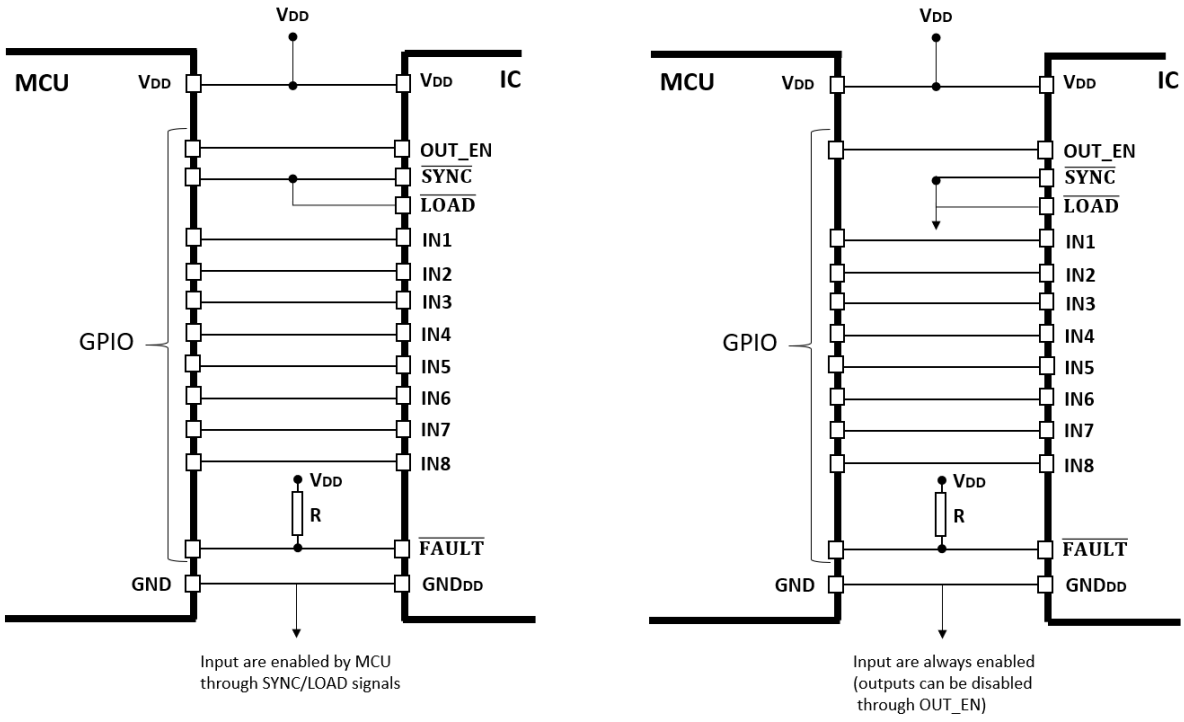
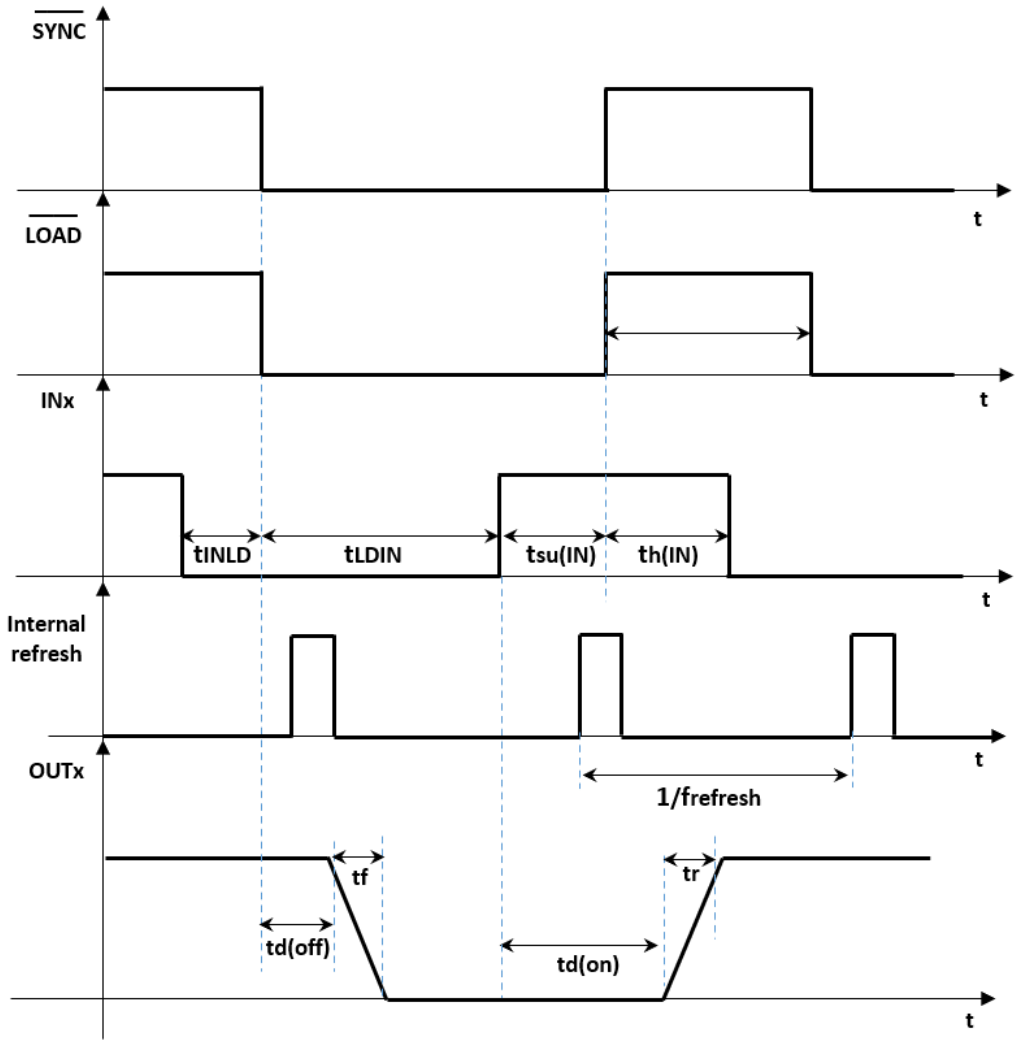


Figure 11. **Direct control mode time diagram**



6.3 Synchronous control mode (SCM)

When $\overline{\text{SYNC}}$ and $\overline{\text{LOAD}}$ inputs are independently driven, the device can operate in synchronous control mode (SCM). The SCM is used to reduce the jittering of the outputs and to drive all outputs of different devices at the same time.

In SCM the $\overline{\text{LOAD}}$ signal is forced low to update the input buffer while the $\overline{\text{SYNC}}$ signal is high. The $\overline{\text{LOAD}}$ signal is raised and the $\overline{\text{SYNC}}$ one is forced low for at least $t_{SYNC(SCM)}$. During this period, the internal refresh is disabled and any pending transmission between the low voltage and the isolated side is completed. When the $\overline{\text{SYNC}}$ signal is raised the channel output configuration is changed according to the one stored in the input.

If the $t_{SYNC(SCM)}$ limit is met, the maximum jitter of the channel outputs is t_{jitter}(SCM).

If more devices share the same $\overline{\text{SYNC}}$ signal, all device outputs change simultaneously with a maximum jitter related to maximum delay and maximum jitter for single device.

Table 15. Interface signal operation in synchronous control mode

$\overline{\text{LOAD}}$	$\overline{\text{SYNC}}$	OUT_EN	Device behavior
Don't care	Don't care	Low (1)	The outputs are disabled (turned off)
High	High	High	The outputs are left unchanged
Low	High	High	The input buffer is enabled, the outputs are left unchanged
High	Low	High	The internal refresh signal is disabled, the transmission buffer is updated and the outputs are left unchanged
High	Rising edge	High	The outputs are updated according to the current transmission buffer value
Low	Low	High	Should be avoided (DCM operation only)

1. *The outputs are turned off on OUT_EN falling edge and they are kept disabled as long as it is low.*

Figure 12. Synchronous control mode IC configuration

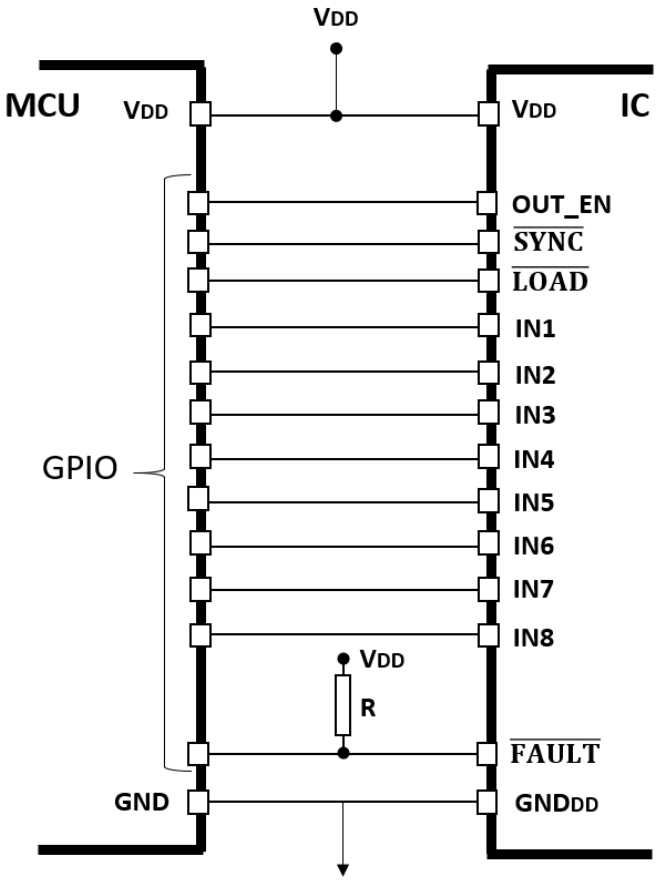


Figure 13. **Synchronous control mode time diagram**

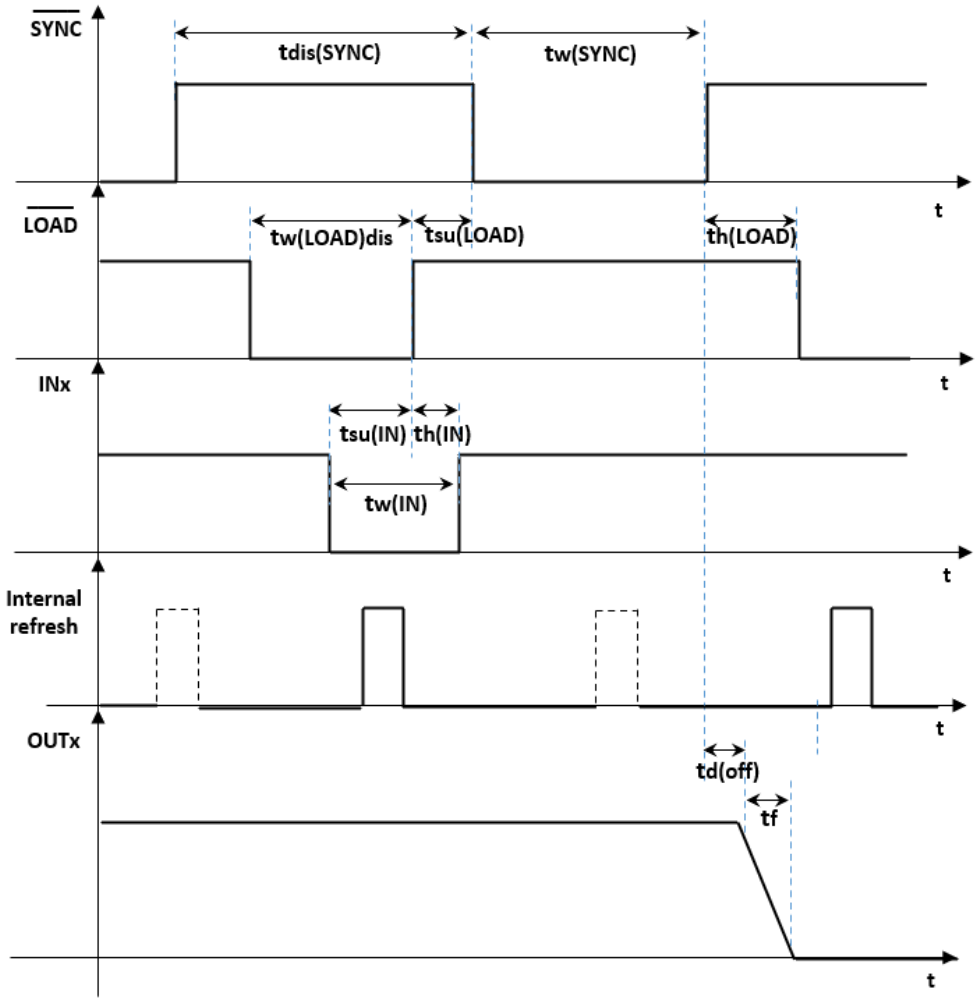
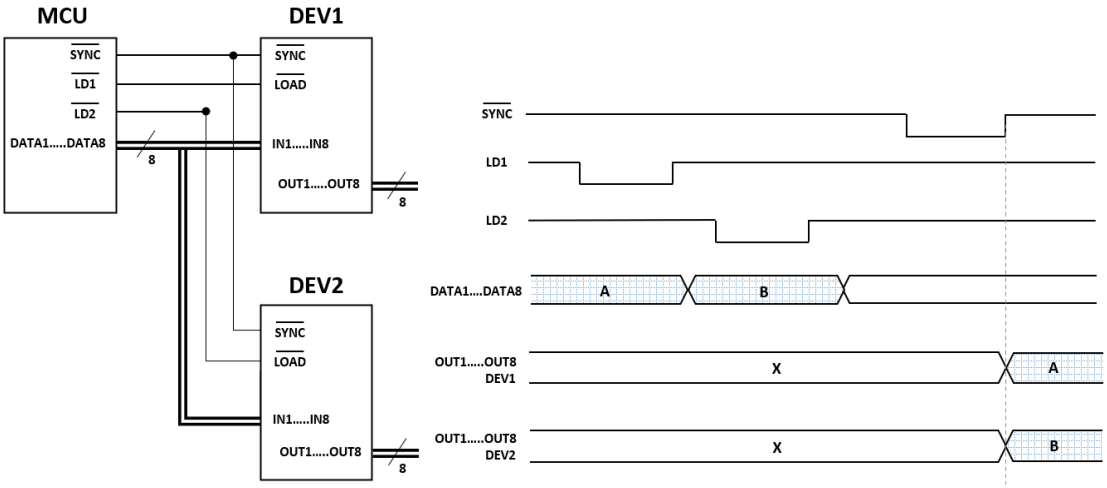


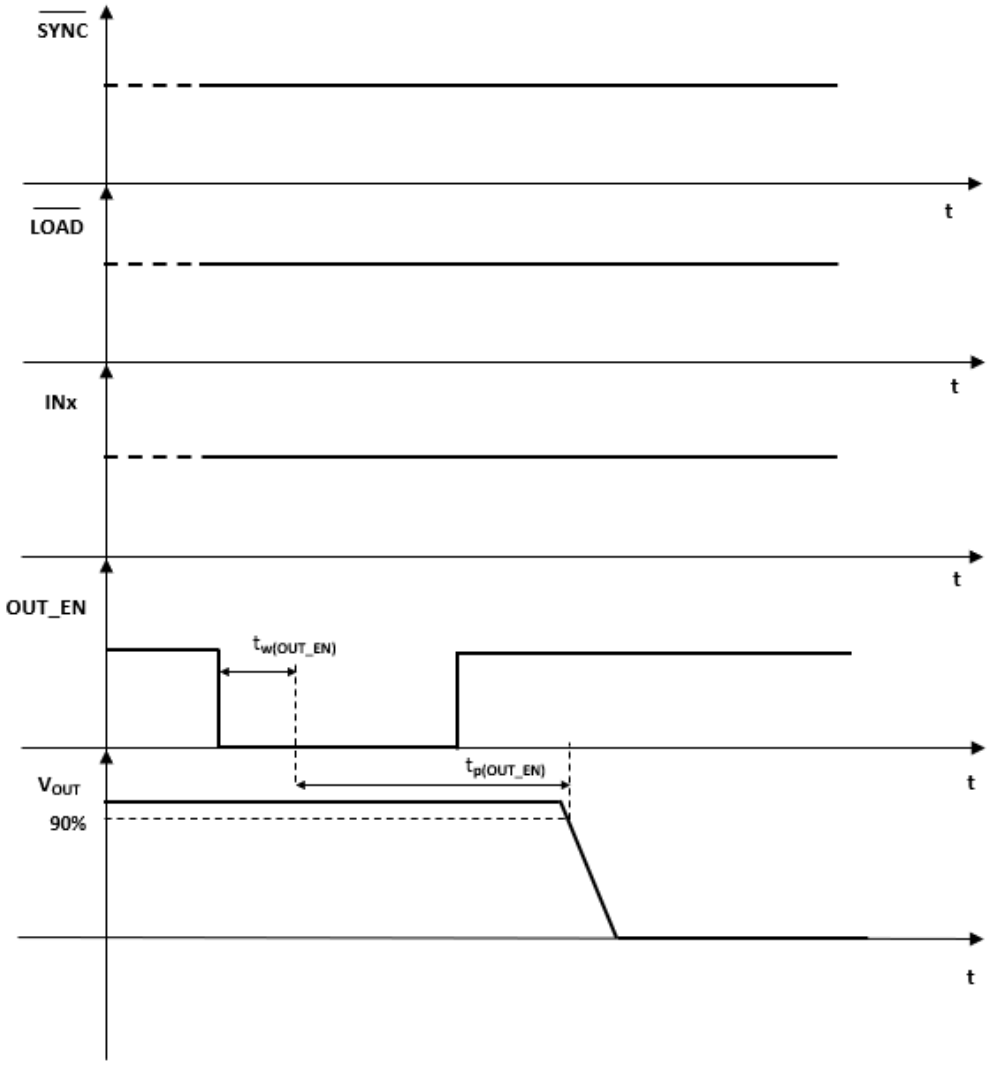
Figure 14. **Multiple device synchronous control mode**



6.3.1 OUT_EN behavior in Synchronous Control Mode

In SCM the OUT_EN signal acts as a reset for the internal data register driving the output switches. When the OUT_EN pin is driven low for at least $t_{w(OUT\_EN)}$ (see Figure 15), all the eight outputs are disabled. OUT_X remains low even if OUT_EN is raised with IN_X already high: a new transition of $\overline{LOAD}$ and $\overline{SYNC}$ is required (see Figure 13).

Figure 15. OUT_EN behavior in Synchronous Control Mode, time diagram



6.4 Fault indication

The $\overline{FAULT}$ pin is an active low open-drain output indicating fault conditions. This pin is active when at least one of the following conditions occurs:

- Junction over-temperature of one or more channels ($T_J > T_{TJSD}$) or case shut-down protection ($T_C > T_{CSD}$) is active
- Communication error

The communication error is intended as an internal data corruption event in the data transfer through isolation. In case of communication error the outputs are initially kept in the previous status and then reset (turned off) at the first communication error during data transfer of the refresh signal.

6.4.1 Junction over-temperature and case over-temperature

The thermal status of the device is updated during each transmission sequence between the two isolated sides.

In SCM operation, when the $\overline{\text{LOAD}}$ signal is high and the $\overline{\text{SYNC}}$ one is low, the communication is disabled. In this case the thermal status of the device cannot be updated and the $\overline{\text{FAULT}}$ indication can be different from the current status. In any case, the thermal protection of the output channel in the Process Stage is always operative.

Figure 16. Thermal status update (DCM)

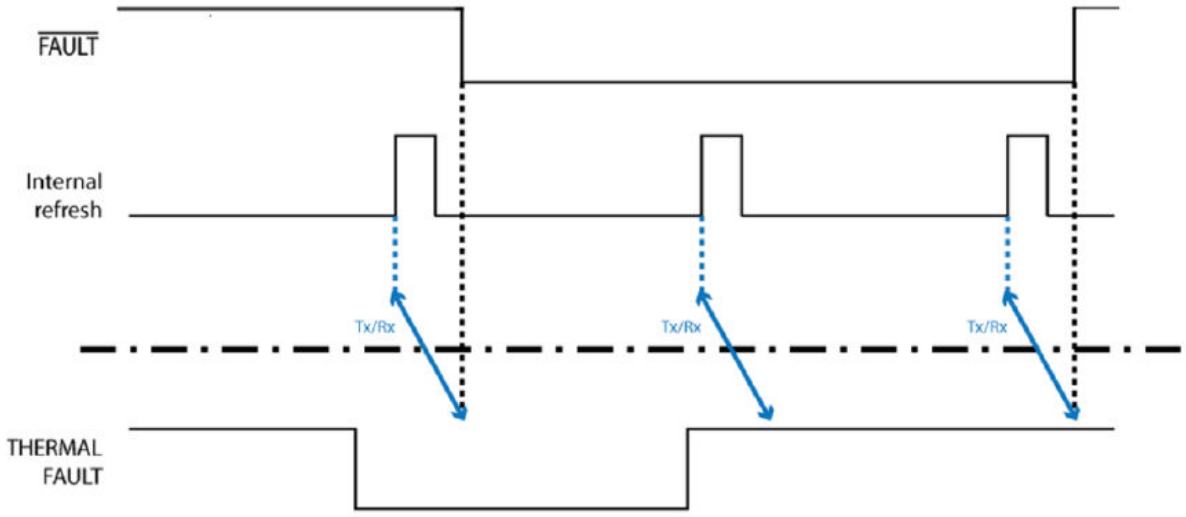
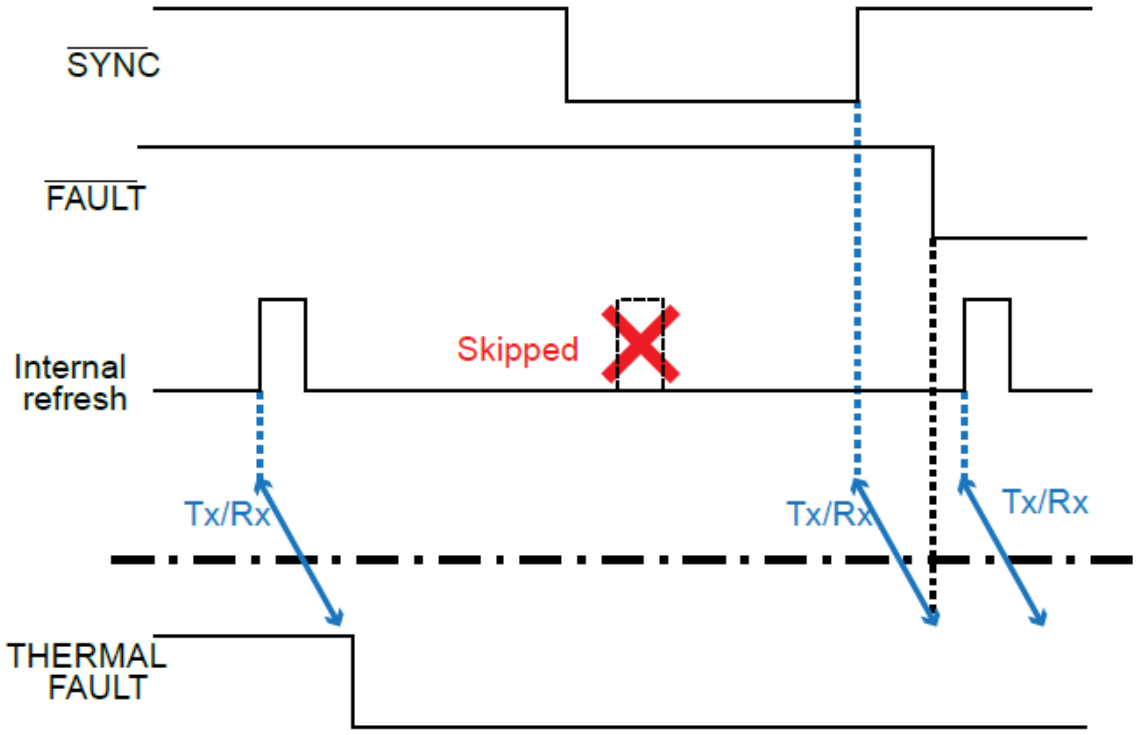


Figure 17. Thermal status update (SCM)



6.5 Truth table

Table 16. Truth table

x = maintain the previous condition.

Condition	Input IN_x	OUT_x	FAULT
Normal operation	H	ON	H (not active)
	L	OFF	
Thermal Junction ($T_{JX} > T_{JSD}$)	H	OFF	L (active)
	L	OFF	H (not active)
Thermal Case $T_C > T_{CSD}$	See Figure 24		H (not active)(1)
V_{CC} UVLO FAULT	L	OFF	X
	H		
V_{DD} UVLO (Watchdog)	X	OFF	H (not active)
Internal communication error	X	X	L (active)

1. *Usually, the thermal case is consequence of thermal junction event latching the FAULT pin low until the thermal junction event resets. If the thermal case is triggered without any thermal junction event (for example in case of very high ambient temperature) then the FAULT pin is not activated*

7 Power section

7.1 Current limitation

The current limitation process is active when the current sense connected on the output stage measures a current value, which is higher than a fixed threshold.

When this condition is verified the gate voltage is modulated to avoid the increase of the output current over the limitation value.

The following figures show typical output current waveforms with different load conditions.

Figure 18. Switching on resistive load

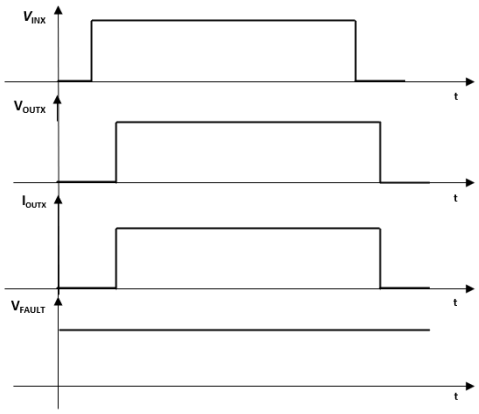


Figure 19. Switching on bulb lamp

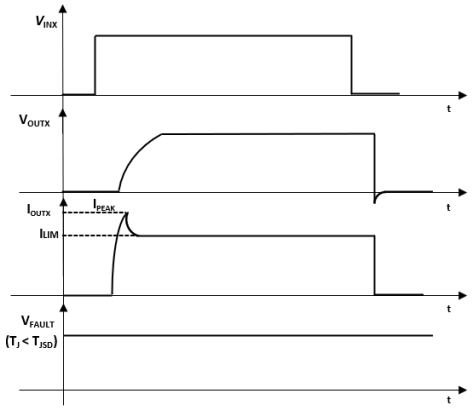


Figure 20. Switching on light inductive load

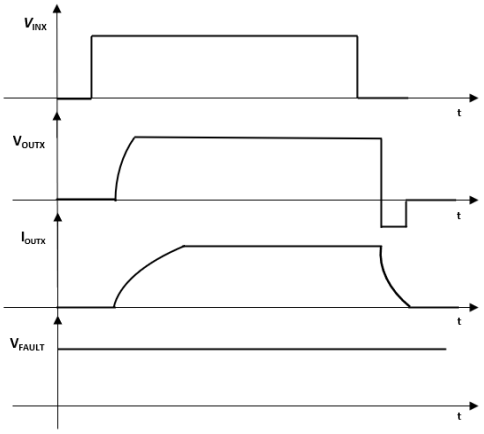


Figure 21. Switching on heavy inductive load

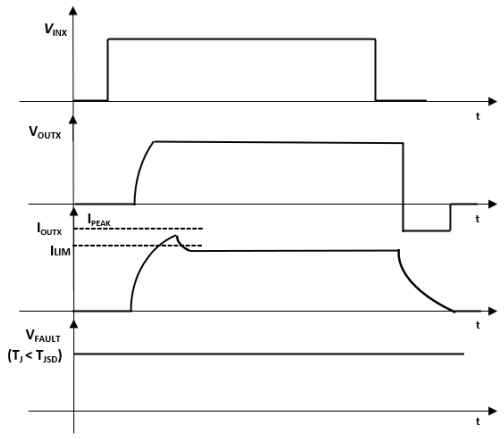


Figure 22. **Short-circuit (with OVT) during ON state**

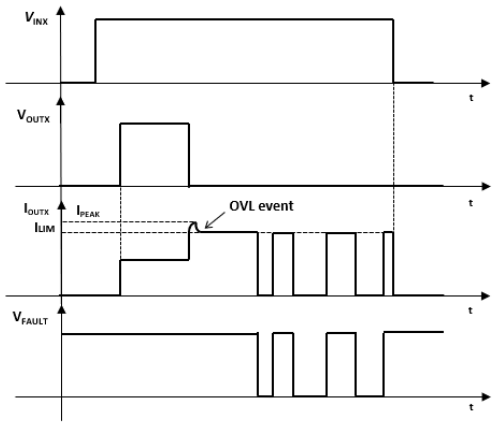
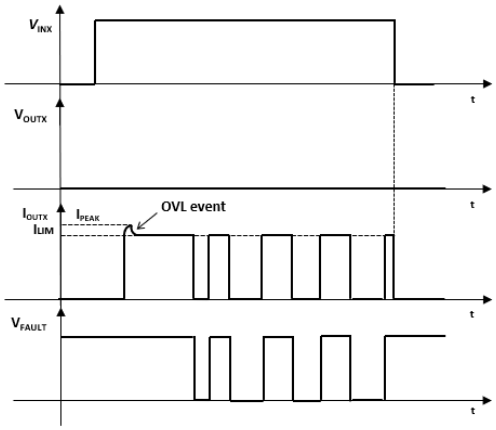


Figure 23. **Switching on short-circuit (with OVT)**



7.2 Thermal protection

The device is protected against overheating in case of overload conditions. During the driving period, if the output is overloaded, the device suffers two different thermal stresses, the former related to the junction, and the latter related to the case.

The two faults have different trigger thresholds: the junction protection threshold (T_{JSD}) is higher than the case protection one (T_{CSD}). Generally, the first protection that is activated in thermal stress conditions is the junction thermal shutdown. The output is turned off when the temperature is higher than the related threshold and turned back on when it goes below the reset threshold (T_{JR}). This behavior continues until the fault on the output is present.

If the thermal protection is active and the temperature of the package increases over the fixed case protection threshold, the case protection is activated and the output is switched off and back on when the junction temperature of each channel in fault and case temperature is below the respective reset thresholds.

Figure 24 shows the thermal protection behavior, while Figure 25 and Figure 26, reports typical temperature trends and output vs. input state.

Figure 24. **Thermal protection flowchart**

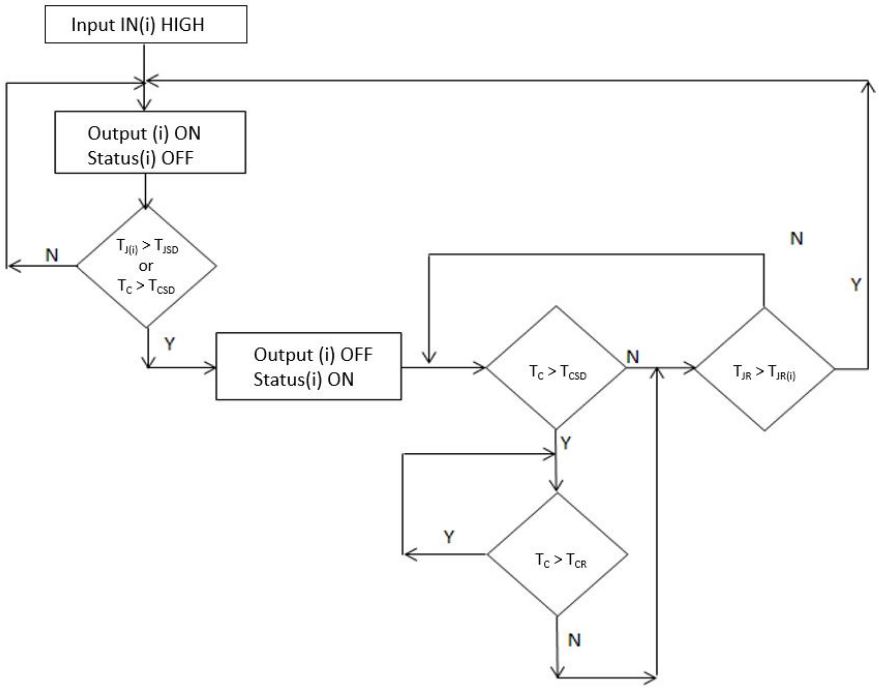


Figure 25. Thermal protection and fault behavior (T_{JSD} triggered before T_{CSD})

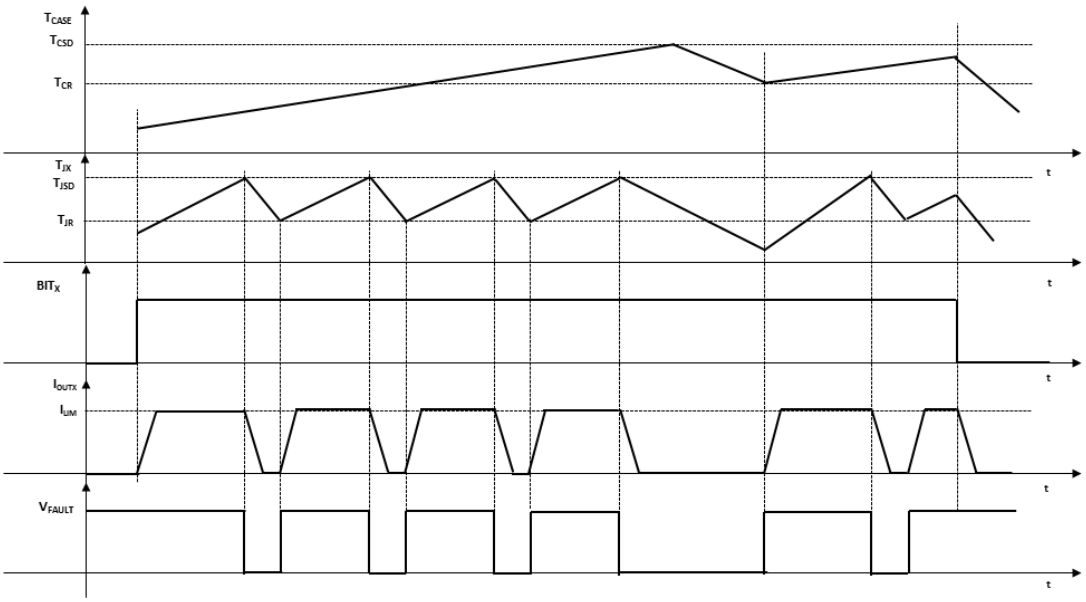
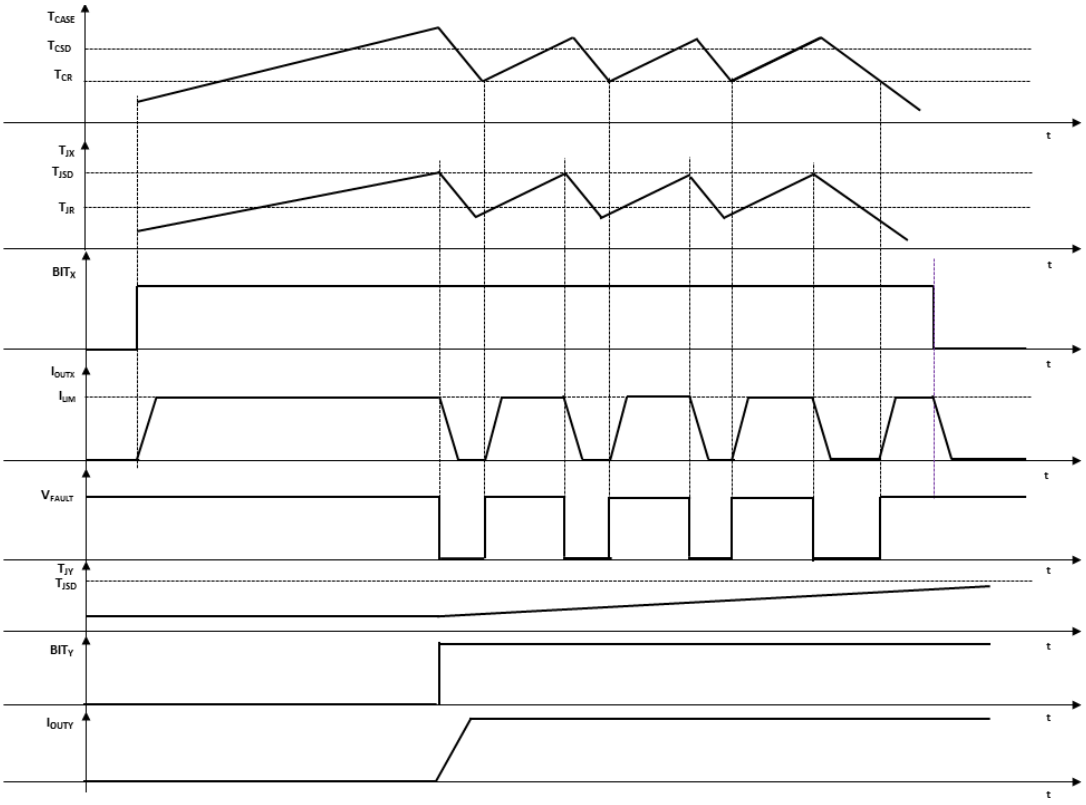


Figure 26. Thermal protection and fault behavior (T_{CSD} triggered before T_{JSD})



8 Reverse polarity protection

Reverse polarity protection can be implemented on board using two different solutions (or both, which is recommended):

1. Placing a resistor (R_{GND}) between IC GND pin and load GND
2. Placing a diode in parallel to a resistor between IC GND pin and load GND

If option 1 is selected, the minimum resistance value must be selected according to the following equation:

$$R_{GND} \geq \frac{V_{CC}}{I_{GND_{CC}}} \quad (1)$$

where $I_{GND_{CC}}$ is the DC reverse ground pin current and can be found in Table 2.

The power dissipated by R_{GND} during reverse polarity is:

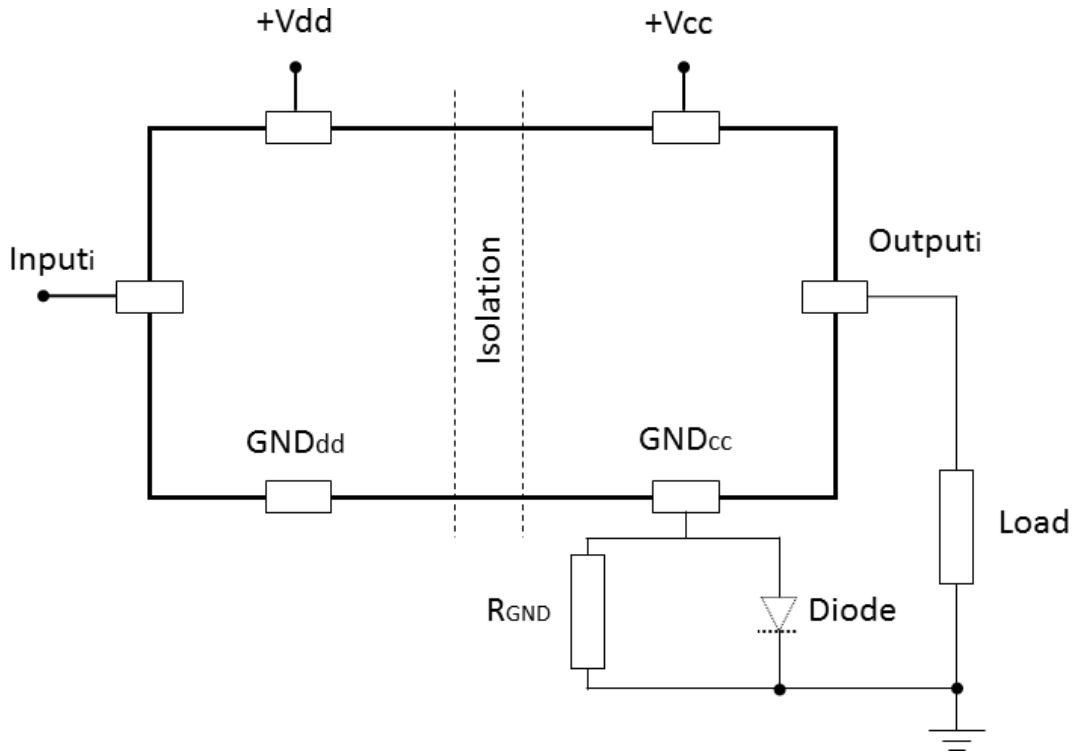
$$P_D = \frac{(V_{CC})^2}{R_{GND}} \quad (2)$$

If option 2 is selected, the diode has to be chosen by taking into account $V_{RRM} > |V_{CC}|$ and its power dissipation capability:

$$P_D \geq I_S \times V_F \quad (3)$$

*Note: In normal operation (no reverse polarity), there is a voltage drop (ΔV) between GND of the device and GND of the system. Using option 1, ΔV = Rgnd * Icc. Using option 2, ΔV = VF@(IF).*

Figure 27. Reverse polarity protection



Note: Input(i) is intended as any input pin on logic side.
This schematic can be used with any type of load.

9 Reverse polarity on V_{DD}

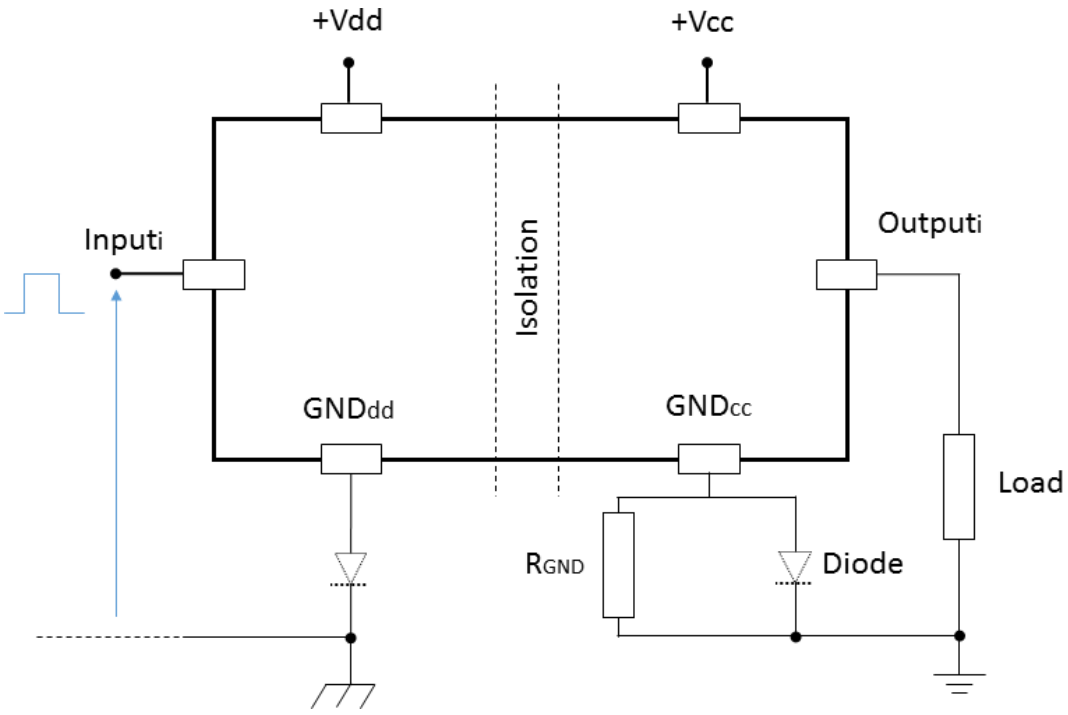
The reverse polarity on V_{DD} can be implemented on board by placing a diode between the GND_{DD} pin and GND digital ground.

The diode must be chosen by taking into account $V_{RRM} > |V_{DD}|$ and its power dissipation capability:

$$P_D \geq I_{DD} \times V_F \quad (4)$$

Note: In normal operation (no reverse polarity), due to the diode, there is a voltage drop (ΔV = VF@(Idd)) between GND_{DD} of the device and digital ground of the system. In order to guarantee to proper triggering of the input signal, ΔV(max.) must result lower than $V_{IH(MIN)}$.

Figure 28. Reverse polarity protection on V_{DD}



Note: Input(i) is intended as any input pin on logic side.

10 Demagnetization energy

Figure 29. Single pulse demagnetization energy vs. load current, typical values T_{amb}= 125 °C

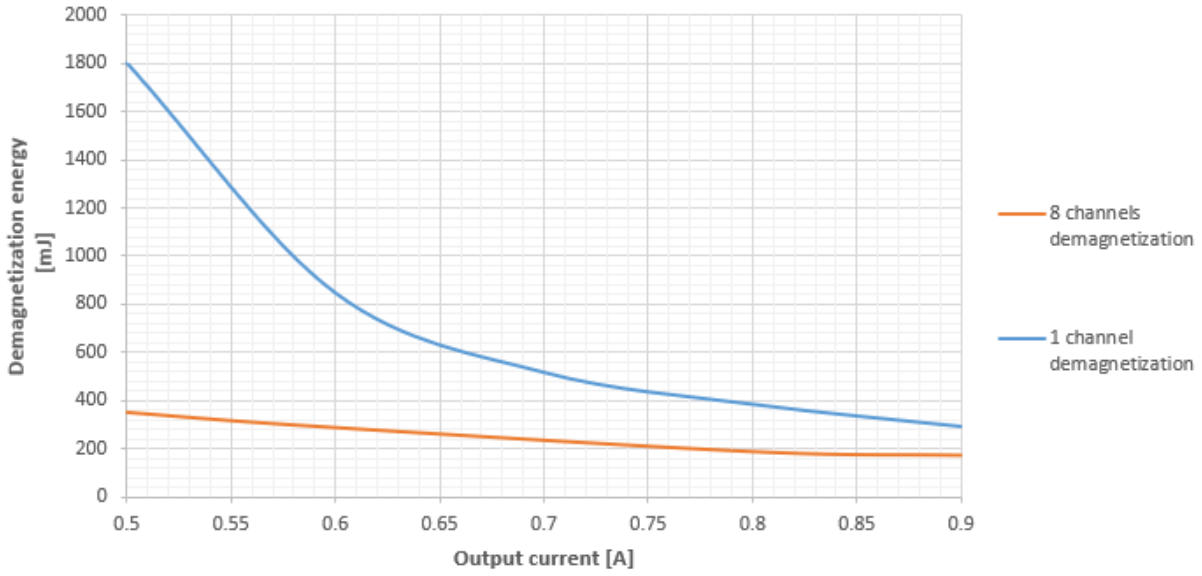


Figure 29 shows the single pulse (not repetitive) demagnetization capability per channel, according to the channels switched simultaneously

Figure 30. Single pulse inductive load capability vs. load current, typical values T_{amb}= 125 °C

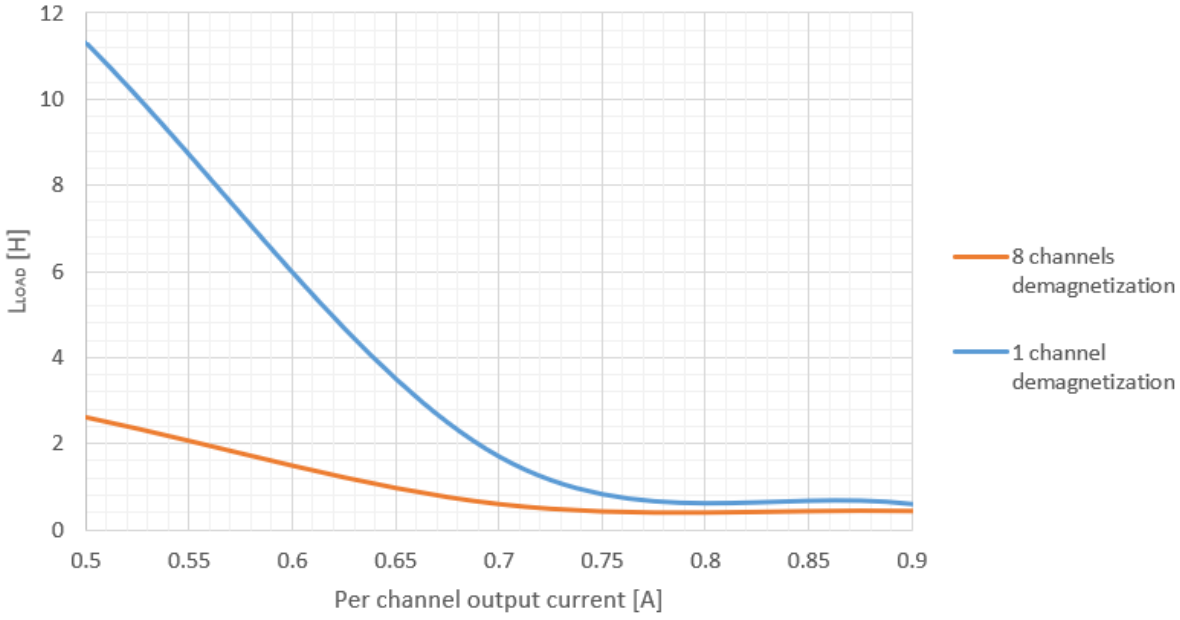


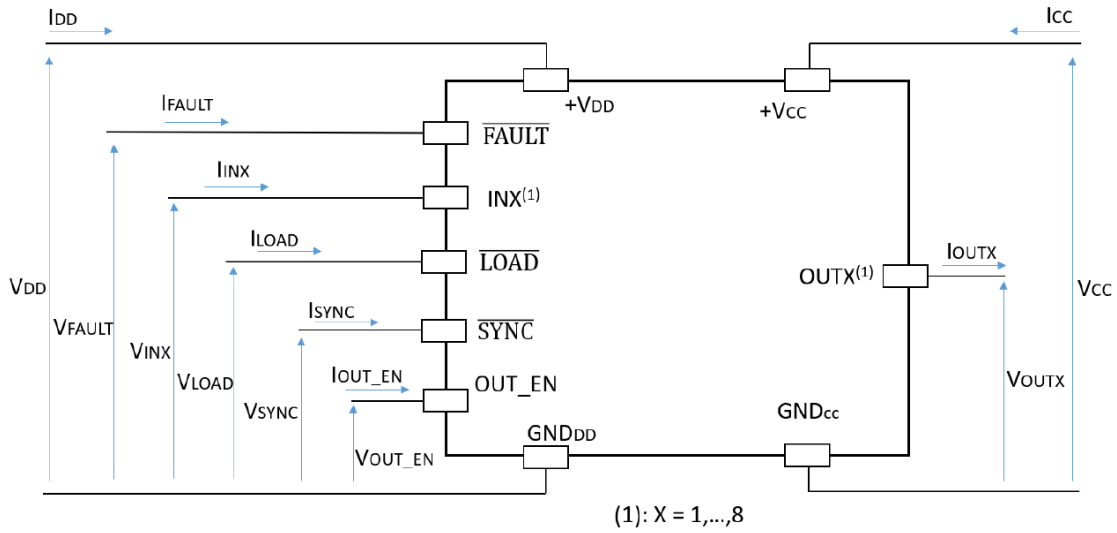
Figure 30 shows the single pulse (not repetitive) inductive load capability per channel, according to the channels switched simultaneously

11 Conventions

11.1 Supply voltage and power output conventions

Figure below shows the convention used in this paper for voltage and current usage.

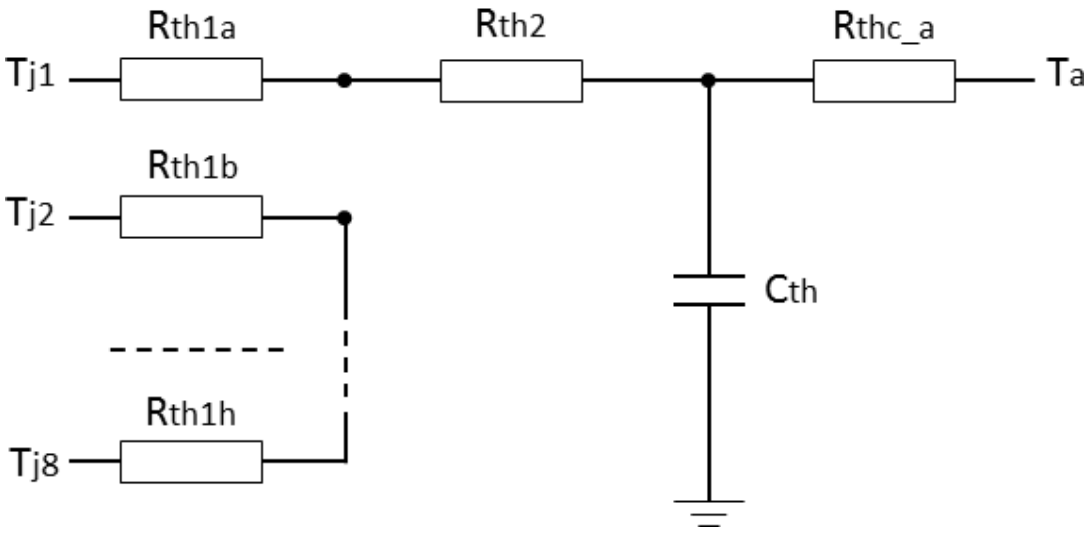
Figure 31. Supply voltage and power output conventions



12 Thermal information

12.1 Thermal impedance

Figure 32. **Simplified thermal model**



13 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

13.1 TFQFPN32 package information

Figure 33. TFQFPN32 package outline

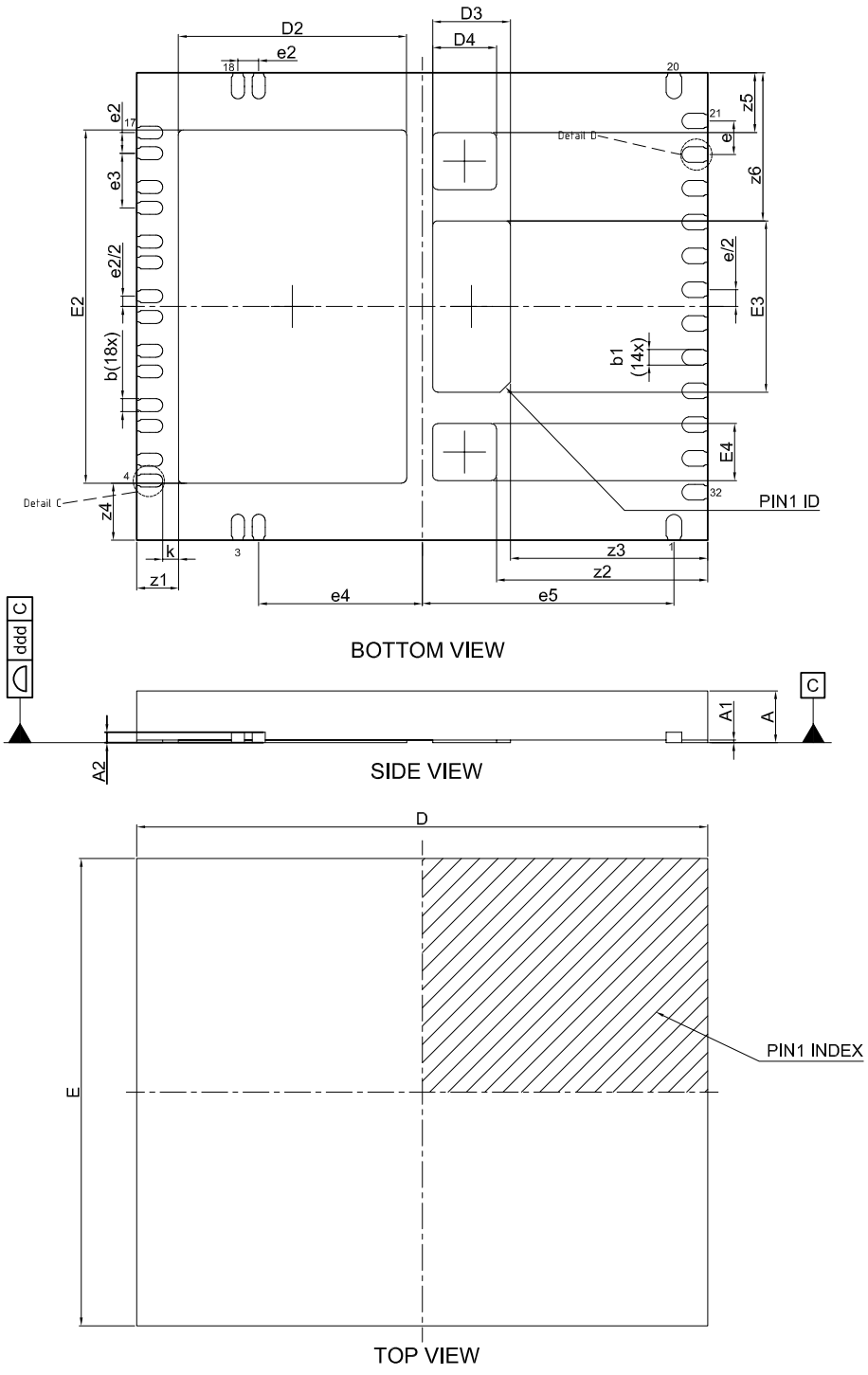


Figure 34. **TFQFPN32 package detail outline**

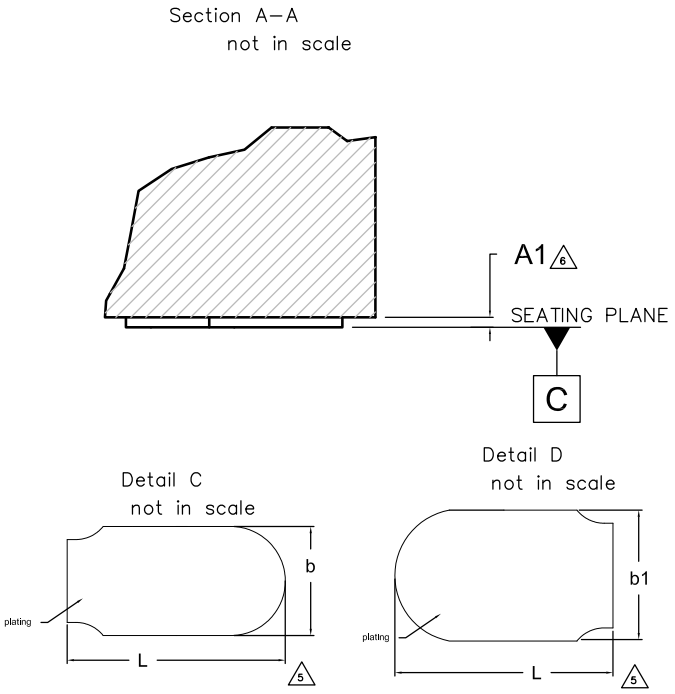


Figure 35. **TFQFPN32 suggested footprint (measured in mm)**

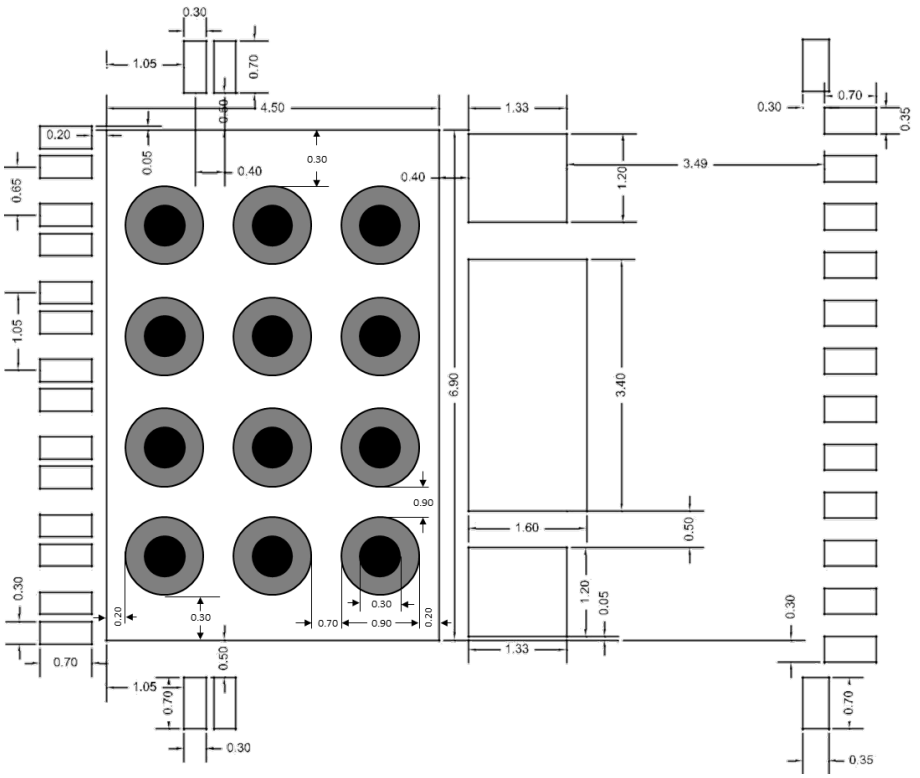


Table 17. TFQFPN32 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.95	1.00	1.05
A1	0	-	0.05
A2	-	0.20 REF	-
b (1)	0.20	0.25	0.30
b1(1)	0.25	0.30	0.35
D	10.90	11.0	11.10
E(1)	8.90	9.00	9.10
D2	4.30	4.40	4.50
E2	6.70	6.80	6.90
D3	1.40	1.50	1.60
E3	3.20	3.30	3.40
D4	1.13	1.23	1.33
E4	1.00	1.10	1.20
e	-	0.65	-
e2	-	0.40	-
e3	-	1.05	-
e4	-	3.15	-
e5	-	4.85	-
k	0	0.30	-
z1	-	0.80	-
z2	-	4.07	-
z3	-	3.80	-
z4	-	1.10	-
z5	-	1.15	-
z6	-	2.85	-
L(1)	0.45	0.50	0.55

1. *Dimensions “b” and “L” are measured on terminal plating surface.*

Table 18. Tolerance of form and position

Symbol	Tolerance of form and position	Definition	Notes
Aaa	0.15	The bilateral profile tolerance that controls the position of the plastic body sides. The centers of the profile zones are defined by the basic dimensions D and E.	-
Bbb	0.10	The tolerance that controls the position of the entire terminal pattern with respect to datums A and B. The center of the tolerance zone for each terminal is defined by the basic dimension "e" as related to datum's A and B.	-
Ccc	0.10	The tolerance located parallel to the seating plane in which the top surface of the package must be located.	-
ddd	0.08	The tolerance that controls the position of the terminals to each other. The centers of the profile zones are defined by basic dimension "e".	This tolerance is normally compounded with tolerance zone defined by bbb.
eee	0.08	The unilateral tolerance located above the seating plane where in the bottom surface of all terminals must be located.	This tolerance is commonly known as the "coplanarity" of the package terminals.
fff	0.10	The tolerance that controls the position of the exposed metal heat feature. The center of the tolerance zone will be datum's defined by the centerlines of the package body.	-
REF	-	-	No tolerance for A2

14 Packing information

14.1 TFQFPN32 packing information

Figure 36. **Tape and reel packing method concept**

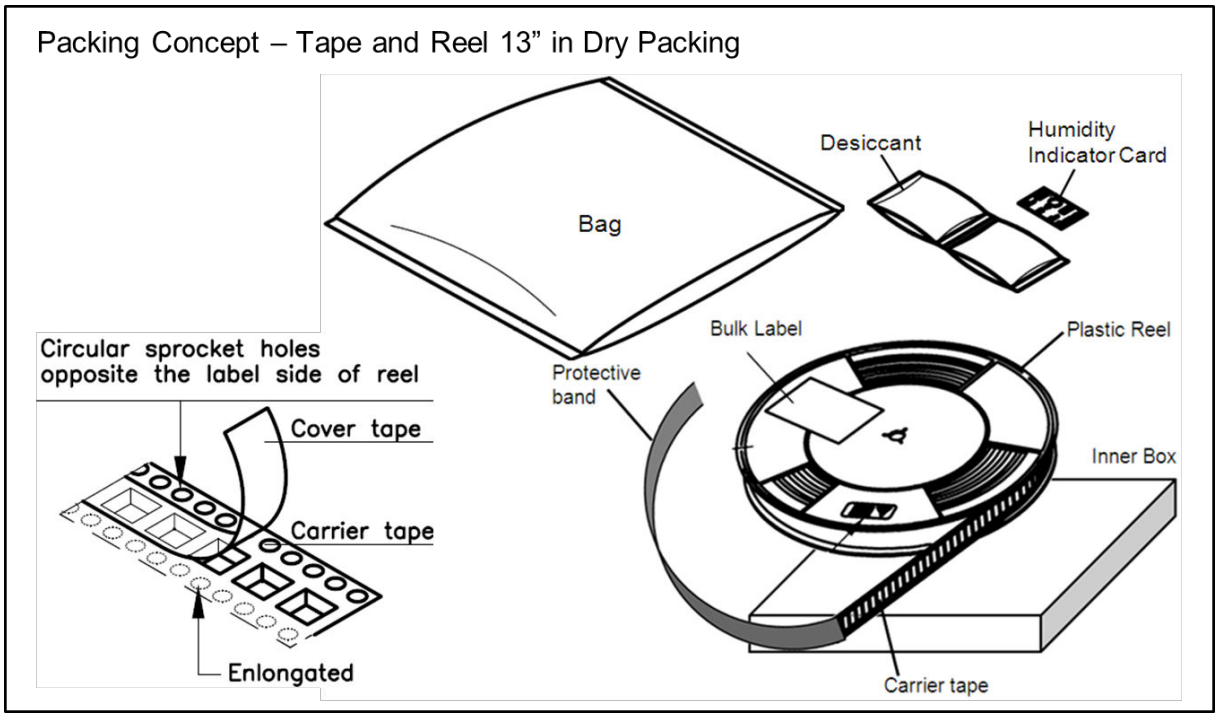


Figure 37. **Winding direction**

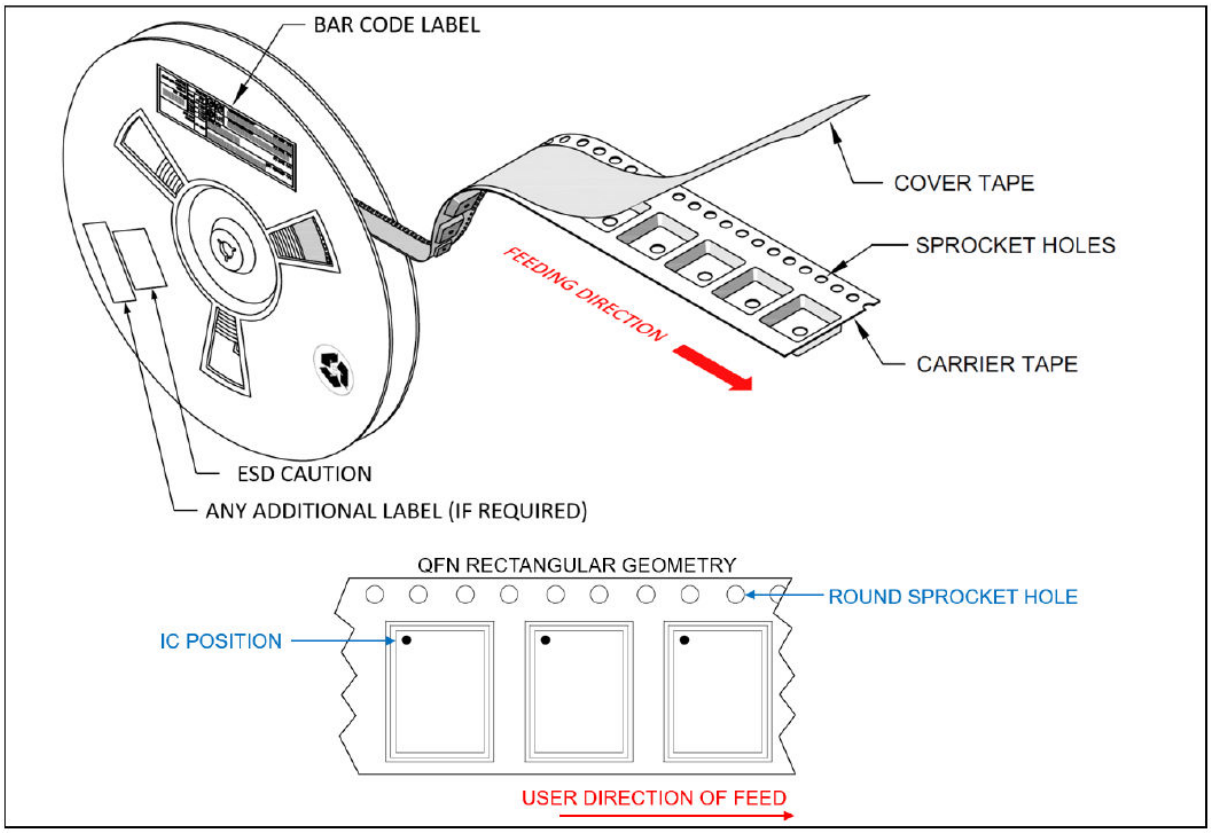
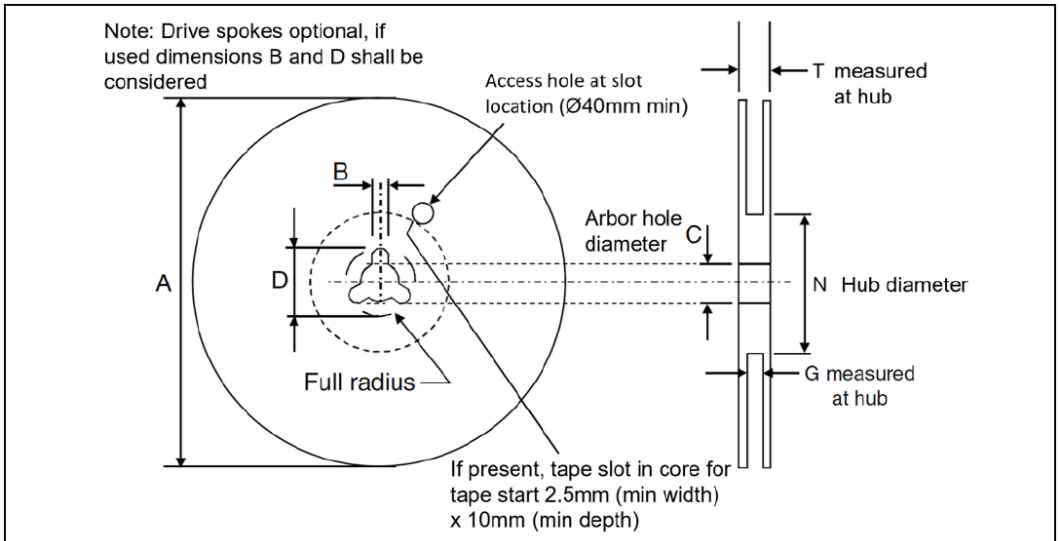
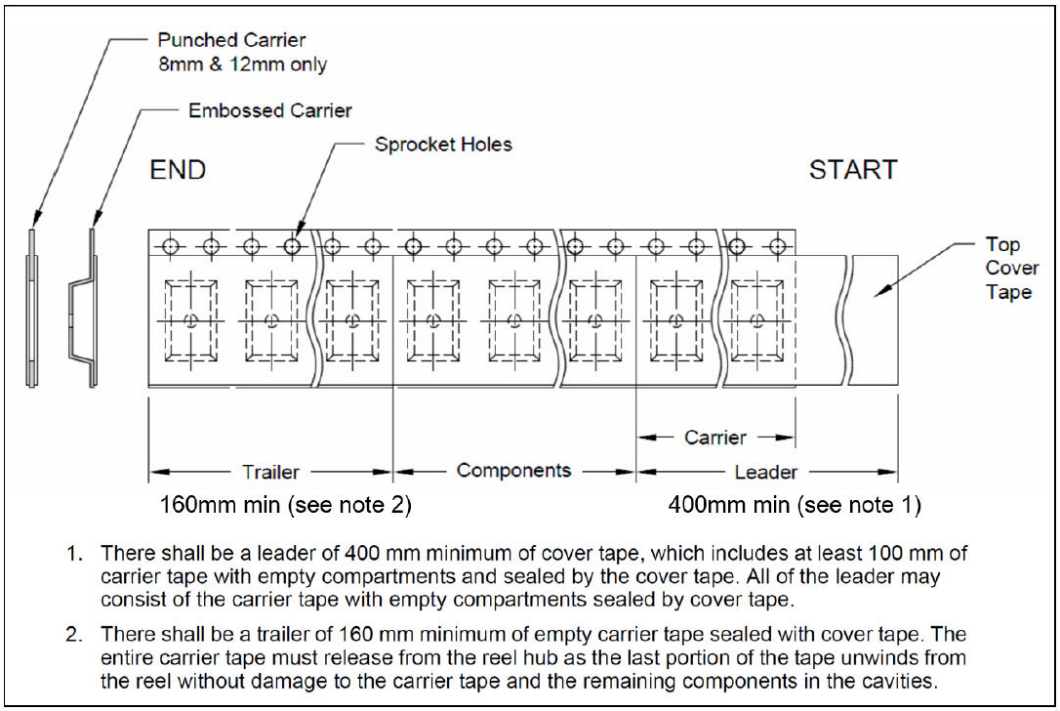


Figure 38. **Reel dimensions (as per EIA-481 specification)**



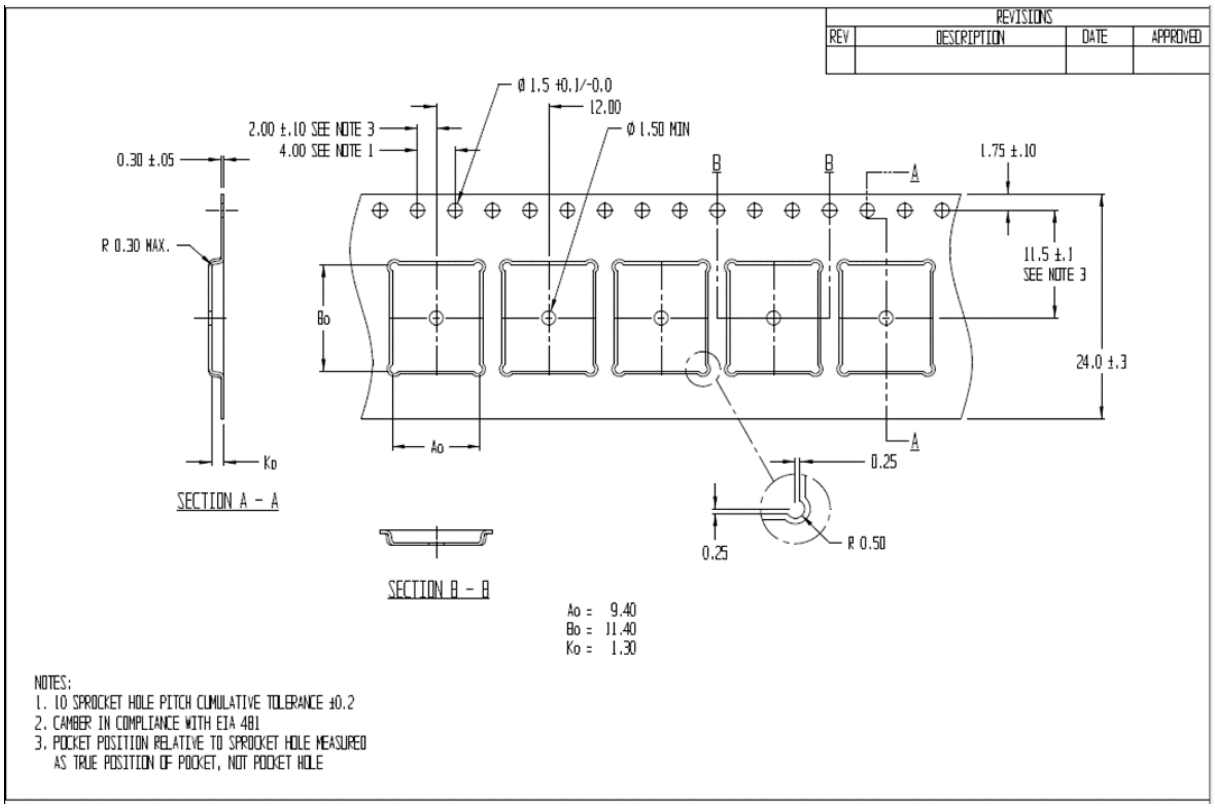
Tape width (mm)	(A) max Reel diameter (mm)	(B) min (mm)	(C) Center hole diameter (mm)	(D) min (mm)	(G) Reel thickness (mm)	(N) min Hub diameter (mm)	(T) max Total thickness (mm)
24	330 ± 2.0	1.5	13 + 0.5 -0.2	20.2	24.4 ± 2.0	100 ± 2.0	30.4

Figure 39. **Leader and Trailer dimensions (as per EIA-481 specification)**



1. There shall be a leader of 400 mm minimum of cover tape, which includes at least 100 mm of carrier tape with empty compartments and sealed by the cover tape. All of the leader may consist of the carrier tape with empty compartments sealed by cover tape.
2. There shall be a trailer of 160 mm minimum of empty carrier tape sealed with cover tape. The entire carrier tape must release from the reel hub as the last portion of the tape unwinds from the reel without damage to the carrier tape and the remaining components in the cavities.

Figure 40. **TFQFPN32 carrier tape**



15 Ordering information

Table 19. **Ordering information**

Order code	Package	Packing
ISO8200BQ	TFQFPN32	Tube
ISO8200BQTR	TFQFPN32	Tape and reel

Revision history

Table 20. **Document revision history**

Date	Revision	Changes
15-Dec-2014	1	Initial release.
10-Jun-2015	2	Updated Description. Updated Table 1. Updated E_{AS} max value in Table 2. Updated $V_{CC(THOFF)}$ and $V_{CC(hys)}$ min value in Table 4. Updated Table 5. Updated test conditions of I_{PEAK} , I_{LIM} and H_{yst} in Table 6. Changed Figure 21
17-Nov-2016	3	Datasheet promoted from preliminary to production data. Updated Table 6: Diagnostic pin and output protection function.
21-Apr-2017	4	Updated Table 10: “Insulation and safety-related specifications”. Minor text changes.
05-Oct-2017	5	Updated Table 11: "IEC 60747-5-2 insulation characteristics".
18-May-2018	6	Updated Section: Features on page 1. Replaced Vdd by VDD in whole document. Updated titles of Table 7 on page 11 and Table 9 on page 14. Updated titles of Figure 3 on page 12, Figure 5 on page 13, Figure 6 on page 13, Figure 20 on page 29 and Figure 21 on page 30. Added cross-reference to Section 6.2 in Table 13 on page 17. Updated Figure 9 on page 20 and Figure 11 on page 21 (replaced ISO8200B by ISO8200BQ). Added Section on page 34. Minor modifications throughout document.
24-Apr-2019	7	Added Table 12: Safety limits on page 15. Updated Table 2: Absolute maximum ratings on page 9. Updated Section: Features on page 1. Minor text changes.
18-Oct-2018	8	Updated Section: Features on page 1.
08-May-2020	9	Table 4, 11 and 16 updated. Figure 24 replaced. Table 17 added.
12-Jan-2024	10	Replaced the document with a newer format. Front page: written features section with a different arrangement and moved the description section a page ahead. Table 1: added footnote for OUT_X pins and fixed description for TAB(GND_{CC}) pin. Table 2: parameter V_{DD}, V_{IN} , V_{FAULT} reduced max value; renamed $-I_{OUT}$ as I_{RX} adding a footnote in the table. Table 3: Added a footnote regarding the maximum power dissipation. Table 4: added test condition description for parameters: $V_{CC(THON)}$, $V_{CC(THOFF)}$; added V_{CC} testing value for I_{CC}. Table 5: added test condition description for parameters: $V_{DD(THON)}$, $V_{DD(THOFF)}$. Table 7: re-arranged parameters and test conditions. Table 8: removed t_{WM} parameter. Table 9: removed $f_{refresh}$ parameter. Table 10 table with t_{WM} and $f_{refresh}$. Table 11: added footnote 1 and 2. Table 12: removed any reference to V_{IORM} parameter. In rev 9 Table 13 is removed. Figure 8 in rev 9 is replaced with Figure 8 and Figure 9 in rev 10. Added new Section 6.3.1 with Figure 15 and Section 6.5 with Table 16. Figure 16 in rev 9 is replaced with Figure 18, Figure 19, Figure 20, Figure 21, Figure 22, Figure 23 in rev 10. Added Figure 30 in Section 10. Throughout the document, replaced pictures (not changed) with new ones.

Contents

List of tables

List of figures