HOLT INTEGRATED CIRCUITS INC.

HI-8597

3.3V Single-Rail ARINC 429 Differential Line Driver with Integrated DO-160G Level 3 Lightning Protection

November 2023

GENERAL DESCRIPTION

The HI-8597 is a 3.3V single supply ARINC 429 line driver with built-in lightning protection. The internal lightning protection circuitry allows compliance with RTCA/DO-160G, Section 22 Level 3 Pin Injection Test Waveform Set A (3 & 4), Set B (3 & 5A) and Set Z (3 & 5B) without the use of any external components, an industry first. Pin surge levels for Level 3 are summarized as follows:

Waveform 3	Waveform 4	Waveform 5A	Waveform 5B
Voc/Isc	Voc/Isc	Voc/Isc	Voc/Isc
600V/24A	300V/60A	300V/300A	300V/300A

An internal 37.5 Ohm resistor on each output enables direct connection to the ARINC 429 bus.

In addition, the device includes a dual polarity voltage doubler, allowing it to operate from a single +3.3V supply using only four external capacitors.

Other features include high-impedance outputs (tri-state) when both data inputs are taken high, allowing multiple line drivers to be connected to a common bus.

Bus pins feature built-in 8kV ESD input protection (HBM), with 6kV capability on all other pins. All logic inputs are 5V or 3.3V compatible.

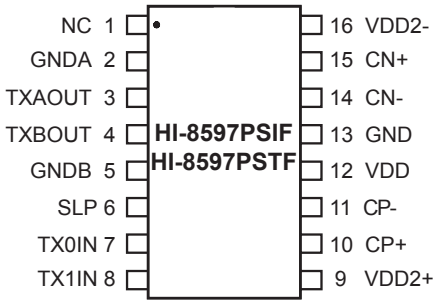
The HI-8597 line driver is intended for use where logic signals must be converted to ARINC 429 levels such as when using an FPGA or the HI-3586 ARINC 429 protocol IC. The single supply operation and internal lightning protection circuitry enable huge board space saving, making HI-8597 the most compact, cost effective ARINC 429 line driver on the market today.

The part is available in Industrial -40°C to +85°C, or Extended, -55°C to +125°C temperature ranges. Optional burn-in is available on the extended temperature range.

FEATURES

- Internal lightning protection circuitry allows compliance with RTCA/DO-160G, Section 22 Level 3 Pin Injection Test Waveform Set A (3 & 4), Set B (3 & 5A) and Set Z (3 & 5B).
- Operates from a single +3.3V supply
- Superb short circuit capability on ARINC 429 outputs (±50V for 1 second)
- All ARINC 429 voltage levels generated on-chip
- Digitally selectable rise and fall times
- Tri-state Outputs
- 37.5 Ohm output resistance allows direct connection to ARINC 429 bus
- Industrial and Extended temperature ranges
- Burn-in available

PIN CONFIGURATION (TOP VIEW)



16-Pin Plastic ESOIC package (Wide Body)

Table 1. Function Table

TX1IN	TX0IN	SLP	TXAOUT	TXBOUT	SLOPE
0	0	X	0V	0V	N/A
0	1	0	-5V	5V	10µs
0	1	1	-5V	5V	1.5µs
1	0	0	5V	-5V	10µs
1	0	1	5V	-5V	1.5µs
1	1	X	Hi-Z	Hi-Z	N/A

BLOCK DIAGRAM

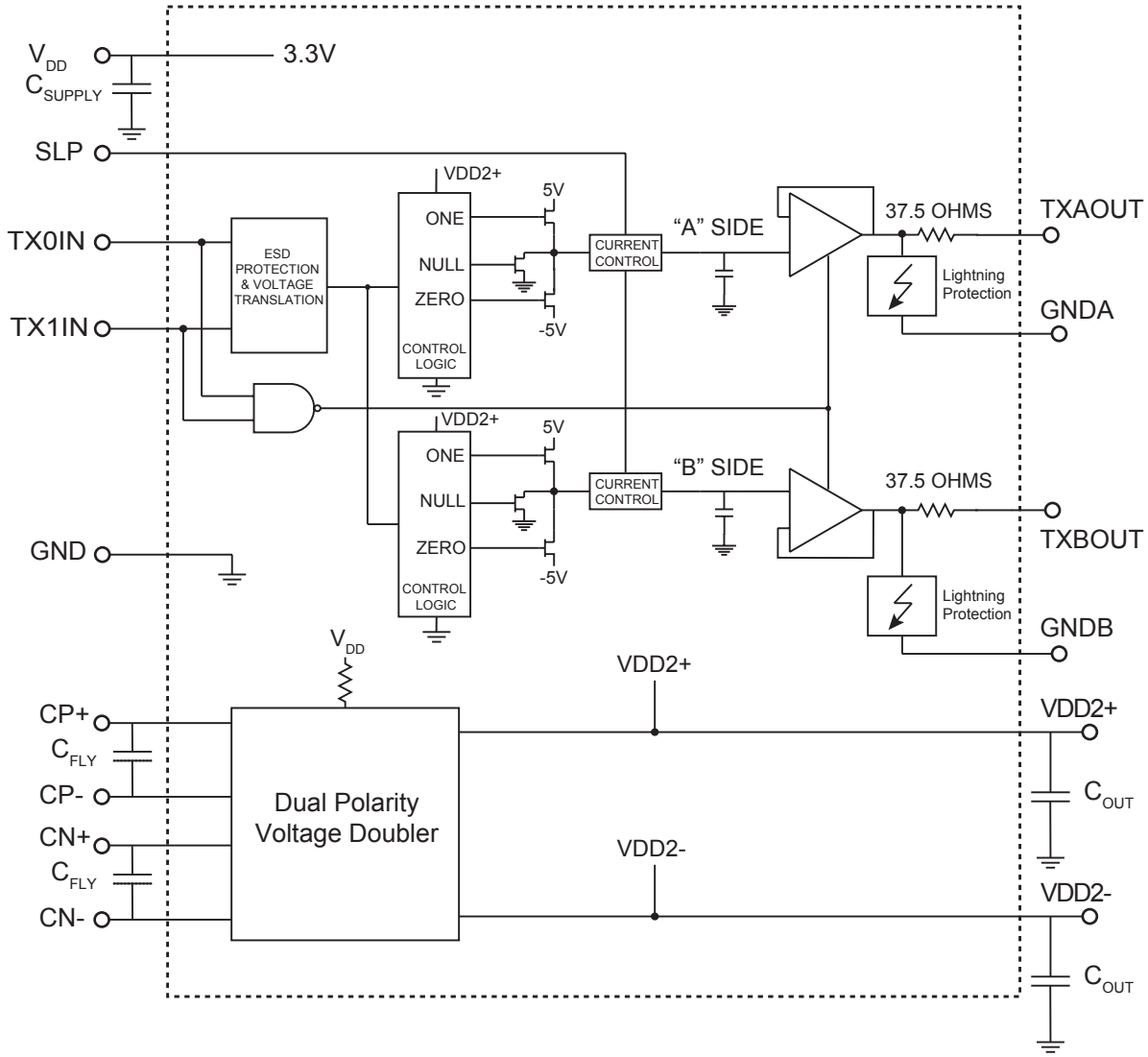


Figure 1. HI-8597 Block Diagram

PIN DESCRIPTIONS

Table 2. Pin Descriptions

Pin No.	Pin Name	Function	Description
1	NC	None	No connect.
2	GNDA	POWER	Ground connection of internal lightning protection circuitry for ARINC high output. MUST be tied to chip ground pin, GND.
3	TXAOUT	OUTPUT	ARINC high output with 37.5 Ohms series resistance
4	TXBOUT	OUTPUT	ARINC low output with 37.5 Ohms series resistance
5	GNDB	POWER	Ground connection of internal lightning protection circuitry for ARINC low output. MUST be tied to chip ground pin, GND.
6	SLP	INPUT	Output slew rate control. High selects ARINC 429 high-speed. Low selects ARINC 429 low-speed.
7	TX0IN	INPUT	Data input zero
8	TX1IN	INPUT	Data input one
9	V_{DD2+}	OUTPUT	Voltage doubler positive output (~6.25V for 3.3V supply)
10	CP+	ANALOG	V_{DD2+} flyback capacitor, C_{FLY}; positive terminal
11	CP-	ANALOG	V_{DD2+} flyback capacitor, C_{FLY}; negative terminal
12	V_{DD}	POWER	+3.3V power supply
13	GND	POWER	Ground supply
14	CN-	ANALOG	V_{DD2-} flyback capacitor, C_{FLY}; negative terminal
15	CN+	ANALOG	V_{DD2-} flyback capacitor, C_{FLY}; positive terminal
16	V_{DD2-}	OUTPUT	Voltage doubler negative output (~ -6.1V for 3.3V supply)

FUNCTIONAL DESCRIPTION

Figure 1 shows a block diagram of the line driver. The HI-8597 is internally lightning protected in compliance with RTCA/DO-160G, Section 22 Level 3 Pin Injection Test Waveform Set A (3 & 4), Set B (3 & 5A) and Set Z (3 & 5B). The waveforms are shown in Figure 5 through Figure 7. The device requires only a single +3.3V power supply. An integrated inverting / non-inverting voltage doubler generates the rail voltages (±6.6V) which are then used to produce the ±5V ARINC-429 output levels.

The internal dual polarity charge pump circuit requires four external capacitors, two for each polarity generated by the doubler. CP+ and CP- connect the external charge transfer or "fly" capacitor, C_{FLY}, to the positive portion of the doubler, resulting in twice V_{DD} at the V_{DD2+} pin. An output "hold" capacitor, C_{OUT}, is placed between V_{DD2+} and GND. C_{OUT} should be ten times the size of C_{FLY}. The inverting or negative portion of the converter works in a similar fashion, with C_{FLY} and C_{OUT} placed between CN+ / CN- and V_{DD2-} / GND respectively.

Currents for slope control are set by on-chip resistors.

The TX0IN and TX1IN inputs receive logic signals from a control transmitter chip such as the HI-3584 or HI-3586. TXAOUT and TXBOUT hold each side of the ARINC bus at Ground until one of the inputs becomes a One. If for example TX1IN goes high, a charging path is enabled to 5V on an "A" side internal capacitor while the "B" side is enabled to -5V. The charging current is selected by the SLP pin. If the SLP pin is high, the capacitor is nominally charged from 10% to 90% in 1.5µs. If SLP is low, the rise and fall times are 10µs.

A unity gain buffer receives the internally generated slopes and differentially drives the ARINC line. Current is limited by the series output resistors at each pin. There are no fuses at the outputs of the HI-8597.

The HI-8597 has 37.5 ohms in series with each TXOUT output, allowing direct connection to the ARINC 429 bus. The outputs are automatically lightning protected in compliance with RTCA/DO-160G, Section 22 Level 3 Pin Injection Test Waveform Set A (3 & 4), Set B (3 & 5A) and Set Z (3 & 5B) without any external components.

Tri-stateable outputs allow multiple line drivers to be connected to the same ARINC 429 bus. Setting TX1IN and TX0IN both to a logic "1" puts the outputs in the high-impedance state.

PACKAGE HEAT SINK

The HI-8597 package includes a metal heat sink located on the bottom surface of the device. The heat sink is electrically isolated and may be optionally soldered to any convenient power or ground plane for optimum thermal dissipation.

ABSOLUTE MAXIMUM RATINGS

Supply Voltages
V_{DD} ..... +5V
Junction Temperature (T_{JMAX}) ..... 175°C
Solder Temperature (reflow) ..... 260°C
Storage Temperature ..... -65°C to +150°C

RTCA/DO-160G, Section 22 pin injection	
Waveform	Voc/Isc
3	800V/32A
4	375V/75A
5A	375V/375A
5B	375V/375A

RECOMMENDED OPERATING CONDITIONS

Supply Voltages
V_{DD} ..... +3.0V to +3.6V
Temperature Range
Industrial Screening ..... -40°C to +85°C
Hi-Temp Screening ..... -55°C to +125°C

NOTE: Stresses above absolute maximum ratings or outside recommended operating conditions may cause permanent damage to the device. These are stress ratings only. Operation at the limits is not recommended.

ELECTRICAL CHARACTERISTICS

Table 3. DC Electrical Characteristics

V_{DD} = +3.3V, T_A = Operating Temperature Range (unless otherwise stated)

Parameters	Symbol	Test Conditions	Min	Typ	Max	Units
Input Voltage (TX1IN, TX0IN, SLP)						
High	V_{IH}		$0.7V_{DD}$	-	-	V
Low	V_{IL}		-	-	$0.3V_{DD}$	V
Input Current (TX1IN, TX0IN, SLP)		(73kΩ Internal Pulldown)				
	I_{IH}	V_{IN} = 3.3V	-	45	-	µA
	I_{IL}	V_{IN} = 0V	-	-	-0.1	µA
ARINC Output Voltage (Differential)						
one	V_{DIFF1}	no load; TXAOUT - TXBOUT	9	10	11	V
zero	V_{DIFF0}	no load; TXAOUT - TXBOUT	-11	-10	-9	V
null	V_{DIFFN}	no load; TXAOUT - TXBOUT	-0.5	0	0.5	V
ARINC Output Voltage (Ref. to GND)						
one or zero	V_{DOUT}	no load & magnitude at pin	4.5	5.0	5.5	V
null	V_{NOUT}	no load	-0.25	0	0.25	V
Operating Supply Current		SLP = V_{DD}				
No load	I_{DDNL}	TX1IN & TX0IN = 0V	-	28	40	mA
Max. Load	I_{DDL}	100kHz, 400Ω load	-	65	-	mA
ARINC Outputs Shorted	I_{DDS}	See Note 1	-	165	-	mA
Power Dissipation in device[2]		SLP = V_{DD}				
No load	P_{DDNL}	TX1IN & TX0IN = 0V	-	93	132	mW
Max. Load (TXAOUT to TXBOUT)	P_{DDLT}	100kHz, 400Ω load	-	215	-	mW
ARINC Outputs Shorted (TXOUT outputs)	P_{DDST}	See Note 1	-	545	-	mW
ARINC Output Impedance	Z_{OUT}					
TXOUT pins			35	37.5	40	Ohms
ARINC Output Tri-State Current	I_{OZ}	TX0IN = TX1IN = V_{DD}, T_A = 25ºC -5.5V < V_{OUT} < +5.5V	-200		200	µA
ARINC Output Tri-State Voltage	V_{OZ}	TX0IN = TX1IN = V_{DD}, T_A = 25ºC -150µA < I_{OUT} < +150µA	-5.5	-	+5.5	V

Note 1: TXAOUT and/or TXBOUT shorted to each other or ground.

Note 2: Estimate junction temperature using Theta JB or Theta JA values available on Holt's website, www.holtic.com. $T_J \leq T_{JMAX}$.

Table 4. Converter Characteristics

V_{DD} = +3.3V, T_A = Operating Temperature Range (unless otherwise stated)

Parameters	Symbol	Test Conditions	Min	Typ	Max	Units
Start-up transient (V+, V-)	t_{START}		-	-	10	ms
Operating Switching Frequency	f_{sw}		-	650	-	kHz
Worst case maximum voltage doubler output	$V_{DD2+(max)}$	V_{DD} = 3.6V. T = -55ºC. Open load.			6.93	V
DC/DC convertor capacitor recommendations. **For optimum performance use typical (not min.) values. For EMC compliance, see AN-135.**						
Ratio of bulk storage to fly-back capacitors	C_{OUT} / C_{FLY}		2.2	10		
Fly-back capacitor (Recommend ceramic, preferably multilayer, dielectric XR7 caps, 10V min.).	C_{FLY} $C_{FLY(ESR)}$	C_{OUT} / C_{FLY} >= 10 [0.5, 1.0]Mhz	1.0	4.7	- 500	µF mΩ
Bulk storage capacitor (Recommend ceramic, preferably multilayer, dielectric XR7 caps, 10V min.).	C_{OUT} $C_{OUT(ESR)}$	C_{OUT} / C_{FLY} >= 10 [0.5, 1.0]Mhz	2.2	47	- 300	µF mΩ
By-pass capacitor (Recommend ceramic cap, 10V min.).	C_{SUPPLY}	C_{SUPPLY} >= C_{OUT} (connect from V_{DD} to GND)				

Table 5. AC Electrical Characteristics

V_{DD} = +3.3V, T_A = Operating Temperature Range (unless otherwise stated)

Parameters	Symbol	Test Conditions	Min	Typ	Max	Units
Line Driver Propogation Delay						
Output high to low	t_{phlx}	defined in Figure 2, no load	-	500	-	ns
Output low to high	t_{plhx}		-	500	-	ns
Line Driver Transition Times						
High Speed		SLP pin = Logic “1”				
Output high to low	t_{fx}		1.0	1.5	2.0	µs
Output low to high	t_{rx}		1.0	1.5	2.0	µs
Low Speed		SLP pin = Logic “0”				
Output high to low	t_{fx}		5.0	10.0	15.0	µs
Output low to high	t_{rx}		5.0	10.0	15.0	µs
Input Capacitance (Logic)[1]	C_{IN}		-	-	10	pF
Output Capacitance (Tri-state)[1]	C_{OUT}	TX0IN = TX1IN = V_{DD}	-	-	10	pF

Notes: 1. Guaranteed but not tested

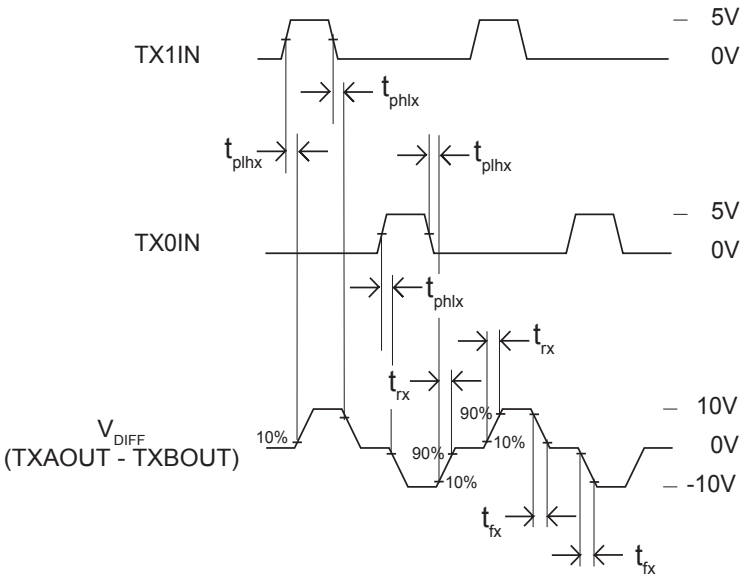


Figure 2. Line Driver Timing

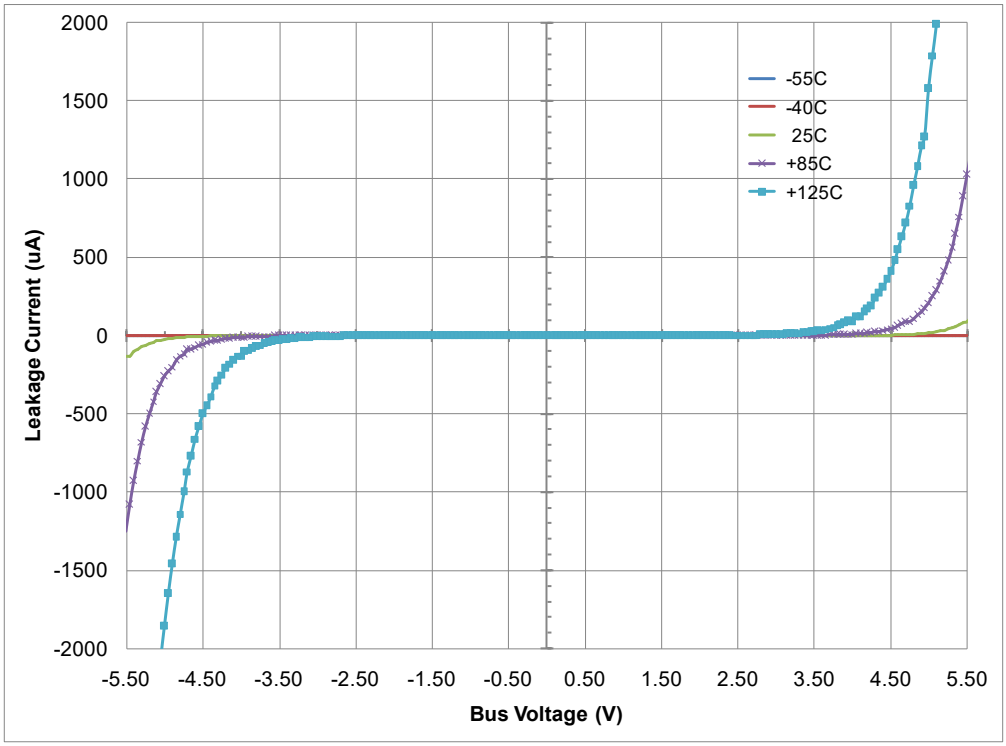


Figure 3. Tri-State Leakage Current vs Bus Voltage at Temperature.

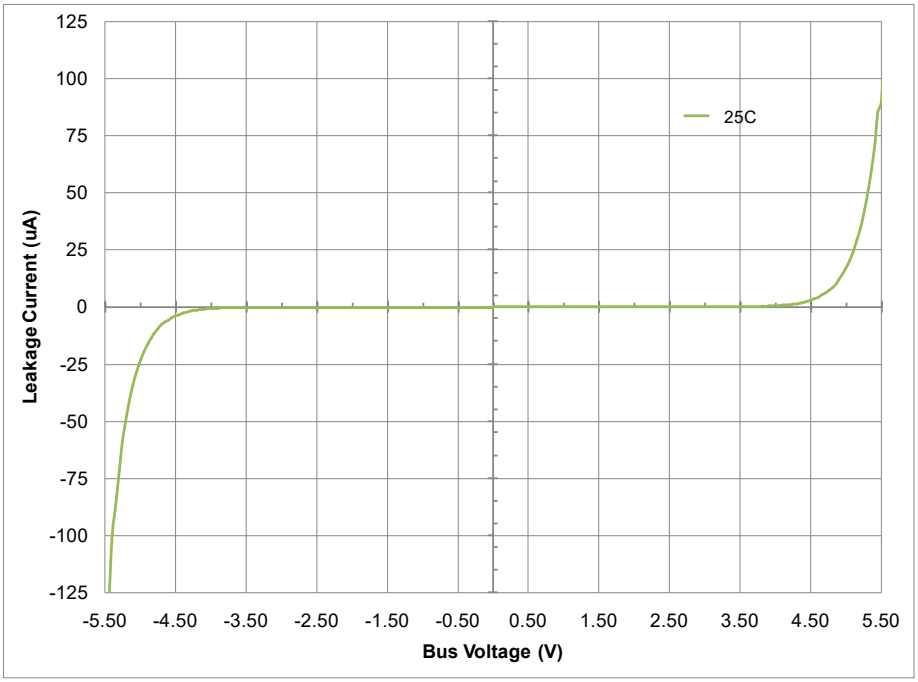


Figure 4. Tri-State Leakage Current vs Bus Voltage at Room Temperature.

LIGHTNING INDUCED TRANSIENT VOLTAGE WAVEFORMS

Waveform 3.

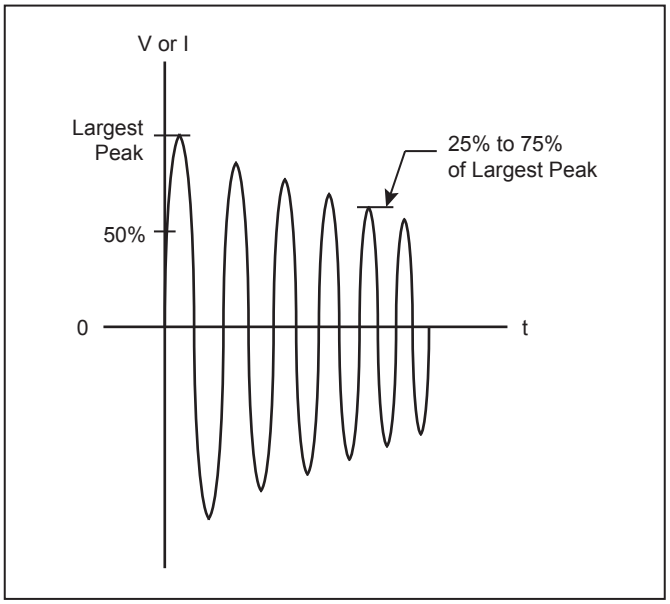


Figure 5. DO-160G Lightning Induced Transient Voltage Waveform 3.
Voc = 600V, Isc = 24A, Frequency = 1MHz ± 20%.

Waveform 4.

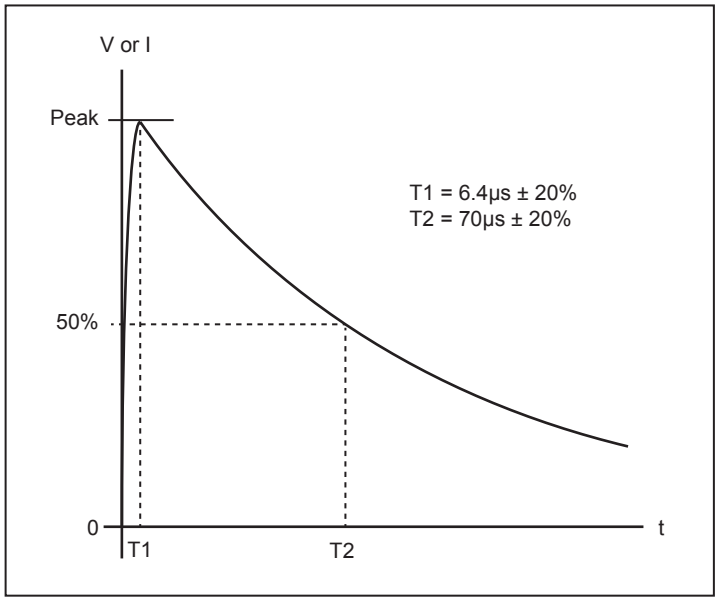


Figure 6. DO-160G Lightning Induced Transient Voltage Waveform 4.
Voc = 300V, Isc = 60A.

Waveform 5.

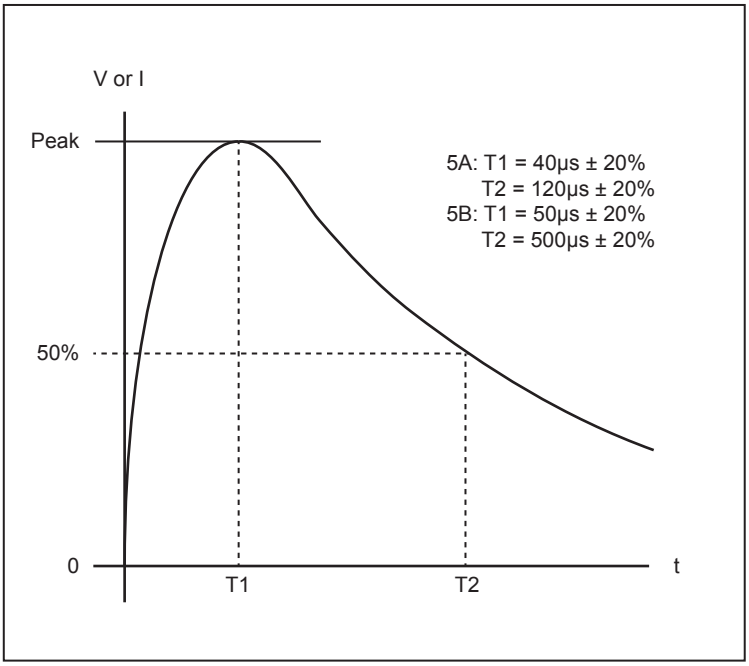


Figure 7. DO-160G Lightning Induced Transient Voltage Waveforms 5A and 5B.
Voc = 300V, Isc = 300A.

ORDERING INFORMATION

HI - 8597PS x F (Plastic)

PART NUMBER	LEAD FINISH
F	100% Matte Tin (Pb-free, RoHS compliant)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C to +85°C	I	No
T	-55°C to +125°C	T	No
M	-55°C to +125°C	M	Yes

PART NUMBER	PACKAGE DESCRIPTION
8597PS	16 PIN PLASTIC SMALL OUTLINE - WB SOIC (16HWE)

REVISION HISTORY

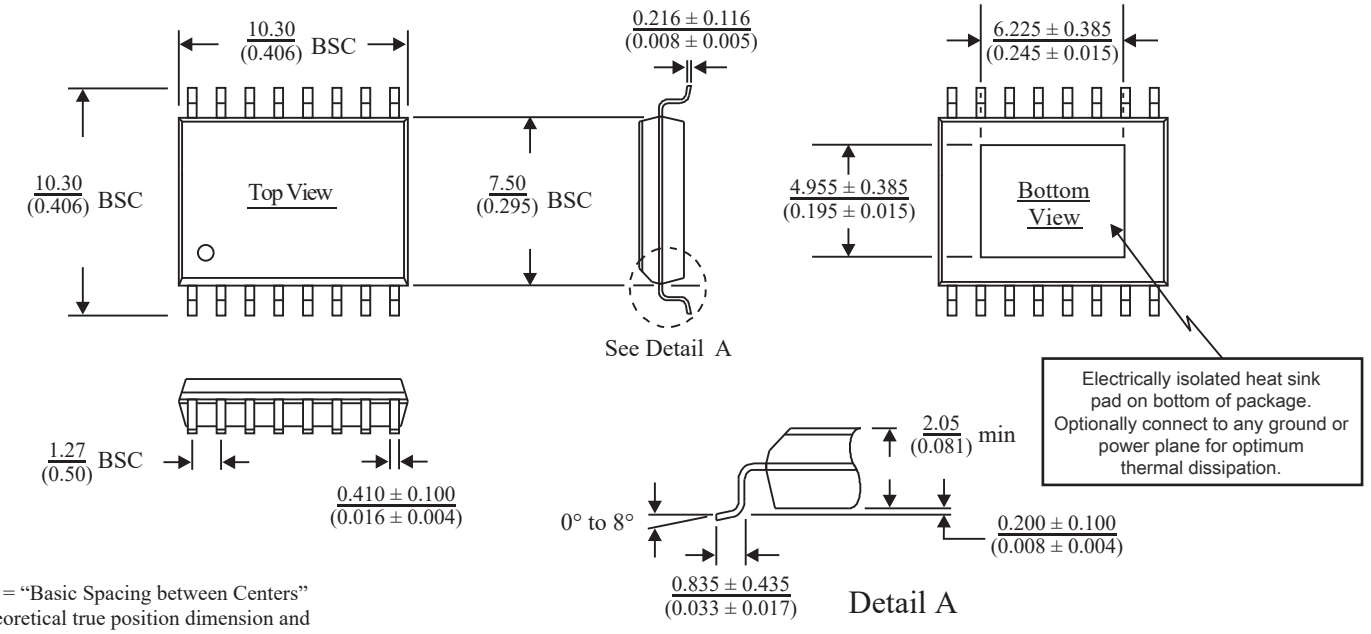
Revision	Date	Description of Change
DS8597, Rev. New	11/9/12	Initial Release
Rev. A	12/11/12	Clarify operating supply current for shorted ARINC outputs.
Rev. B	01/21/13	Change “VSS” pin label to “GND” and “-” to “NC” for clarification. Add pin numbers to Pin Description table. Rephrase “guarantees” compliance with DO-160G Level 3 to “allows” compliance with DO-160G Level 3. Update tri-state leakage parameter to 200µA. Add Absolute Maximum Ratings for lightning waveforms.
Rev. C	03/14/13	Remove erroneous references to AMPA and AMPB outputs in footnote on page 5.
Rev. D	05/08/13	Corrected state of SLP pin and erroneous reference to pin 1 in Test Conditions for Line Driver Transition Times (see AC Characteristics Table).
Rev. E	06/13/13	Update operating supply current.
Rev. F	07/19/13	Update operating supply current from 85mA to 100mA max.
Rev. G	10/02/14	Correct converter caps ESR values to be maximum instead of minimum. Update 16HWE package drawing.
Rev. H	12/09/14	Update Operating Supply Current and ARINC Output Impedance in “Table 3. DC Electrical Characteristics”.
Rev. I	01/21/15	Delete Max. Power Dissipation in Absolute Maximum Ratings table. Add Max. Junction Temperature to table. Add Device Power Dissipation to DC Electrical Characteristics in Table 3. Recommend ceramic converter caps only (no tantalum) in “Converter Characteristics”.
Rev. J	07/22/15	Clarify Load condition for Power Dissipation in DC Electrical Characteristics in Table 3.
Rev. K	02/21/17	Clarify ordering information. Only lead-free option offered in 16-pin WB SOIC.
Rev. L	11/18/2021	Add note on soldering of package heat sink.
Rev. M	11/29/2021	Add note to package drawing on soldering of package heat sink.
Rev. N	07/08/2022	Clarify test conditions for I_{IH} and I_{IL} parameters.
Rev. P	11/30/2023	Correct typo in Input Current pulldown resistor value on TX1IN, TX0IN and SLP pins.

PACKAGE DIMENSIONS

16-PIN PLASTIC SMALL OUTLINE (ESOIC) - WB
(Wide Body, Thermally Enhanced)

millimeters (inches)

Package Type: 16HWE



BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)