

MIXED SIGNAL MICROCONTROLLER

FEATURES

- Low Supply Voltage Range 1.8 V to 3.6 V
- Ultra-Low Power Consumption
 - Active Mode: 220 μ A at 1 MHz, 2.2 V
 - Standby Mode: 0.5 μ A
 - Off Mode (RAM Retention): 0.1 μ A
- Five Power-Saving Modes
- Ultra-Fast Wake-Up From Standby Mode in Less Than 1 μ s
- 16-Bit RISC Architecture, 62.5-ns Instruction Cycle Time
- Basic Clock Module Configurations:
 - Internal Frequencies up to 16 MHz With Four Calibrated Frequencies to $\pm 1\%$
 - Internal Very Low-Power Low-Frequency Oscillator
 - 32-kHz Crystal
 - External Digital Clock Source
- 16-Bit Timer_A With Two Capture/Compare Registers
- On-Chip Comparator for Analog Signal Compare Function or Slope A/D (MSP430F20x1)
- 10-Bit 200-ksps A/D Converter With Internal Reference, Sample-and-Hold, and Autoscan (MSP430F20x2)
- 16-Bit Sigma-Delta A/D Converter With Differential PGA Inputs and Internal Reference (MSP430F20x3)
- Universal Serial Interface (USI) Supporting SPI and I2C (MSP430F20x2 and MSP430F20x3)
- Brownout Detector
- Serial Onboard Programming, No External Programming Voltage Needed, Programmable Code Protection by Security Fuse
- On-Chip Emulation Logic With Spy-Bi-Wire Interface
- Family Members:
 - MSP430F2001
 - 1KB + 256B Flash Memory
 - 128B RAM
 - MSP430F2011
 - 2KB + 256B Flash Memory
 - 128B RAM
 - MSP430F2002
 - 1KB + 256B Flash Memory
 - 128B RAM
 - MSP430F2012
 - 2KB + 256B Flash Memory
 - 128B RAM
 - MSP430F2003
 - 1KB + 256B Flash Memory
 - 128B RAM
 - MSP430F2013
 - 2KB + 256B Flash Memory
 - 128B RAM
- Available in 14-Pin Plastic Small-Outline Thin Package (TSSOP), 14-Pin Plastic Dual Inline Package (PDIP), and 16-Pin QFN
- For Complete Module Descriptions, See the *MSP430x2xx Family User's Guide* ([SLAU144](#))

DESCRIPTION

The Texas Instruments MSP430 family of ultra-low-power microcontrollers consist of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low-power modes is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 1 μ s.

The MSP430F20xx series is an ultra-low-power mixed signal microcontroller with a built-in 16-bit timer and ten I/O pins. In addition, the MSP430F20x1 has a versatile analog comparator. The MSP430F20x2 and MSP430F20x3 have built-in communication capability using synchronous protocols (SPI or I2C) and a 10-bit A/D converter (MSP430F20x2) or a 16-bit sigma-delta A/D converter (MSP430F20x3).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Typical applications include sensor systems that capture analog signals, convert them to digital values, and then process the data for display or for transmission to a host system. Stand alone RF sensor front end is another area of application.

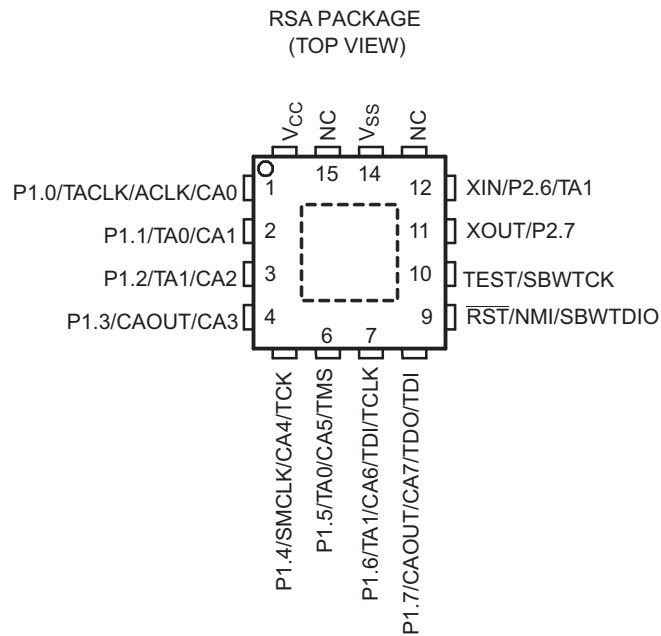
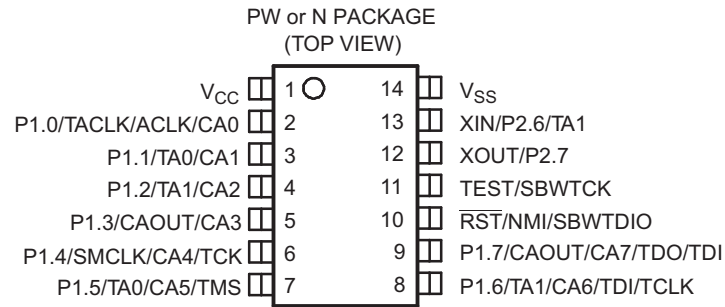
Table 1. Available Options⁽¹⁾

| T _A | PACKAGED DEVICES ⁽²⁾ | | |
|----------------|--|--|--|
| | PLASTIC 14-PIN TSSOP (PW) | PLASTIC 14-PIN DIP (N) | PLASTIC 16-PIN QFN (RSA) |
| -40°C to 85°C | MSP430F2001IPW MSP430F2011IPW MSP430F2002IPW MSP430F2012IPW MSP430F2003IPW MSP430F2013IPW | MSP430F2001IN MSP430F2011IN MSP430F2002IN MSP430F2012IN MSP430F2003IN MSP430F2013IN | MSP430F2001IRSA MSP430F2011IRSA MSP430F2002IRSA MSP430F2012IRSA MSP430F2003IRSA MSP430F2013IRSA |
| -40°C to 105°C | MSP430F2001TPW MSP430F2011TPW MSP430F2002TPW MSP430F2012TPW MSP430F2003TPW MSP430F2013TPW | MSP430F2001TN MSP430F2011TN MSP430F2002TN MSP430F2012TN MSP430F2003TN MSP430F2013TN | MSP430F2001TRSA MSP430F2011TRSA MSP430F2002TRSA MSP430F2012TRSA MSP430F2003TRSA MSP430F2013TRSA |

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

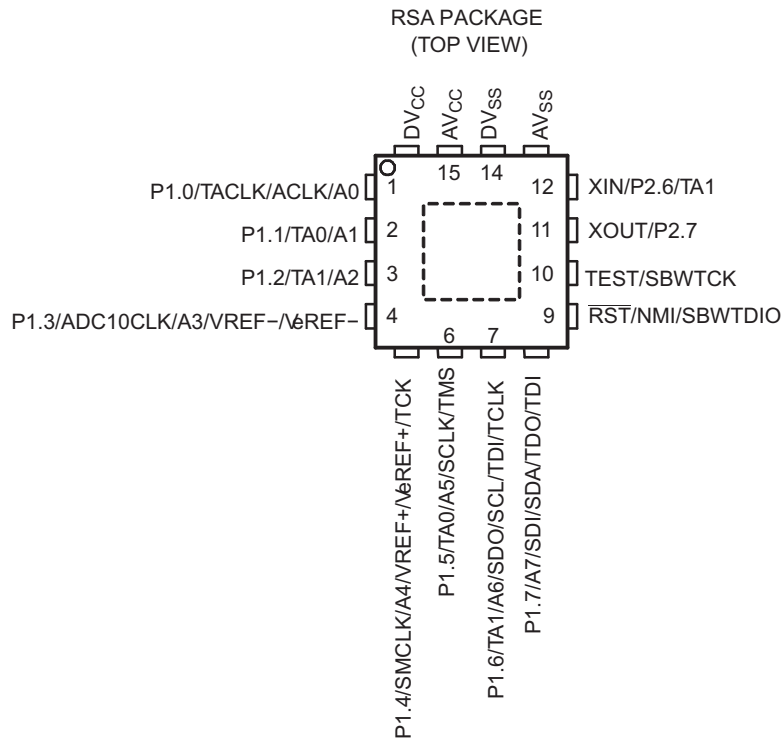
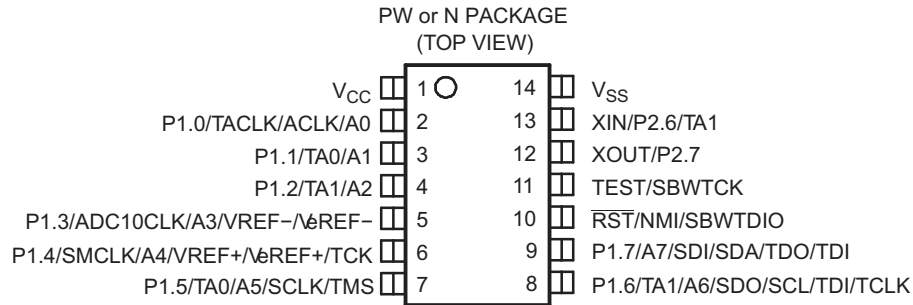
Device Pinout, MSP430F20x1

See port schematics section for detailed I/O information.



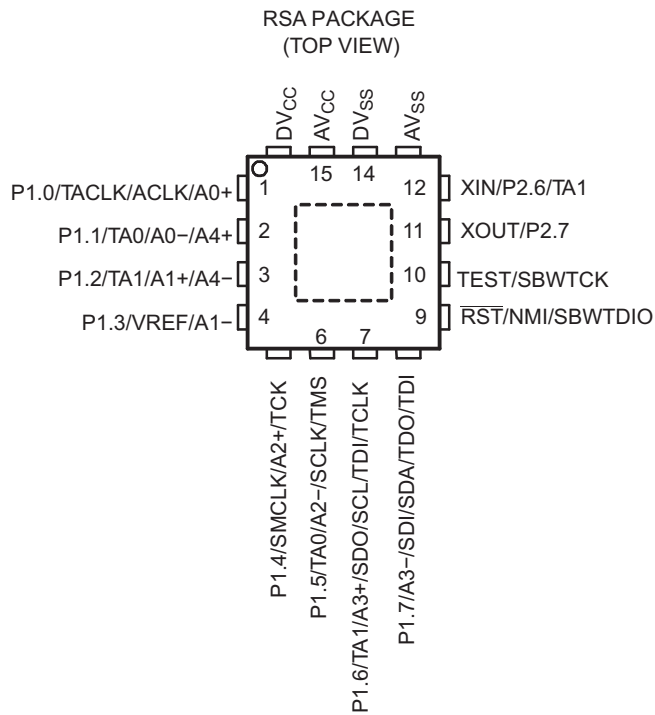
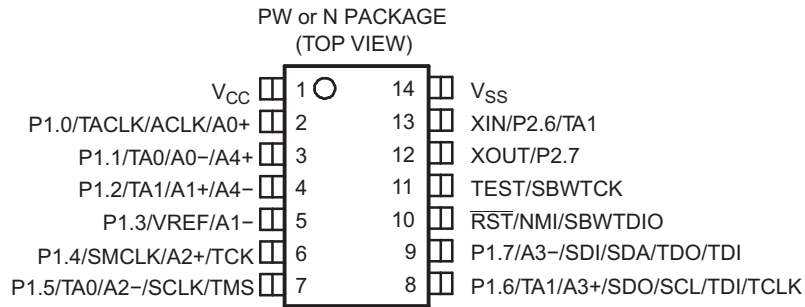
Device Pinout, MSP430F20x2

See port schematics section for detailed I/O information.

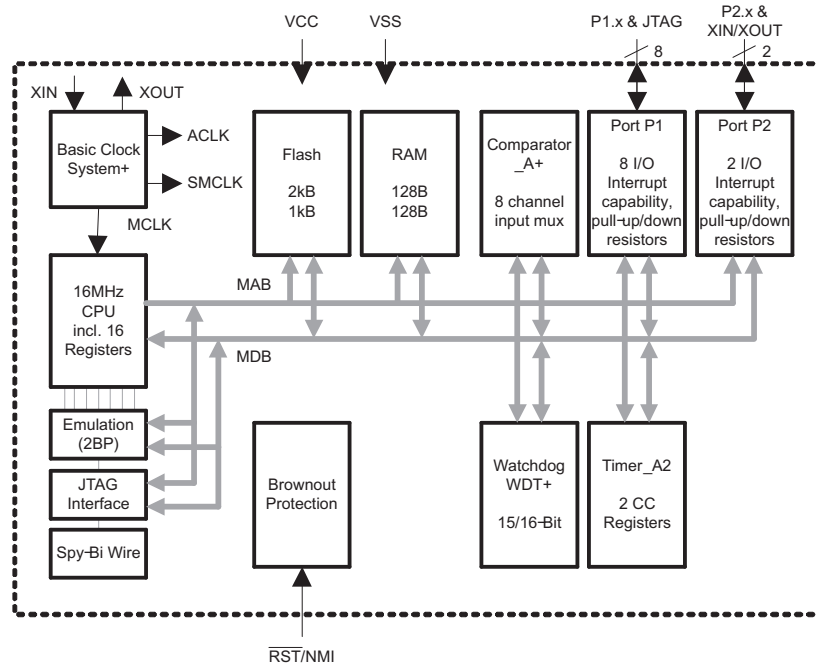


Device Pinout, MSP430F20x3

See port schematics section for detailed I/O information.

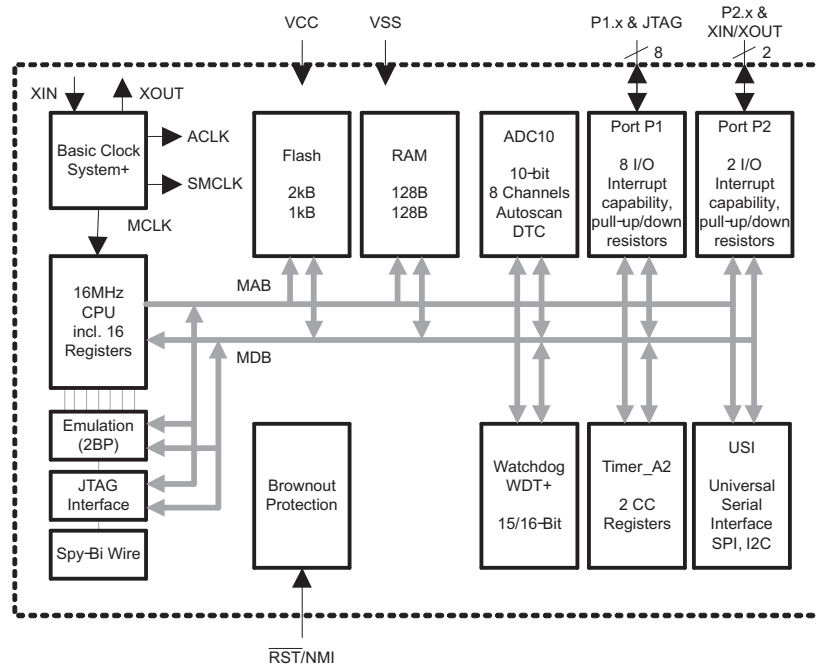


Functional Block Diagram, MSP430F20x1



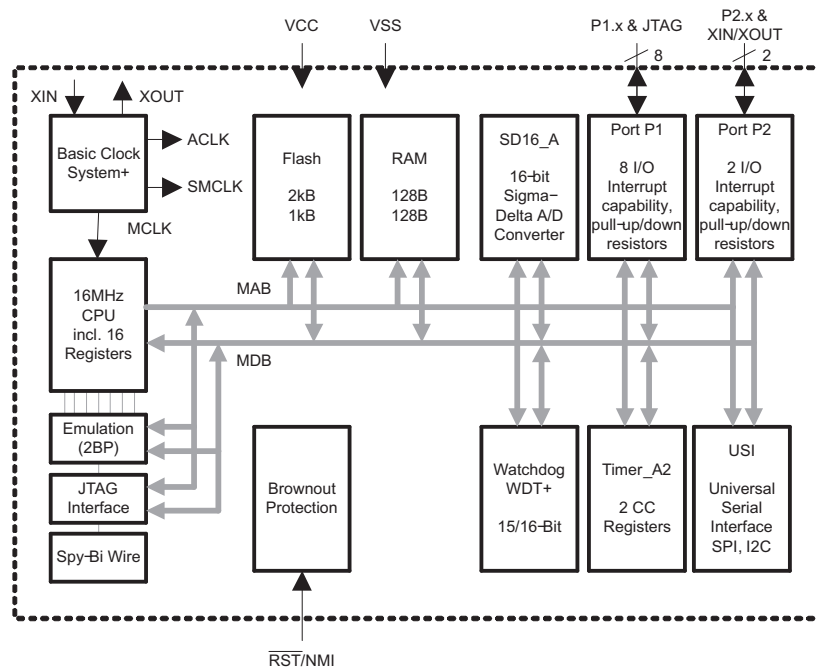
NOTE: See port schematics section for detailed I/O information.

Functional Block Diagram, MSP430F20x2



NOTE: See port schematics section for detailed I/O information.

Functional Block Diagram, MSP430F20x3



NOTE: See port schematics section for detailed I/O information.

Table 2. Terminal Functions, MSP430F20x1

| TERMINAL | | | | DESCRIPTION |
|---------------------------------------|-------|--------|-----|---|
| NAME | NO. | | I/O | |
| | PW, N | RSA | | |
| P1.0/TACLK/ACLK/CA0 | 2 | 1 | I/O | General-purpose digital I/O pin Timer_A, clock signal TACLK input ACLK signal output Comparator_A+, CA0 input |
| P1.1/TA0/CA1 | 3 | 2 | I/O | General-purpose digital I/O pin Timer_A, capture: CC10A input, compare: Out0 output Comparator_A+, CA1 input |
| P1.2/TA1/CA2 | 4 | 3 | I/O | General-purpose digital I/O pin Timer_A, capture: CC11A input, compare: Out1 output Comparator_A+, CA2 input |
| P1.3/CAOUT/CA3 | 5 | 4 | I/O | General-purpose digital I/O pin Comparator_A+, output / CA3 input |
| P1.4/SMCLK/C4/TCK | 6 | 5 | I/O | General-purpose digital I/O pin SMCLK signal output Comparator_A+, CA4 input JTAG test clock, input terminal for device programming and test |
| P1.5/TA0/CA5/TMS | 7 | 6 | I/O | General-purpose digital I/O pin Timer_A, compare: Out0 output Comparator_A+, CA5 input JTAG test mode select, input terminal for device programming and test |
| P1.6/TA1/CA6/TDI/TCLK | 8 | 7 | I/O | General-purpose digital I/O pin Timer_A, compare: Out1 output Comparator_A+, CA6 input JTAG test data input or test clock input during programming and test |
| P1.7/CAOUT/CA7/TDO/TDI ⁽¹⁾ | 9 | 8 | I/O | General-purpose digital I/O pin Comparator_A+, output / CA7 input JTAG test data output terminal or test data input during programming and test |
| XIN/P2.6/TA1 | 13 | 12 | I/O | Input terminal of crystal oscillator General-purpose digital I/O pin Timer_A, compare: Out1 output |
| XOUT/P2.7 | 12 | 11 | I/O | Output terminal of crystal oscillator General-purpose digital I/O pin ⁽²⁾ |
| $\overline{\text{RST}}$ /NMI/SBWDIO | 10 | 9 | I | Reset or nonmaskable interrupt input Spy-Bi-Wire test data input/output during programming and test |
| TEST/SBWTCK | 11 | 10 | I | Selects test mode for JTAG pins on Port 1. The device protection fuse is connected to TEST. Spy-Bi-Wire test clock input during programming and test |
| V _{CC} | 1 | 16 | | Supply voltage |
| V _{SS} | 14 | 14 | | Ground reference |
| NC | NA | 13, 15 | | Not connected |
| QFN Pad | NA | Pad | NA | QFN package pad. Connection to VSS is recommended. |

(1) TDO or TDI is selected via JTAG instruction.

(2) If XOUT/P2.7 is used as an input, excess current flows until P2SEL.7 is cleared. This is due to the oscillator output driver connection to this pad after reset.

Table 3. Terminal Functions, MSP430F20x2

| TERMINAL | | | | DESCRIPTION |
|--|-------|-----|-----|--|
| NAME | NO. | | I/O | |
| | PW, N | RSA | | |
| P1.0/TACLK/ACLK/A0 | 2 | 1 | I/O | General-purpose digital I/O pin Timer_A, clock signal TACLK input ACLK signal output ADC10 analog input A0 |
| P1.1/TA0/A1 | 3 | 2 | I/O | General-purpose digital I/O pin Timer_A, capture: CC10A input, compare: Out0 output ADC10 analog input A1 |
| P1.2/TA1/A2 | 4 | 3 | I/O | General-purpose digital I/O pin Timer_A, capture: CC11A input, compare: Out1 output ADC10 analog input A2 |
| P1.3/ADC10CLK/A3/ VREF-/VeREF- | 5 | 4 | I/O | General-purpose digital I/O pin ADC10 conversion clock output ADC10 analog input A3 Input for negative external reference voltage/negative internal reference voltage output |
| P1.4/SMCLK/A4/VREF+/ VeREF+/TCK | 6 | 5 | I/O | General-purpose digital I/O pin SMCLK signal output ADC10 analog input A4 Input for positive external reference voltage/positive internal reference voltage output JTAG test clock, input terminal for device programming and test |
| P1.5/TA0/A5/SCLK/TMS | 7 | 6 | I/O | General-purpose digital I/O pin Timer_A, compare: Out0 output ADC10 analog input A5 USI: external clock input in SPI or I2C mode; clock output in SPI mode JTAG test mode select, input terminal for device programming and test |
| P1.6/TA1/A6/SDO/SCL/ TDI/TCLK | 8 | 7 | I/O | General-purpose digital I/O pin Timer_A, capture: CC11B input, compare: Out1 output ADC10 analog input A6 USI: Data output in SPI mode; I2C clock in I2C mode JTAG test data input or test clock input during programming and test |
| P1.7/A7/SDI/SDA/ TDO/TDI ⁽¹⁾ | 9 | 8 | I/O | General-purpose digital I/O pin ADC10 analog input A7 USI: Data input in SPI mode; I2C data in I2C mode JTAG test data output terminal or test data input during programming and test |
| XIN/P2.6/TA1 | 13 | 12 | I/O | Input terminal of crystal oscillator General-purpose digital I/O pin Timer_A, compare: Out1 output |
| XOUT/P2.7 | 12 | 11 | I/O | Output terminal of crystal oscillator General-purpose digital I/O pin ⁽²⁾ |
| $\overline{\text{RST}}$ /NMI/SBWDIO | 10 | 9 | I | Reset or nonmaskable interrupt input Spy-Bi-Wire test data input/output during programming and test |
| TEST/SBWTK | 11 | 10 | I | Selects test mode for JTAG pins on Port 1. The device protection fuse is connected to TEST. Spy-Bi-Wire test clock input during programming and test |
| V _{CC} | 1 | NA | | Supply voltage |
| V _{SS} | 14 | NA | | Ground reference |
| DV _{CC} | NA | 16 | | Digital supply voltage |
| AV _{CC} | NA | 15 | | Analog supply voltage |
| DV _{SS} | NA | 14 | | Digital ground reference |
| AV _{SS} | NA | 13 | | Analog ground reference |
| QFN Pad | NA | Pad | NA | QFN package pad. Connection to VSS is recommended. |

(1) TDO or TDI is selected via JTAG instruction.

(2) If XOUT/P2.7 is used as an input, excess current flows until P2SEL.7 is cleared. This is due to the oscillator output driver connection to this pad after reset.

Table 4. Terminal Functions, MSP430F20x3

| TERMINAL | | | | DESCRIPTION |
|---|-------|-----|-----|--|
| NAME | NO. | | I/O | |
| | PW, N | RSA | | |
| P1.0/TACLK/ACLK/A0+ | 2 | 1 | I/O | General-purpose digital I/O pin Timer_A, clock signal TACLK input ACLK signal output SD16_A positive analog input A0 |
| P1.1/TA0/A0-/A4+ | 3 | 2 | I/O | General-purpose digital I/O pin Timer_A, capture: CCI0A input, compare: Out0 output SD16_A negative analog input A0 SD16_A positive analog input A4 |
| P1.2/TA1/A1+/A4- | 4 | 3 | I/O | General-purpose digital I/O pin Timer_A, capture: CCI1A input, compare: Out1 output SD16_A positive analog input A1 SD16_A negative analog input A4 |
| P1.3/VREF/A1- | 5 | 4 | I/O | General-purpose digital I/O pin Input for an external reference voltage/internal reference voltage output (can be used as mid-voltage) SD16_A negative analog input A1 |
| P1.4/SMCLK/A2+/TCK | 6 | 5 | I/O | General-purpose digital I/O pin SMCLK signal output SD16_A positive analog input A2 JTAG test clock, input terminal for device programming and test |
| P1.5/TA0/A2-/SCLK/TMS | 7 | 6 | I/O | General-purpose digital I/O pin Timer_A, compare: Out0 output SD16_A negative analog input A2 USI: external clock input in SPI or I2C mode; clock output in SPI mode JTAG test mode select, input terminal for device programming and test |
| P1.6/TA1/A3+/SDO/SCL/TDI/TCLK | 8 | 7 | I/O | General-purpose digital I/O pin Timer_A, capture: CCI1B input, compare: Out1 output SD16_A positive analog input A3 USI: Data output in SPI mode; I2C clock in I2C mode JTAG test data input or test clock input during programming and test |
| P1.7/A3-/SDI/SDA/TDO/TDI ⁽¹⁾ | 9 | 8 | I/O | General-purpose digital I/O pin SD16_A negative analog input A3 USI: Data input in SPI mode; I2C data in I2C mode JTAG test data output terminal or test data input during programming and test |
| XIN/P2.6/TA1 | 13 | 12 | I/O | Input terminal of crystal oscillator General-purpose digital I/O pin Timer_A, compare: Out1 output |
| XOUT/P2.7 | 12 | 11 | I/O | Output terminal of crystal oscillator General-purpose digital I/O pin ⁽²⁾ |
| $\overline{\text{RST}}$ /NMI/SBWDIO | 10 | 9 | I | Reset or nonmaskable interrupt input Spy-Bi-Wire test data input/output during programming and test |
| TEST/SBWTCK | 11 | 10 | I | Selects test mode for JTAG pins on Port 1. The device protection fuse is connected to TEST. Spy-Bi-Wire test clock input during programming and test |
| V _{CC} | 1 | NA | | Supply voltage |
| V _{SS} | 14 | NA | | Ground reference |
| DV _{CC} | NA | 16 | | Digital supply voltage |
| AV _{CC} | NA | 15 | | Analog supply voltage |
| DV _{SS} | NA | 14 | | Digital ground reference |
| AV _{SS} | NA | 13 | | Analog ground reference |
| QFN Pad | NA | Pad | NA | QFN package pad. Connection to VSS is recommended. |

(1) TDO or TDI is selected via JTAG instruction.

(2) If XOUT/P2.7 is used as an input, excess current flows until P2SEL.7 is cleared. This is due to the oscillator output driver connection to this pad after reset.

SHORT-FORM DESCRIPTION

CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

Instruction Set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. [Table 5](#) shows examples of the three types of instruction formats; [Table 6](#) shows the address modes.

| | |
|--------------------------|-----------|
| Program Counter | PC/R0 |
| Stack Pointer | SP/R1 |
| Status Register | SR/CG1/R2 |
| Constant Generator | CG2/R3 |
| General-Purpose Register | R4 |
| General-Purpose Register | R5 |
| General-Purpose Register | R6 |
| General-Purpose Register | R7 |
| General-Purpose Register | R8 |
| General-Purpose Register | R9 |
| General-Purpose Register | R10 |
| General-Purpose Register | R11 |
| General-Purpose Register | R12 |
| General-Purpose Register | R13 |
| General-Purpose Register | R14 |
| General-Purpose Register | R15 |

Table 5. Instruction Word Formats

| INSTRUCTION FORMAT | EXAMPLE | OPERATION |
|-----------------------------------|-----------|-----------------------|
| Dual operands, source-destination | ADD R4,R5 | R4 + R5 --> R5 |
| Single operands, destination only | CALL R8 | PC -->(TOS), R8--> PC |
| Relative jump, un/conditional | JNE | Jump-on-equal bit = 0 |

Table 6. Address Mode Descriptions

| ADDRESS MODE | S ⁽¹⁾ | D ⁽¹⁾ | SYNTAX | EXAMPLE | OPERATION |
|------------------------|------------------|------------------|-----------------|------------------|----------------------------------|
| Register | ✓ | ✓ | MOV Rs,Rd | MOV R10,R11 | R10 --> R11 |
| Indexed | ✓ | ✓ | MOV X(Rn),Y(Rm) | MOV 2(R5),6(R6) | M(2+R5)--> M(6+R6) |
| Symbolic (PC relative) | ✓ | ✓ | MOV EDE,TONI | | M(EDE) --> M(TONI) |
| Absolute | ✓ | ✓ | MOV &MEM,&TCDAT | | M(MEM) --> M(TCDAT) |
| Indirect | ✓ | | MOV @Rn,Y(Rm) | MOV @R10,Tab(R6) | M(R10) --> M(Tab+R6) |
| Indirect autoincrement | ✓ | | MOV @Rn+,Rm | MOV @R10+,R11 | M(R10) --> R11 R10 + 2--> R10 |
| Immediate | ✓ | | MOV #X,TONI | MOV #45,TONI | #45 --> M(TONI) |

(1) S = source, D = destination

Operating Modes

The MSP430 has one active mode and five software-selectable low-power modes of operation. An interrupt event can wake the device from any of the five low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode (AM)
 - All clocks are active
- Low-power mode 0 (LPM0)
 - CPU is disabled
 - ACLK and SMCLK remain active
 - MCLK is disabled
- Low-power mode 1 (LPM1)
 - CPU is disabled
 - ACLK and SMCLK remain active. MCLK is disabled
 - DCO's dc-generator is disabled if DCO not used in active mode
- Low-power mode 2 (LPM2)
 - CPU is disabled
 - MCLK and SMCLK are disabled
 - DCO's dc-generator remains enabled
 - ACLK remains active
- Low-power mode 3 (LPM3)
 - CPU is disabled
 - MCLK and SMCLK are disabled
 - DCO's dc-generator is disabled
 - ACLK remains active
- Low-power mode 4 (LPM4)
 - CPU is disabled
 - ACLK is disabled
 - MCLK and SMCLK are disabled
 - DCO's dc-generator is disabled
 - Crystal oscillator is stopped

Interrupt Vector Addresses

The interrupt vectors and the power-up starting address are located in the address range of 0FFFFh to 0FFC0h. The vector contains the 16-bit address of the appropriate interrupt handler instruction sequence.

If the reset vector (located at address 0FFFEh) contains 0FFFFh (for example, flash is not programmed) the CPU goes into LPM4 immediately after power-up.

Table 7. Interrupt Sources

| INTERRUPT SOURCE | INTERRUPT FLAG | SYSTEM INTERRUPT | WORD ADDRESS | PRIORITY |
|--|---|--|------------------|-----------------|
| Power-up External reset Watchdog Timer+ Flash key violation PC out-of-range ⁽¹⁾ | PORIFG RSTIFG WDTIFG KEYV See ⁽²⁾ | Reset | 0FFFEh | 31, highest |
| NMI Oscillator fault Flash memory access violation | NMIIFG OFIFG ACCVIFG ⁽²⁾⁽³⁾ | (non)-maskable, (non)-maskable, (non)-maskable | 0FFFCh | 30 |
| | | | 0FFFAh | 29 |
| | | | 0FFF8h | 28 |
| Comparator_A+ (MSP430F20x1) | CAIFG ⁽⁴⁾ | maskable | 0FFF6h | 27 |
| Watchdog Timer+ | WDTIFG | maskable | 0FFF4h | 26 |
| Timer_A2 | TACCR0 CCIFG ⁽⁴⁾ | maskable | 0FFF2h | 25 |
| Timer_A2 | TACCR1 CCIFG.TAIFG ⁽²⁾⁽⁴⁾ | maskable | 0FFF0h | 24 |
| | | | 0FFEEh | 23 |
| | | | 0FFECCh | 22 |
| ADC10 (MSP430F20x2) | ADC10IFG ⁽⁴⁾ | maskable | 0FFEAh | 21 |
| SD16_A (MSP430F20x3) | SD16CCTL0 SD16OVIFG, SD16CCTL0 SD16IFG ⁽²⁾⁽⁴⁾ | maskable | | |
| USI (MSP430F20x2, MSP430F20x3) | USIIFG, USISTTIFG ⁽²⁾⁽⁴⁾ | maskable | 0FFE8h | 20 |
| I/O Port P2 (two flags) | P2IFG.6 to P2IFG.7 ⁽²⁾⁽⁴⁾ | maskable | 0FFE6h | 19 |
| I/O Port P1 (eight flags) | P1IFG.0 to P1IFG.7 ⁽²⁾⁽⁴⁾ | maskable | 0FFE4h | 18 |
| | | | 0FFE2h | 17 |
| | | | 0FFE0h | 16 |
| See ⁽⁵⁾ | | | 0FFDEh to 0FFC0h | 15 to 0, lowest |

(1) A reset is generated if the CPU tries to fetch instructions from within the module register memory address range (0h to 01FFh) or from within unused address ranges.

(2) Multiple source flags

(3) (non)-maskable: the individual interrupt-enable bit can disable an interrupt event, but the general interrupt enable cannot.

(4) Interrupt flags are located in the module.

(5) The interrupt vectors at addresses 0FFDEh to 0FFC0h are not used in this device and can be used for regular program code if necessary.

Special Function Registers

Most interrupt and module enable bits are collected into the lowest address space. Special function register bits not allocated to a functional purpose are not physically present in the device. Simple software access is provided with this arrangement.






| | | |
|---------------|---|---|
| Legend | rw: | Bit can be read and written. |
| | rw-0,1: | Bit can be read and written. It is reset or set by PUC. |
| | rw-(0,1): | Bit can be read and written. It is reset or set by POR. |
| |  | SFR bit is not present in device. |




Table 8. Interrupt Enable Register 1 and 2

| Address | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|--------|-------|--|---|------|-------|
| 00h |  |  | ACCVIE | NMIIE |  |  | OFIE | WDTIE |
| | | | rw-0 | rw-0 | | | rw-0 | rw-0 |



WDTIE Watchdog Timer interrupt enable. Inactive if watchdog mode is selected. Active if Watchdog Timer is configured in interval timer mode.
OFIE Oscillator fault interrupt enable
NMIIE (Non)maskable interrupt enable
ACCVIE Flash access violation interrupt enable

| Address | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|--|---|---|---|
| 01h |  |  |  |  |  |  |  |  |

Table 9. Interrupt Flag Register 1 and 2

| Address | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|--------|--------|--------|-------|--------|
| 02h |  |  |  | NMIIFG | RSTIFG | PORIFG | OFIFG | WDTIFG |
| | | | | rw-0 | rw-(0) | rw-(1) | rw-1 | rw-(0) |

WDTIFG Set on watchdog timer overflow (in watchdog mode) or security key violation. Reset on V_{CC} power-on or a reset condition at the RST/NMI pin in reset mode.
OFIFG Flag set on oscillator fault.
PORIFG Power-On Reset interrupt flag. Set on V_{CC} power-up.
RSTIFG External reset interrupt flag. Set on a reset condition at RST/NMI pin in reset mode. Reset on V_{CC} power-up.
NMIIFG Set via RST/NMI pin

| Address | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|--|---|---|---|
| 03h |  |  |  |  |  |  |  |  |

Memory Organization

Table 10. Memory Organization

| | | MSP430F200x | MSP430F201x |
|---|------------------------------|---|---|
| Memory Main: interrupt vector Main: code memory | Size Flash Flash | 1KB Flash 0FFFFh-0FFC0h 0FFFFh-0FC00h | 2KB Flash 0FFFFh-0FFC0h 0FFFFh-0F800h |
| Information memory | Size Flash | 256 Byte 010FFh - 01000h | 256 Byte 010FFh - 01000h |
| RAM | Size | 128 Byte 027Fh - 0200h | 128 Byte 027Fh - 0200h |
| Peripherals | 16-bit 8-bit 8-bit SFR | 01FFh - 0100h 0FFh - 010h 0Fh - 00h | 01FFh - 0100h 0FFh - 010h 0Fh - 00h |

Flash Memory

The flash memory can be programmed via the Spy-Bi-Wire/JTAG port, or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 64 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually, or as a group with segments 0 to n. Segments A to D are also called *information memory*.
- Segment A contains calibration data. After reset segment A is protected against programming and erasing. It can be unlocked but care should be taken not to erase this segment if the device-specific calibration data is required.

Peripherals

Peripherals are connected to the CPU through data, address, and control busses and can be handled using all instructions. For complete module descriptions, refer to the *MSP430F2xx Family User's Guide*.

Oscillator and System Clock

The clock system is supported by the basic clock module that includes support for a 32768-Hz watch crystal oscillator, an internal very-low-power low-frequency oscillator and an internal digitally-controlled oscillator (DCO). The basic clock module is designed to meet the requirements of both low system cost and low power consumption. The internal DCO provides a fast turn-on clock source and stabilizes in less than 1 μ s. The basic clock module provides the following clock signals:

- Auxiliary clock (ACLK), sourced either from a 32768-Hz watch crystal or the internal LF oscillator.
- Main clock (MCLK), the system clock used by the CPU.
- Sub-Main clock (SMCLK), the sub-system clock used by the peripheral modules.

Table 11. DCO Calibration Data (Provided From Factory in Flash Information Memory Segment A)

| DCO FREQUENCY | CALIBRATION REGISTER | SIZE | ADDRESS |
|---------------|----------------------|------|---------|
| 1 MHz | CALBC1_1MHZ | byte | 010FFh |
| | CALDCO_1MHZ | byte | 010FEh |
| 8 MHz | CALBC1_8MHZ | byte | 010FDh |
| | CALDCO_8MHZ | byte | 010FCh |
| 12 MHz | CALBC1_12MHZ | byte | 010FBh |
| | CALDCO_12MHZ | byte | 010FAh |
| 16 MHz | CALBC1_16MHZ | byte | 010F9h |
| | CALDCO_16MHZ | byte | 010F8h |

Brownout

The brownout circuit is implemented to provide the proper internal reset signal to the device during power on and power off.

Digital I/O

There is one 8-bit I/O port implemented—port P1—and two bits of I/O port P2:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt condition is possible.
- Edge-selectable interrupt input capability for all the eight bits of port P1 and the two bits of port P2.
- Read and write access to port-control registers is supported by all instructions.
- Each I/O has an individually programmable pullup or pulldown resistor.

Watchdog Timer (WDT+)

The primary function of the watchdog timer (WDT+) module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be disabled or configured as an interval timer and can generate interrupts at selected time intervals.

Timer_A2

Timer_A2 is a 16-bit timer/counter with two capture/compare registers. Timer_A2 can support multiple capture/compares, PWM outputs, and interval timing. Timer_A2 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 12. Timer_A2 Signal Connections (MSP430F20x1)

| INPUT PIN NUMBER | | DEVICE INPUT SIGNAL | MODULE INPUT NAME | MODULE BLOCK | MODULE OUTPUT SIGNAL | OUTPUT PIN NUMBER | |
|------------------|----------|---------------------|-------------------|--------------|----------------------|-------------------|-----------|
| PW, N | RSA | | | | | PW, N | RSA |
| 2 - P1.0 | 1 - P1.0 | TACLK | TACLK | Timer | NA | | |
| | | ACLK | ACLK | | | | |
| | | SMCLK | SMCLK | | | | |
| 2 - P1.0 | 1 - P1.0 | TACLK | INCLK | | | | |
| 3 - P1.1 | 2 - P1.1 | TA0 | CC10A | CCR0 | TA0 | 3 - P1.1 | 2 - P1.1 |
| | | ACLK (internal) | CC10B | | | 7 - P1.5 | 6 - P1.5 |
| | | V _{SS} | GND | | | | |
| | | V _{CC} | V _{CC} | | | | |
| 4 - P1.2 | 3 - P1.2 | TA1 | CC11A | CCR1 | TA1 | 4 - P1.2 | 3 - P1.2 |
| | | CAOUT (internal) | CC11B | | | 8 - P1.6 | 7 - P1.6 |
| | | V _{SS} | GND | | | 13 - P2.6 | 12 - P2.6 |
| | | V _{CC} | V _{CC} | | | | |

Table 13. Timer_A2 Signal Connections (MSP430F20x2, MSP430F20x3)

| INPUT PIN NUMBER | | DEVICE INPUT SIGNAL | MODULE INPUT NAME | MODULE BLOCK | MODULE OUTPUT SIGNAL | OUTPUT PIN NUMBER | |
|------------------|----------|---------------------|-------------------|--------------|----------------------|-------------------|-----------|
| PW, N | RSA | | | | | PW, N | RSA |
| 2 - P1.0 | 1 - P1.0 | TACLK | TACLK | Timer | NA | | |
| | | ACLK | ACLK | | | | |
| | | SMCLK | SMCLK | | | | |
| 2 - P1.0 | 1 - P1.0 | TACLK | INCLK | | | | |
| 3 - P1.1 | 2 - P1.1 | TA0 | CC10A | CCR0 | TA0 | 3 - P1.1 | 2 - P1.1 |
| 7 - P1.5 | 6 - P1.5 | ACLK (internal) | CC10B | | | 7 - P1.5 | 6 - P1.5 |
| | | V _{SS} | GND | | | | |
| | | V _{CC} | V _{CC} | | | | |
| 4 - P1.2 | 3 - P1.2 | TA1 | CC11A | CCR1 | TA1 | 4 - P1.2 | 3 - P1.2 |
| 8 - P1.6 | 7 - P1.6 | TA1 | CC11B | | | 8 - P1.6 | 7 - P1.6 |
| | | V _{SS} | GND | | | 13 - P2.6 | 12 - P2.6 |
| | | V _{CC} | V _{CC} | | | | |

Comparator_A+ (MSP430F20x1)

The primary function of the comparator_A+ module is to support precision slope analog-to-digital conversions, battery-voltage supervision, and monitoring of external analog signals.

USI (MSP430F20x2 and MSP430F20x3)

The universal serial interface (USI) module is used for serial data communication and provides the basic hardware for synchronous communication protocols like SPI and I2C.

ADC10 (MSP430F20x2)

The ADC10 module supports fast, 10-bit analog-to-digital conversions. The module implements a 10-bit SAR core, sample select control, reference generator and data transfer controller, or DTC, for automatic conversion result handling, allowing ADC samples to be converted and stored without any CPU intervention.

SD16_A (MSP430F20x3)

The SD16_A module supports 16-bit analog-to-digital conversions. The module implements a 16-bit sigma-delta core and reference generator. In addition to external analog inputs, internal V_{CC} sense and temperature sensors are also available.

Peripheral File Map
Table 14. Peripherals With Word Access

| | | | |
|--------------------------------|---|--|---|
| ADC10 (MSP430F20x2) | ADC control 0 ADC control 1 ADC memory ADC data transfer start address | ADC10CTL0 ADC10CTL1 ADC10MEM ADC10SA | 01B0h 01B2h 01B4h 01BCh |
| SD16_A (MSP430F20x3) | General Control Channel 0 Control Interrupt vector word register Channel 0 conversion memory | SD16CTL SD16CCCTL0 SD16IV SD16MEM0 | 0100h 0102h 0110h 0112h |
| Timer_A | Capture/compare register Capture/compare register Timer_A register Capture/compare control Capture/compare control Timer_A control Timer_A interrupt vector | TACCR1 TACCR0 TAR TACCTL1 TACCTL0 TACTL TAIV | 0174h 0172h 0170h 0164h 0162h 0160h 012Eh |
| Flash Memory | Flash control 3 Flash control 2 Flash control 1 | FCTL3 FCTL2 FCTL1 | 012Ch 012Ah 0128h |
| Watchdog Timer+ | Watchdog/timer control | WDTCTL | 0120h |

Table 15. Peripherals With Byte Access

| | | | |
|---|---|--|--|
| ADC10 (MSP430F20x2) | Analog enable ADC data transfer control register 1 ADC data transfer control register 0 | ADC10AE ADC10DTC1 ADC10DTC0 | 04Ah 049h 048h |
| SD16_A (MSP430F20x3) | Channel 0 Input Control Analog Enable | SD16INCTL0 SD16AE | 0B0h 0B7h |
| USI (MSP430F20x2 and MSP430F20x3) | USI control 0 USI control 1 USI clock control USI bit counter USI shift register | USICTL0 USICTL1 USICKCTL USICNT USISR | 078h 079h 07Ah 07Bh 07Ch |
| Comparator_A+ (MSP430F20x1) | Comparator_A+ port disable Comparator_A+ control 2 Comparator_A+ control 1 | CAPD CACTL2 CACTL1 | 05Bh 05Ah 059h |
| Basic Clock System+ | Basic clock system control 3 Basic clock system control 2 Basic clock system control 1 DCO clock frequency control | BCSCTL3 BCSCTL2 BCSCTL1 DCOCTL | 053h 058h 057h 056h |
| Port P2 | Port P2 resistor enable Port P2 selection Port P2 interrupt enable Port P2 interrupt edge select Port P2 interrupt flag Port P2 direction Port P2 output Port P2 input | P2REN P2SEL P2IE P2IES P2IFG P2DIR P2OUT P2IN | 02Fh 02Eh 02Dh 02Ch 02Bh 02Ah 029h 028h |
| Port P1 | Port P1 resistor enable Port P1 selection Port P1 interrupt enable Port P1 interrupt edge select Port P1 interrupt flag Port P1 direction Port P1 output Port P1 input | P1REN P1SEL P1IE P1IES P1IFG P1DIR P1OUT P1IN | 027h 026h 025h 024h 023h 022h 021h 020h |
| Special Function | SFR interrupt flag 2 SFR interrupt flag 1 SFR interrupt enable 2 SFR interrupt enable 1 | IFG2 IFG1 IE2 IE1 | 003h 002h 001h 000h |

Absolute Maximum Ratings⁽¹⁾

| | | | |
|---|------------------------------------|----------------------------|----------------|
| Voltage applied at V_{CC} to V_{SS} | | -0.3 V to 4.1 V | |
| Voltage applied to any pin ⁽²⁾ | | -0.3 V to $V_{CC} + 0.3$ V | |
| Diode current at any device terminal | | ± 2 mA | |
| T_{stg} | Storage temperature ⁽³⁾ | Unprogrammed device | -55°C to 150°C |
| | | Programmed device | -55°C to 150°C |

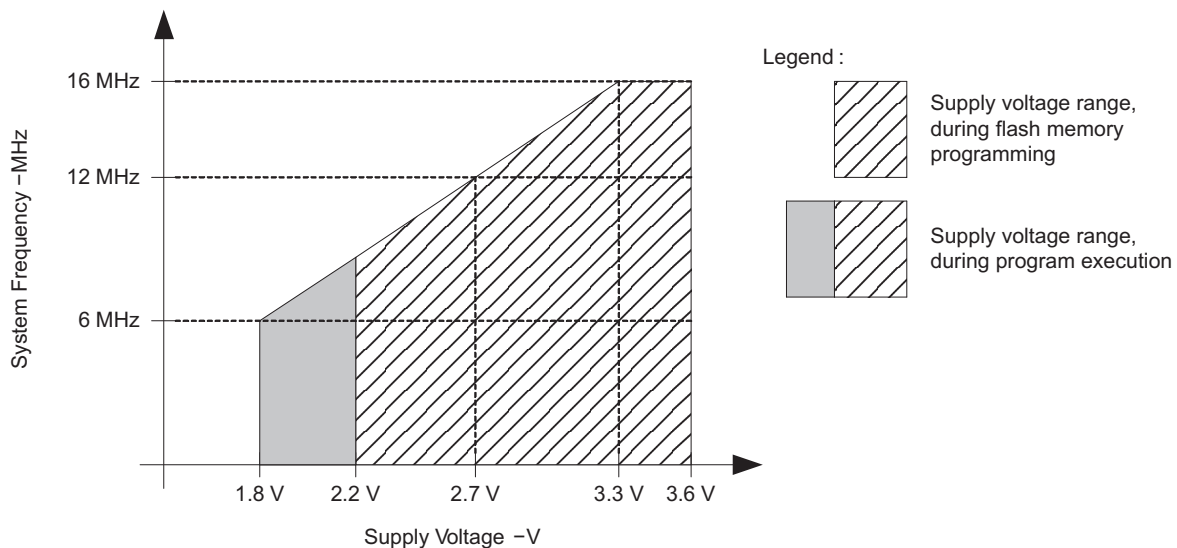
- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages referenced to V_{SS} . The JTAG fuse-blow voltage, V_{FB} , is allowed to exceed the absolute maximum rating. The voltage is applied to the TEST pin when blowing the JTAG fuse.
- (3) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

Recommended Operating Conditions

Typical values are specified at $V_{CC} = 3.3$ V and $T_A = 25^\circ\text{C}$ (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|--------------|--|--|-----|-----|------|
| V_{CC} | Supply voltage | During program execution | 1.8 | 3.6 | V |
| | | During flash program/erase | 2.2 | 3.6 | |
| V_{SS} | Supply voltage | 0 | | | V |
| T_A | Operating free-air temperature | I version | -40 | 85 | °C |
| | | T version | -40 | 105 | |
| f_{SYSTEM} | Processor frequency (maximum MCLK frequency) ⁽¹⁾⁽²⁾ | $V_{CC} = 1.8$ V, Duty cycle = 50% \pm 10% | dc | 6 | MHz |
| | | $V_{CC} = 2.7$ V, Duty cycle = 50% \pm 10% | dc | 12 | |
| | | $V_{CC} \geq 3.3$ V, Duty cycle = 50% \pm 10% | dc | 16 | |

- (1) The MSP430 CPU is clocked directly with MCLK. Both the high and low phase of MCLK must not exceed the pulse width of the specified maximum frequency.
- (2) Modules might have a different maximum input clock specification. See the specification of the respective module in this data sheet.



Note: Minimum processor frequency is defined by system clock. Flash program or erase operations require a minimum V_{CC} of 2.2 V.

Figure 1. Safe Operating Area

Electrical Characteristics

Active Mode Supply Current Into V_{CC} Excluding External Current

 over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾⁽²⁾

| PARAMETER | TEST CONDITIONS | T_A | V_{CC} | | | UNIT |
|--|--|---------------|----------|-----|-----|---------------|
| | | | MIN | TYP | MAX | |
| $I_{AM,1MHz}$ Active mode (AM) current (1 MHz) | $f_{DCO} = f_{MCLK} = f_{SMCLK} = 1\text{ MHz}$, $f_{ACLK} = 32768\text{ Hz}$, Program executes in flash, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0 | | 2.2 V | 220 | 270 | μA |
| | | | 3 V | 300 | 370 | |
| $I_{AM,1MHz}$ Active mode (AM) current (1 MHz) | $f_{DCO} = f_{MCLK} = f_{SMCLK} = 1\text{ MHz}$, $f_{ACLK} = 32768\text{ Hz}$, Program executes in RAM, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0 | | 2.2 V | 190 | | μA |
| | | | 3 V | 260 | | |
| $I_{AM,4kHz}$ Active mode (AM) current (4 kHz) | $f_{MCLK} = f_{SMCLK} = f_{ACLK} = 32768\text{ Hz}/8 = 4096\text{ Hz}$, $f_{DCO} = 0\text{ Hz}$, Program executes in flash, SELMx = 11, SELS = 1, DIVMx = DIVSx = DIVAx = 11, CPUOFF = 0, SCG0 = 1, SCG1 = 0, OSCOFF = 0 | -40°C to 85°C | 2.2 V | 1.2 | 3 | μA |
| | | 105°C | 2.2 V | | 6 | |
| | | -40°C to 85°C | 3 V | 1.6 | 4 | |
| | | 105°C | 3 V | | 7 | |
| $I_{AM,100kHz}$ Active mode (AM) current (100 kHz) | $f_{MCLK} = f_{SMCLK} = f_{DCO(0,0)} \approx 100\text{ kHz}$, $f_{ACLK} = 0\text{ Hz}$, Program executes in flash, RSELx = 0, DCOx = 0, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 1 | -40°C to 85°C | 2.2 V | 37 | 50 | μA |
| | | 105°C | 2.2 V | | 60 | |
| | | -40°C to 85°C | 3 V | 40 | 55 | |
| | | 105°C | 3 V | | 65 | |

(1) All inputs are tied to 0 V or to V_{CC} . Outputs do not source or sink any current.

(2) The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance is chosen to closely match the required 9 pF.

Typical Characteristics - Active Mode Supply Current (Into V_{CC})

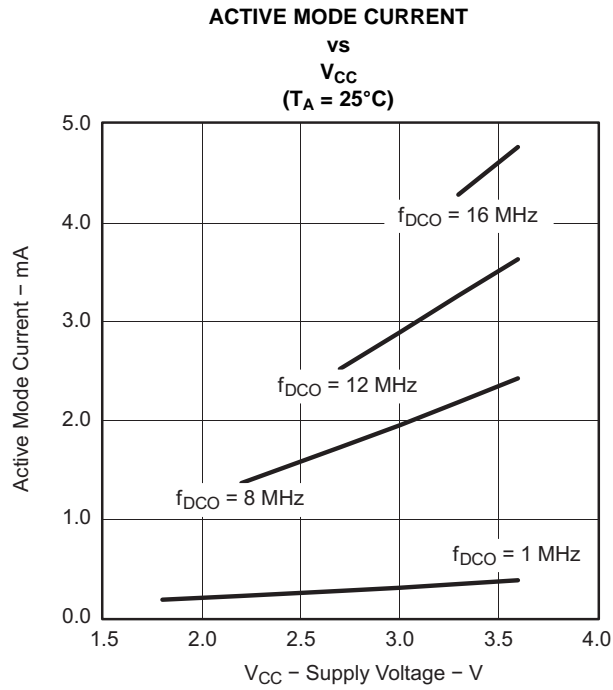


Figure 2.

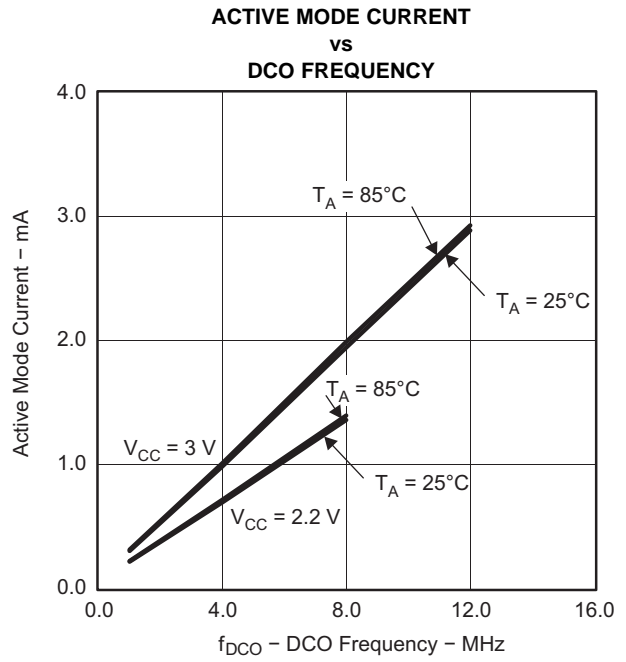


Figure 3.

Low-Power Mode Supply Currents (Into V_{CC}) Excluding External Current

 over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)^{(1) (2)}

| PARAMETER | TEST CONDITIONS | T_A | V_{CC} | MIN | TYP | MAX | UNIT |
|-------------------|--|---------------|------------|-----|-----|-----|---------|
| $I_{LPM0,1MHz}$ | Low-power mode 0 (LPM0) current ⁽³⁾ $f_{MCLK} = 0$ MHz, $f_{SMCLK} = f_{DCO} = 1$ MHz, $f_{ACLK} = 32,768$ Hz, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0 | | 2.2 V | | 65 | 80 | μ A |
| | | | 3 V | | 85 | 100 | |
| $I_{LPM0,100kHz}$ | Low-power mode 0 (LPM0) current ⁽³⁾ $f_{MCLK} = 0$ MHz, $f_{SMCLK} = f_{DCO(0,0)} \approx 100$ kHz, $f_{ACLK} = 0$ Hz, RSELX = 0, DCOx = 0, CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 1 | | 2.2 V | | 37 | 48 | μ A |
| | | | 3 V | | 41 | 52 | |
| I_{LPM2} | Low-power mode 2 (LPM2) current ⁽⁴⁾ $f_{MCLK} = f_{SMCLK} = 0$ MHz, $f_{DCO} = 1$ MHz, $f_{ACLK} = 32,768$ Hz, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0 | -40°C to 85°C | 2.2 V | | 22 | 29 | μ A |
| | | 105°C | | | 31 | | |
| | | -40°C to 85°C | 3 V | | 25 | 32 | |
| | | 105°C | | | 34 | | |
| $I_{LPM3,LFXT1}$ | Low-power mode 3 (LPM3) current ⁽³⁾ $f_{DCO} = f_{MCLK} = f_{SMCLK} = 0$ MHz, $f_{ACLK} = 32,768$ Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 | -40°C | 2.2 V | | 0.7 | 1.2 | μ A |
| | | 25°C | | | 0.7 | 1 | |
| | | 85°C | | | 1.4 | 2.3 | |
| | | 105°C | | | 3 | 6 | |
| | | -40°C | 3 V | | 0.9 | 1.2 | |
| | | 25°C | | | 0.9 | 1.2 | |
| | | 85°C | | | 1.6 | 2.8 | |
| | | 105°C | | | 3 | 7 | |
| $I_{LPM3,VLO}$ | Low-power mode 3 (LPM3) current ⁽⁴⁾ $f_{DCO} = f_{MCLK} = f_{SMCLK} = 0$ MHz, f_{ACLK} from internal LF oscillator (VLO), CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 | -40°C | 2.2 V | | 0.4 | 0.7 | μ A |
| | | 25°C | | | 0.5 | 0.7 | |
| | | 85°C | | | 1 | 1.6 | |
| | | 105°C | | | 2 | 5 | |
| | | -40°C | 3 V | | 0.5 | 0.9 | |
| | | 25°C | | | 0.6 | 0.9 | |
| | | 85°C | | | 1.3 | 1.8 | |
| | | 105°C | | | 2.5 | 6 | |
| I_{LPM4} | Low-power mode 4 (LPM4) current ⁽⁵⁾ $f_{DCO} = f_{MCLK} = f_{SMCLK} = 0$ MHz, $f_{ACLK} = 0$ Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1 | -40°C | 2.2 V, 3 V | | 0.1 | 0.5 | μ A |
| | | 25°C | | | 0.1 | 0.5 | |
| | | 85°C | | | 0.8 | 1.5 | |
| | | 105°C | | | 2 | 4 | |

(1) All inputs are tied to 0 V or to V_{CC} . Outputs do not source or sink any current.

(2) The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF.

(3) Current for brownout and WDT clocked by SMCLK included.

(4) Current for brownout and WDT clocked by ACLK included.

(5) Current for brownout included.

Schmitt-Trigger Inputs (Ports P1 and P2)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|--|--|-----------------|----------------------|-----|----------------------|------|
| V _{IT+} Positive-going input threshold voltage | | | 0.45 V _{CC} | | 0.75 V _{CC} | V |
| | | 2.2 V | 1.00 | | 1.65 | |
| | | 3 V | 1.35 | | 2.25 | |
| V _{IT-} Negative-going input threshold voltage | | | 0.25 V _{CC} | | 0.55 V _{CC} | V |
| | | 2.2 V | 0.55 | | 1.20 | |
| | | 3 V | 0.75 | | 1.65 | |
| V _{hys} Input voltage hysteresis (V _{IT+} - V _{IT-}) | | 2.2 V | 0.2 | | 1.0 | V |
| | | 3 V | 0.3 | | 1.0 | |
| R _{Pull} Pullup/pulldown resistor | For pullup: V _{IN} = V _{SS} , For pulldown: V _{IN} = V _{CC} | | 20 | 35 | 50 | kΩ |
| C _I Input capacitance | V _{IN} = V _{SS} or V _{CC} | | | 5 | | pF |

Inputs (Ports P1 and P2)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|--|--|-----------------|-----|-----|-----|------|
| t _(int) External interrupt timing | Port P1, P2: P1.x to P2.x, External trigger pulse width to set interrupt flag ⁽¹⁾ | 2.2 V, 3 V | 20 | | | ns |

- (1) An external signal sets the interrupt flag every time the minimum interrupt pulse width t_(int) is met. It may be set even with trigger signals shorter than t_(int).

Leakage Current (Ports P1 and P2)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | MAX | UNIT |
|---|-----------------|-----------------|-----|-----|------|
| I _{lkG(Px.y)} High-impedance leakage current | (1) (2) | 2.2 V, 3 V | | ±50 | nA |

- (1) The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pins, unless otherwise noted.
(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup or pulldown resistor is disabled.

Outputs (Ports P1 and P2)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-----------------|---------------------------|---|-----------------|------------------------|-----|------------------------|------|
| V _{OH} | High-level output voltage | I _(OHmax) = -1.5 mA ⁽¹⁾ | 2.2 V | V _{CC} - 0.25 | | V _{CC} | V |
| | | I _(OHmax) = -6 mA ⁽²⁾ | 2.2 V | V _{CC} - 0.6 | | V _{CC} | |
| | | I _(OHmax) = -1.5 mA ⁽¹⁾ | 3 V | V _{CC} - 0.25 | | V _{CC} | |
| | | I _(OHmax) = -6 mA ⁽²⁾ | 3 V | V _{CC} - 0.6 | | V _{CC} | |
| V _{OL} | Low-level output voltage | I _(OLmax) = 1.5 mA ⁽¹⁾ | 2.2 V | V _{SS} | | V _{SS} + 0.25 | V |
| | | I _(OLmax) = 6 mA ⁽²⁾ | 2.2 V | V _{SS} | | V _{SS} + 0.6 | |
| | | I _(OLmax) = 1.5 mA ⁽¹⁾ | 3 V | V _{SS} | | V _{SS} + 0.25 | |
| | | I _(OLmax) = 6 mA ⁽²⁾ | 3 V | V _{SS} | | V _{SS} + 0.6 | |

(1) The maximum total current, I_(OHmax) and I_(OLmax), for all outputs combined should not exceed ±12 mA to hold the maximum voltage drop specified.

(2) The maximum total current, I_(OHmax) and I_(OLmax), for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.

Output Frequency (Ports P1 and P2)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-----------------------|-----------------------------------|---|-----------------|-----|-----|-----|------|
| f _{Px,y} | Port output frequency (with load) | P1.4/SMCLK, C _L = 20 pF, R _L = 1 kΩ ⁽¹⁾ ⁽²⁾ | 2.2 V | | | 10 | MHz |
| | | | 3 V | | | 12 | |
| f _{Port*CLK} | Clock output frequency | P2.0/ACLK, P1.4/SMCLK, C _L = 20 pF ⁽²⁾ | 2.2 V | | | 12 | MHz |
| | | | 3 V | | | 16 | |

(1) A resistive divider with 2 × 0.5 kΩ between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider.

(2) The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.

Typical Characteristics - Outputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

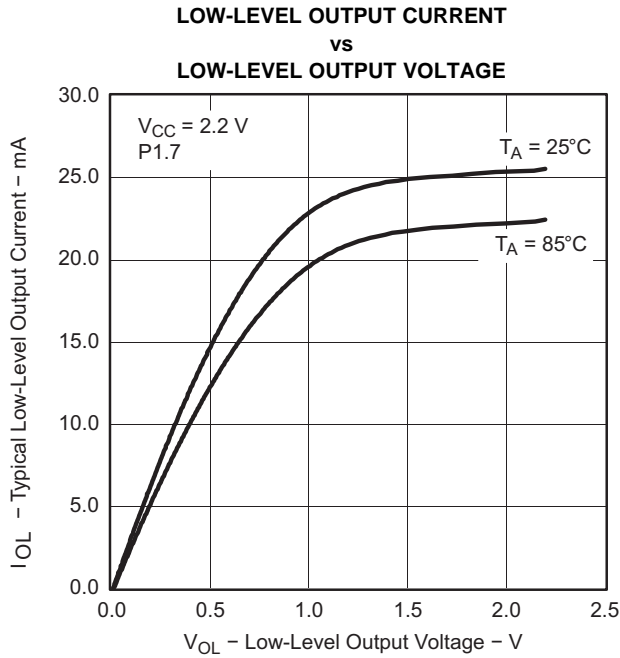


Figure 4.

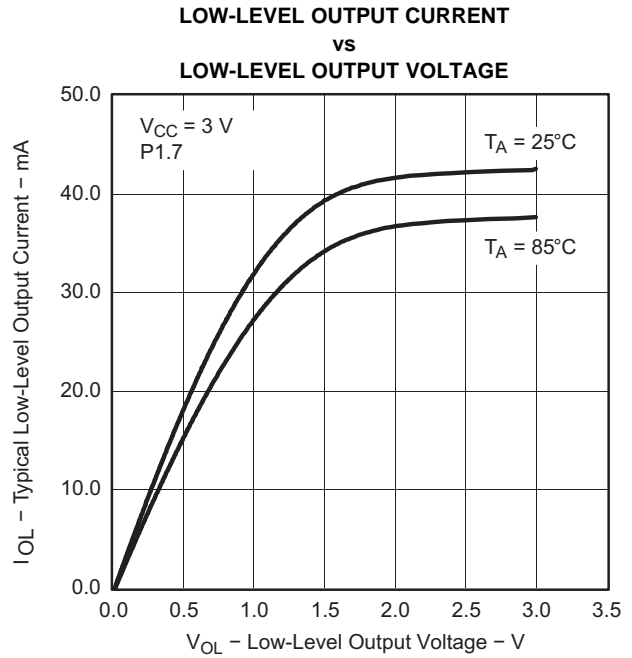


Figure 5.

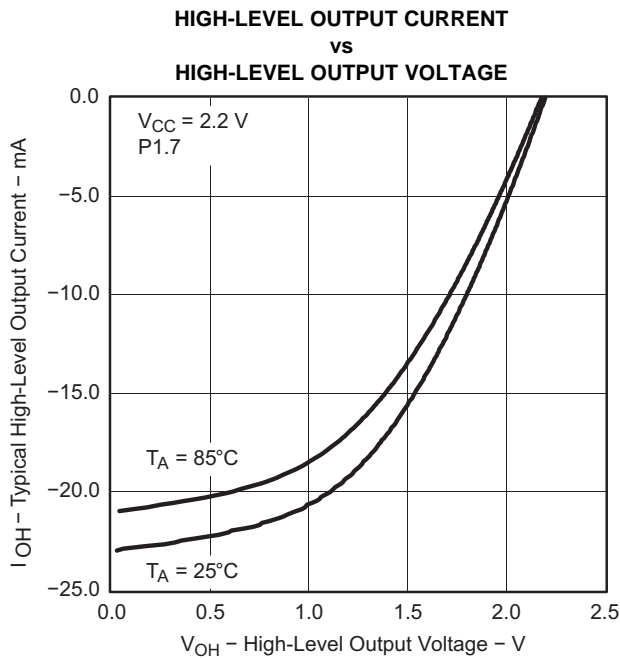


Figure 6.

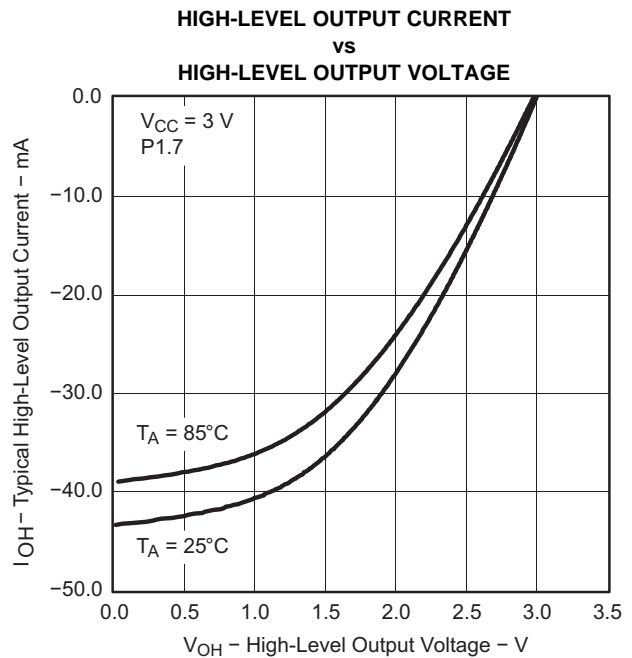


Figure 7.

POR and Brownout Reset (BOR)⁽¹⁾⁽²⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-------------------------|--|------------------------------|-----------------|-----|-------------------------------|------|------|
| V _{CC(start)} | See Figure 8 | dV _{CC} /dt ≤ 3 V/s | | | 0.7 × V _(B_IT-) | | V |
| V _(B_IT-) | See Figure 8 through Figure 10 | dV _{CC} /dt ≤ 3 V/s | | | | 1.71 | V |
| V _{hys(B_IT-)} | See Figure 8 | dV _{CC} /dt ≤ 3 V/s | | 70 | 130 | 210 | mV |
| t _{d(BOR)} | See Figure 8 | | | | | 2000 | μs |
| t _(reset) | Pulse duration needed at $\overline{\text{RST}}/\text{NMI}$ pin to accept reset internally | | 2.2 V, 3 V | 2 | | | μs |

- (1) The current consumption of the brownout module is already included in the I_{CC} current consumption data. The voltage level V_(B_IT-) + V_{hys(B_IT-)} is ≤ 1.8 V.
- (2) During power up, the CPU begins code execution following a period of t_{d(BOR)} after V_{CC} = V_(B_IT-) + V_{hys(B_IT-)}. The default DCO settings must not be changed until V_{CC} ≥ V_{CC(min)}, where V_{CC(min)} is the minimum supply voltage for the desired operating frequency.

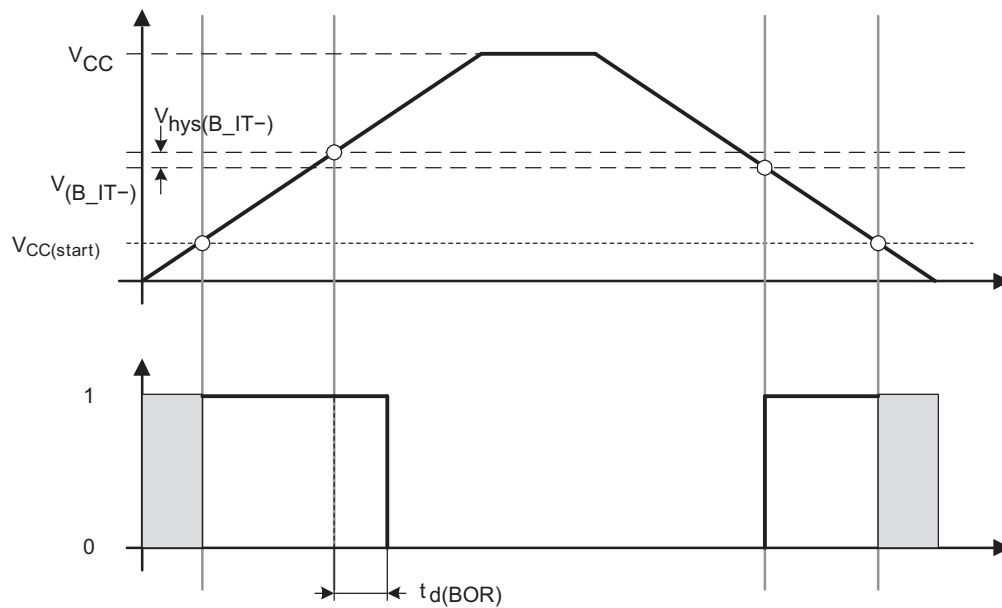


Figure 8. POR/Brownout Reset (BOR) vs Supply Voltage

Typical Characteristics - POR/Brownout Reset (BOR)

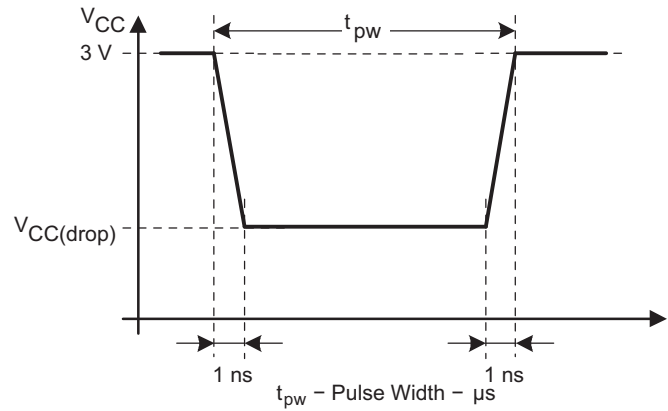
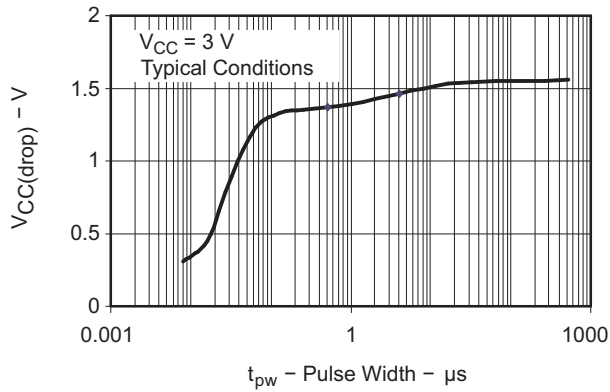


Figure 9. $V_{CC(drop)}$ Level With a Square Voltage Drop to Generate a POR/Brownout Signal

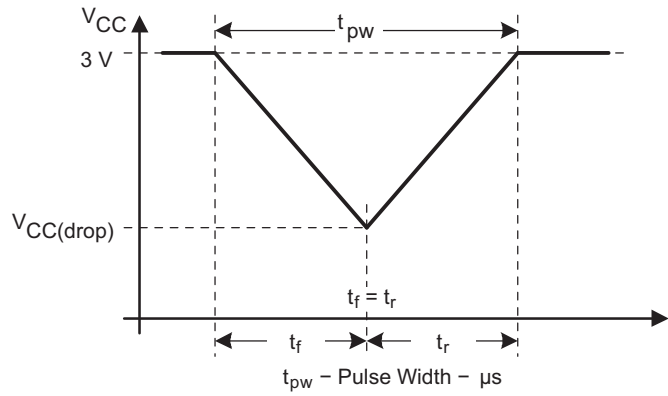
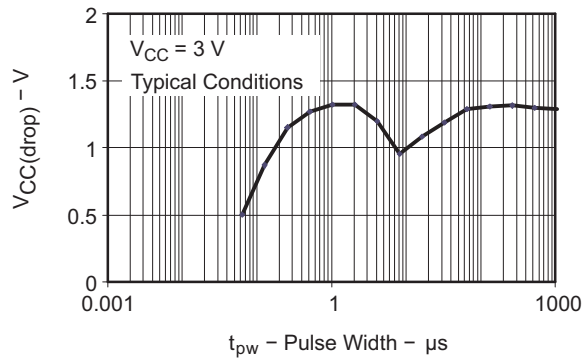


Figure 10. $V_{CC(drop)}$ Level With a Triangle Voltage Drop to Generate a POR/Brownout Signal

Main DCO Characteristics

- All ranges selected by RSELx overlap with RSELx + 1: RSELx = 0 overlaps RSELx = 1, ... RSELx = 14 overlaps RSELx = 15.
- DCO control bits DCOx have a step size as defined by parameter S_{DCO}.
- Modulation control bits MODx select how often f_{DCO(RSEL,DCO+1)} is used within the period of 32 DCOCLK cycles. The frequency f_{DCO(RSEL,DCO)} is used for the remaining cycles. The frequency is an average equal to:

$$f_{\text{average}} = \frac{32 \times f_{\text{DCO(RSEL,DCO)}} \times f_{\text{DCO(RSEL,DCO+1)}}}{\text{MOD} \times f_{\text{DCO(RSEL,DCO)}} + (32 - \text{MOD}) \times f_{\text{DCO(RSEL,DCO+1)}}$$

DCO Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|------------------------|--|--|-----------------|------|------|------|-------|
| V _{CC} | Supply voltage | RSELx < 14 | | 1.8 | | 3.6 | V |
| | | RSELx = 14 | | 2.2 | | 3.6 | |
| | | RSELx = 15 | | 3.0 | | 3.6 | |
| f _{DCO(0,0)} | DCO frequency (0, 0) | RSELx = 0, DCOx = 0, MODx = 0 | 2.2 V, 3 V | 0.06 | | 0.14 | MHz |
| f _{DCO(0,3)} | DCO frequency (0, 3) | RSELx = 0, DCOx = 3, MODx = 0 | 2.2 V, 3 V | 0.07 | | 0.17 | MHz |
| f _{DCO(1,3)} | DCO frequency (1, 3) | RSELx = 1, DCOx = 3, MODx = 0 | 2.2 V, 3 V | 0.10 | | 0.20 | MHz |
| f _{DCO(2,3)} | DCO frequency (2, 3) | RSELx = 2, DCOx = 3, MODx = 0 | 2.2 V, 3 V | 0.14 | | 0.28 | MHz |
| f _{DCO(3,3)} | DCO frequency (3, 3) | RSELx = 3, DCOx = 3, MODx = 0 | 2.2 V, 3 V | 0.20 | | 0.40 | MHz |
| f _{DCO(4,3)} | DCO frequency (4, 3) | RSELx = 4, DCOx = 3, MODx = 0 | 2.2 V, 3 V | 0.28 | | 0.54 | MHz |
| f _{DCO(5,3)} | DCO frequency (5, 3) | RSELx = 5, DCOx = 3, MODx = 0 | 2.2 V, 3 V | 0.39 | | 0.77 | MHz |
| f _{DCO(6,3)} | DCO frequency (6, 3) | RSELx = 6, DCOx = 3, MODx = 0 | 2.2 V, 3 V | 0.54 | | 1.06 | MHz |
| f _{DCO(7,3)} | DCO frequency (7, 3) | RSELx = 7, DCOx = 3, MODx = 0 | 2.2 V, 3 V | 0.80 | | 1.50 | MHz |
| f _{DCO(8,3)} | DCO frequency (8, 3) | RSELx = 8, DCOx = 3, MODx = 0 | 2.2 V, 3 V | 1.10 | | 2.10 | MHz |
| f _{DCO(9,3)} | DCO frequency (9, 3) | RSELx = 9, DCOx = 3, MODx = 0 | 2.2 V, 3 V | 1.60 | | 3.00 | MHz |
| f _{DCO(10,3)} | DCO frequency (10, 3) | RSELx = 10, DCOx = 3, MODx = 0 | 2.2 V, 3 V | 2.50 | | 4.30 | MHz |
| f _{DCO(11,3)} | DCO frequency (11, 3) | RSELx = 11, DCOx = 3, MODx = 0 | 2.2 V, 3 V | 3.00 | | 5.50 | MHz |
| f _{DCO(12,3)} | DCO frequency (12, 3) | RSELx = 12, DCOx = 3, MODx = 0 | 2.2 V, 3 V | 4.30 | | 7.30 | MHz |
| f _{DCO(13,3)} | DCO frequency (13, 3) | RSELx = 13, DCOx = 3, MODx = 0 | 2.2 V, 3 V | 6.00 | | 9.60 | MHz |
| f _{DCO(14,3)} | DCO frequency (14, 3) | RSELx = 14, DCOx = 3, MODx = 0 | 2.2 V, 3 V | 8.60 | | 13.9 | MHz |
| f _{DCO(15,3)} | DCO frequency (15, 3) | RSELx = 15, DCOx = 3, MODx = 0 | 3 V | 12.0 | | 18.5 | MHz |
| f _{DCO(15,7)} | DCO frequency (15, 7) | RSELx = 15, DCOx = 7, MODx = 0 | 3 V | 16.0 | | 26.0 | MHz |
| S _{RSEL} | Frequency step between range RSEL and RSEL+1 | S _{RSEL} = f _{DCO(RSEL+1,DCO)} /f _{DCO(RSEL,DCO)} | 2.2 V, 3 V | | | 1.55 | ratio |
| S _{DCO} | Frequency step between tap DCO and DCO+1 | S _{DCO} = f _{DCO(RSEL,DCO+1)} /f _{DCO(RSEL,DCO)} | 2.2 V, 3 V | 1.05 | 1.08 | 1.12 | |
| | Duty cycle | Measured at P1.4/SMCLK | 2.2 V, 3 V | 40 | 50 | 60 | % |

Calibrated DCO Frequencies - Tolerance at Calibration

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | T _A | V _{CC} | MIN | TYP | MAX | UNIT |
|--|--|----------------|-----------------|-------|------|-------|------|
| Frequency tolerance at calibration | | 25°C | 3 V | -1 | ±0.2 | +1 | % |
| f _{CAL(1MHz)} 1-MHz calibration value | BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, Gating time: 5 ms | 25°C | 3 V | 0.990 | 1 | 1.010 | MHz |
| f _{CAL(8MHz)} 8-MHz calibration value | BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, Gating time: 5 ms | 25°C | 3 V | 7.920 | 8 | 8.080 | MHz |
| f _{CAL(12MHz)} 12-MHz calibration value | BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, Gating time: 5 ms | 25°C | 3 V | 11.88 | 12 | 12.12 | MHz |
| f _{CAL(16MHz)} 16-MHz calibration value | BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, Gating time: 2 ms | 25°C | 3 V | 15.84 | 16 | 16.16 | MHz |

Calibrated DCO Frequencies - Tolerance Over Temperature 0°C to 85°C

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | T _A | V _{CC} | MIN | TYP | MAX | UNIT |
|--|--|----------------|-----------------|-------|------|-------|------|
| 1-MHz tolerance over temperature | | 0°C to 85°C | 3 V | -2.5 | ±0.5 | +2.5 | % |
| 8-MHz tolerance over temperature | | 0°C to 85°C | 3 V | -2.5 | ±1.0 | +2.5 | % |
| 12-MHz tolerance over temperature | | 0°C to 85°C | 3 V | -2.5 | ±1.0 | +2.5 | % |
| 16-MHz tolerance over temperature | | 0°C to 85°C | 3 V | -3 | ±2.0 | +3 | % |
| f _{CAL(1MHz)} 1-MHz calibration value | BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, Gating time: 5 ms | 0°C to 85°C | 2.2 V | 0.97 | 1 | 1.03 | MHz |
| | | | 3 V | 0.975 | 1 | 1.025 | |
| | | | 3.6 V | 0.97 | 1 | 1.03 | |
| f _{CAL(8MHz)} 8-MHz calibration value | BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, Gating time: 5 ms | 0°C to 85°C | 2.2 V | 7.76 | 8 | 8.4 | MHz |
| | | | 3 V | 7.8 | 8 | 8.2 | |
| | | | 3.6 V | 7.6 | 8 | 8.24 | |
| f _{CAL(12MHz)} 12-MHz calibration value | BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, Gating time: 5 ms | 0°C to 85°C | 2.2 V | 11.7 | 12 | 12.3 | MHz |
| | | | 3 V | 11.7 | 12 | 12.3 | |
| | | | 3.6 V | 11.7 | 12 | 12.3 | |
| f _{CAL(16MHz)} 16-MHz calibration value | BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, Gating time: 2 ms | 0°C to 85°C | 3 V | 15.52 | 16 | 16.48 | MHz |
| | | | 3.6 V | 15 | 16 | 16.48 | |

Calibrated DCO Frequencies - Tolerance Over Supply Voltage V_{CC}

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

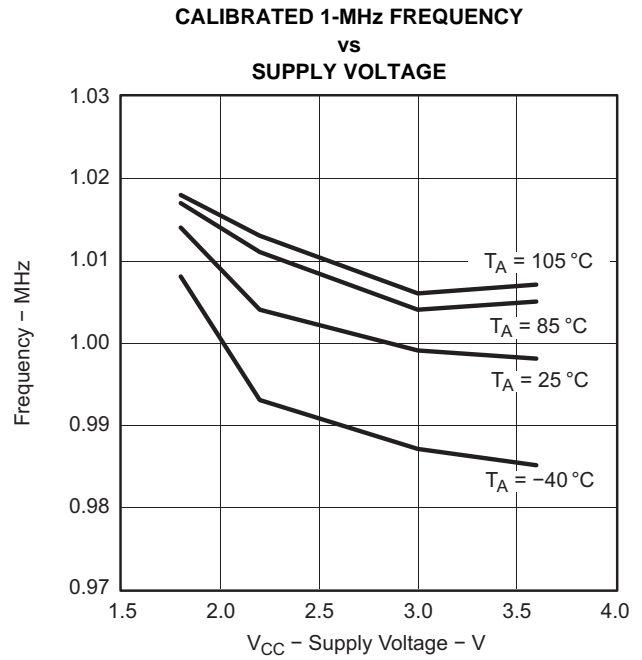
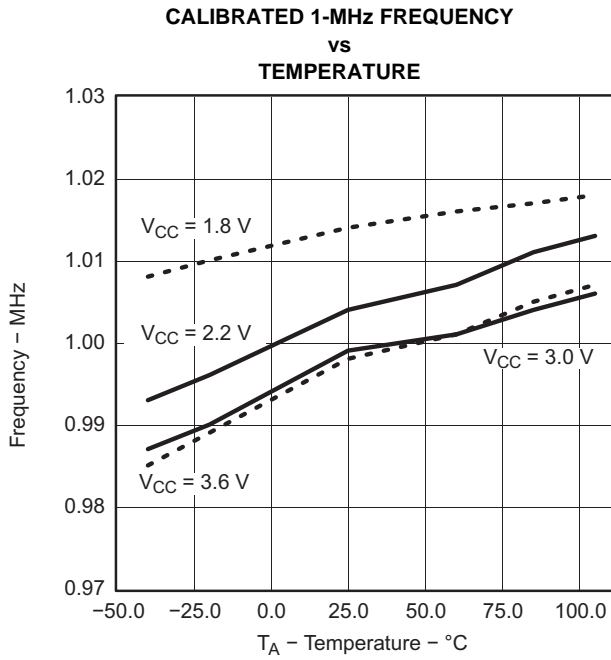
| PARAMETER | TEST CONDITIONS | T_A | V_{CC} | MIN | TYP | MAX | UNIT |
|---|--|-------|----------------|-------|-----|-------|------|
| 1-MHz tolerance over V_{CC} | | 25°C | 1.8 V to 3.6 V | -3 | ±2 | +3 | % |
| 8-MHz tolerance over V_{CC} | | 25°C | 1.8 V to 3.6 V | -3 | ±2 | +3 | % |
| 12-MHz tolerance over V_{CC} | | 25°C | 2.2 V to 3.6 V | -3 | ±2 | +3 | % |
| 16-MHz tolerance over V_{CC} | | 25°C | 3 V to 3.6 V | -6 | ±2 | +3 | % |
| $f_{CAL(1MHz)}$ 1-MHz calibration value | BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, Gating time: 5 ms | 25°C | 1.8 V to 3.6 V | 0.97 | 1 | 1.03 | MHz |
| $f_{CAL(8MHz)}$ 8-MHz calibration value | BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, Gating time: 5 ms | 25°C | 1.8 V to 3.6 V | 7.76 | 8 | 8.24 | MHz |
| $f_{CAL(12MHz)}$ 12-MHz calibration value | BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, Gating time: 5 ms | 25°C | 2.2 V to 3.6 V | 11.64 | 12 | 12.36 | MHz |
| $f_{CAL(16MHz)}$ 16-MHz calibration value | BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, Gating time: 2 ms | 25°C | 3 V to 3.6 V | 15 | 16 | 16.48 | MHz |

Calibrated DCO Frequencies - Overall Tolerance

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | T_A | V_{CC} | MIN | TYP | MAX | UNIT |
|---|--|---------------------------------------|----------------|------|-----|------|------|
| 1-MHz tolerance overall | | I: -40°C to 85°C T: -40°C to 105°C | 1.8 V to 3.6 V | -5 | ±2 | +5 | % |
| 8-MHz tolerance overall | | I: -40°C to 85°C T: -40°C to 105°C | 1.8 V to 3.6 V | -5 | ±2 | +5 | % |
| 12-MHz tolerance overall | | I: -40°C to 85°C T: -40°C to 105°C | 2.2 V to 3.6 V | -5 | ±2 | +5 | % |
| 16-MHz tolerance overall | | I: -40°C to 85°C T: -40°C to 105°C | 3 V to 3.6 V | -6 | ±3 | +6 | % |
| $f_{CAL(1MHz)}$ 1-MHz calibration value | BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, Gating time: 5 ms | I: -40°C to 85°C T: -40°C to 105°C | 1.8 V to 3.6 V | 0.95 | 1 | 1.05 | MHz |
| $f_{CAL(8MHz)}$ 8-MHz calibration value | BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, Gating time: 5 ms | I: -40°C to 85°C T: -40°C to 105°C | 1.8 V to 3.6 V | 7.6 | 8 | 8.4 | MHz |
| $f_{CAL(12MHz)}$ 12-MHz calibration value | BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, Gating time: 5 ms | I: -40°C to 85°C T: -40°C to 105°C | 2.2 V to 3.6 V | 11.4 | 12 | 12.6 | MHz |
| $f_{CAL(16MHz)}$ 16-MHz calibration value | BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, Gating time: 2 ms | I: -40°C to 85°C T: -40°C to 105°C | 3 V to 3.6 V | 15 | 16 | 17 | MHz |

Typical Characteristics - Calibrated 1-MHz DCO Frequency



Wake-Up From Lower-Power Modes (LPM3, LPM4)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|--|--|-----------------|-----|--|-----|------|
| t _{DCO,LPM3/4} DCO clock wake-up time from LPM3 or LPM4 ⁽¹⁾ | BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ | 2.2 V, 3 V | | | 2 | μs |
| | BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ | | | 1.5 | | |
| | BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ | | | 1 | | |
| | BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ | 3 V | | 1 | | |
| t _{CPU,LPM3/4} CPU wake-up time from LPM3 or LPM4 ⁽²⁾ | | | | 1 / f _{MCLK} + t _{clock,LPM3/4} | | |

- (1) The DCO clock wake-up time is measured from the edge of an external wake-up signal (for example, port interrupt) to the first clock edge observable externally on a clock pin (MCLK or SMCLK).
- (2) Parameter applicable only if DCOCLK is used for MCLK.

Typical Characteristics - DCO Clock Wake-Up Time From LPM3 or LPM4

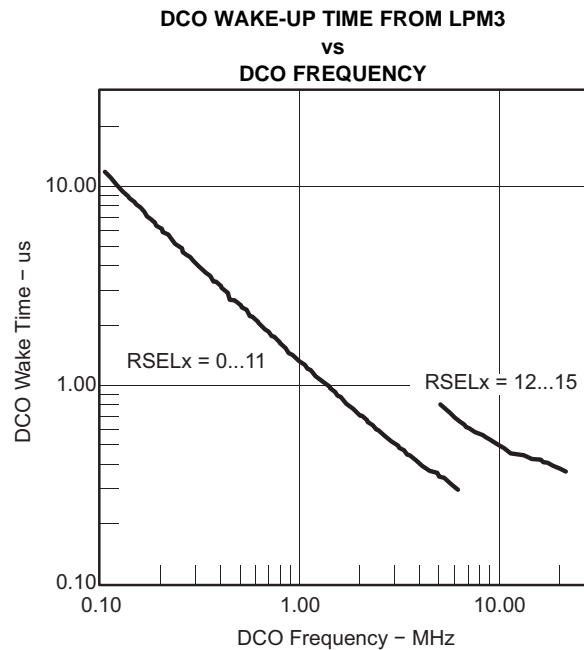


Figure 13.

Crystal Oscillator, XT1, Low-Frequency Mode⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-----------------------------|---|---|-----------------|-------|-------|-------|------|
| f _{LFXT1,LF} | LFXT1 oscillator crystal frequency, LF mode 0, 1 | XTS = 0, LFXT1Sx = 0 or 1 | 1.8 V to 3.6 V | | 32768 | | Hz |
| f _{LFXT1,LF,logic} | LFXT1 oscillator logic level square wave input frequency, LF mode | XTS = 0, LFXT1Sx = 3 | 1.8 V to 3.6 V | 10000 | 32768 | 50000 | Hz |
| O _{A,LF} | Oscillation allowance for LF crystals | XTS = 0, LFXT1Sx = 0, f _{LFXT1,LF} = 32768 Hz, C _{L,eff} = 6 pF | | | 500 | | kΩ |
| | | XTS = 0, LFXT1Sx = 0, f _{LFXT1,LF} = 32768 Hz, C _{L,eff} = 12 pF | | | 200 | | |
| C _{L,eff} | Integrated effective load capacitance, LF mode ⁽²⁾ | XTS = 0, XCAPx = 0 | | | 1 | | pF |
| | | XTS = 0, XCAPx = 1 | | | 5.5 | | |
| | | XTS = 0, XCAPx = 2 | | | 8.5 | | |
| | | XTS = 0, XCAPx = 3 | | | 11 | | |
| | Duty cycle, LF mode | XTS = 0, Measured at P1.0/ACLK, f _{LFXT1,LF} = 32768 Hz | 2.2 V, 3 V | 30 | 50 | 70 | % |
| f _{Fault,LF} | Oscillator fault frequency, LF mode ⁽³⁾ | XTS = 0, LFXT1Sx = 3 ⁽⁴⁾ | 2.2 V, 3 V | 10 | | 10000 | Hz |

- (1) To improve EMI on the XT1 oscillator, the following guidelines should be observed.
 - (a) Keep the trace between the device and the crystal as short as possible.
 - (b) Design a good ground plane around the oscillator pins.
 - (c) Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
 - (d) Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
 - (e) Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
 - (f) If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
 - (g) Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.
- (2) Includes parasitic bond and package capacitance (approximately 2 pF per pin).
Since the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.
- (3) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies in between might set the flag.
- (4) Measured with logic-level input frequency but also applies to operation with crystals.

Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | T _A | V _{CC} | MIN | TYP | MAX | UNIT |
|-------------------------------------|---|---------------------------------------|-----------------|-----|-----|-----|------|
| f _{VLO} | VLO frequency | -40°C to 85°C | 2.2 V, 3 V | 4 | 12 | 20 | kHz |
| | | 105°C | | | | | |
| df _{VLO} /dT | VLO frequency temperature drift ⁽¹⁾ | I: -40°C to 85°C T: -40°C to 105°C | 2.2 V, 3 V | | 0.5 | | %/°C |
| df _{VLO} /dV _{CC} | VLO frequency supply voltage drift ⁽²⁾ | 25°C | 1.8 V to 3.6 V | | 4 | | %/V |

- (1) Calculated using the box method:
I: (MAX(-40 to 85°C) - MIN(-40 to 85°C)) / MIN(-40 to 85°C) / (85°C - (-40°C))
T: (MAX(-40 to 105°C) - MIN(-40 to 105°C)) / MIN(-40 to 105°C) / (105°C - (-40°C))
- (2) Calculated using the box method: (MAX(1.8 to 3.6 V) - MIN(1.8 to 3.6 V)) / MIN(1.8 to 3.6 V) / (3.6 V - 1.8 V)

Timer_A

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

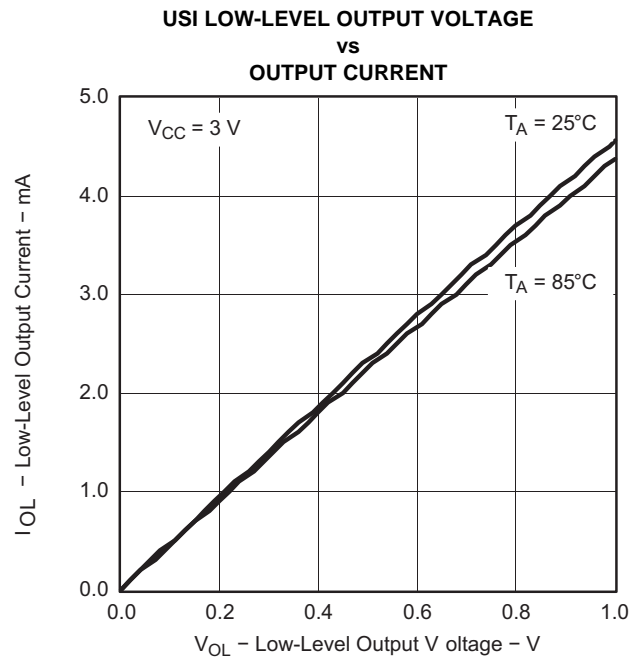
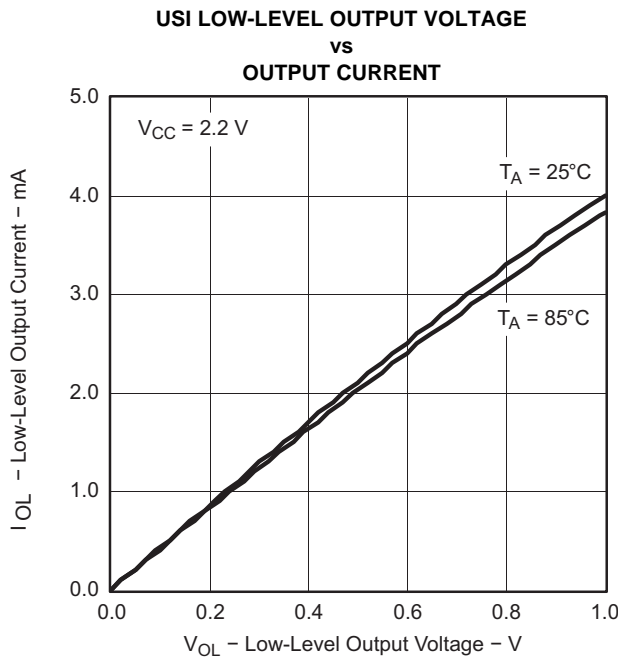
| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|---------------------|-------------------------|---|-----------------|-----|-----|-----|------|
| f _{TA} | Timer_A clock frequency | Internal: SMCLK, ACLK External: TACLK, INCLK Duty cycle = 50% ± 10% | 2.2 V | | | 10 | MHz |
| | | | 3 V | | | 16 | |
| t _{TA,cap} | Timer_A capture timing | TA0, TA1 | 2.2 V, 3 V | 20 | | | ns |

USI, Universal Serial Interface (MSP430F20x2, MSP430F20x3)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|---|---|-----------------|-----------------|-----|-----------------------|------|
| f _{USI} USI clock frequency | External: SCLK, Duty cycle = 50% ±10%, SPI slave mode | 2.2 V | | | 10 | MHz |
| | | 3 V | | | 16 | |
| V _{OL,I2C} Low-level output voltage on SDA and SCL | USI module in I2C mode, I _(OLmax) = 1.5 mA | 2.2 V, 3 V | V _{SS} | | V _{SS} + 0.4 | V |

Typical Characteristics, USI Low-Level Output Voltage on SDA and SCL (MSP430F20x2, MSP430F20x3)



Comparator_A+ (MSP430F20x1)⁽¹⁾

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|------------------------------------|---|---|-----------------|------|------|---------------------|------|
| I _(DD) | | CAON = 1, CARSEL = 0, CAREF = 0 | 2.2 V | | 25 | 40 | μA |
| | | | 3 V | | 45 | 60 | |
| I _(Ref ladder/RefDiode) | | CAON = 1, CARSEL = 0, CAREF = 1/2/3, No load at P1.0/CA0 and P1.1/CA1 | 2.2 V | | 30 | 50 | μA |
| | | | 3 V | | 45 | 71 | |
| V _{IC} | Common-mode input voltage range | CAON = 1 | 2.2 V, 3 V | 0 | | V _{CC} - 1 | V |
| V _(Ref025) | Voltage at 0.25 V _{CC} node / V _{CC} | PCA0 = 1, CARSEL = 1, CAREF = 1, No load at P1.0/CA0 and P1.1/CA1 | 2.2 V, 3 V | 0.23 | 0.24 | 0.25 | |
| V _(Ref050) | Voltage at 0.5 V _{CC} node / V _{CC} | PCA0 = 1, CARSEL = 1, CAREF = 2, No load at P1.0/CA0 and P1.1/CA1 | 2.2 V, 3 V | 0.47 | 0.48 | 0.5 | |
| V _(RefVT) | See Figure 20 and Figure 21 | PCA0 = 1, CARSEL = 1, CAREF = 3, No load at P1.0/CA0 and P1.1/CA1, T _A = 85°C | 2.2 V | 390 | 480 | 540 | mV |
| | | | 3 V | 400 | 490 | 550 | |
| V _p - V _S | Offset voltage ⁽²⁾ | | 2.2 V, 3 V | -30 | | 30 | mV |
| V _{hys} | Input hysteresis | CAON = 1 | 2.2 V, 3 V | 0 | 0.7 | 1.4 | mV |
| t _(response) | Response time (low-high and high-low) | T _A = 25°C, Overdrive 10 mV, Without filter: CAF = 0 ⁽³⁾ (see Figure 16 and Figure 17) | 2.2 V | 80 | 165 | 300 | ns |
| | | | 3 V | 70 | 120 | 240 | |
| | | | 2.2 V | 1.4 | 1.9 | 2.8 | μs |
| | | | | | | | |

(1) The leakage current for the Comparator_A+ terminals is identical to I_{lkg(Px,y)} specification.

(2) The input offset voltage can be cancelled by using the CAEX bit to invert the Comparator_A+ inputs on successive measurements. The two successive measurements are then summed together.

(3) Response time measured at P1.3/CAOUT

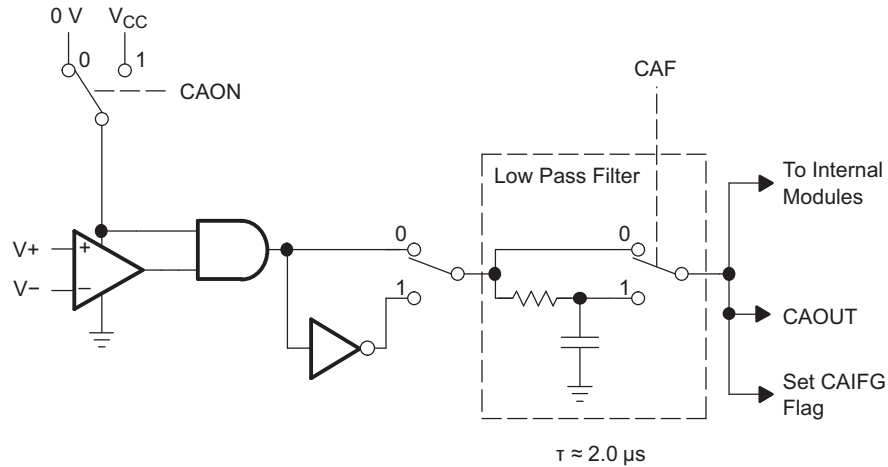


Figure 16. Block Diagram of Comparator_A+ Module

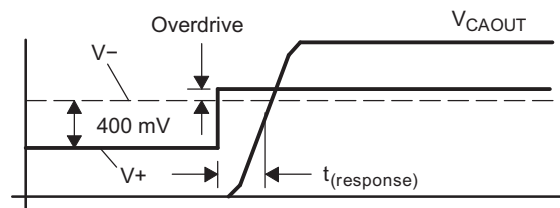


Figure 17. Overdrive Definition

Figure 18. Comparator_A+ Short Resistance Test Condition

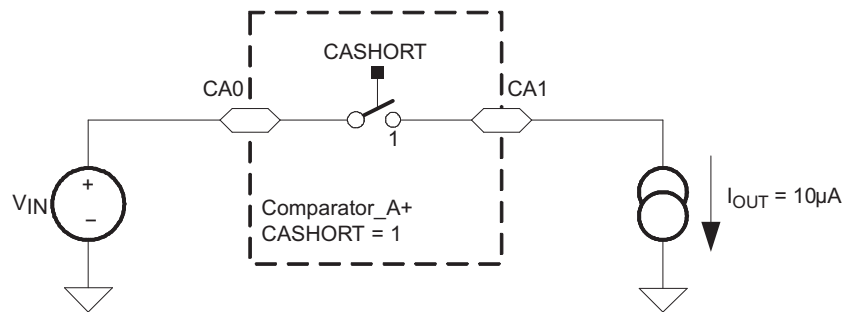


Figure 19. Comparator_A+ Short Resistance Test Condition

Typical Characteristics, Comparator_A+ (MSP430x20x1)

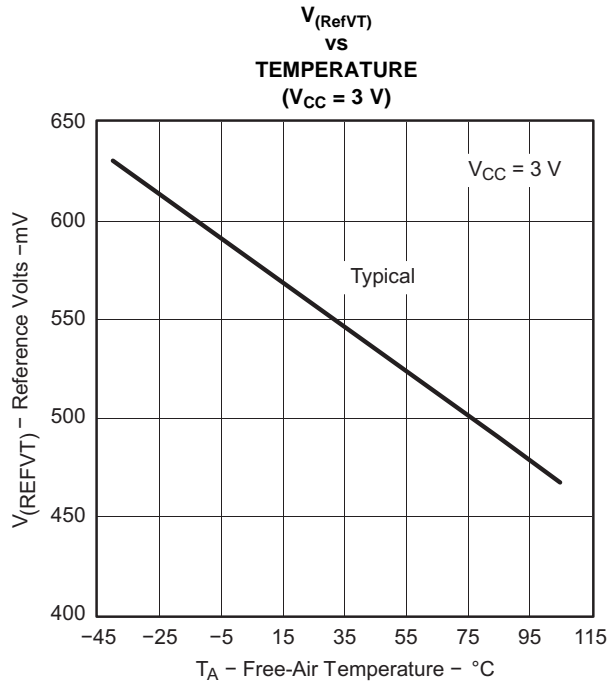


Figure 20.

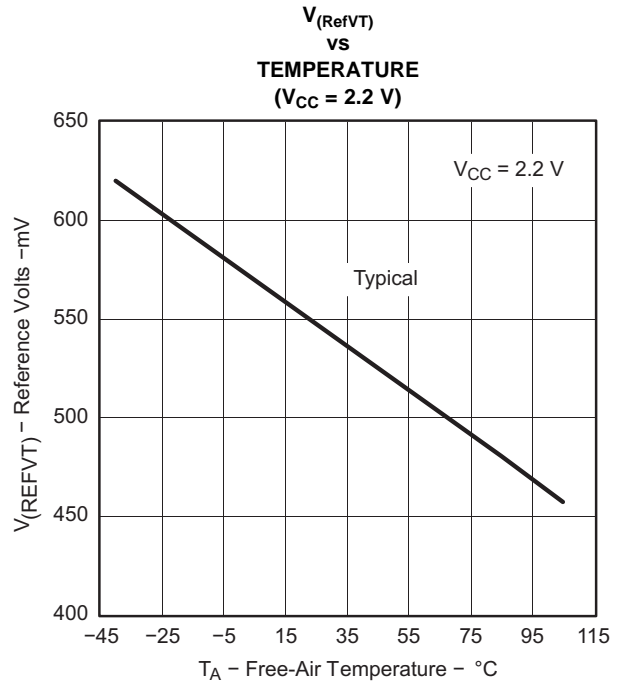


Figure 21.

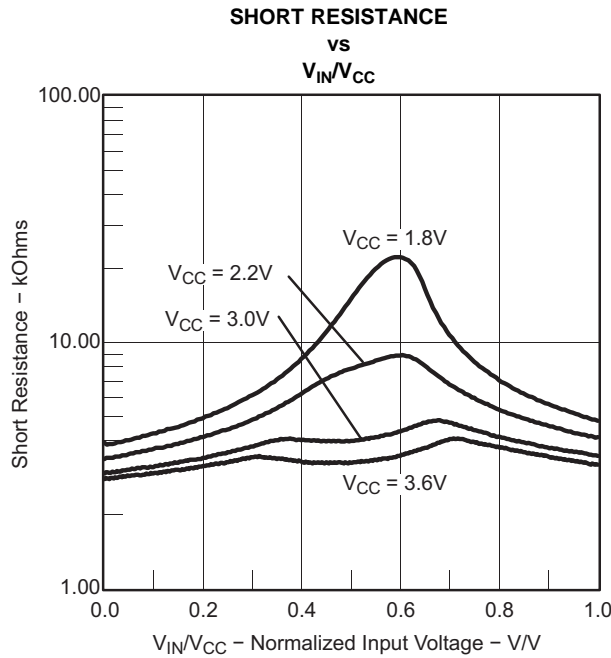


Figure 22.

10-Bit ADC, Power Supply and Input Range Conditions (MSP430F20x2)⁽¹⁾

 over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

| PARAMETER | | TEST CONDITIONS | T _A | V _{CC} | MIN | TYP | MAX | UNIT |
|---------------------|--|--|---------------------------------------|-----------------|------|------|-----------------|------|
| V _{CC} | Analog supply voltage range | V _{SS} = 0 V | | | 2.2 | | 3.6 | V |
| V _{Ax} | Analog input voltage range ⁽²⁾ | All Ax terminals, Analog inputs selected in ADC10AE register | | | 0 | | V _{CC} | V |
| I _{ADC10} | ADC10 supply current ⁽³⁾ | f _{ADC10CLK} = 5 MHz, ADC10ON = 1, REFON = 0, ADC10SHT0 = 1, ADC10SHT1 = 0, ADC10DIV = 0 | I: -40°C to 85°C T: -40°C to 105°C | 2.2 V | 0.52 | 1.05 | mA | |
| | | | | 3 V | 0.6 | 1.2 | | |
| I _{REF+} | Reference supply current, reference buffer disabled ⁽⁴⁾ | f _{ADC10CLK} = 5 MHz, ADC10ON = 0, REF2_5V = 0, REFON = 1, REFOUT = 0 f _{ADC10CLK} = 5 MHz, ADC10ON = 0, REF2_5V = 1, REFON = 1, REFOUT = 0 | I: -40°C to 85°C T: -40°C to 105°C | 2.2 V, 3 V | 0.25 | 0.4 | mA | |
| | | | | 3 V | 0.25 | 0.4 | | |
| I _{REFB,0} | Reference buffer supply current with ADC10SR = 0 ⁽⁴⁾ | f _{ADC10CLK} = 5 MHz, ADC10ON = 0, REFON = 1, REF2_5V = 0, REFOUT = 1, ADC10SR = 0 | -40°C to 85°C | 2.2 V, 3 V | 1.1 | 1.4 | mA | |
| | | | 105°C | 2.2 V, 3 V | | 1.8 | | |
| I _{REFB,1} | Reference buffer supply current with ADC10SR = 1 ⁽⁴⁾ | f _{ADC10CLK} = 5 MHz, ADC10ON = 0, REFON = 1, REF2_5V = 0, REFOUT = 1, ADC10SR = 1 | -40°C to 85°C | 2.2 V, 3 V | 0.5 | 0.7 | mA | |
| | | | 105°C | 2.2 V, 3 V | | 0.8 | | |
| C _I | Input capacitance | Only one terminal Ax selected at a time | I: -40°C to 85°C T: -40°C to 105°C | | | | 27 | pF |
| R _I | Input MUX ON resistance | 0 V ≤ V _{Ax} ≤ V _{CC} | I: -40°C to 85°C T: -40°C to 105°C | 2.2 V, 3 V | | | 2000 | Ω |

- (1) The leakage current is defined in the leakage current table with P_{x.x}/A_x parameter.
- (2) The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion results.
- (3) The internal reference supply current is not included in current consumption parameter I_{ADC10}.
- (4) The internal reference current is supplied via terminal V_{CC}. Consumption is independent of the ADC10ON control bit, unless a conversion is active. The REFON bit enables the built-in reference to settle before starting an A/D conversion.

10-Bit ADC, Built-In Voltage Reference (MSP430F20x2)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | V _{CC} | MIN | TYP | MAX | UNIT |
|---|---|---|-------------|-----------------|------|-----|------|--------|
| V _{CC,REF+} | Positive built-in reference analog supply voltage range | I _{VREF+} ≤ 1 mA, REF2_5V = 0 | | | 2.2 | | | V |
| | | I _{VREF+} ≤ 0.5 mA, REF2_5V = 1 | | | 2.8 | | | |
| | | I _{VREF+} ≤ 1 mA, REF2_5V = 1 | | | 2.9 | | | |
| V _{REF+} | Positive built-in reference voltage | I _{VREF+} ≤ I _{VREF+max} , REF2_5V = 0 | | 2.2 V, 3 V | 1.41 | 1.5 | 1.59 | V |
| | | I _{VREF+} ≤ I _{VREF+max} , REF2_5V = 1 | | 3 V | 2.35 | 2.5 | 2.65 | |
| I _{LD,VREF+} | Maximum V _{REF+} load current | | | 2.2 V | ±0.5 | | | mA |
| | | | | 3 V | ±1 | | | |
| V _{REF+} load regulation | | I _{VREF+} = 500 μA ± 100 μA, Analog input voltage V _{AX} ≈ 0.75 V, REF2_5V = 0 | | 2.2 V, 3 V | ±2 | | | LSB |
| | | I _{VREF+} = 500 μA ± 100 μA, Analog input voltage V _{AX} ≈ 1.25 V, REF2_5V = 1 | | 3 V | ±2 | | | |
| V _{REF+} load regulation response time | | I _{VREF+} = 100 μA to 900 μA, V _{AX} ≈ 0.5 × V _{REF+} , Error of conversion result ≤ 1 LSB | ADC10SR = 0 | 3 V | 400 | | | ns |
| | | | ADC10SR = 1 | | 2000 | | | |
| C _{VREF+} | Maximum capacitance at pin V _{REF+} ⁽¹⁾ | I _{VREF+} ≤ ±1 mA, REFON = 1, REFOUT = 1 | | 2.2 V, 3 V | 100 | | | pF |
| T _{CREF+} | Temperature coefficient | I _{VREF+} = constant with 0 mA ≤ I _{VREF+} ≤ 1 mA | | 2.2 V, 3 V | ±100 | | | ppm/°C |
| t _{REFON} | Settling time of internal reference voltage ⁽²⁾ | I _{VREF+} = 0.5 mA, REF2_5V = 0, REFON = 0 to 1 | | 3.6 V | 30 | | | μs |
| t _{REFBURST} | Settling time of reference buffer ⁽²⁾ | I _{VREF+} = 0.5 mA, REF2_5V = 0, REFON = 1, REFBURST = 1 | ADC10SR = 0 | 2.2 V | 1 | | | μs |
| | | | ADC10SR = 1 | | 2.5 | | | |
| | | I _{VREF+} = 0.5 mA, REF2_5V = 1, REFON = 1, REFBURST = 1 | ADC10SR = 0 | 3 V | 2 | | | |
| | | | ADC10SR = 1 | | 4.5 | | | |

(1) The capacitance applied to the internal buffer operational amplifier, if switched to terminal P1.4/SMCLK/A4/VREF+/VeREF+/TCK (REFOUT = 1), must be limited; otherwise, the reference buffer may become unstable.

(2) The condition is that the error in a conversion started after t_{REFON} or t_{RefBuf} is less than ±0.5 LSB.

10-Bit ADC, External Reference (MSP430F20x2)⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | MAX | UNIT |
|---------------------|---|--|-----------------|-----|-----------------|------|
| V _{eREF+} | Positive external reference input voltage range ⁽²⁾ | V _{eREF+} > V _{eREF-} , SREF1 = 1, SREF0 = 0 | | 1.4 | V _{CC} | V |
| | | V _{eREF-} ≤ V _{eREF+} ≤ V _{CC} - 0.15 V, SREF1 = 1, SREF0 = 1 ⁽³⁾ | | 1.4 | 3 | |
| V _{eREF-} | Negative external reference input voltage range ⁽⁴⁾ | V _{eREF+} > V _{eREF-} | | 0 | 1.2 | V |
| ΔV _{eREF} | Differential external reference input voltage range ΔV _{eREF} = V _{eREF+} - V _{eREF-} | V _{eREF+} > V _{eREF-} ⁽⁵⁾ | | 1.4 | V _{CC} | V |
| I _{VeREF+} | Static input current into V _{eREF+} | 0 V ≤ V _{eREF+} ≤ V _{CC} , SREF1 = 1, SREF0 = 0 | 2.2 V, 3 V | | ±1 | μA |
| | | 0 V ≤ V _{eREF+} ≤ V _{CC} - 0.15 V ≤ 3 V, SREF1 = 1, SREF0 = 1 ⁽³⁾ | | | 0 | |
| I _{VeREF-} | Static input current into V _{eREF-} | 0 V ≤ V _{eREF-} ≤ V _{CC} | 2.2 V, 3 V | | ±1 | μA |

- (1) The external reference is used during conversion to charge and discharge the capacitance array. The input capacitance, C_I, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 10-bit accuracy.
- (2) The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
- (3) Under this condition, the external reference is internally buffered. The reference buffer is active and requires the reference buffer supply current I_{REFB}. The current consumption can be limited to the sample and conversion period with REBURST = 1.
- (4) The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
- (5) The accuracy limits the minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.

10-Bit ADC, Timing Parameters (MSP430F20x2)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-----------------------|---|---|-----------------|-------------|------|--|------|
| f _{ADC10CLK} | ADC10 input clock frequency | For specified performance of ADC10 linearity parameters | 2.2 V, 3 V | ADC10SR = 0 | 0.45 | 6.3 | MHz |
| | | | | ADC10SR = 1 | 0.45 | 1.5 | |
| f _{ADC10OSC} | ADC10 built-in oscillator frequency | ADC10DIVx = 0, ADC10SSELx = 0, f _{ADC10CLK} = f _{ADC10OSC} | 2.2 V, 3 V | 3.7 | | 6.3 | MHz |
| t _{CONVERT} | Conversion time | ADC10 built-in oscillator, ADC10SSELx = 0, f _{ADC10CLK} = f _{ADC10OSC} | 2.2 V, 3 V | 2.06 | | 3.51 | μs |
| | | f _{ADC10CLK} from ACLK, MCLK or SMCLK, ADC10SSELx ≠ 0 | | | | 13 × ADC10DIVx × 1/f _{ADC10CLK} | |
| t _{ADC10ON} | Turn on settling time of the ADC ⁽¹⁾ | | | | | 100 | ns |

- (1) The condition is that the error in a conversion started after t_{ADC10ON} is less than ±0.5 LSB. The reference and input signal are already settled.

10-Bit ADC, Linearity Parameters (MSP430F20x2)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|----------------|------------------------------|---|-----------------|-----|------|-----|------|
| E _I | Integral linearity error | | 2.2 V, 3 V | | | ±1 | LSB |
| E _D | Differential linearity error | | 2.2 V, 3 V | | | ±1 | LSB |
| E _O | Offset error | Source impedance R _S < 100 Ω | 2.2 V, 3 V | | | ±1 | LSB |
| E _G | Gain error | | 2.2 V, 3 V | | ±1.1 | ±2 | LSB |
| E _T | Total unadjusted error | | 2.2 V, 3 V | | ±2 | ±5 | LSB |

10-Bit ADC, Temperature Sensor and Built-In V_{MID} (MSP430F20x2)⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT | | |
|-----------------------------|--|---|-----------------|--|------|------|-------|------|----|
| I _{SENSOR} | Temperature sensor supply current ⁽¹⁾ | REFON = 0, INCHx = 0Ah, T _A = 25°C | 2.2 V | | 40 | 120 | μA | | |
| | | | 3 V | | 60 | 160 | | | |
| TC _{SENSOR} | | ADC10ON = 1, INCHx = 0Ah ⁽²⁾ | 2.2 V, 3 V | 3.44 | 3.55 | 3.66 | mV/°C | | |
| V _{Offset, Sensor} | Sensor offset voltage | ADC10ON = 1, INCHx = 0Ah ⁽²⁾ | | -100 | | 100 | mV | | |
| V _{SENSOR} | Sensor output voltage ⁽³⁾ | | 2.2 V, 3 V | Temperature sensor voltage at T _A = 105°C (T version only) | | 1265 | 1365 | 1465 | mV |
| | | | | Temperature sensor voltage at T _A = 85°C | | 1195 | 1295 | 1395 | |
| | | | | Temperature sensor voltage at T _A = 25°C | | 985 | 1085 | 1185 | |
| | | | | Temperature sensor voltage at T _A = 0°C | | 895 | 995 | 1095 | |
| t _{SENSOR(sample)} | Sample time required if channel 10 is selected ⁽⁴⁾ | ADC10ON = 1, INCHx = 0Ah, Error of conversion result ≤ 1 LSB | 2.2 V, 3 V | 30 | | | μs | | |
| I _{VMID} | Current into divider at channel 11 ⁽⁴⁾ | ADC10ON = 1, INCHx = 0Bh | 2.2 V | | | N/A | μA | | |
| | | | 3 V | | | N/A | | | |
| V _{MID} | V _{CC} divider at channel 11 | ADC10ON = 1, INCHx = 0Bh, V _{MID} ≈ 0.5 × V _{CC} | 2.2 V | 1.06 | 1.1 | 1.14 | V | | |
| | | | 3 V | 1.46 | 1.5 | 1.54 | | | |
| t _{VMID(sample)} | Sample time required if channel 11 is selected ⁽⁵⁾ | ADC10ON = 1, INCHx = 0Bh, Error of conversion result ≤ 1 LSB | 2.2 V | 1400 | | | ns | | |
| | | | 3 V | 1220 | | | | | |

- (1) The sensor current I_{SENSOR} is consumed if (ADC10ON = 1 and REFON = 1), or (ADC10ON = 1 and INCH = 0Ah and sample signal is high). When REFON = 1, I_{SENSOR} is included in I_{REF+}. When REFON = 0, I_{SENSOR} applies during conversion of the temperature sensor input (INCH = 0Ah).
- (2) The following formula can be used to calculate the temperature sensor output voltage:
V_{Sensor,typ} = TC_{Sensor} (273 + T [°C]) + V_{Offset,sensor} [mV] or
V_{Sensor,typ} = TC_{Sensor} T [°C] + V_{Sensor}(T_A = 0°C) [mV]
- (3) Results based on characterization and/or production test, not TC_{Sensor} or V_{Offset,sensor}.
- (4) No additional current is needed. The V_{MID} is used during sampling.
- (5) The on time, t_{VMID(on)}, is included in the sampling time, t_{VMID(sample)}; no additional on time is needed.

SD16_A, Power Supply and Recommended Operating Conditions (MSP430F20x3)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | T _A | V _{CC} | MIN | TYP | MAX | UNIT |
|-------------------|--|--|---------------|----------------|-----------------|------|------|------|------|
| AV _{CC} | Analog supply voltage range | AV _{CC} = DV _{CC} = V _{CC} , AV _{SS} = DV _{SS} = V _{SS} = 0 V | | | | 2.5 | | 3.6 | V |
| I _{SD16} | Analog supply current including internal reference | SD16LP = 0, f _{SD16} = 1 MHz, SD16OSR = 256 | GAIN: 1,2 | -40°C to 85°C | 3 V | | 730 | 1050 | μA |
| | | | | 105°C | | | 1170 | | |
| | | | GAIN: 4,8,16 | -40°C to 85°C | | | 810 | 1150 | |
| | | | | 105°C | | | 1300 | | |
| | | GAIN: 32 | -40°C to 85°C | | | 1160 | 1700 | | |
| | | | 105°C | | | 1850 | | | |
| | | SD16LP = 1, f _{SD16} = 0.5 MHz, SD16OSR = 256 | GAIN: 1 | -40°C to 85°C | | | 720 | 1030 | |
| | | | | 105°C | | | 1160 | | |
| | GAIN: 32 | -40°C to 85°C | | 810 | 1150 | | | | |
| | | 105°C | | 1300 | | | | | |
| f _{SD16} | SD16 input clock frequency | SD16LP = 0 (Low power mode disabled) | | | 3 V | 0.03 | 1 | 1.1 | MHz |
| | | SD16LP = 1 (Low power mode enabled) | | | | 0.03 | 0.5 | | |

SD16_A, Input Range (MSP430F20x3)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | V _{CC} | MIN | TYP | MAX | UNIT |
|---------------------|---|----------------------------|----------------|-----------------|------------------------|------|---------------------|------|
| V _{ID,FSR} | Differential full scale input voltage range ⁽¹⁾ | Bipolar mode, SD16UNI = 0 | | | $-(V_{REF}/2)/GAIN$ | | $+(V_{REF}/2)/GAIN$ | mV |
| | | Unipolar mode, SD16UNI = 1 | | | 0 | | $+(V_{REF}/2)/GAIN$ | |
| V _{ID} | Differential input voltage range for specified performance ⁽¹⁾ | SD16REFON = 1 | SD16GAINx = 1 | | | ±500 | | mV |
| | | | SD16GAINx = 2 | | | ±250 | | |
| | | | SD16GAINx = 4 | | | ±125 | | |
| | | | SD16GAINx = 8 | | | ±62 | | |
| | | | SD16GAINx = 16 | | | ±31 | | |
| | | | SD16GAINx = 32 | | | ±15 | | |
| Z _I | Input impedance (one input pin to AV _{SS}) | f _{SD16} = 1 MHz | SD16GAINx = 1 | 3 V | | 200 | | kΩ |
| | | | SD16GAINx = 32 | | | 75 | | |
| Z _{ID} | Differential input impedance (IN+ to IN-) | f _{SD16} = 1 MHz | SD16GAINx = 1 | 3 V | 300 | 400 | | kΩ |
| | | | SD16GAINx = 32 | | 100 | 150 | | |
| V _I | Absolute input voltage range | | | | AV _{SS} - 0.1 | | AV _{CC} | V |
| V _{IC} | Common-mode input voltage range | | | | AV _{SS} - 0.1 | | AV _{CC} | V |

(1) The analog input range depends on the reference voltage applied to V_{REF}. If V_{REF} is sourced externally, the full-scale range is defined by V_{FSR+} = +(V_{REF}/2)/GAIN and V_{FSR-} = -(V_{REF}/2)/GAIN. The analog input range should not exceed 80% of V_{FSR+} or V_{FSR-}.

SD16_A, SINAD Performance ($f_{SD16} = 1 \text{ MHz}$, $SD16OSRx = 1024$, $SD16REFON = 1$) (MSP430F20x3)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V_{CC} | PW, N | | RSA | | UNIT |
|---|--|----------|-------|-----|-----|-----|------|
| | | | MIN | TYP | MIN | TYP | |
| SINAD ₁₀₂₄ Signal-to-noise + distortion ratio (OSR = 1024) | SD16GAINx = 1, Signal amplitude: $V_{IN} = 500 \text{ mV}$, Signal frequency: $f_{IN} = 100 \text{ Hz}$ | 3 V | 84 | 85 | 86 | 87 | dB |
| | SD16GAINx = 2, Signal amplitude: $V_{IN} = 250 \text{ mV}$, Signal frequency: $f_{IN} = 100 \text{ Hz}$ | | 82 | 83 | 82 | 83 | |
| | SD16GAINx = 4, Signal amplitude: $V_{IN} = 125 \text{ mV}$, Signal frequency: $f_{IN} = 100 \text{ Hz}$ | | 78 | 79 | 78 | 79 | |
| | SD16GAINx = 8, Signal amplitude: $V_{IN} = 62 \text{ mV}$, Signal frequency: $f_{IN} = 100 \text{ Hz}$ | | 73 | 74 | 73 | 74 | |
| | SD16GAINx = 16, Signal amplitude: $V_{IN} = 31 \text{ mV}$, Signal frequency: $f_{IN} = 100 \text{ Hz}$ | | 68 | 69 | 68 | 69 | |
| | SD16GAINx = 32, Signal amplitude: $V_{IN} = 15 \text{ mV}$, Signal frequency: $f_{IN} = 100 \text{ Hz}$ | | 62 | 63 | 62 | 63 | |

SD16_A, SINAD Performance ($f_{SD16} = 1 \text{ MHz}$, $SD16OSRx = 256$, $SD16REFON = 1$) (MSP430F20x3)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V_{CC} | PW, N | | RSA | | UNIT |
|---|--|----------|-------|-----|-----|-----|------|
| | | | MIN | TYP | MIN | TYP | |
| SINAD ₂₅₆ Signal-to-noise + distortion ratio (OSR = 256) | SD16GAINx = 1, Signal amplitude: $V_{IN} = 500 \text{ mV}$, Signal frequency: $f_{IN} = 100 \text{ Hz}$ | 3 V | 80 | 81 | 82 | 83 | dB |
| | SD16GAINx = 2, Signal amplitude: $V_{IN} = 250 \text{ mV}$, Signal frequency: $f_{IN} = 100 \text{ Hz}$ | | 74 | 75 | 76 | 77 | |
| | SD16GAINx = 4, Signal amplitude: $V_{IN} = 125 \text{ mV}$, Signal frequency: $f_{IN} = 100 \text{ Hz}$ | | 69 | 70 | 71 | 72 | |
| | SD16GAINx = 8, Signal amplitude: $V_{IN} = 62 \text{ mV}$, Signal frequency: $f_{IN} = 100 \text{ Hz}$ | | 63 | 64 | 67 | 68 | |
| | SD16GAINx = 16, Signal amplitude: $V_{IN} = 31 \text{ mV}$, Signal frequency: $f_{IN} = 100 \text{ Hz}$ | | 58 | 59 | 63 | 64 | |
| | SD16GAINx = 32, Signal amplitude: $V_{IN} = 15 \text{ mV}$, Signal frequency: $f_{IN} = 100 \text{ Hz}$ | | 52 | 53 | 57 | 58 | |

Typical Characteristics, SD16_A SINAD Performance Over OSR (MSP430F20x3)

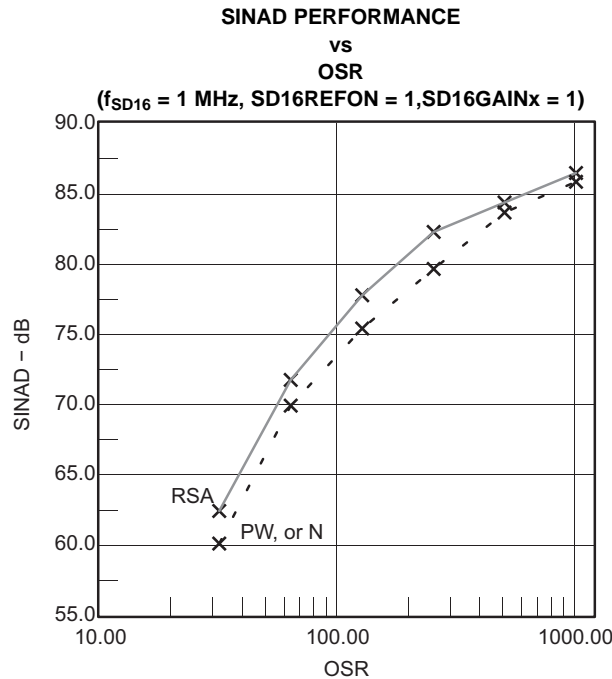


Figure 23.

SD16_A, Performance ($f_{SD16} = 1$ MHz, $SD16OSRx = 256$, $SD16REFON = 1$) (MSP430F20x3)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT | |
|--------------------------|--------------------------------------|-----------------|----------------|-------|-------|------------|-------|
| G | Nominal gain | 3 V | 0.97 | 1.00 | 1.02 | | |
| | | | SD16GAINx = 2 | 1.90 | 1.96 | | 2.02 |
| | | | SD16GAINx = 4 | 3.76 | 3.86 | | 3.96 |
| | | | SD16GAINx = 8 | 7.36 | 7.62 | | 7.84 |
| | | | SD16GAINx = 16 | 14.56 | 15.04 | | 15.52 |
| | | | SD16GAINx = 32 | 27.20 | 28.35 | | 29.76 |
| $\Delta G/\Delta T$ | Gain temperature drift | 3 V | | 15 | | ppm/°C | |
| E _{OS} | Offset error | 3 V | | | ±0.2 | %FSR | |
| | | | | | ±1.5 | | |
| $\Delta E_{OS}/\Delta T$ | Offset error temperature coefficient | 3 V | | ±4 | ±20 | ppm FSR/°C | |
| | | | | ±20 | ±100 | | |
| CMRR | Common-mode rejection ratio | 3 V | | >90 | | dB | |
| | | | | | >75 | | |
| DC PSR | DC power supply rejection | 2.5 V to 3.6 V | | 0.35 | | %V | |
| AC PSRR | AC power supply rejection ratio | 3 V | | >80 | | dB | |

(1) Calculated using the box method: (MAX(-40°C to 85°C) - MIN(-40°C to 85°C)) / MIN(-40°C to 85°C) / (85°C - (-40°C))

(2) Calculated using the ADC output code and the box method:

(MAX-code(2.5 V to 3.6 V) - MIN-code(2.5 V to 3.6 V)) / MIN-code(2.5 V to 3.6 V) / (3.6 V - 2.5 V)

SD16_A, Built-In Voltage Reference (MSP430F20x3)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | T _A | V _{CC} | MIN | TYP | MAX | UNIT |
|-------------------|--|---|----------------|-----------------|------|------|------|--------|
| V _{REF} | Internal reference voltage | SD16REFON = 1, SD16VMIDON = 0 | | 3 V | 1.14 | 1.20 | 1.26 | V |
| I _{REF} | Reference supply current | SD16REFON = 1, SD16VMIDON = 0 | -40°C to 85°C | 3 V | | 190 | 280 | μA |
| | | | 105°C | | | | | |
| TC | Temperature coefficient | SD16REFON = 1, SD16VMIDON = 0 | | 3 V | | 18 | 50 | ppm/°C |
| C _{REF} | V _{REF} load capacitance | SD16REFON = 1, SD16VMIDON = 0 ⁽¹⁾ | | | | 100 | | nF |
| I _{LOAD} | V _{REF(I)} maximum load current | SD16REFON = 1, SD16VMIDON = 0 | | 3 V | | | ±200 | nA |
| t _{ON} | Turn-on time | SD16REFON = 0 → 1, SD16VMIDON = 0, C _{REF} = 100 nF | | 3 V | | 5 | | ms |
| DC PSR | DC power supply rejection ΔV _{REF} /ΔV _{CC} | SD16REFON = 1, SD16VMIDON = 0, V _{CC} = 2.5 V to 3.6 V | | 2.5 V to 3.6 V | | 100 | | μV/V |

(1) There is no capacitance required on V_{REF}. However, a capacitance of at least 100 nF is recommended to reduce any reference voltage noise.

SD16_A, Reference Output Buffer (MSP430F20x3)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | T _A | V _{CC} | MIN | TYP | MAX | UNIT |
|-----------------------|--|--|----------------|-----------------|-----|-----|-----|------|
| V _{REF,BUF} | Reference buffer output voltage | SD16REFON = 1, SD16VMIDON = 1 | | 3 V | | 1.2 | | V |
| I _{REF,BUF} | Reference supply + reference output buffer quiescent current | SD16REFON = 1, SD16VMIDON = 1 | -40°C to 85°C | 3 V | | 385 | 600 | μA |
| | | | 105°C | | | | | |
| C _{REF(O)} | Required load capacitance on V _{REF} | SD16REFON = 1, SD16VMIDON = 1 | | | | 470 | | nF |
| I _{LOAD,Max} | Maximum load current on V _{REF} | SD16REFON = 1, SD16VMIDON = 1 | | 3 V | | | ±1 | mA |
| | Maximum voltage variation vs load current | I _{LOAD} = 0 to 1 mA | | 3 V | | -15 | +15 | mV |
| t _{ON} | Turn on time | SD16REFON = 0 → 1, SD16VMIDON = 1, C _{REF} = 470 nF | | 3 V | | 100 | | μs |

SD16_A, External Reference Input (MSP430F20x3)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|---------------------|---------------------|-----------------|-----------------|-----|------|-----|------|
| V _{REF(I)} | Input voltage range | SD16REFON = 0 | 3 V | 1 | 1.25 | 1.5 | V |
| I _{REF(I)} | Input current | SD16REFON = 0 | 3 V | | | 50 | nA |

SD16_A, Temperature Sensor⁽¹⁾ (MSP430F20x3)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|----------------------------|--------------------------------------|---|-----------------|------|------|------|-------|
| TC _{Sensor} | Sensor temperature coefficient | | | 1.18 | 1.32 | 1.46 | mV/°C |
| V _{Offset,Sensor} | Sensor offset voltage | | | -100 | | 100 | mV |
| V _{Sensor} | Sensor output voltage ⁽²⁾ | Temperature sensor voltage at T _A = 85°C | 3 V | 435 | 475 | 515 | mV |
| | | Temperature sensor voltage at T _A = 25°C | | 355 | 395 | 435 | |
| | | Temperature sensor voltage at T _A = 0°C | | 320 | 360 | 400 | |

(1) Values are not based on calculations using TC_{Sensor} or V_{Offset,sensor} but on measurements.

(2) The following formula can be used to calculate the temperature sensor output voltage:

$$V_{\text{Sensor,typ}} = TC_{\text{Sensor}} (273 + T [^{\circ}\text{C}]) + V_{\text{Offset,sensor}} [\text{mV}] \text{ or}$$

$$V_{\text{Sensor,typ}} = TC_{\text{Sensor}} T [^{\circ}\text{C}] + V_{\text{Sensor}}(T_A = 0^{\circ}\text{C}) [\text{mV}]$$

Flash Memory

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|----------------------------|---|-----------------------|-----------------|-----------------|-----------------|-----|------------------|
| V _{CC(PGM/ERASE)} | Program and erase supply voltage | | | 2.2 | | 3.6 | V |
| f _{FTG} | Flash timing generator frequency | | | 257 | | 476 | kHz |
| I _{PGM} | Supply current from V _{CC} during program | | 2.2 V/3.6 V | | 1 | 5 | mA |
| I _{ERASE} | Supply current from V _{CC} during erase | | 2.2 V/3.6 V | | 1 | 7 | mA |
| t _{CPT} | Cumulative program time ⁽¹⁾ | | 2.2 V/3.6 V | | | 10 | ms |
| t _{CMErase} | Cumulative mass erase time | | 2.2 V/3.6 V | 20 | | | ms |
| | Program/erase endurance | | | 10 ⁴ | 10 ⁵ | | cycles |
| t _{Retention} | Data retention duration | T _J = 25°C | | 100 | | | years |
| t _{Word} | Word or byte program time | ⁽²⁾ | | | 30 | | t _{FTG} |
| t _{Block, 0} | Block program time for first byte or word | ⁽²⁾ | | | 25 | | t _{FTG} |
| t _{Block, 1-63} | Block program time for each additional byte or word | ⁽²⁾ | | | 18 | | t _{FTG} |
| t _{Block, End} | Block program end-sequence wait time | ⁽²⁾ | | | 6 | | t _{FTG} |
| t _{Mass Erase} | Mass erase time | ⁽²⁾ | | | 10593 | | t _{FTG} |
| t _{Seg Erase} | Segment erase time | ⁽²⁾ | | | 4819 | | t _{FTG} |

(1) The cumulative program time must not be exceeded when writing to a 64-byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.

(2) These values are hardwired into the Flash Controller's state machine (t_{FTG} = 1/f_{FTG}).

RAM

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---------------------|---|-----------------|-----|-----|------|
| V _(RAMh) | RAM retention supply voltage ⁽¹⁾ | CPU halted | 1.6 | | V |

(1) This parameter defines the minimum supply voltage V_{CC} when the data in RAM remains unchanged. No program execution should happen during this supply voltage condition.

JTAG and Spy-Bi-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | V _{CC} | MIN | TYP | MAX | UNIT |
|-----------------------|---|-----------------|-------|-----|-----|------|
| f _{SBW} | Spy-Bi-Wire input frequency | 2.2 V, 3 V | 0 | | 20 | MHz |
| t _{SBW,Low} | Spy-Bi-Wire low clock pulse length | 2.2 V, 3 V | 0.025 | | 15 | μs |
| t _{SBW,En} | Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge ⁽¹⁾) | 2.2 V, 3 V | | | 1 | μs |
| t _{SBW,Ret} | Spy-Bi-Wire return to normal operation time | 2.2 V, 3 V | 15 | | 100 | μs |
| f _{TCK} | TCK input frequency ⁽²⁾ | 2.2 V | 0 | | 5 | MHz |
| | | 3 V | 0 | | 10 | MHz |
| R _{Internal} | Internal pulldown resistance on TEST | 2.2 V, 3 V | 25 | 60 | 90 | kΩ |

(1) Tools accessing the Spy-Bi-Wire interface need to wait for the maximum t_{SBW,En} time after pulling the TEST/SBWCLK pin high before applying the first SBWCLK clock edge.

(2) f_{TCK} may be restricted to meet the timing requirements of the module selected.

JTAG Fuse⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---------------------|---|-----------------------|-----|-----|------|
| V _{CC(FB)} | Supply voltage during fuse-blow condition | T _A = 25°C | 2.5 | | V |
| V _{FB} | Voltage level on TEST for fuse blow | | 6 | 7 | V |
| I _{FB} | Supply current into TEST during fuse blow | | | 100 | mA |
| t _{FB} | Time to blow fuse | | | 1 | ms |

(1) Once the fuse is blown, no further access to the JTAG/Test, Spy-Bi-Wire, and emulation feature is possible, and JTAG is switched to bypass mode.

APPLICATION INFORMATION, MSP430F20X1

Port P1 (P1.0 to P1.3) Pin Schematics, MSP430F20x1

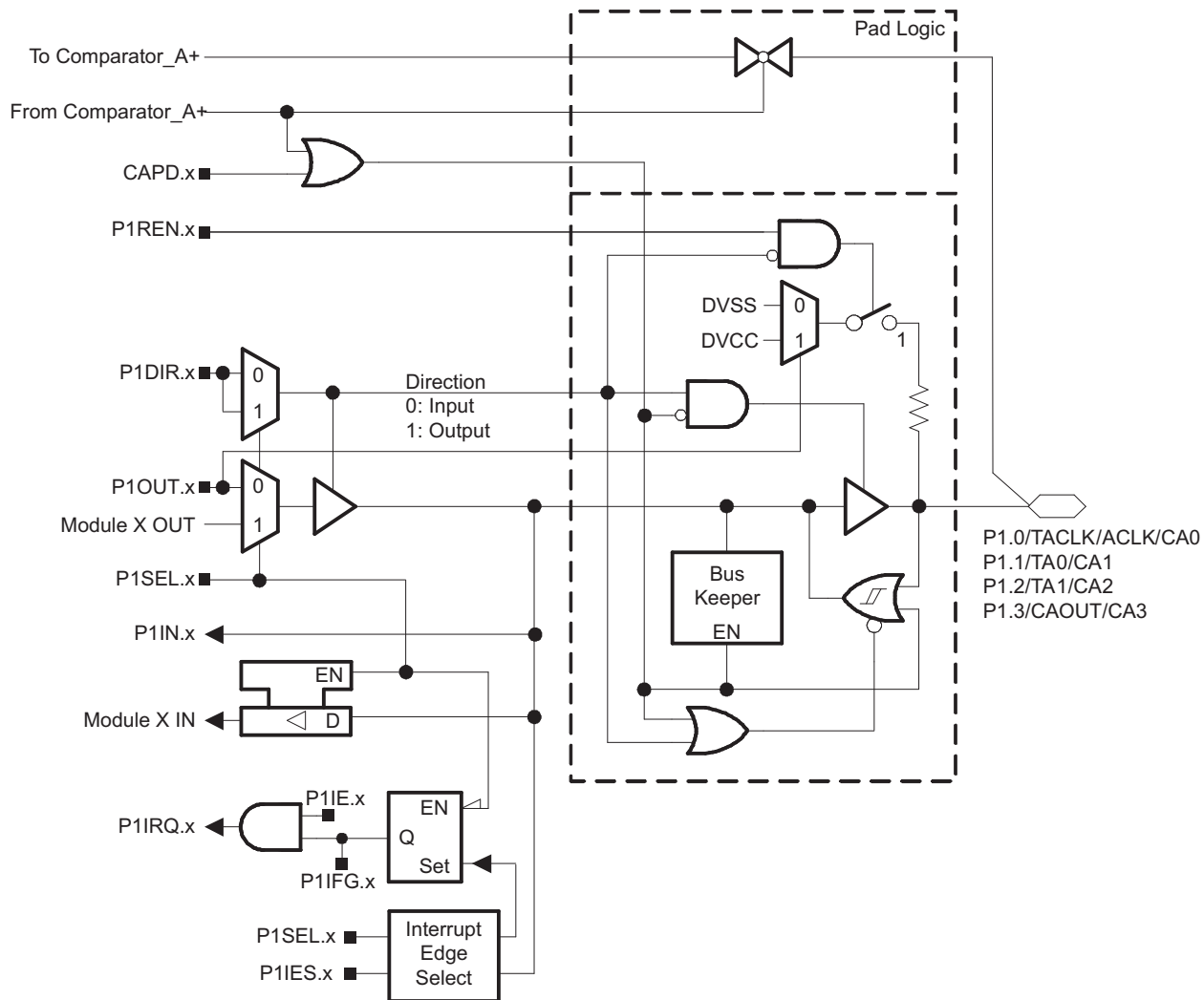


Table 16. Control Signal "From Comparator_A+"

| PIN NAME | FUNCTION | SIGNAL "From Comparator_A+" = 1 ⁽¹⁾ | | | | | |
|---------------------|----------|--|-------|----|-------|-------|-------|
| | | P2CA4 | P2CA0 | OR | P2CA3 | P2CA2 | P2CA1 |
| P1.0/TACLK/ACLK/CA0 | CA0 | 0 | 1 | | N/A | N/A | N/A |
| P1.1/TA0/CA1 | CA1 | 1 | 0 | | 0 | 0 | 1 |
| P1.2/TA1/CA2 | CA2 | 1 | 1 | | 0 | 1 | 0 |
| P1.3/CAOUT/CA3 | CA3 | N/A | N/A | 0 | 1 | 1 | |

(1) N/A = Not available or not applicable

Table 17. Port P1 (P1.0 to P1.3) Pin Functions, MSP430F20x1

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS / SIGNALS ⁽¹⁾ | | |
|---------------------|---|----------------------------------|---------------------------------------|---------|--------|
| | | | P1DIR.x | P1SEL.x | CAPD.x |
| P1.0/TACLK/ACLK/CA0 | 0 | P1.0 ⁽²⁾ input/output | 0/1 | 0 | 0 |
| | | Timer_A2.TACLK/INCLK | 0 | 1 | 0 |
| | | ACLK | 1 | 1 | 0 |
| | | CA0 ⁽³⁾ | X | X | 1 |
| P1.1/TA0/CA1 | 1 | P1.1 ⁽²⁾ input/output | 0/1 | 0 | 0 |
| | | Timer_A2.CCI0A | 0 | 1 | 0 |
| | | Timer_A2.TA0 | 1 | 1 | 0 |
| | | CA1 ⁽³⁾ | X | X | 1 |
| P1.2/TA1/CA2 | 2 | P1.2 ⁽²⁾ input/output | 0/1 | 0 | 0 |
| | | Timer_A2.CCI1A | 0 | 1 | 0 |
| | | Timer_A2.TA1 | 1 | 1 | 0 |
| | | CA2 ⁽³⁾ | X | X | 1 |
| P1.3/CAOUT/CA3 | 3 | P1.3 ⁽²⁾ input/output | 0/1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | CAOUT | 1 | 1 | 0 |
| | | CA3 ⁽³⁾ | X | X | 1 |

(1) X = Don't care

(2) Default after reset (PUC/POR)

(3) Setting the CAPD.x bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the CAx input pin to the comparator multiplexer with the P2CAx bits automatically disables the input buffer for that pin, regardless of the state of the associated CAPD.x bit.

Port P1 (P1.4 to P1.6) Pin Schematics, MSP430F20x1

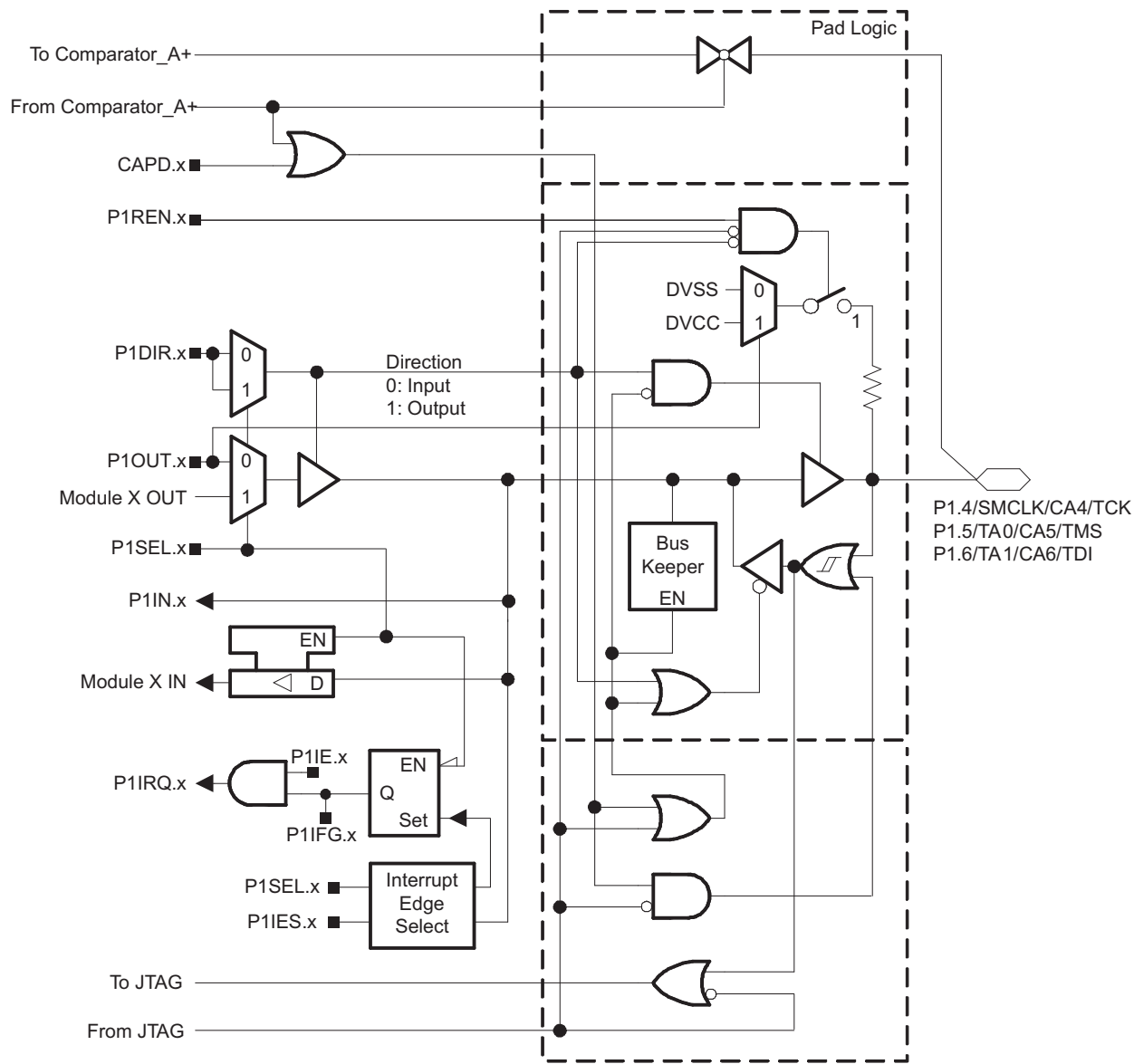


Table 18. Control Signal "From Comparator_A+"

| PIN NAME | FUNCTION | SIGNAL "From Comparator_A+" = 1 | | |
|--------------------|----------|---------------------------------|-------|-------|
| | | P2CA3 | P2CA2 | P2CA1 |
| P1.4/SMCLK/CA4/TCK | CA4 | 1 | 0 | 0 |
| P1.5/TA0/CA5/TMS | CA5 | 1 | 0 | 1 |
| P1.6/TA1/CA6/TDI | CA6 | 1 | 1 | 0 |

Port P1 (P1.7) Pin Schematics, MSP430F20x1

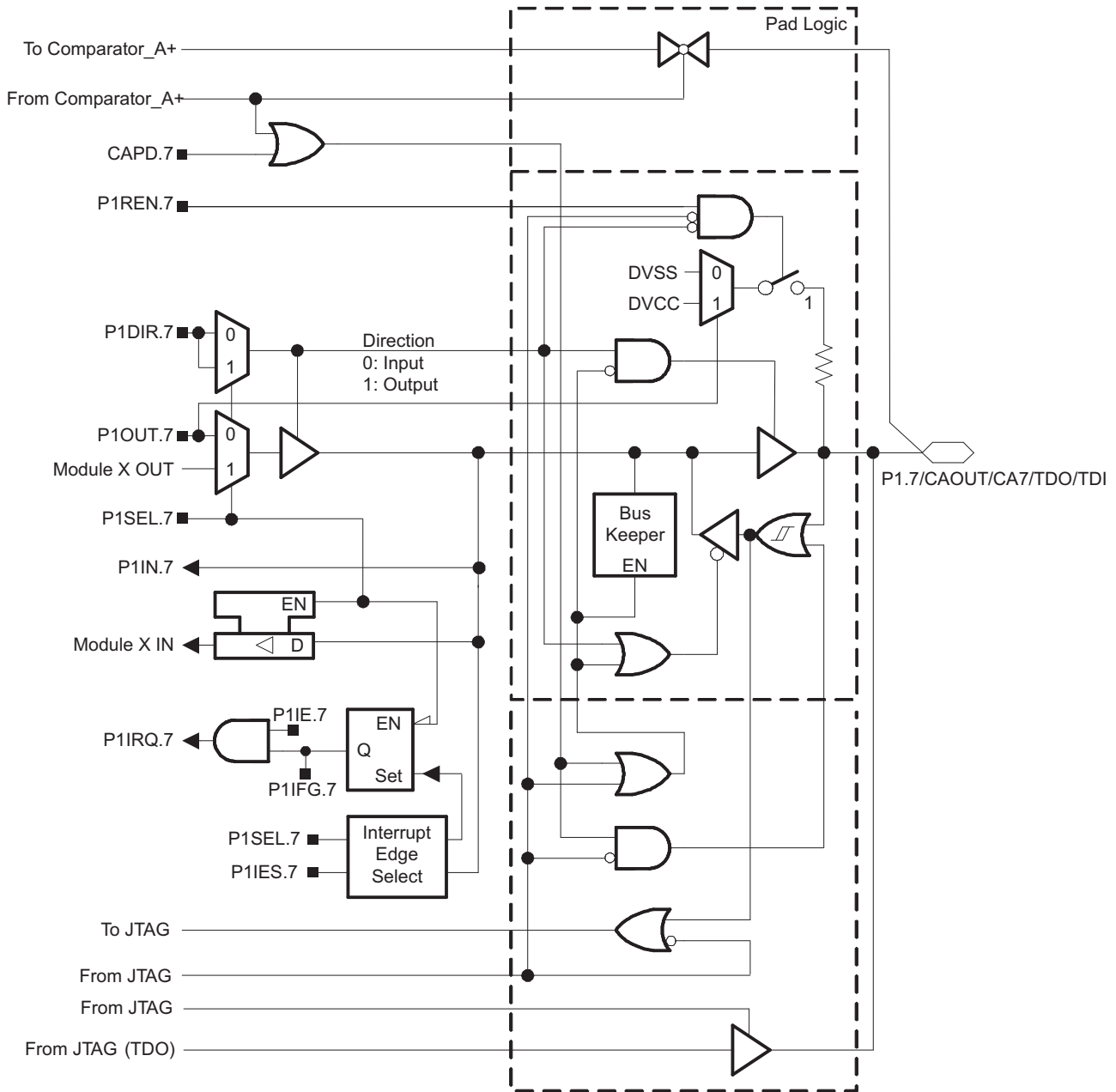


Table 19. Control Signal "From Comparator_A+"

| PIN NAME | FUNCTION | SIGNAL "From Comparator_A+" = 1 | | |
|------------------------|----------|---------------------------------|-------|-------|
| | | P2CA3 | P2CA2 | P2CA1 |
| P1.7/CAOUT/CA7/TDO/TDI | CA7 | 1 | 1 | 1 |

Table 20. Port P1 (P1.4 to P1.7) Pin Functions, MSP430F20x1

| PIN NAME (P1.x) | x | FUNCTION ⁽¹⁾ | CONTROL BITS / SIGNALS ⁽²⁾ | | | |
|------------------------|---|----------------------------------|---------------------------------------|---------|--------|-----------|
| | | | P1DIR.x | P1SEL.x | CAPD.x | JTAG Mode |
| P1.4/SMCLK/CA4/TCK | 4 | P1.4 ⁽³⁾ input/output | 0/1 | 0 | 0 | 0 |
| | | N/A | 0 | 1 | 0 | 0 |
| | | SMCLK | 1 | 1 | 0 | 0 |
| | | CA4 ⁽⁴⁾ | X | X | 1 | 0 |
| | | TCK ⁽⁵⁾ | X | X | X | 1 |
| P1.5/TA0/CA5/TMS | 5 | P1.5 ⁽³⁾ input/output | 0/1 | 0 | 0 | 0 |
| | | N/A | 0 | 1 | 0 | 0 |
| | | Timer_A2.TA0 | 1 | 1 | 0 | 0 |
| | | CA5 ⁽⁴⁾ | X | X | 1 | 0 |
| | | TMS ⁽⁵⁾ | X | X | X | 1 |
| P1.6/TA1/CA6/TDI | 6 | P1.6 ⁽³⁾ input/output | 0/1 | 0 | 0 | 0 |
| | | N/A | 0 | 1 | 0 | 0 |
| | | Timer_A2.TA1 | 1 | 1 | 0 | 0 |
| | | CA6 ⁽⁴⁾ | X | X | 1 | 0 |
| | | TDI ⁽⁵⁾ | X | X | X | 1 |
| P1.7/CAOUT/CA7/TDO/TDI | 7 | P1.7 ⁽³⁾ input/output | 0/1 | 0 | 0 | 0 |
| | | N/A | 0 | 1 | 0 | 0 |
| | | CAOUT | 1 | 1 | 0 | 0 |
| | | CA7 ⁽⁴⁾ | X | X | 1 | 0 |
| | | TDO/TDI ⁽⁵⁾⁽⁶⁾ | X | X | X | 1 |

(1) N/A = Not available or not applicable

(2) X = Don't care

(3) Default after reset (PUC/POR)

(4) Setting the CAPD.x bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the CAx input pin to the comparator multiplexer with the P2CAx bits automatically disables the input buffer for that pin, regardless of the state of the associated CAPD.x bit.

(5) In JTAG mode the internal pullup/down resistors are disabled.

(6) Function controlled by JTAG

Port P2 (P2.6) Pin Schematics, MSP430F20x1

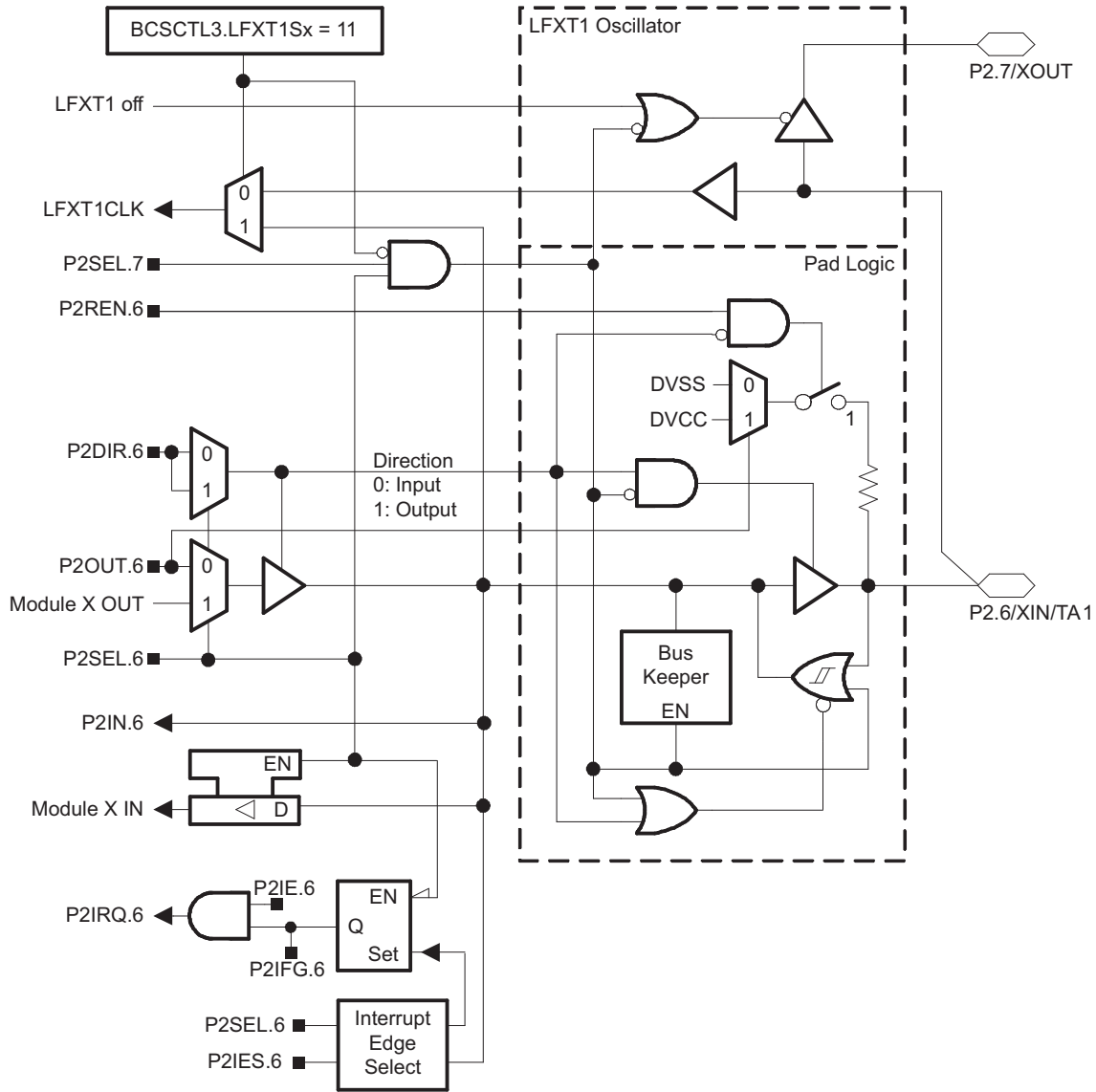


Table 21. Port P2 (P2.6) Pin Functions, MSP430F20x1

| PIN NAME (P2.x) | x | FUNCTION | CONTROL BITS / SIGNALS | |
|-----------------|---|-----------------------|------------------------|---------|
| | | | P2DIR.x | P2SEL.x |
| P2.6/XIN/TA1 | 6 | P2.6 input/output | 0/1 | 0 |
| | | XIN ⁽¹⁾⁽²⁾ | 0 | 1 |
| | | Timer_A2.TA1 | 1 | 1 |

(1) Default after reset (PUC/POR)

(2) XIN is used as digital clock input if the bits LFXT1Sx in register BCSCCTL3 are set to 11.

Port P2 (P2.7) Pin Schematics, MSP430F20x1

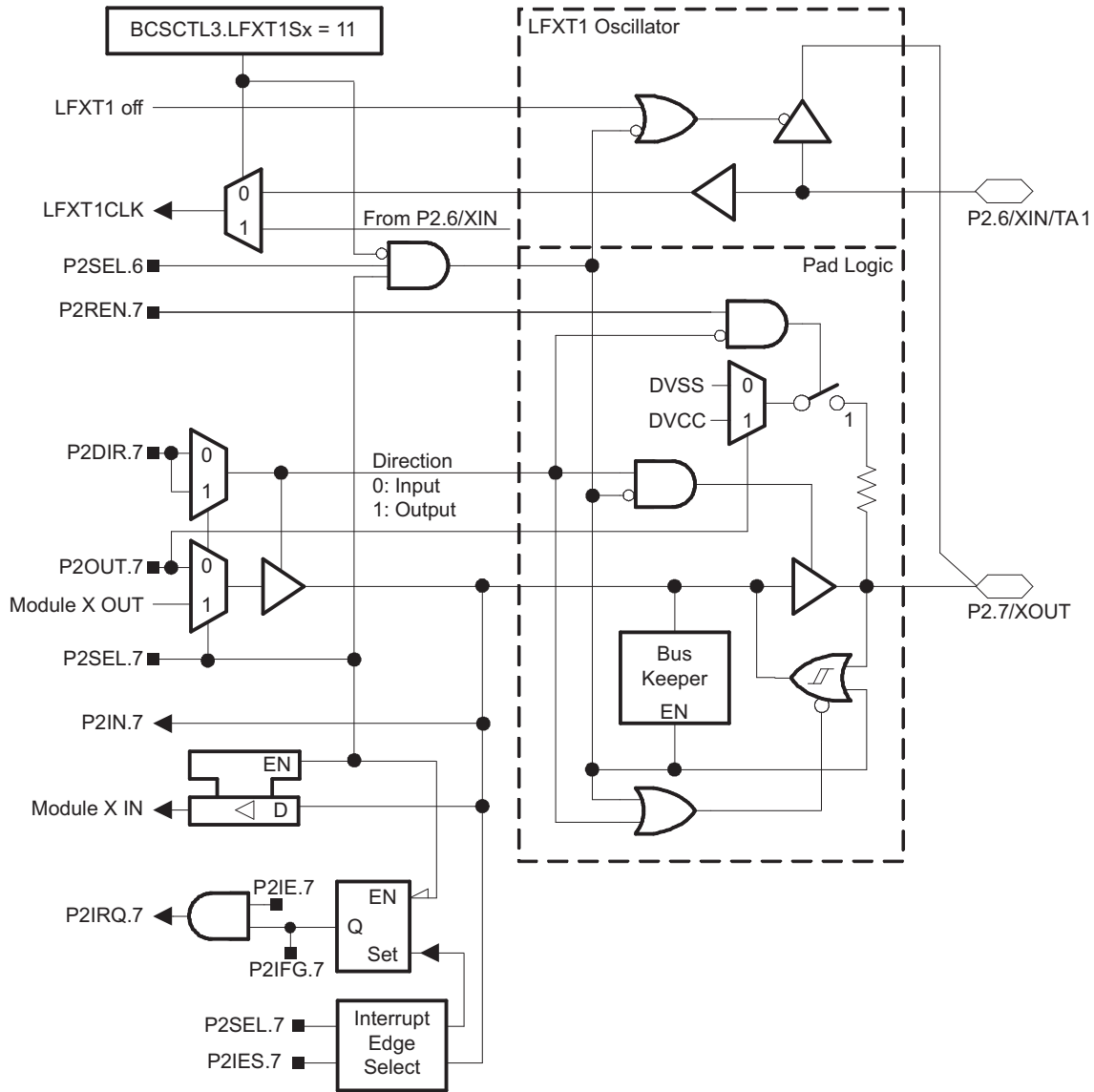


Table 22. Port P2 (P2.7) Pin Functions, MSP430F20x1

| PIN NAME (P2.x) | x | FUNCTION | CONTROL BITS / SIGNALS | |
|-----------------|---|------------------------|------------------------|---------|
| | | | P2DIR.x | P2SEL.x |
| P2.7/XOUT | 7 | P2.7 input/output | 0/1 | 0 |
| | | DVSS | 0 | 1 |
| | | XOUT ⁽¹⁾⁽²⁾ | 1 | 1 |

(1) Default after reset (PUC/POR)

(2) If the pin P2.7/XOUT is used as an input a current can flow until P2SEL.7 is cleared due to the oscillator output driver connection to this pin after reset.

APPLICATION INFORMATION, MSP430F20X2

Port P1 (P1.0 to P1.2) Pin Schematics, MSP430F20x2

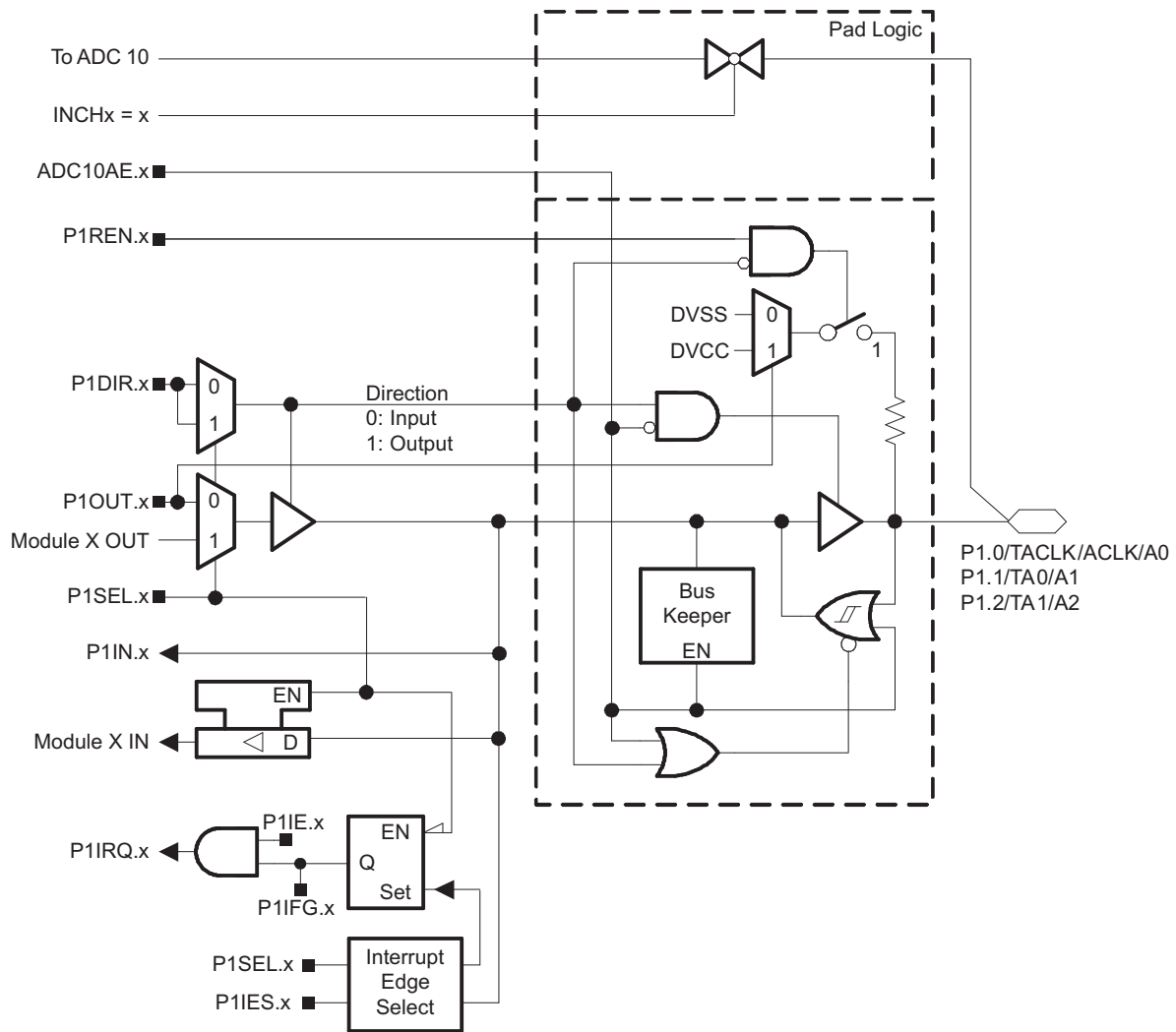


Table 23. Port P1 (P1.0 to P1.2) Pin Functions, MSP430F20x2

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS / SIGNALS ⁽¹⁾⁽²⁾ | | | |
|--------------------|---|----------------------------------|--|---------|-----------|-------|
| | | | P1DIR.x | P1SEL.x | ADC10AE.x | INCHx |
| P1.0/TACLK/ACLK/A0 | 0 | P1.0 ⁽³⁾ input/output | 0/1 | 0 | 0 | N/A |
| | | Timer_A2.TACLK/INCLK | 0 | 1 | 0 | N/A |
| | | ACLK | 1 | 1 | 0 | N/A |
| | | A0 ⁽⁴⁾ | X | X | 1 | 0 |
| P1.1/TA0/A1 | 1 | P1.1 ⁽³⁾ input/output | 0/1 | 0 | 0 | N/A |
| | | Timer_A2.CCI0A | 0 | 1 | 0 | N/A |
| | | Timer_A2.TA0 | 1 | 1 | 0 | N/A |
| | | A1 ⁽⁴⁾ | X | X | 1 | 1 |
| P1.2/TA1/A2 | 2 | P1.2 ⁽³⁾ input/output | 0/1 | 0 | 0 | N/A |
| | | Timer_A2.CCI1A | 0 | 1 | 0 | N/A |
| | | Timer_A2.TA1 | 1 | 1 | 0 | N/A |
| | | A2 ⁽⁴⁾ | X | X | 1 | 2 |

(1) X = Don't care

(2) N/A = Not available or not applicable

(3) Default after reset (PUC/POR)

(4) Setting the ADC10AE.x bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

Port P1 (P1.3) Pin Schematics, MSP430F20x2

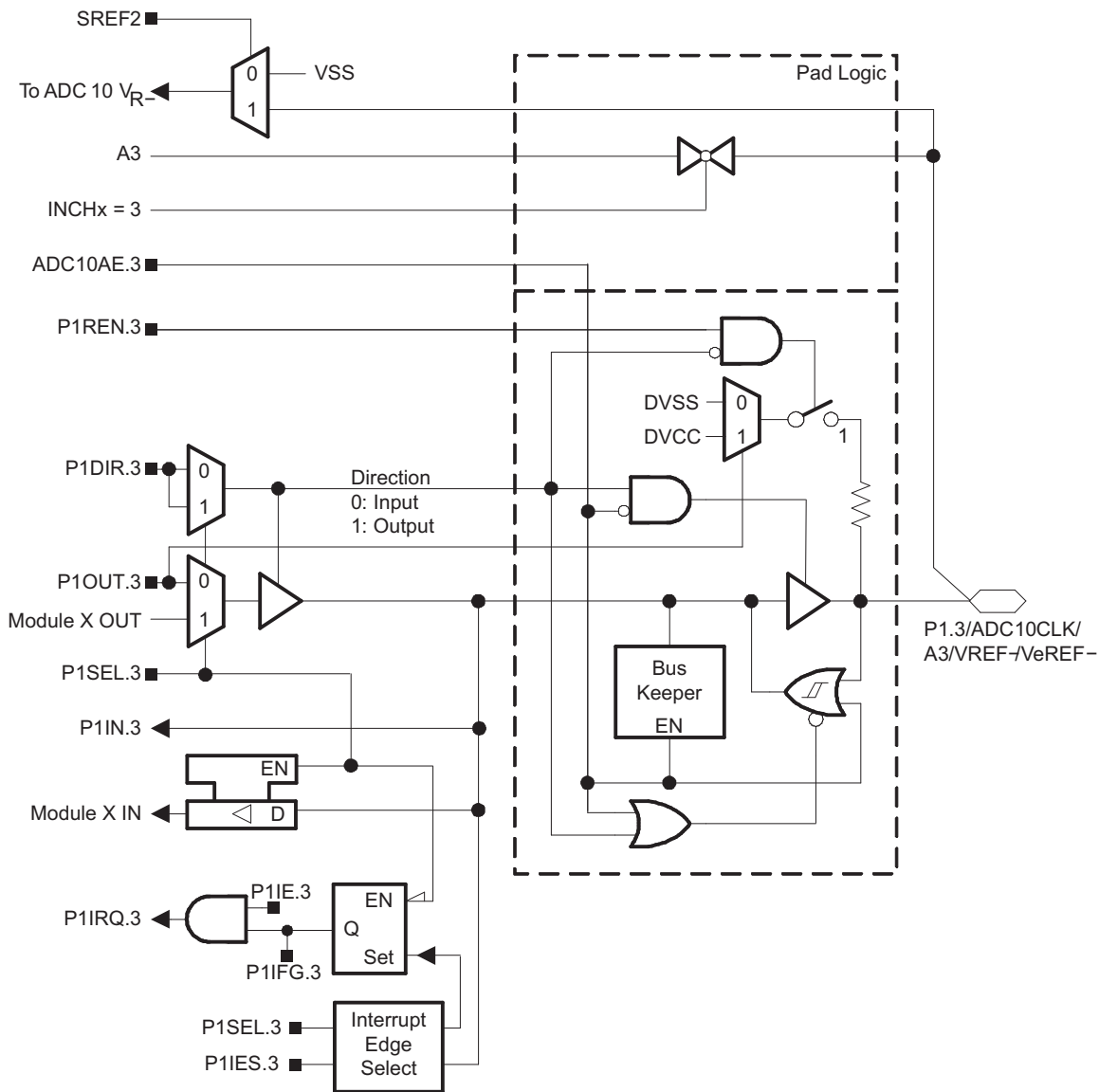
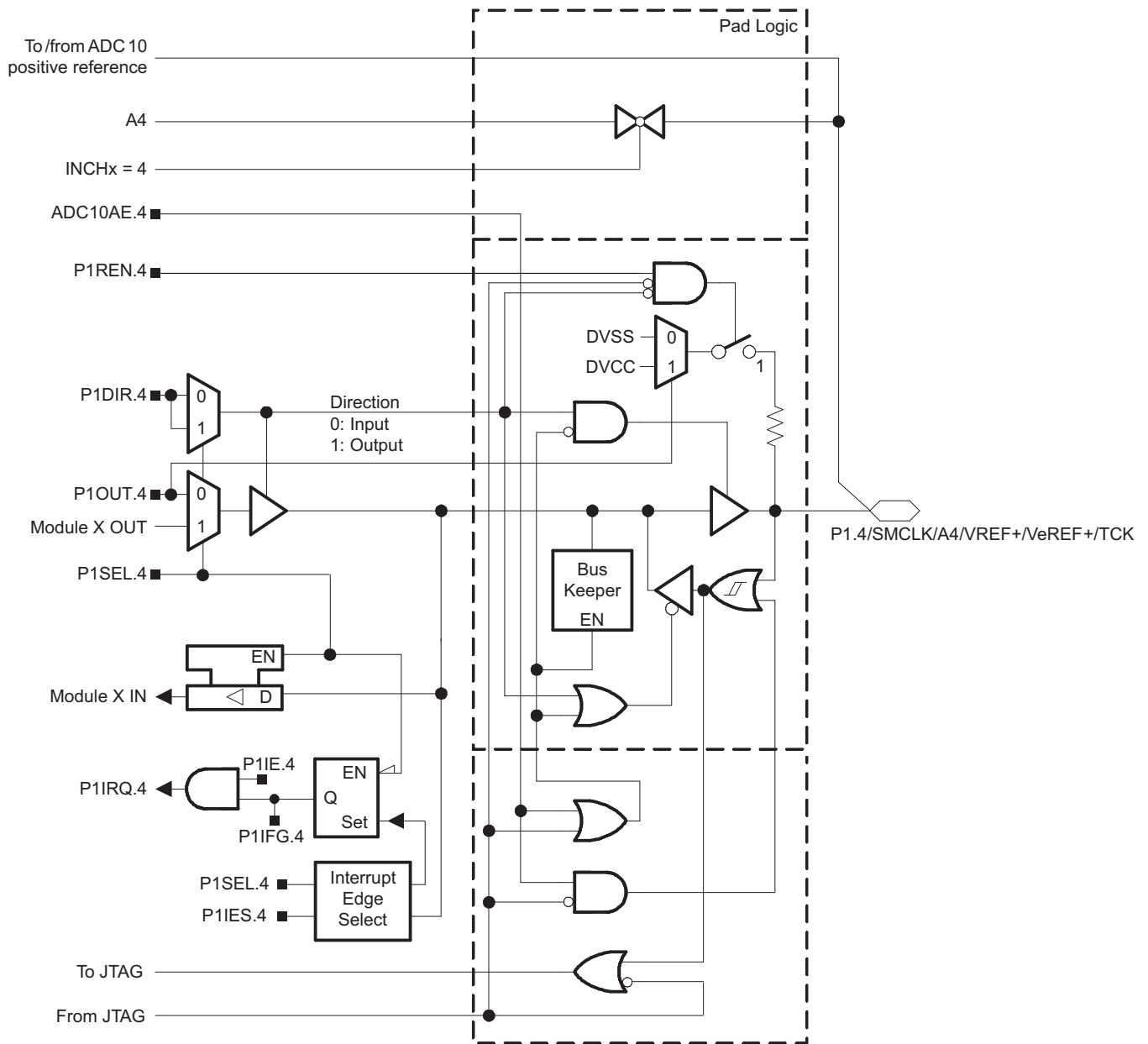


Table 24. Port P1 (P1.3) Pin Functions, MSP430F20x2

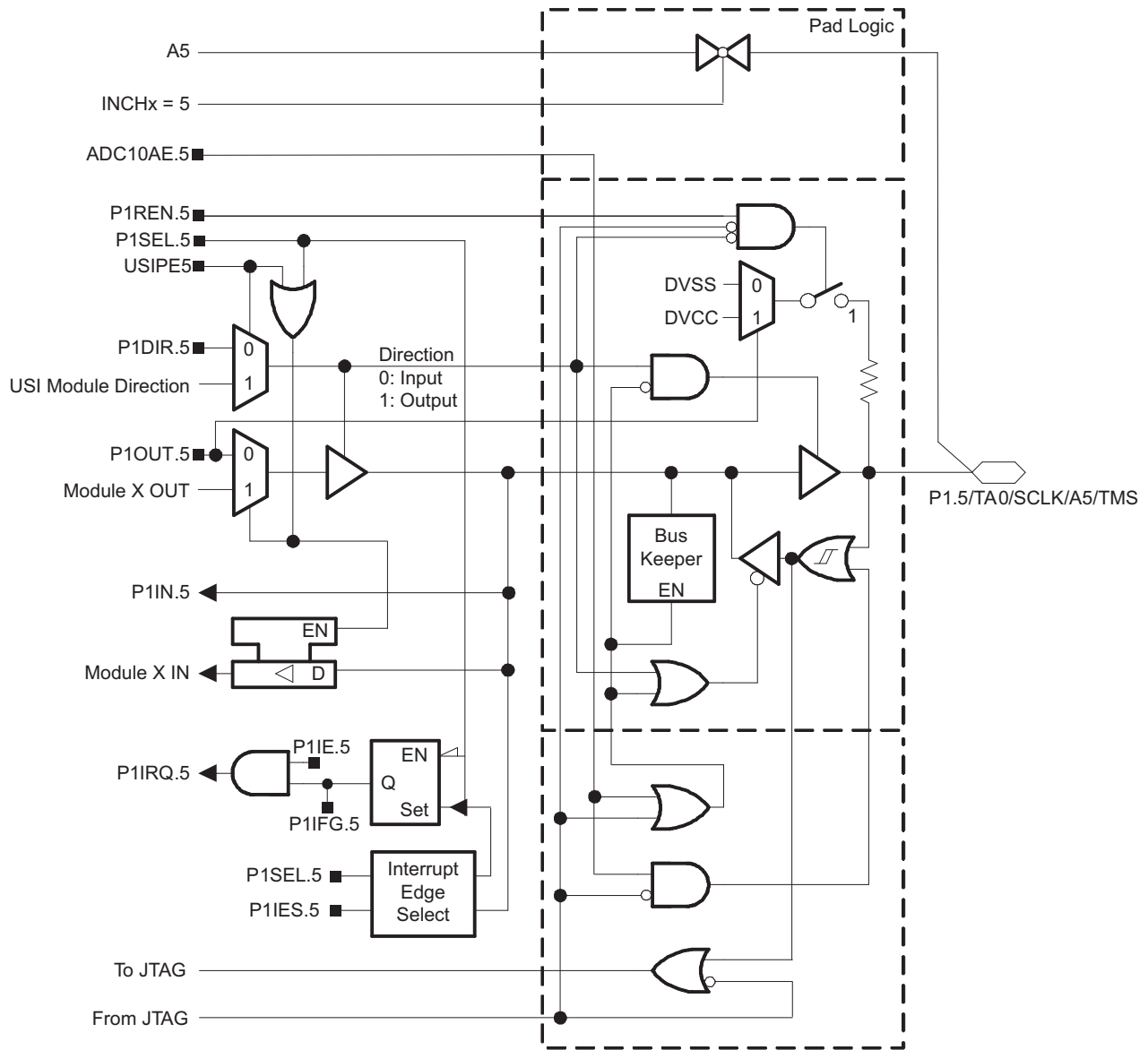
| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS / SIGNALS ⁽¹⁾⁽²⁾ | | | |
|------------------------------------|---|----------------------------------|--|---------|-----------|-------|
| | | | P1DIR.x | P1SEL.x | ADC10AE.x | INCHx |
| P1.3/ADC10CLK/A3/ VREF- /VeREF- | 3 | P1.3 ⁽³⁾ input/output | 0/1 | 0 | 0 | N/A |
| | | N/A | 0 | 1 | 0 | N/A |
| | | ADC10CLK | 1 | 1 | 0 | N/A |
| | | A3 ⁽⁴⁾ | X | X | 1 | 3 |
| | | VREF-/VeREF- ⁽⁴⁾⁽⁵⁾ | X | X | 1 | N/A |

- (1) X = Don't care
- (2) N/A = Not available or not applicable
- (3) Default after reset (PUC/POR)
- (4) Setting the ADC10AE.x bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
- (5) An applied voltage is used as negative reference if bit SREF3 in register ADC10CTL0 is set.

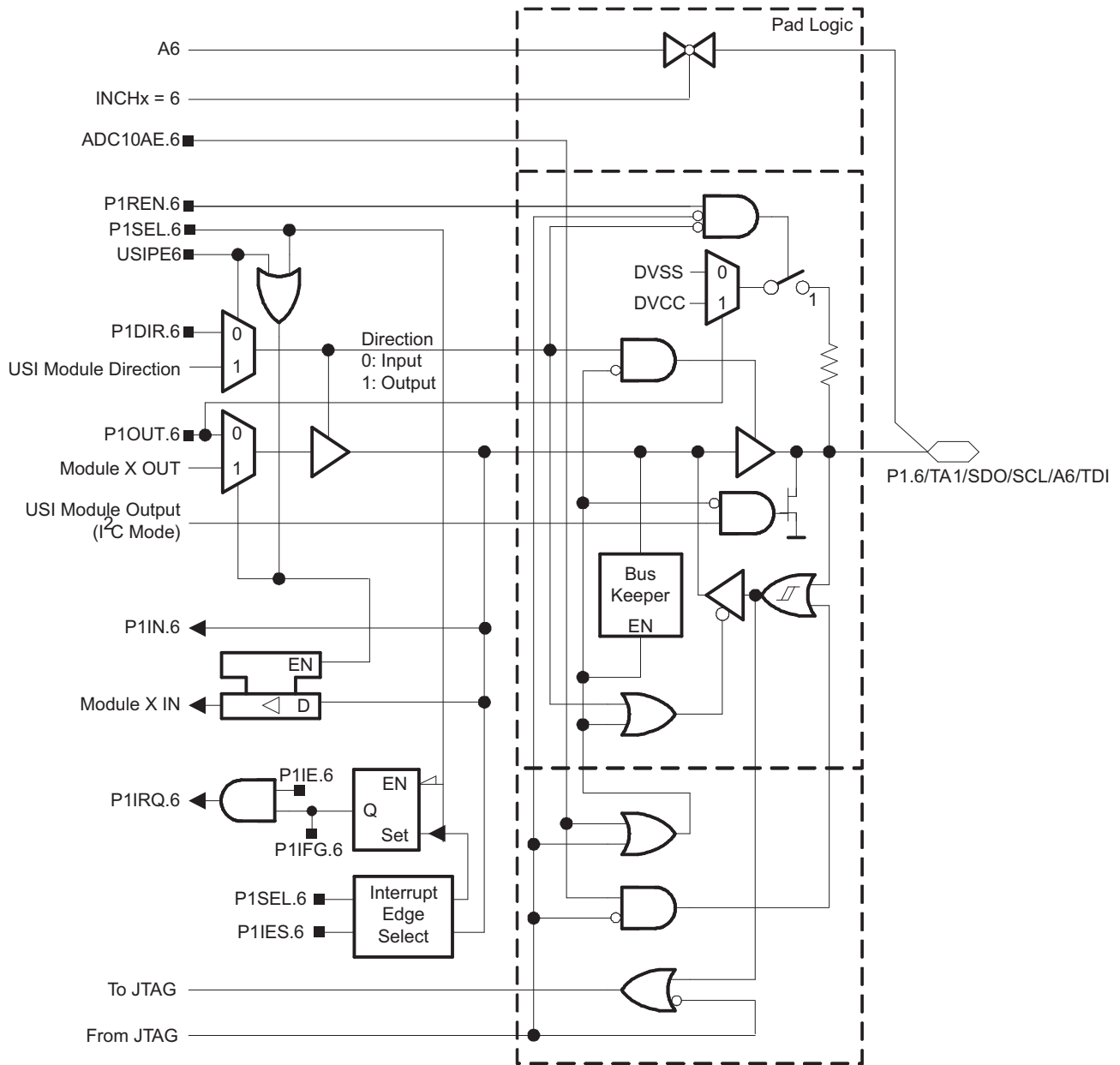
Port P1 (P1.4) Pin Schematic, MSP430F20x2



Port P1 (P1.5) Pin Schematics, MSP430F20x2



Port P1 (P1.6) Pin Schematics, MSP430F20x2



Port P1 (P1.7) Pin Schematics, MSP430F20x2

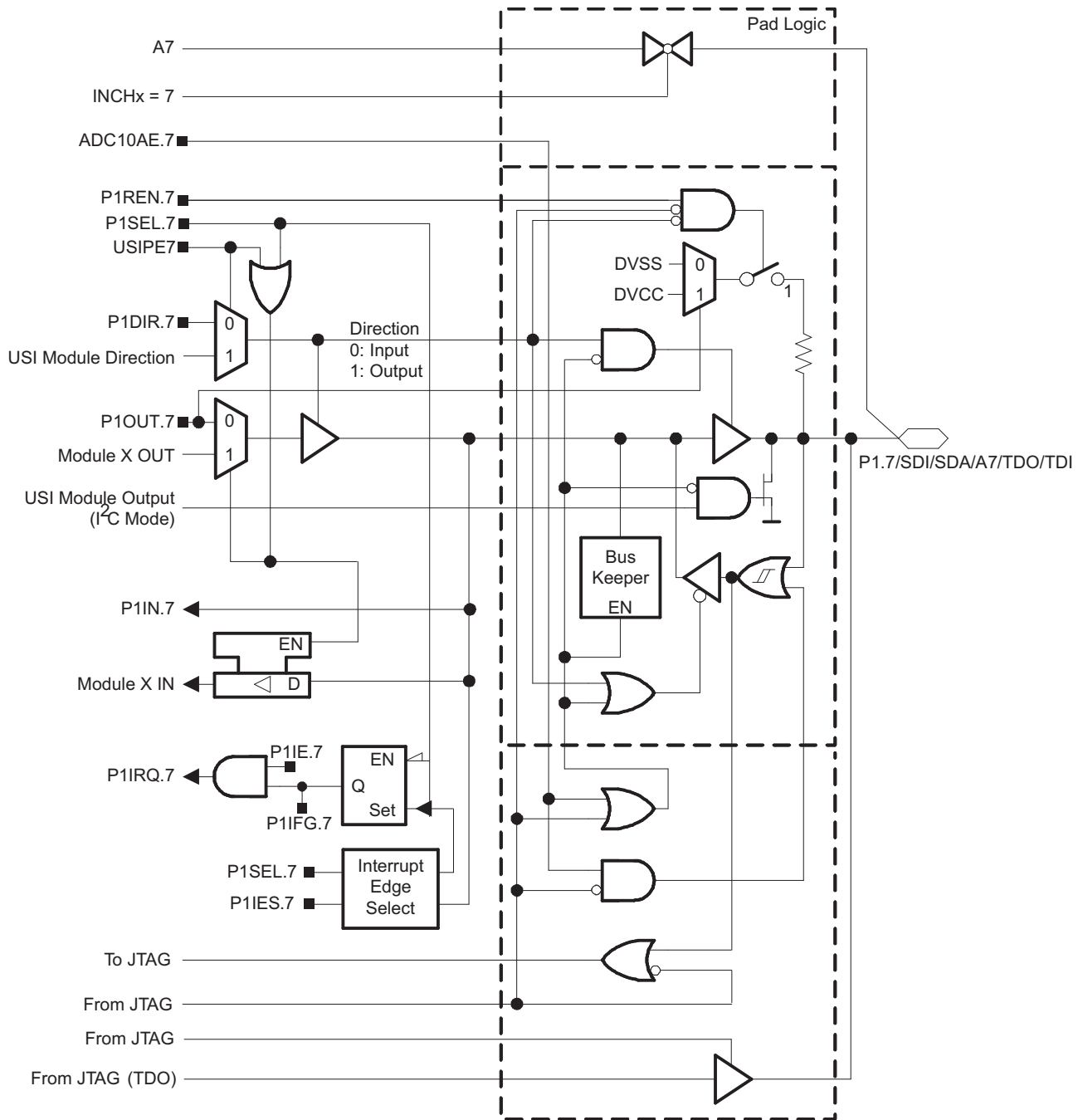


Table 25. Port P1 (P1.4 to P1.7) Pin Functions, MSP430F20x2

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS / SIGNALS ⁽¹⁾⁽²⁾ | | | | | |
|------------------------------------|---|----------------------------------|--|---------|--------|-----------|-------|-----------|
| | | | P1DIR.x | P1SEL.x | USIP.x | ADC10AE.x | INCHx | JTAG Mode |
| P1.4/SMCLK/A4/ VREF+/VeREF+/TCK | 4 | P1.4 ⁽³⁾ input/output | 0/1 | 0 | N/A | 0 | N/A | 0 |
| | | N/A | 0 | 1 | N/A | 0 | N/A | 0 |
| | | SMCLK | 1 | 1 | N/A | 0 | N/A | 0 |
| | | A4 ⁽⁴⁾ | X | X | N/A | 1 | 4 | 0 |
| | | VREF+/VeREF+ ⁽⁴⁾⁽⁵⁾ | X | X | N/A | 1 | N/A | 0 |
| | | TCK ⁽⁶⁾ | X | X | N/A | X | X | 1 |
| P1.5/TA0/SCLK/A5/TMS | 5 | P1.5 ⁽³⁾ input/output | 0/1 | 0 | 0 | 0 | N/A | 0 |
| | | N/A | 0 | 1 | 0 | 0 | N/A | 0 |
| | | Timer_A2.TA0 | 1 | 1 | 0 | 0 | N/A | 0 |
| | | SCLK | X | X | 1 | 0 | N/A | 0 |
| | | A5 ⁽⁴⁾ | X | X | X | 1 | 5 | 0 |
| | | TMS ⁽⁶⁾ | X | X | X | X | X | 1 |
| P1.6/TA1/SDO/SCL/A6/TDI | 6 | P1.6 ⁽³⁾ input/output | 0/1 | 0 | 0 | 0 | N/A | 0 |
| | | Timer_A2.CCI1B | 0 | 1 | 0 | 0 | N/A | 0 |
| | | Timer_A2.TA1 | 1 | 1 | 0 | 0 | N/A | 0 |
| | | SDO (SPI) / SCL (I2C) | X | X | 1 | 0 | N/A | 0 |
| | | A6 ⁽⁴⁾ | X | X | X | 1 | 6 | 0 |
| | | TDI ⁽⁶⁾ | X | X | X | X | X | 1 |
| P1.7/SDI/SDA/A7/TDO/TDI | 7 | P1.7 ⁽³⁾ input/output | 0/1 | 0 | 0 | 0 | N/A | 0 |
| | | N/A | 0 | 1 | 0 | 0 | N/A | 0 |
| | | DVSS | 1 | 1 | 0 | 0 | N/A | 0 |
| | | SDI (SPI) / SDA (I2C) | X | X | 1 | 0 | N/A | 0 |
| | | A7 ⁽⁴⁾ | X | X | X | 1 | 7 | 0 |
| | | TDO/TDI ⁽⁶⁾⁽⁷⁾ | X | X | X | X | X | 1 |

(1) X = Don't care

(2) N/A = Not available or not applicable

(3) Default after reset (PUC/POR)

(4) Setting the ADC10AE.x bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

(5) The reference voltage is output if bit REFOUT in register ADC10CTL0 is set. An applied voltage is used as positive reference if bits SREF0/1 in register ADC10CTL0 are set to 10 or 11.

(6) In JTAG mode the internal pullup/down resistors are disabled.

(7) Function controlled by JTAG.

Port P2 (P2.6) Pin Schematics, MSP430F20x2

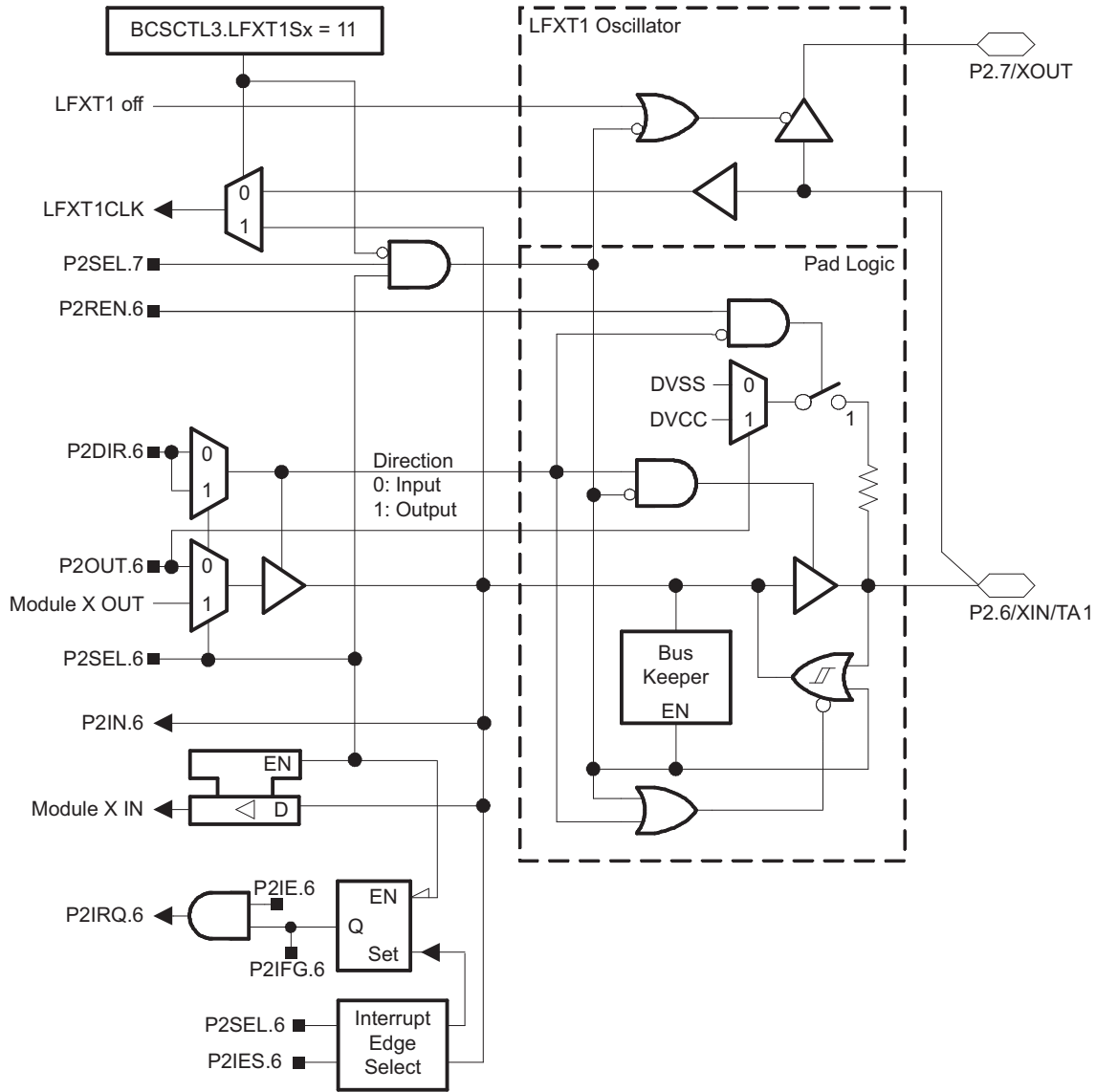


Table 26. Port P2 (P2.6) Pin Functions, MSP430F20x2

| PIN NAME (P2.x) | x | FUNCTION | CONTROL BITS / SIGNALS | |
|-----------------|---|-----------------------|------------------------|---------|
| | | | P2DIR.x | P2SEL.x |
| P2.6/XIN/TA1 | 6 | P2.6 input/output | 0/1 | 0 |
| | | XIN ⁽¹⁾⁽²⁾ | 0 | 1 |
| | | Timer_A2.TA1 | 1 | 1 |

(1) Default after reset (PUC/POR)

(2) XIN is used as digital clock input if the bits LFXT1Sx in register BCSCCTL3 are set to 11.

Port P2 (P2.7) Pin Schematics, MSP430F20x2

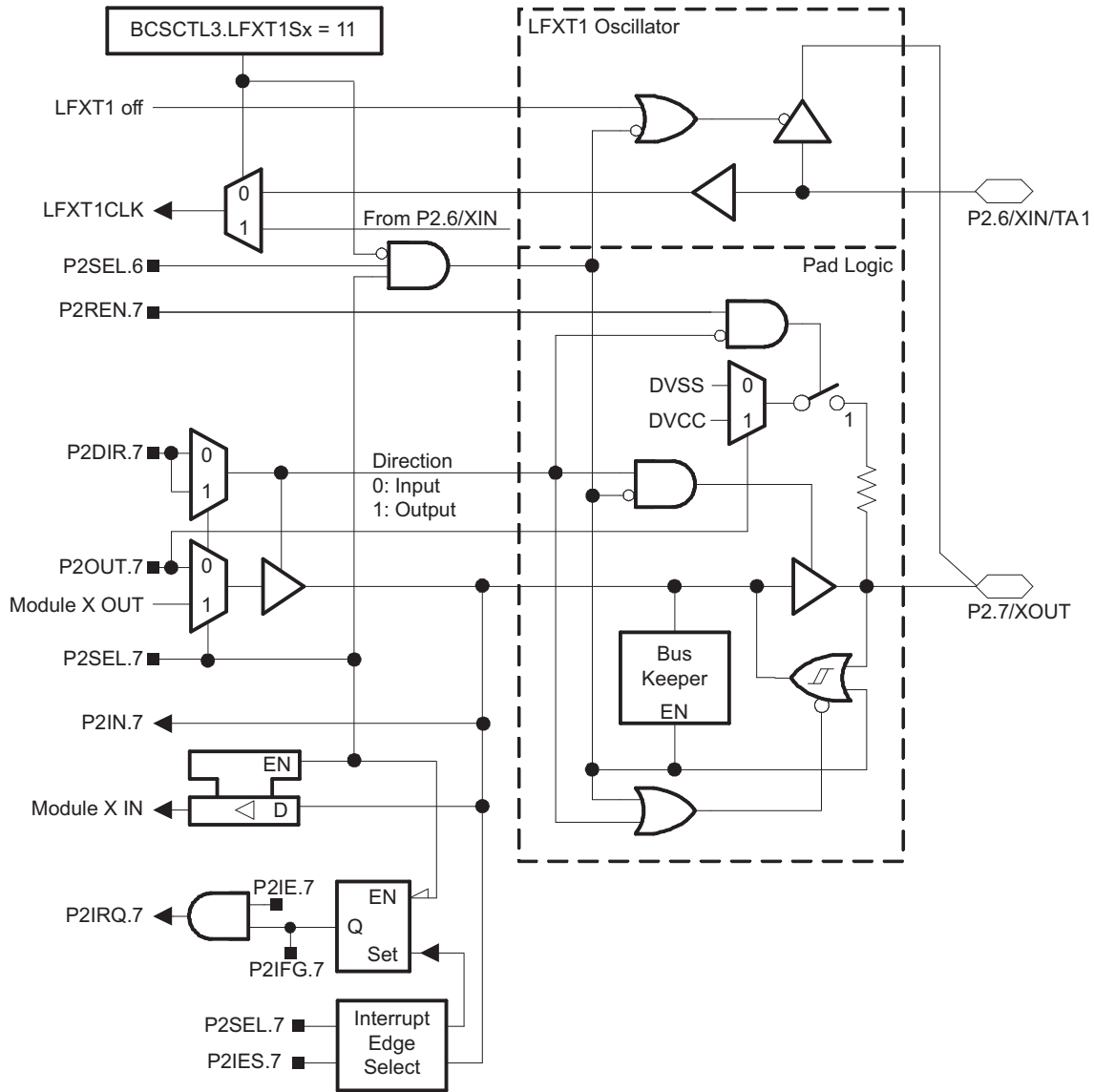


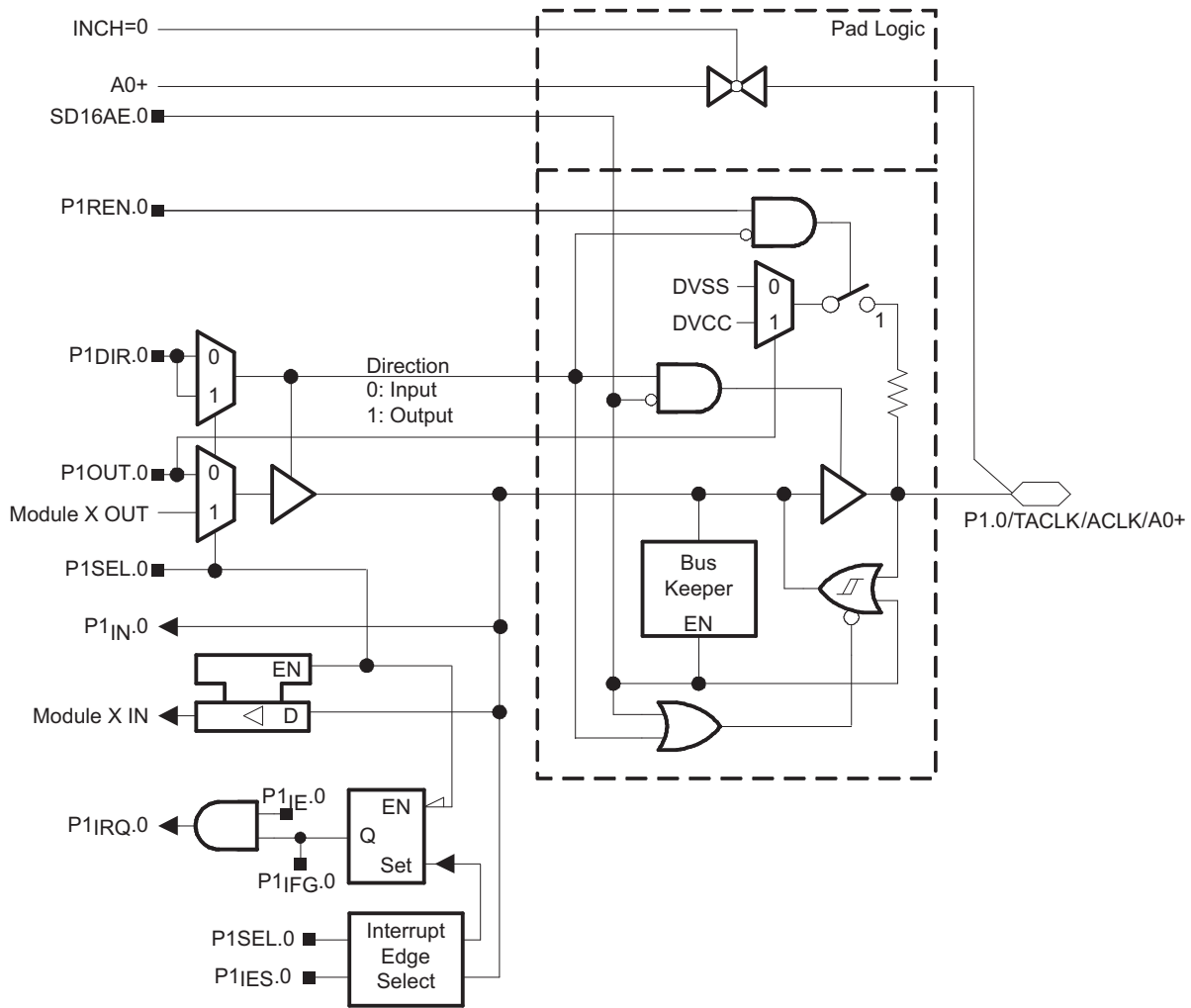
Table 27. Port P2 (P2.7) Pin Functions, MSP430F20x2

| PIN NAME (P2.x) | x | FUNCTION | CONTROL BITS / SIGNALS | |
|-----------------|---|------------------------|------------------------|---------|
| | | | P2DIR.x | P2SEL.x |
| P2.7/XOUT | 7 | P2.7 input/output | 0/1 | 0 |
| | | DVSS | 0 | 1 |
| | | XOUT ⁽¹⁾⁽²⁾ | 1 | 1 |

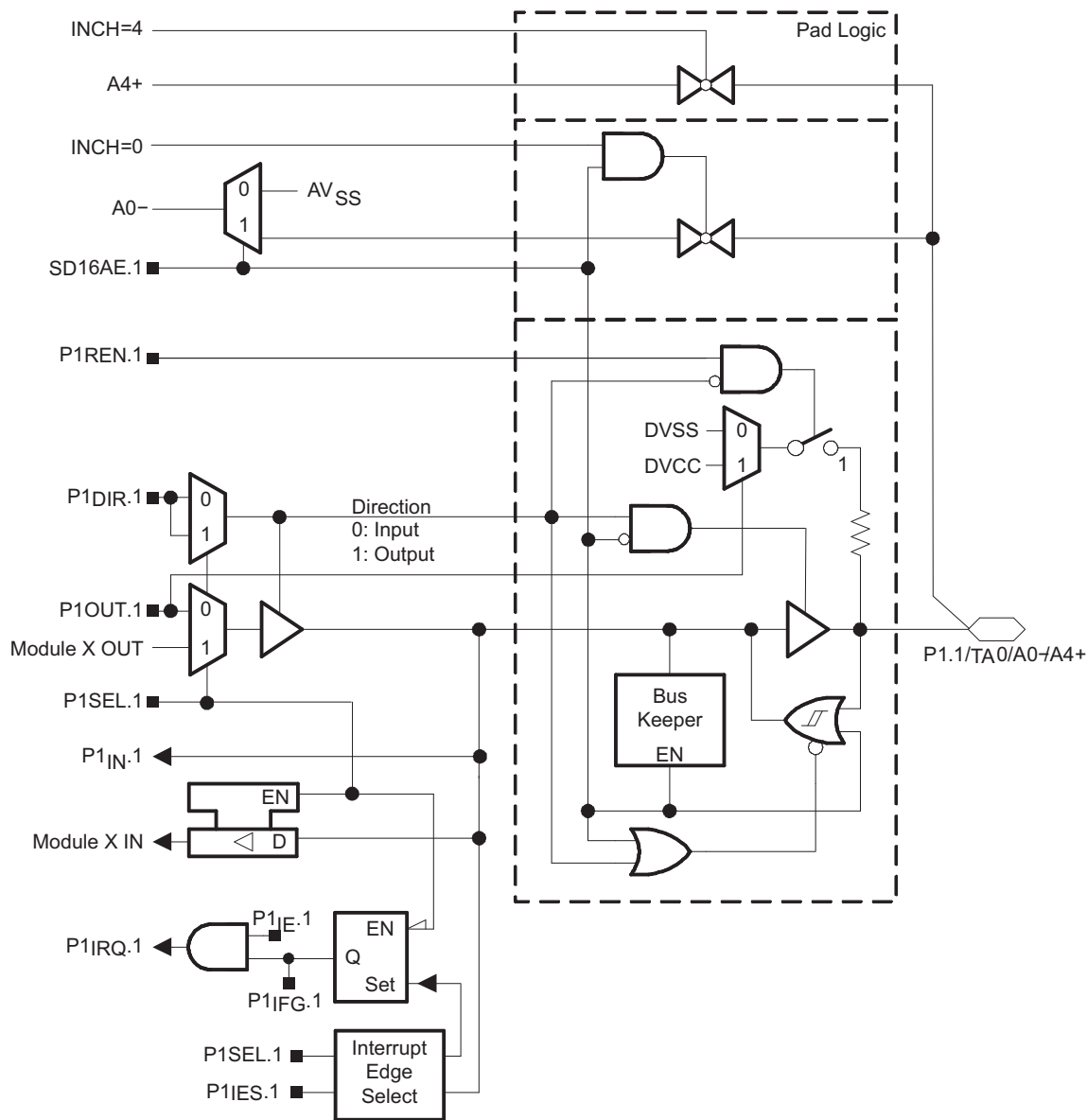
(1) Default after reset (PUC/POR)
 (2) If the pin P2.7/XOUT is used as an input a current can flow until P2SEL.7 is cleared due to the oscillator output driver connection to this pin after reset.

APPLICATION INFORMATION, MSP430F20X3

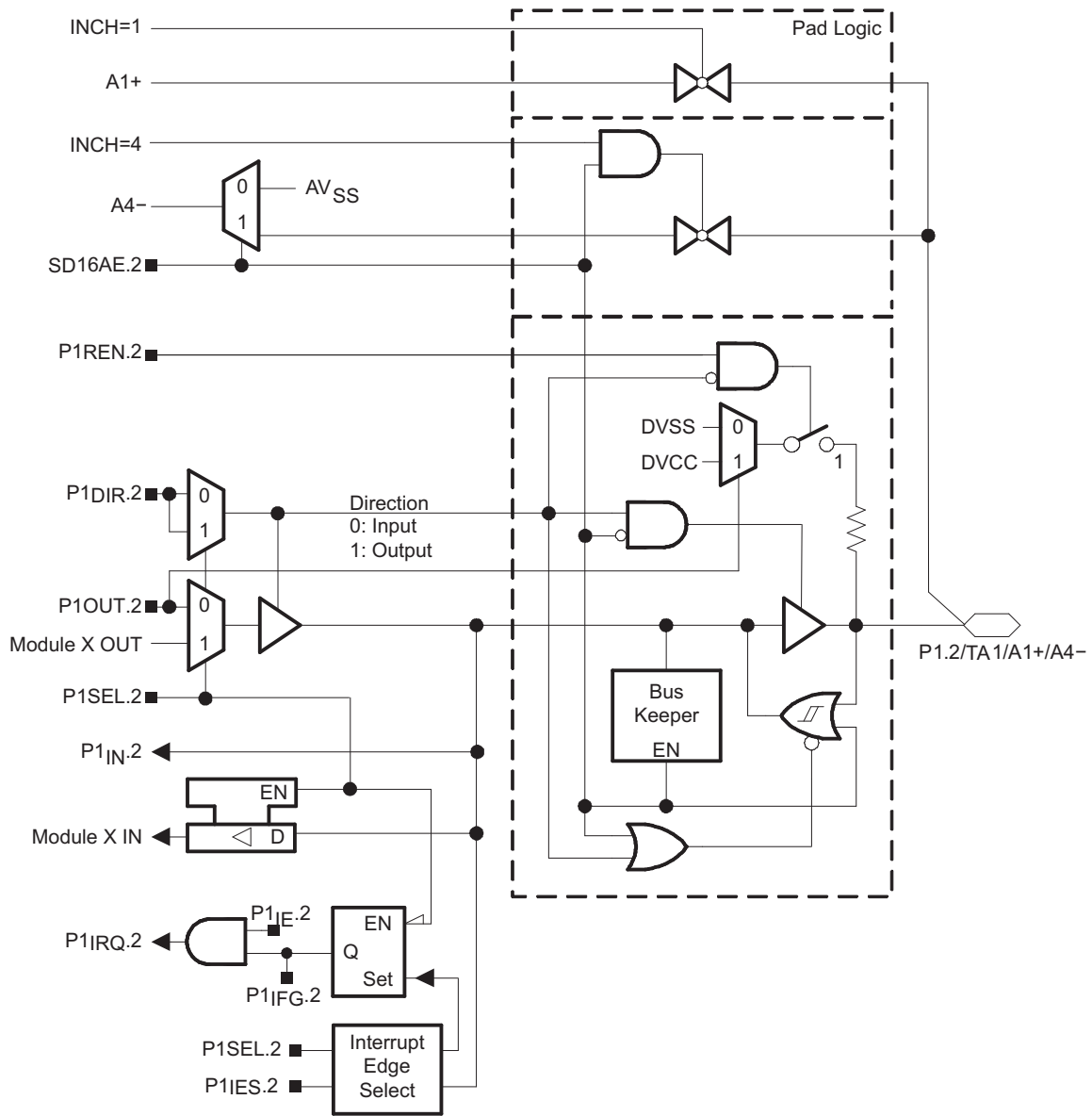
Port P1 (P1.0) Pin Schematics, MSP430F20x3



Port P1 (P1.1) Pin Schematics, MSP430F20x3



Port P1 (P1.2) Pin Schematics, MSP430F20x3



Port P1 (P1.3) Pin Schematics, MSP430F20x3

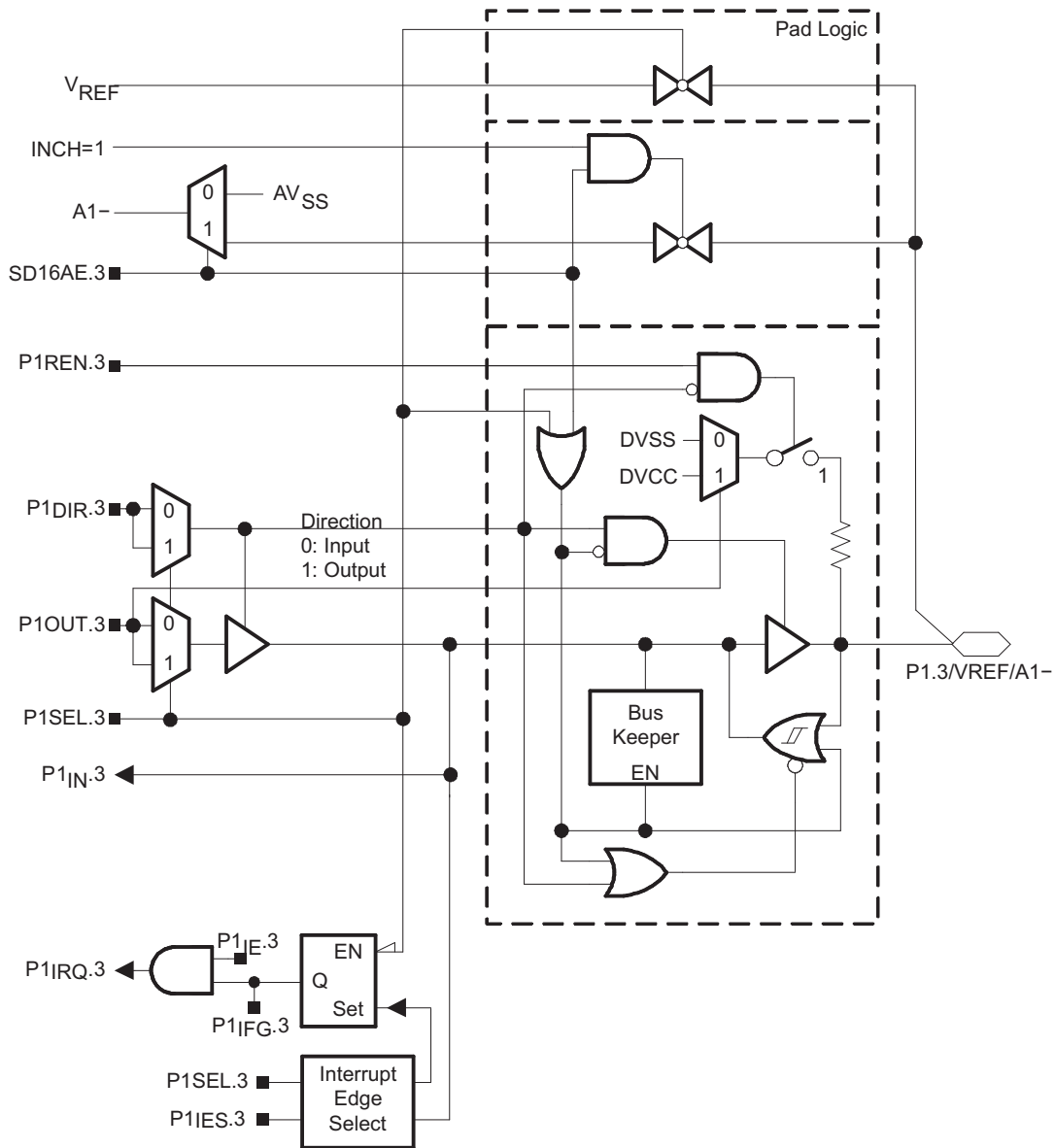
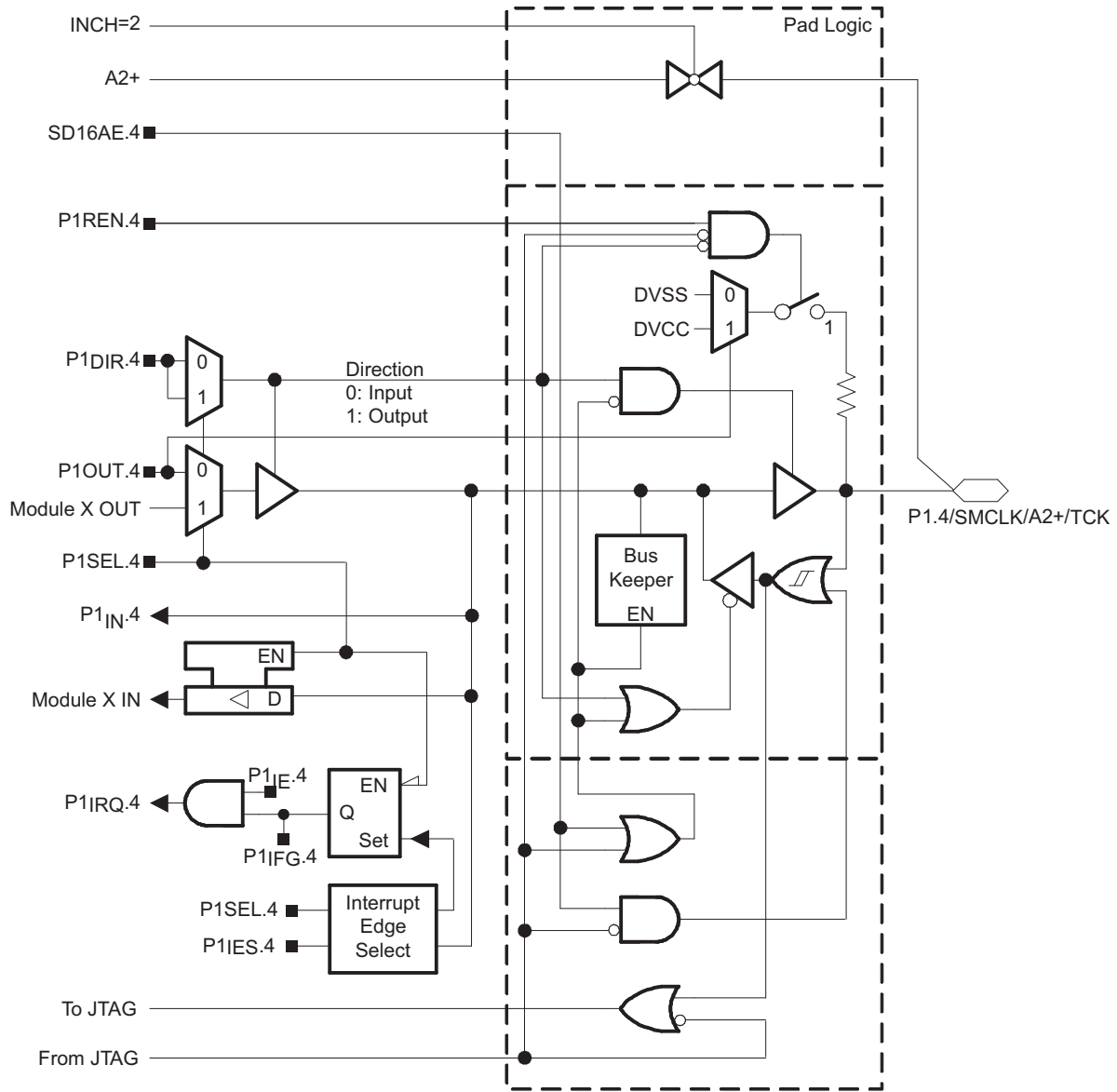


Table 28. Port P1 (P1.0 to P1.3) Pin Functions, MSP430F20x3

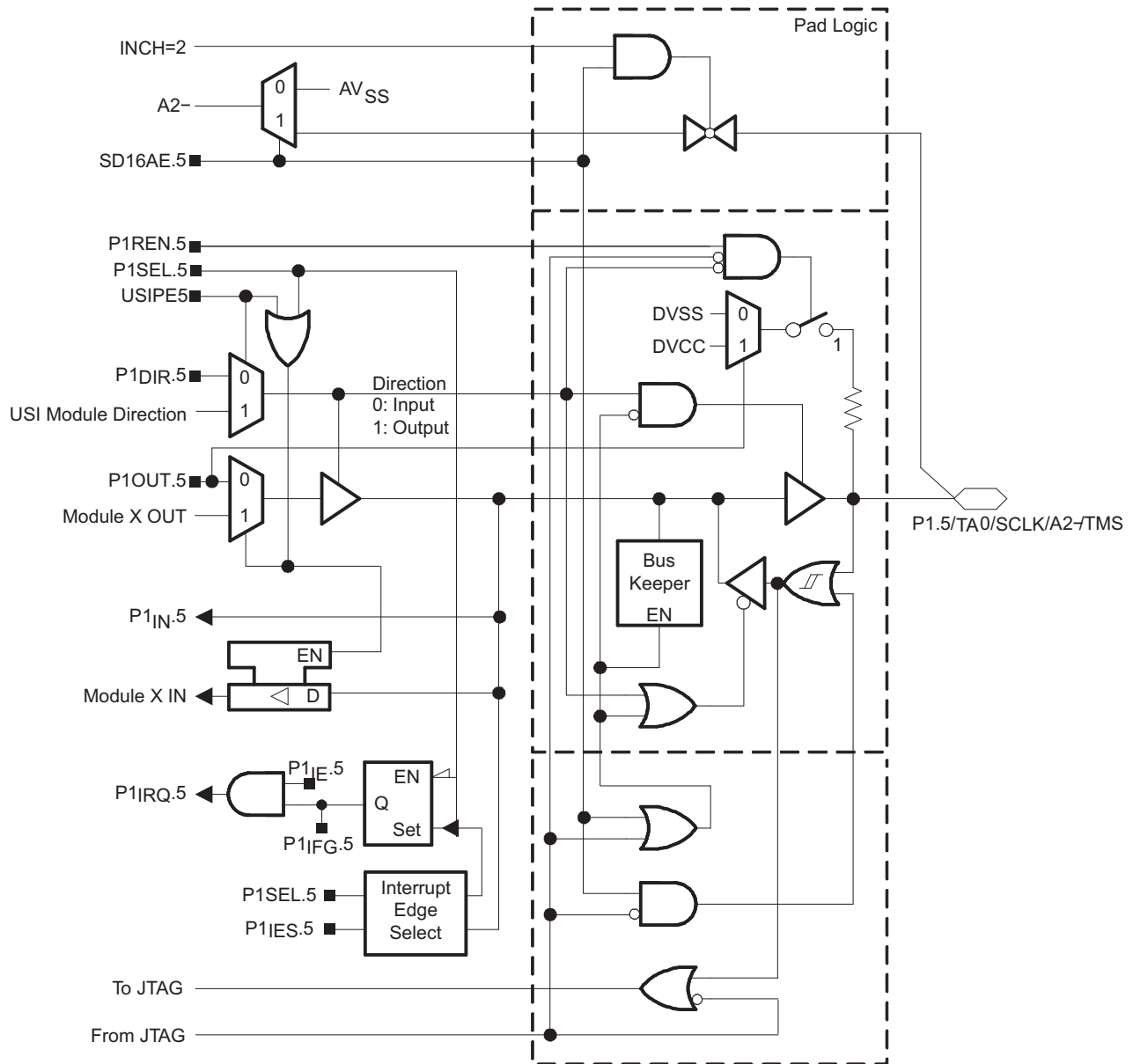
| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS / SIGNALS ⁽¹⁾⁽²⁾ | | | |
|---------------------|---|----------------------------------|--|---------|----------|-------|
| | | | P1DIR.x | P1SEL.x | SD16AE.x | INCHx |
| P1.0/TACLK/ACLK/A0+ | 0 | P1.0 ⁽³⁾ input/output | 0/1 | 0 | 0 | N/A |
| | | Timer_A2.TACLK/INCLK | 0 | 1 | 0 | N/A |
| | | ACLK | 1 | 1 | 0 | N/A |
| | | A0+ ⁽⁴⁾ | X | X | 1 | 0 |
| P1.1/TA0/A0-/A4+ | 1 | P1.1 ⁽³⁾ input/output | 0/1 | 0 | 0 | N/A |
| | | Timer_A2.CCI0A | 0 | 1 | 0 | N/A |
| | | Timer_A2.TA0 | 1 | 1 | 0 | N/A |
| | | A0- ⁽⁴⁾⁽⁵⁾ | X | X | 1 | 0 |
| | | A4+ ⁽⁴⁾ | X | X | 1 | 4 |
| P1.2/TA1/A1+/A4- | 2 | P1.2 ⁽³⁾ input/output | 0/1 | 0 | 0 | N/A |
| | | Timer_A2.CCI1A | 0 | 1 | 0 | N/A |
| | | Timer_A2.TA1 | 1 | 1 | 0 | N/A |
| | | A1+ ⁽⁴⁾ | X | X | 1 | 1 |
| | | A4- ⁽⁴⁾⁽⁵⁾ | X | X | 1 | 4 |
| P1.3/VREF/A1- | 3 | P1.3 ⁽³⁾ input/output | 0/1 | 0 | 0 | N/A |
| | | VREF | X | 1 | 0 | N/A |
| | | A1- ⁽⁴⁾⁽⁵⁾ | X | X | 1 | 1 |

- (1) X = Don't care
- (2) N/A = Not available or not applicable
- (3) Default after reset (PUC/POR)
- (4) Setting the SD16AE.x bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
- (5) With SD16AE.x = 0 the negative inputs are connected to VSS if the corresponding input is selected.

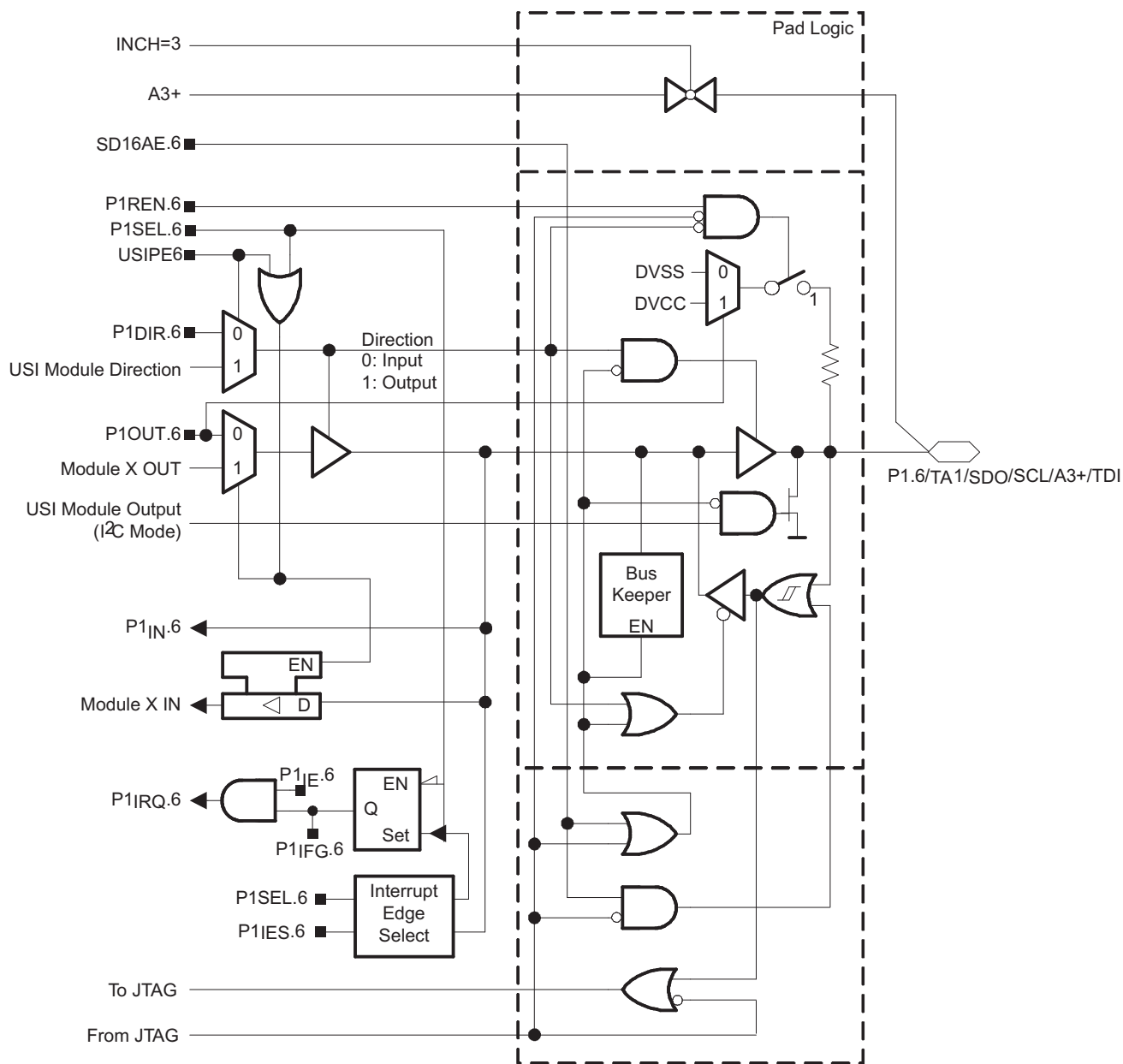
Port P1 (P1.4) Pin Schematics, MSP430F20x3



Port P1 (P1.5) Pin Schematics, MSP430F20x3



Port P1 (P1.6) Pin Schematics, MSP430F20x3



Port P1 (P1.7) Pin Schematics, MSP430F20x3

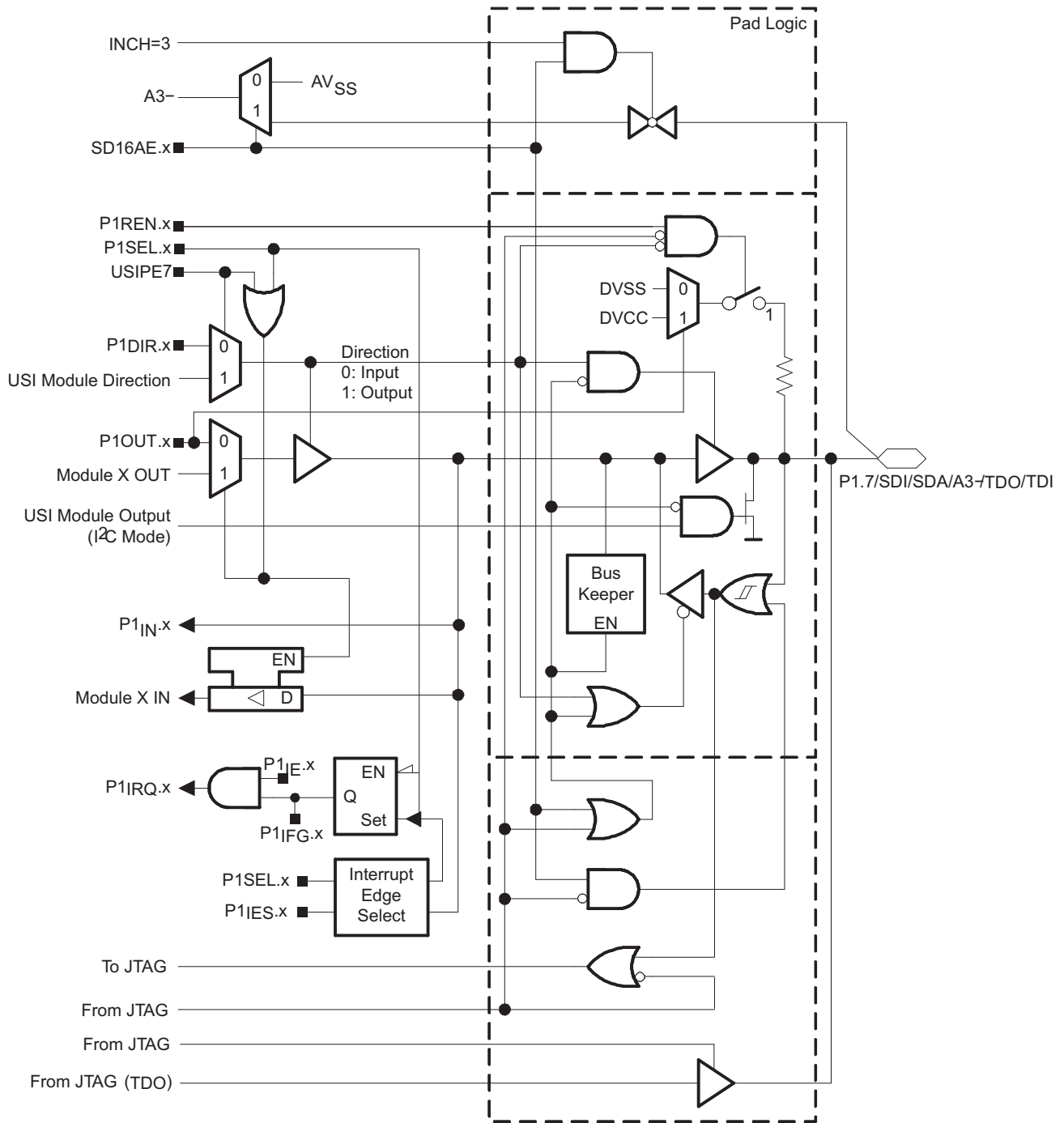


Table 29. Port P1 (P1.4 to P1.7) Pin Functions, MSP430F20x3

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS / SIGNALS ⁽¹⁾⁽²⁾ | | | | | |
|------------------------------|---|----------------------------------|--|---------|--------|----------|-------|-----------|
| | | | P1DIR.x | P1SEL.x | USIP.x | SD16AE.x | INCHx | JTAG Mode |
| P1.4/SMCLK/A2+/TCK | 4 | P1.4 ⁽³⁾ input/output | 0/1 | 0 | N/A | 0 | N/A | 0 |
| | | N/A | 0 | 1 | N/A | 0 | N/A | 0 |
| | | SMCLK | 1 | 1 | N/A | 0 | N/A | 0 |
| | | A2+ ⁽⁴⁾ | X | X | N/A | 1 | 2 | 0 |
| | | TCK ⁽⁵⁾ | X | X | N/A | X | X | 1 |
| P1.5/TA0/SCLK/A2-/TMS | 5 | P1.5 ⁽³⁾ input/output | 0/1 | 0 | 0 | 0 | N/A | 0 |
| | | N/A | 0 | 1 | 0 | 0 | N/A | 0 |
| | | Timer_A2.TA0 | 1 | 1 | 0 | 0 | N/A | 0 |
| | | SCLK | X | X | 1 | 0 | N/A | 0 |
| | | A2- ⁽⁴⁾⁽⁶⁾ | X | X | X | 1 | 2 | 0 |
| | | TMS ⁽⁵⁾ | X | X | X | X | X | 1 |
| P1.6/TA1/SDO/SCL/ A3+/TDI | 6 | P1.6 ⁽³⁾ input/output | 0/1 | 0 | 0 | 0 | N/A | 0 |
| | | Timer_A2.CCI1B | 0 | 1 | 0 | 0 | N/A | 0 |
| | | Timer_A2.TA1 | 1 | 1 | 0 | 0 | N/A | 0 |
| | | SDO (SPI) / SCL (I2C) | X | X | 1 | 0 | N/A | 0 |
| | | A3+ ⁽⁴⁾ | X | X | X | 1 | 3 | 0 |
| | | TDI ⁽⁵⁾ | X | X | X | X | X | 1 |
| P1.7/SDI/SDA/A3-/ TDO/TDI | 7 | P1.7 ⁽³⁾ input/output | 0/1 | 0 | 0 | 0 | N/A | 0 |
| | | N/A | 0 | 1 | 0 | 0 | N/A | 0 |
| | | DVSS | 1 | 1 | 0 | 0 | N/A | 0 |
| | | SDI (SPI) / SDA (I2C) | X | X | 1 | 0 | N/A | 0 |
| | | A3- ⁽⁴⁾⁽⁶⁾ | X | X | X | 1 | 3 | 0 |
| | | TDO/TDI ⁽⁷⁾⁽⁵⁾ | X | X | X | X | X | 1 |

(1) X = Don't care

(2) N/A = Not available or not applicable

(3) Default after reset (PUC/POR)

(4) Setting the SD16AE.x bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

(5) In JTAG mode, the internal pullup and pulldown resistors are disabled.

(6) With SD16AE.x = 0 the negative inputs are connected to VSS if the corresponding input is selected.

(7) Function controlled by JTAG

Port P2 (P2.6) Pin Schematics, MSP430F20x3

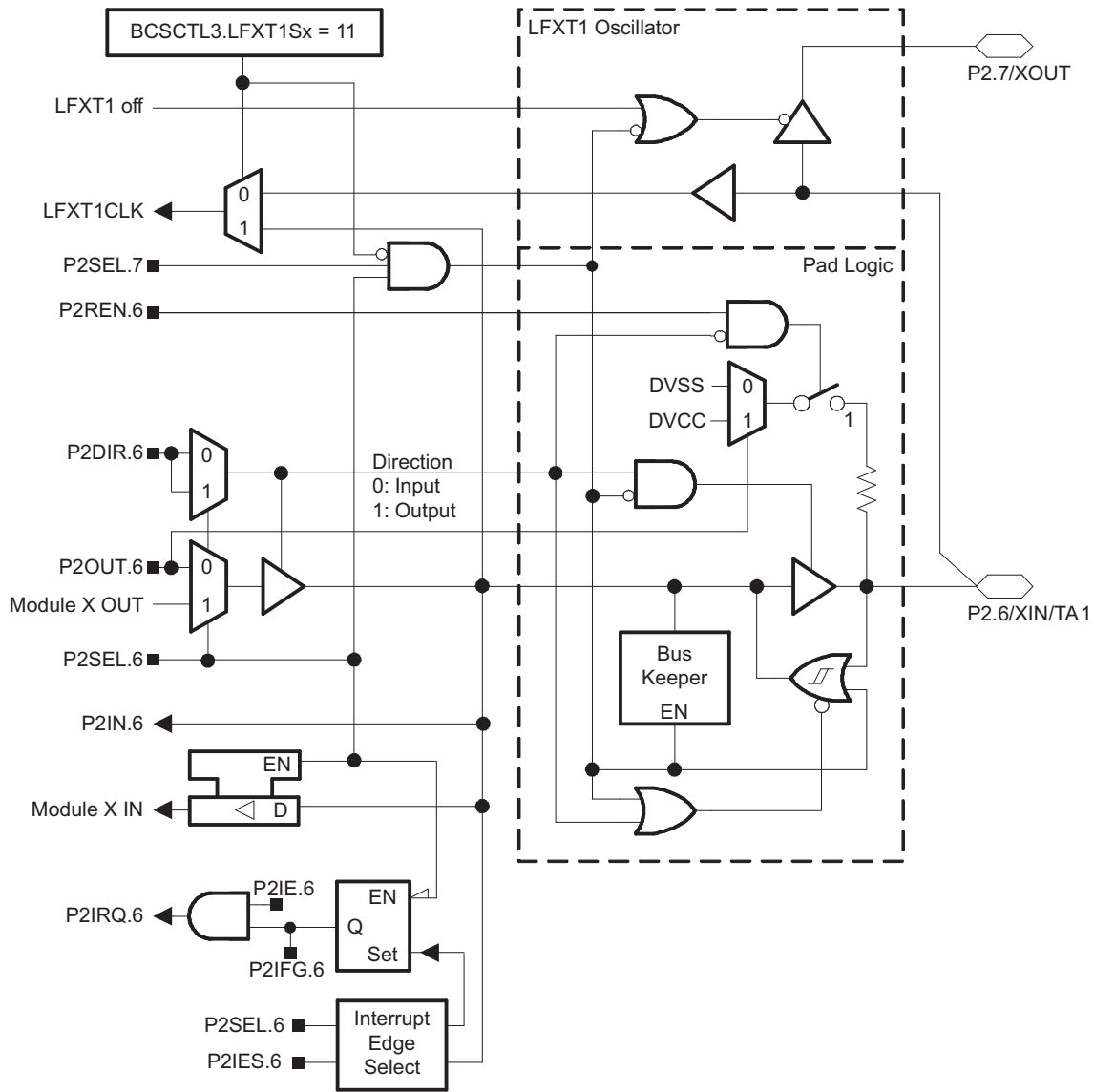


Table 30. Port P2 (P2.6) Pin Functions, MSP430F20x3

| PIN NAME (P2.x) | x | FUNCTION | CONTROL BITS / SIGNALS | |
|-----------------|---|-----------------------|------------------------|---------|
| | | | P2DIR.x | P2SEL.x |
| P2.6/XIN/TA1 | 6 | P2.6 input/output | 0/1 | 0 |
| | | XIN ⁽¹⁾⁽²⁾ | 0 | 1 |
| | | Timer_A2.TA1 | 1 | 1 |

(1) Default after reset (PUC/POR)

(2) XIN is used as digital clock input if the bits LFXT1Sx in register BCSCCTL3 are set to 11.

Port P2 (P2.7) Pin Schematics, MSP430F20x3

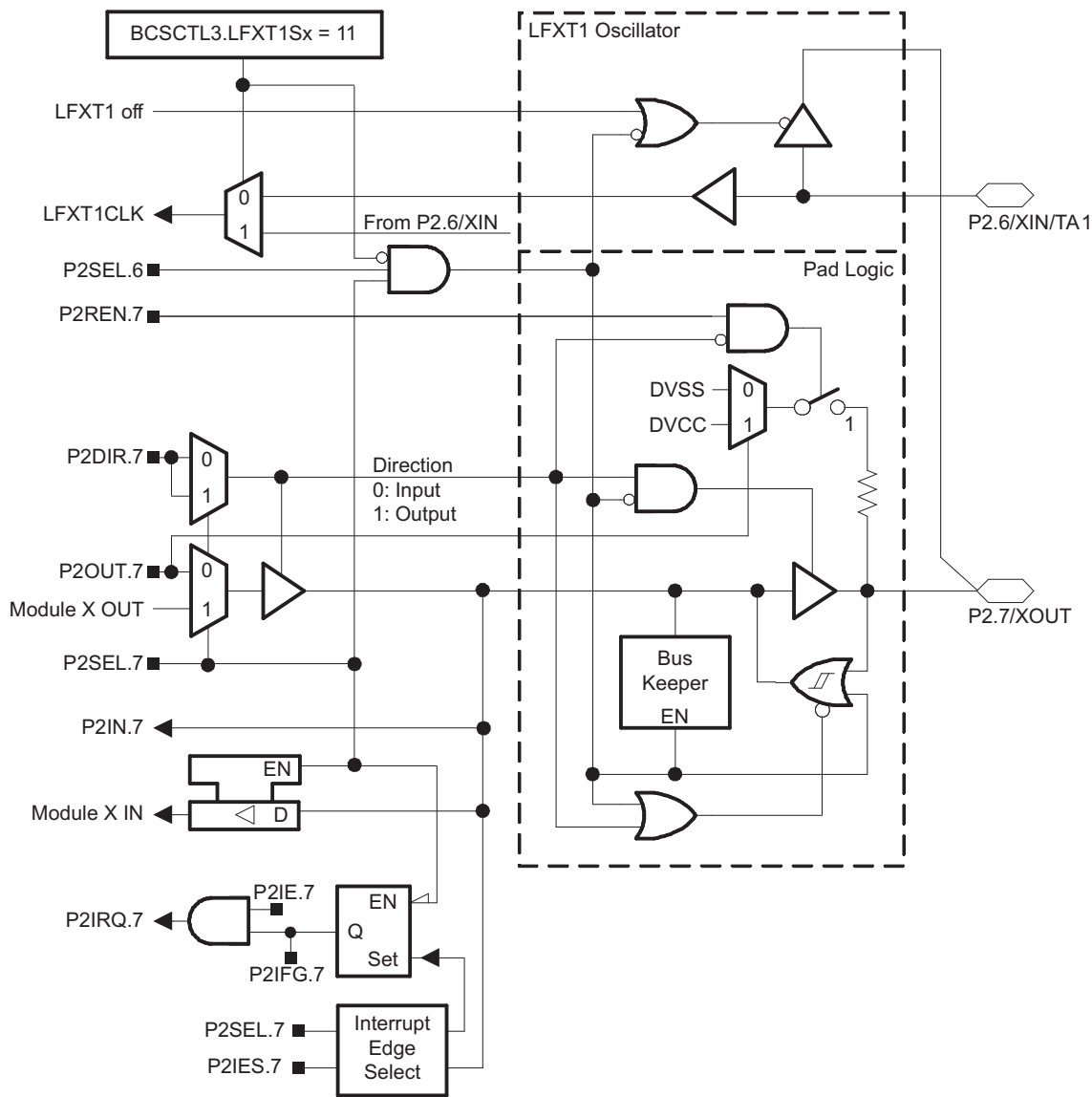


Table 31. Port P2 (P2.7) Pin Functions, MSP430F20x3

| PIN NAME (P2.x) | x | FUNCTION | CONTROL BITS / SIGNALS | |
|-----------------|---|------------------------|------------------------|---------|
| | | | P2DIR.x | P2SEL.x |
| P2.7/XOUT | 7 | P2.7 input/output | 0/1 | 0 |
| | | DVSS | 0 | 1 |
| | | XOUT ⁽¹⁾⁽²⁾ | 1 | 1 |

(1) Default after reset (PUC/POR)

(2) If the pin P2.7/XOUT is used as an input a current can flow until P2SEL.7 is cleared due to the oscillator output driver connection to this pin after reset.

REVISION HISTORY

| LITERATURE NUMBER | SUMMARY |
|-------------------|--|
| SLAS491 | Preliminary PRODUCT PREVIEW data sheet release |
| SLAS491A | Production data sheet release for MSP430F20x3I. Updated specification and added characterization graphs. |
| SLAS491B | Production data sheet release for MSP430F20x3T, MSP430F20x1I and MSP430F20x1T. 105°C characterization results added. SD16_A SINAD characterization results for MSP430F20x3. RSA package added. Updated SD16_A Power Supply Rejection specification. DCO Calibration Register names: lower case "z" changed to upper case "Z". $V_{\text{hys(B_IT-)}}$ MAX specification increased from 180 mV to 210 mV. MIN and MAX percentages for "calibrated DCO frequencies - tolerance over supply voltage VCC" corrected from 2.5% to 3.0% to match the specified frequency ranges. |
| SLAS491C | Production data sheet release for MSP430F20x2I and MSP430F20x2T. |
| SLAS491D | Changed f_{ACLK} to 0 Hz in I_{LPM4} test conditions in Low-Power Mode Supply Currents (Into V_{CC}) Excluding External Current . |
| SLAS491E | Changed T_{stg} maximum for programmed devices to 150°C in Absolute Maximum Ratings . |
| SLAS491F | Added ADC10 data transfer registers to Peripheral File Map |
| SLAS491G | Changed Test Conditions for "Duty cycle, LF mode" in Crystal Oscillator, XT1, Low-Frequency Mode . Changed note (1) on 10-Bit ADC, Built-In Voltage Reference . Changed USIP.x Control Bits in Table 25 and Table 29 . |
| SLAS491H | Changed T_{stg} , Programmed device, to -55°C to 150°C in Absolute Maximum Ratings . |
| SLAS491I | Added typical value test conditions to Recommended Operating Conditions . Added note (2) to POR and Brownout Reset (BOR) . |

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| MSP430F2001IN | ACTIVE | PDIP | N | 14 | 25 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | MSP430F2001 | Samples |
| MSP430F2001IPW | ACTIVE | TSSOP | PW | 14 | 90 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | F2001 | Samples |
| MSP430F2001IPWR | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | F2001 | Samples |
| MSP430F2001IRSAR | ACTIVE | QFN | RSA | 16 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | M430F 2001 | Samples |
| MSP430F2001IRSAT | ACTIVE | QFN | RSA | 16 | 250 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | M430F 2001 | Samples |
| MSP430F2001TN | ACTIVE | PDIP | N | 14 | 25 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | MSP430F2001T | Samples |
| MSP430F2001TPW | ACTIVE | TSSOP | PW | 14 | 90 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | F2001T | Samples |
| MSP430F2001TPWR | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | F2001T | Samples |
| MSP430F2001TRSAR | ACTIVE | QFN | RSA | 16 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | M430F 2001T | Samples |
| MSP430F2001TRSAT | ACTIVE | QFN | RSA | 16 | 250 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | M430F 2001T | Samples |
| MSP430F2002IN | ACTIVE | PDIP | N | 14 | 25 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | MSP430F2002 | Samples |
| MSP430F2002IPW | ACTIVE | TSSOP | PW | 14 | 90 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | F2002 | Samples |
| MSP430F2002IPWR | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | F2002 | Samples |
| MSP430F2002IRSAR | ACTIVE | QFN | RSA | 16 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | M430F 2002 | Samples |
| MSP430F2002IRSAT | ACTIVE | QFN | RSA | 16 | 250 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | M430F 2002 | Samples |
| MSP430F2002TN | ACTIVE | PDIP | N | 14 | 25 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | MSP430F2002T | Samples |
| MSP430F2002TPW | ACTIVE | TSSOP | PW | 14 | 90 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | F2002T | Samples |
| MSP430F2002TPWR | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | F2002T | Samples |
| MSP430F2002TRSAR | ACTIVE | QFN | RSA | 16 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | M430F | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| | | | | | | | | | | 2002T | |
| MSP430F2002TRSAT | ACTIVE | QFN | RSA | 16 | 250 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | M430F 2002T | Samples |
| MSP430F2003IN | ACTIVE | PDIP | N | 14 | 25 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | MSP430F2003 | Samples |
| MSP430F2003IPW | ACTIVE | TSSOP | PW | 14 | 90 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | F2003 | Samples |
| MSP430F2003IPWR | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | F2003 | Samples |
| MSP430F2003IRSAR | ACTIVE | QFN | RSA | 16 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | M430F 2003 | Samples |
| MSP430F2003IRSAT | ACTIVE | QFN | RSA | 16 | 250 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | M430F 2003 | Samples |
| MSP430F2003TN | ACTIVE | PDIP | N | 14 | 25 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | MSP430F2003T | Samples |
| MSP430F2003TPW | ACTIVE | TSSOP | PW | 14 | 90 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | F2003T | Samples |
| MSP430F2003TPWR | ACTIVE | TSSOP | PW | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | F2003T | Samples |
| MSP430F2003TRSAR | ACTIVE | QFN | RSA | 16 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | M430F 2003T | Samples |
| MSP430F2003TRSAT | ACTIVE | QFN | RSA | 16 | 250 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | M430F 2003T | Samples |
| MSP430F2011IN | ACTIVE | PDIP | N | 14 | 25 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | MSP430F2011 | Samples |
| MSP430F2011IPW | ACTIVE | TSSOP | PW | 14 | 90 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | F2011 | Samples |
| MSP430F2011IPWR | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | F2011 | Samples |
| MSP430F2011IRSAR | ACTIVE | QFN | RSA | 16 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | M430F 2011 | Samples |
| MSP430F2011IRSAT | ACTIVE | QFN | RSA | 16 | 250 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | M430F 2011 | Samples |
| MSP430F2011TN | ACTIVE | PDIP | N | 14 | 25 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | MSP430F2011T | Samples |
| MSP430F2011TPW | ACTIVE | TSSOP | PW | 14 | 90 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | F2011T | Samples |
| MSP430F2011TPWR | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | F2011T | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| MSP430F2011TRSAR | ACTIVE | QFN | RSA | 16 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | M430F 2011T | Samples |
| MSP430F2011TRSAT | ACTIVE | QFN | RSA | 16 | 250 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | M430F 2011T | Samples |
| MSP430F2012IN | ACTIVE | PDIP | N | 14 | 25 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | MSP430F2012 | Samples |
| MSP430F2012IPW | ACTIVE | TSSOP | PW | 14 | 90 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | F2012 | Samples |
| MSP430F2012IPWR | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | F2012 | Samples |
| MSP430F2012IRSAR | ACTIVE | QFN | RSA | 16 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | M430F 2012 | Samples |
| MSP430F2012IRSAT | ACTIVE | QFN | RSA | 16 | 250 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | M430F 2012 | Samples |
| MSP430F2012TN | ACTIVE | PDIP | N | 14 | 25 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | MSP430F2012T | Samples |
| MSP430F2012TPW | ACTIVE | TSSOP | PW | 14 | 90 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | F2012T | Samples |
| MSP430F2012TPWR | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | F2012T | Samples |
| MSP430F2012TRSAR | ACTIVE | QFN | RSA | 16 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | M430F 2012T | Samples |
| MSP430F2012TRSAT | ACTIVE | QFN | RSA | 16 | 250 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | M430F 2012T | Samples |
| MSP430F2013IN | ACTIVE | PDIP | N | 14 | 25 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | MSP430F2013 | Samples |
| MSP430F2013IPW | ACTIVE | TSSOP | PW | 14 | 90 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | F2013 | Samples |
| MSP430F2013IPWR | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | F2013 | Samples |
| MSP430F2013IRSAR | ACTIVE | QFN | RSA | 16 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | M430F 2013 | Samples |
| MSP430F2013IRSAT | ACTIVE | QFN | RSA | 16 | 250 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | M430F 2013 | Samples |
| MSP430F2013TN | ACTIVE | PDIP | N | 14 | 25 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | MSP430F2013T | Samples |
| MSP430F2013TPW | ACTIVE | TSSOP | PW | 14 | 90 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | F2013T | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| MSP430F2013TPWR | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | F2013T | Samples |
| MSP430F2013TRSAR | ACTIVE | QFN | RSA | 16 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | M430F 2013T | Samples |
| MSP430F2013TRSAT | ACTIVE | QFN | RSA | 16 | 250 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | M430F 2013T | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF MSP430F2013 :

- Enhanced Product: [MSP430F2013-EP](#)

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

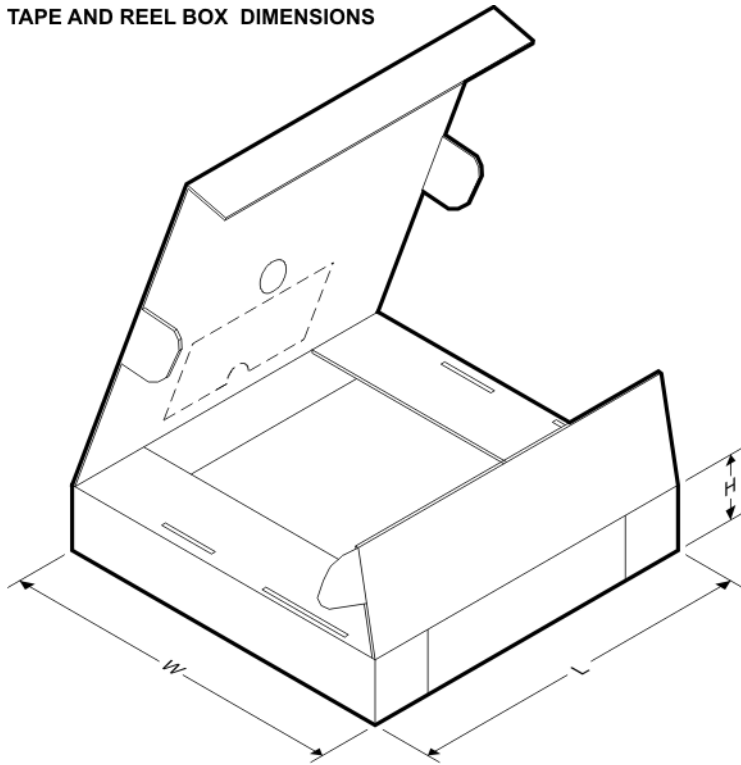


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| MSP430F2001IPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| MSP430F2001IRSAR | QFN | RSA | 16 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSP430F2001IRSAT | QFN | RSA | 16 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSP430F2001TPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| MSP430F2001TRSAR | QFN | RSA | 16 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSP430F2001TRSAT | QFN | RSA | 16 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSP430F2002IPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| MSP430F2002IRSAR | QFN | RSA | 16 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSP430F2002IRSAT | QFN | RSA | 16 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSP430F2002TPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| MSP430F2002TRSAR | QFN | RSA | 16 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSP430F2002TRSAT | QFN | RSA | 16 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSP430F2003IPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| MSP430F2003IRSAR | QFN | RSA | 16 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSP430F2003IRSAT | QFN | RSA | 16 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSP430F2003TPWR | TSSOP | PW | 14 | 2500 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| MSP430F2003TRSAR | QFN | RSA | 16 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSP430F2003TRSAT | QFN | RSA | 16 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| MSP430F2011IPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| MSP430F2011IRSAR | QFN | RSA | 16 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSP430F2011IRSAT | QFN | RSA | 16 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSP430F2011TPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| MSP430F2011TRSAR | QFN | RSA | 16 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSP430F2011TRSAT | QFN | RSA | 16 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSP430F2012IPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| MSP430F2012IRSAR | QFN | RSA | 16 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSP430F2012IRSAT | QFN | RSA | 16 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSP430F2012TPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| MSP430F2012TRSAR | QFN | RSA | 16 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSP430F2012TRSAT | QFN | RSA | 16 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSP430F2013IPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| MSP430F2013IRSAR | QFN | RSA | 16 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSP430F2013IRSAT | QFN | RSA | 16 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSP430F2013TPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| MSP430F2013TRSAR | QFN | RSA | 16 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSP430F2013TRSAT | QFN | RSA | 16 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS

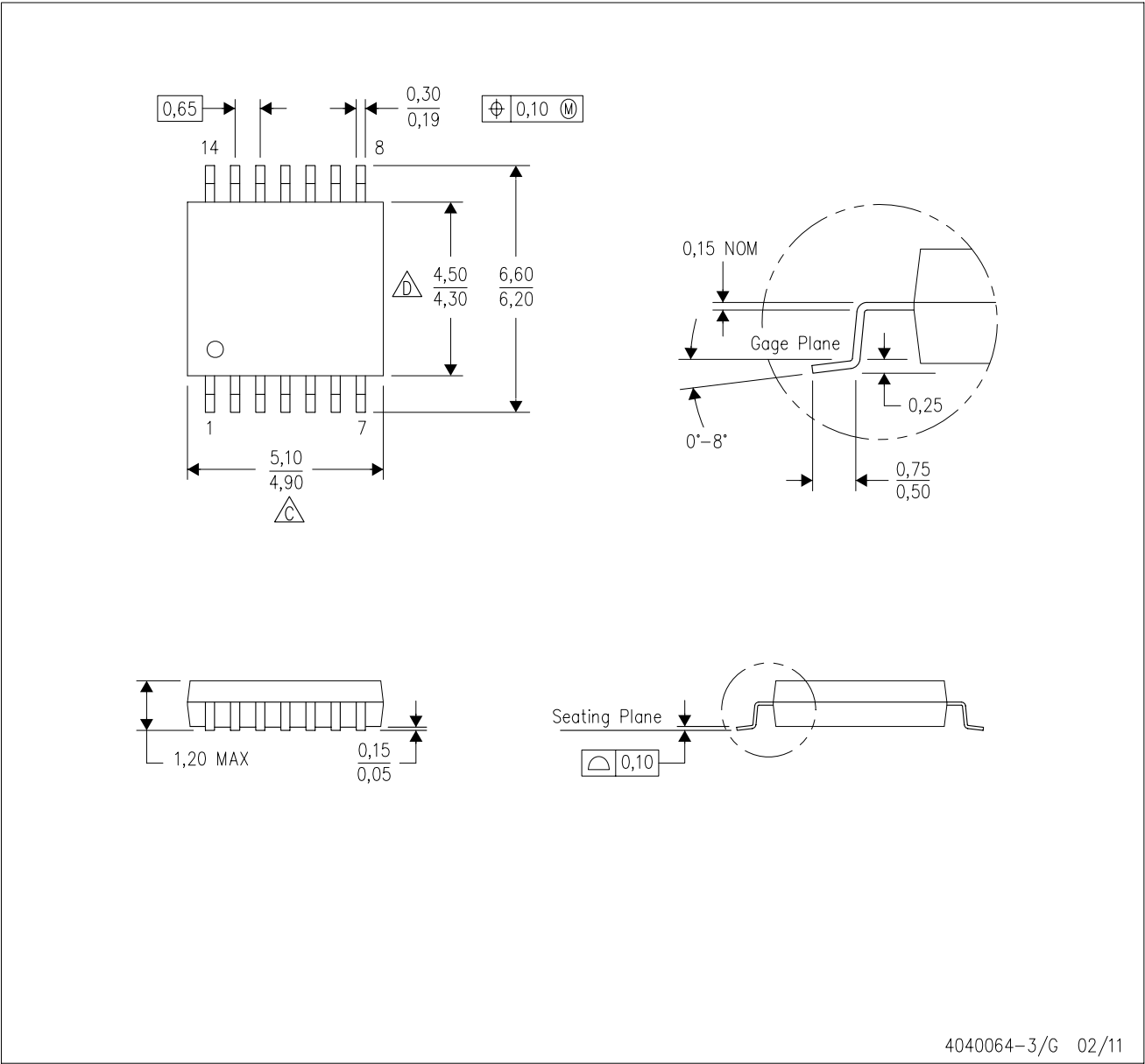


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| MSP430F2001IPWR | TSSOP | PW | 14 | 2000 | 853.0 | 449.0 | 35.0 |
| MSP430F2001IRSAR | QFN | RSA | 16 | 3000 | 367.0 | 367.0 | 35.0 |
| MSP430F2001IRSAT | QFN | RSA | 16 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430F2001TPWR | TSSOP | PW | 14 | 2000 | 853.0 | 449.0 | 35.0 |
| MSP430F2001TRSAR | QFN | RSA | 16 | 3000 | 367.0 | 367.0 | 35.0 |
| MSP430F2001TRSAT | QFN | RSA | 16 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430F2002IPWR | TSSOP | PW | 14 | 2000 | 853.0 | 449.0 | 35.0 |
| MSP430F2002IRSAR | QFN | RSA | 16 | 3000 | 367.0 | 367.0 | 35.0 |
| MSP430F2002IRSAT | QFN | RSA | 16 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430F2002TPWR | TSSOP | PW | 14 | 2000 | 853.0 | 449.0 | 35.0 |
| MSP430F2002TRSAR | QFN | RSA | 16 | 3000 | 367.0 | 367.0 | 35.0 |
| MSP430F2002TRSAT | QFN | RSA | 16 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430F2003IPWR | TSSOP | PW | 14 | 2000 | 853.0 | 449.0 | 35.0 |
| MSP430F2003IRSAR | QFN | RSA | 16 | 3000 | 367.0 | 367.0 | 35.0 |
| MSP430F2003IRSAT | QFN | RSA | 16 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430F2003TPWR | TSSOP | PW | 14 | 2500 | 853.0 | 449.0 | 35.0 |
| MSP430F2003TRSAR | QFN | RSA | 16 | 3000 | 367.0 | 367.0 | 35.0 |
| MSP430F2003TRSAT | QFN | RSA | 16 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430F2011IPWR | TSSOP | PW | 14 | 2000 | 853.0 | 449.0 | 35.0 |
| MSP430F2011IRSAR | QFN | RSA | 16 | 3000 | 367.0 | 367.0 | 35.0 |
| MSP430F2011IRSAT | QFN | RSA | 16 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430F2011TPWR | TSSOP | PW | 14 | 2000 | 853.0 | 449.0 | 35.0 |
| MSP430F2011TRSAR | QFN | RSA | 16 | 3000 | 367.0 | 367.0 | 35.0 |
| MSP430F2011TRSAT | QFN | RSA | 16 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430F2012IPWR | TSSOP | PW | 14 | 2000 | 853.0 | 449.0 | 35.0 |
| MSP430F2012IRSAR | QFN | RSA | 16 | 3000 | 367.0 | 367.0 | 35.0 |
| MSP430F2012IRSAT | QFN | RSA | 16 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430F2012TPWR | TSSOP | PW | 14 | 2000 | 853.0 | 449.0 | 35.0 |
| MSP430F2012TRSAR | QFN | RSA | 16 | 3000 | 367.0 | 367.0 | 35.0 |
| MSP430F2012TRSAT | QFN | RSA | 16 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430F2013IPWR | TSSOP | PW | 14 | 2000 | 853.0 | 449.0 | 35.0 |
| MSP430F2013IRSAR | QFN | RSA | 16 | 3000 | 367.0 | 367.0 | 35.0 |
| MSP430F2013IRSAT | QFN | RSA | 16 | 250 | 210.0 | 185.0 | 35.0 |
| MSP430F2013TPWR | TSSOP | PW | 14 | 2000 | 853.0 | 449.0 | 35.0 |
| MSP430F2013TRSAR | QFN | RSA | 16 | 3000 | 367.0 | 367.0 | 35.0 |
| MSP430F2013TRSAT | QFN | RSA | 16 | 250 | 210.0 | 185.0 | 35.0 |

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211284-2/G 08/15

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

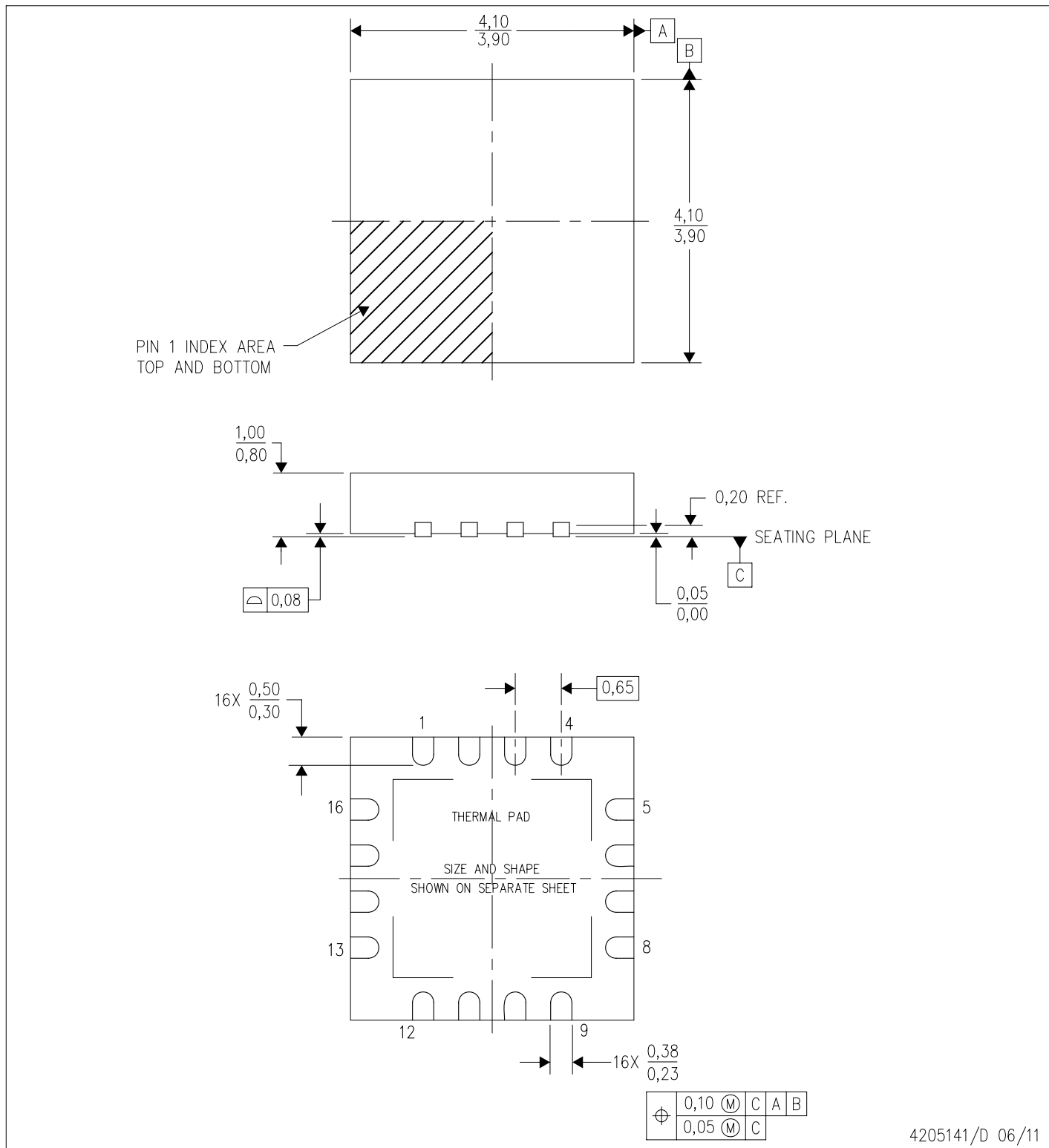
16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

RSA (S-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



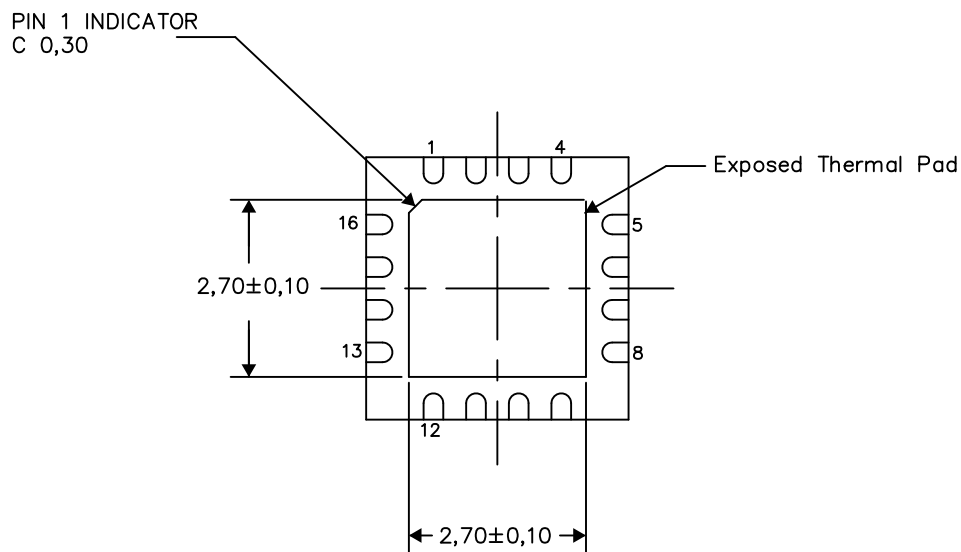
- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Quad Flatpack, No-leads (QFN) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Falls within JEDEC MO-220.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

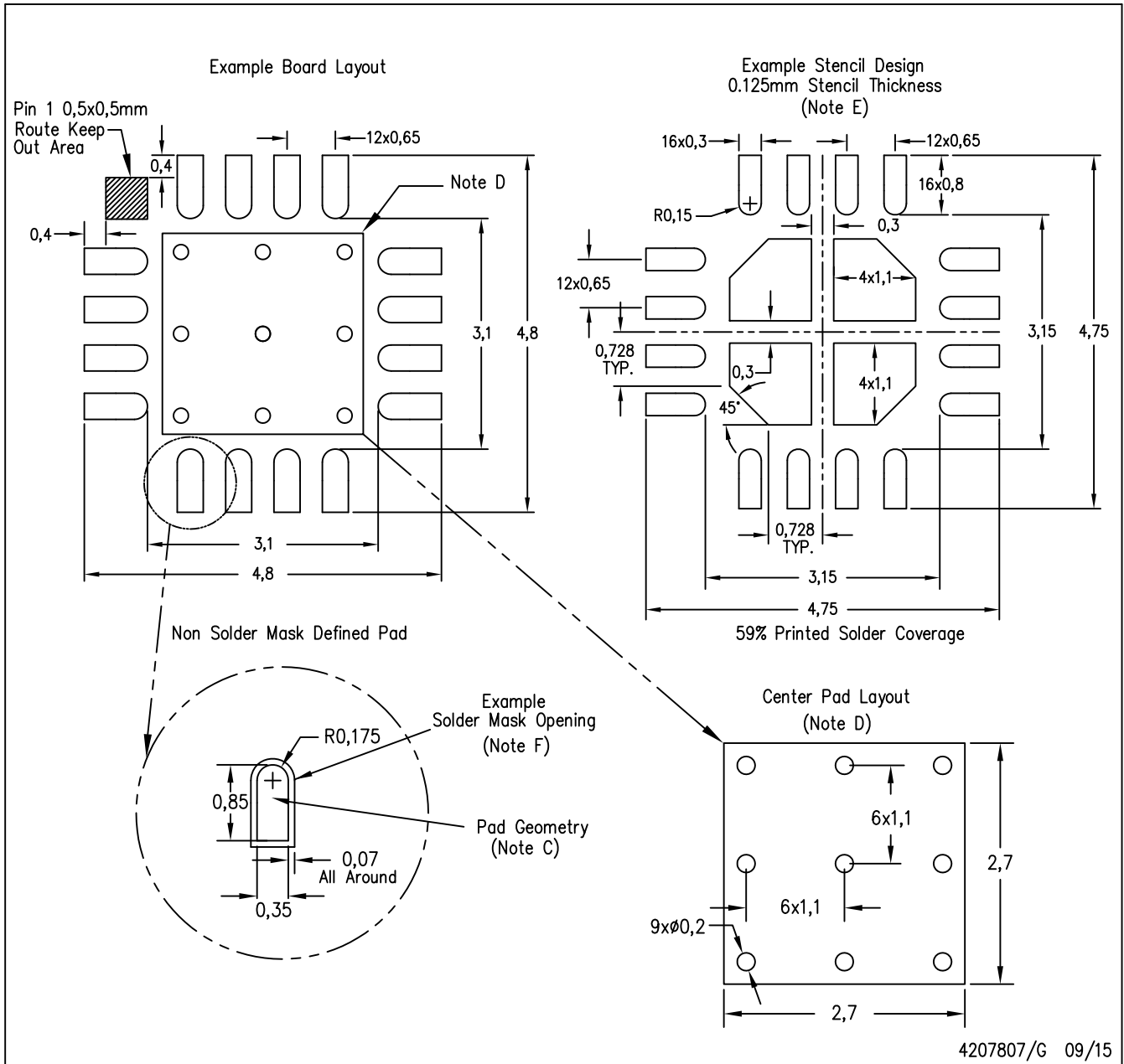
4206364-2/0 09/15

NOTES:

A. All linear dimensions are in millimeters

RSA (S-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - F. Customers should contact their board fabrication site for solder mask tolerances.

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