PM-7542

12-BIT (4-BIT NYBBLE INPUT) MULTIPLYING CMOS D/A CONVERTER

Precision Monolithics Inc.

FEATURES

- 4-Bit Bus Compatible 12-Bit Multiplying DAC
- Complete Microprocessor Interface with On-Chip Address Decoding and Asychronous CLEAR Input
- Fast Interface Timing
- Superior Accuracy: ±1/2 LSB INL Error Over Temperature and ±1 LSB Gain Error
- Excellent Power Supply Rejection ..... 0.002%% Max
- Reduced Digital Charge Injection
- Reduced Output Capicitance
- Small (16-Pin), Narrow (0.3") DIP Packages Suitable for Auto-Insertion and SO Surface Mount Package
- Improved ESD Resistance
- Superior Direct Replacement for AD7542
- Available in Die Form

APPLICATIONS

- Process Control and Industrial Automation
- Programmable Amplifiers
- Digitally-Controlled Power Supplies
- Digitally-Controlled Attenuators
- Digitally-Controlled Filters
- Instrumentation
- Avionics

ORDERING INFORMATION †

GAIN ERROR	NON-LINEARITY	MILITARY* TEMPERATURE –55°C to +125°C	EXTENDED INDUSTRIAL TEMPERATURE –40°C to +85°C	COMMERCIAL TEMPERATURE 0°C to +70°C
±1 LSB	±1/2 LSB	PM7542AQ	PM7542EQ	PM7542GP
±2 LSB	±1 LSB	PM7542BQ	PM7542FQ	–
±2 LSB	±1 LSB	PM7542BRC/883††	PM7542FP	–
±2 LSB	±1 LSB	–	PM7542FS	–

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP and plastic DIP packages. For ordering information, see PMI's Data Book, Section 2.

CROSS REFERENCE

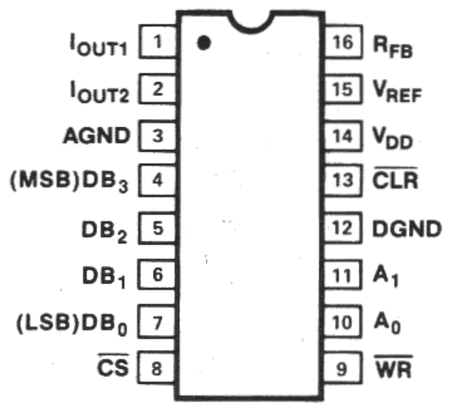
PMI	ADI	TEMPERATURE RANGE
PM7542AQ	AD7542GTD	MIL
PM7542AQ	AD7542TD	
PM7542BQ	AD7542SD	
PM7542EQ	AD7542GBD	IND
PM7542EQ	AD7542BD	
PM7542FQ	AD7542AD	
PM7542GP	AD7542GKN	COM
PM7542GP	AD7542KN	
PM7542FP	AD7542JN	

GENERAL DESCRIPTION

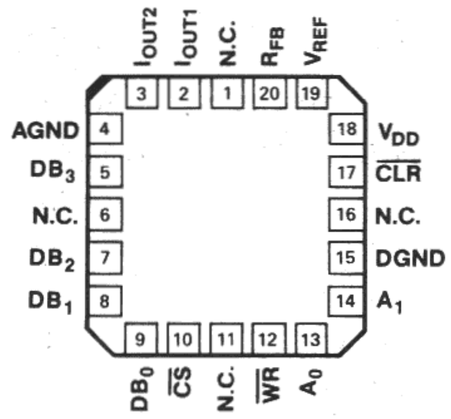
The PM-7542 is a 12-bit resolution, current output, multiplying CMOS DAC with a microprocessor interface to 4-bit busses. Improved analog accuracy, a fast digital interface, and input ESD protective circuitry make this a superior second-source to the industry standard 7542. This improved performance permits the easy upgrading of accuracy and ruggedness in existing designs.

Continued

PIN CONNECTIONS

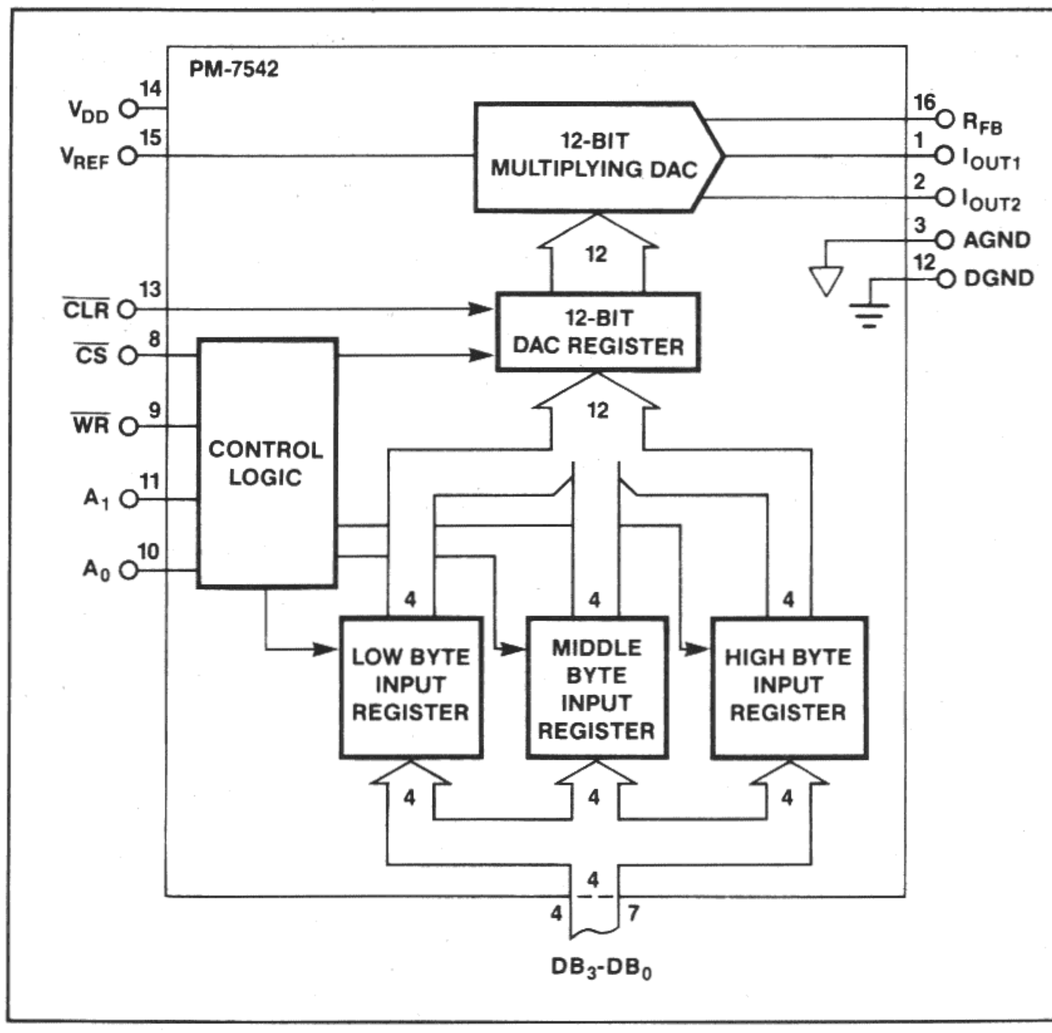


16-PIN CERDIP (Q-Suffix)
16-PIN EPOXY DIP (P-Suffix)
16-PIN SOL (S-Suffix)



20-PIN LCC (RC-Suffix)

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION *Continued*

Under microprocessor control, 4-bit data bytes are loaded from a data bus into three 4-bit input registers. The resulting 12-bit data word can then be transferred to a DAC register, updating the analog output. Data input and transfer operations resemble the WRITE cycle of a static RAM. An asynchronous CLEAR input permits the immediate resetting of the DAC register to all zeros, without affecting the data resident in the input registers.

Improved linearity and gain error performance may permit a reduced circuit parts count through the elimination of trimming components. Fast interface timing reduces design considerations while minimizing microprocessor wait states. The PM-7542 is available in standard plastic and CerDIP packages that are compatible with auto-insertion equipment.

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C, unless otherwise noted.)

V_{DD} (to DGND) ..... +17V
V_{REF} (to DGND) ..... ±25V
V_{RFB} (to DGND) ..... ±25V
AGND to DGND ..... V_{DD} + 0.3V
DGND to AGND ..... V_{DD} + 0.3V
Digital Input Voltage Range ..... –0.3V to V_{DD}
Output Voltage (Pin 1, Pin 2) ..... –0.3V to V_{DD}

Operating Temperature Range
A/B/BRC ..... –55°C to +125°C
E/F Versions ..... –40°C to +85°C
GP Version ..... 0°C to +70°C
Junction Temperature ..... +150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... 300°C

PACKAGE TYPE	Θ_{JA} (NOTE 1)	Θ_{JC}	UNITS
16-Pin Hermetic DIP (Q)	94	12	°C/W
16-Pin Plastic DIP (P)	76	33	°C/W
20-Contact LCC (RC)	88	33	°C/W
16-Pin SOL (S)	92	27	°C/W

NOTE:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SOL package.

CAUTION:
1. Do not apply voltages higher than V_{DD} or less than AGND potential on any terminal except V_{REF} (Pin 15) and R_{FB} (Pin 16).
2. The digital control inputs are zener-protected; however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use.
3. Use proper anti-static handling procedures.
4. Absolute Maximum Ratings apply to both packaged devices and DICE. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device.

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V; V_{REF} = +10V; V_{OUT1} = V_{OUT2} = V_{DGND} = 0V; T_A = –55°C to +125°C for PM-7542AQ/BQ; T_A = –40°C to +85°C for PM-7542EQ/FQ/FP/FS; and T_A = 0°C to +70°C for PM-7542GP, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-7542 MIN	PM-7542 TYP	PM-7542 MAX	UNITS
STATIC ACCURACY						
Resolution	N		12	—	—	Bits
Nonlinearity (Note 1)	INL	PM-7542A/E/G	—	—	±1/2	LSB
		PM-7542B/F	—	—	1	
Differential Nonlinearity (Note 2)	DNL	PM-7542A/E	—	—	±1/2	LSB
		PM-7542B/F/G	—	—	±1	
Gain Error (Note 3)	G_{FSE}	T_A = +25°C				LSB
		PM-7542A/E	—	—	1	
		PM-7542B/F/G	—	—	2	
		T_A = Full Temp. Range				
		All Grades	—	—	2	
Gain Tempco (ΔGain/ΔTemp) (Note 6)	TC_{GFS}		—	—	±5	ppm/°C
Power Supply Rejection Ratio (ΔGain/ΔTemp)	PSRR	ΔV_{DD} = ±5%	—	0.0006	±0.002	%/%
Output Leakage Current (Notes 4, 5)	I_{LKG}	T_A = +25°C	—	—	±5	nA
		T_A = Full Temp. Range				
		PM-7542A/B	—	—	±100	
		PM-7542E/F/G	—	—	±25	
Zero Scale Error (Notes 8, 13)	I_{ZSE}	T_A = +25°C	—	—	**±0.02**	LSB
		T_A = Full Temp. Range				
		PM-7542A/B	—	—	**±0.5**	
		PM-7542E/F/G	—	—	**±0.1**	
Input Resistance (Note 9)	R_{IN}		7	11	15	kΩ

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V; V_{REF} = +10V; V_{OUT1} = V_{OUT2} = V_{AGND} = V_{DGND} = 0V; T_A = –55°C to +125°C for PM-7542AQ/BQ; T_A = –40°C to +85°C for PM-7542EQ/FQ/FP/FS; and T_A = 0°C to +70°C for PM-7542GP, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	PM-7542 MIN	PM-7542 TYP	PM-7542 MAX	UNITS
AC PERFORMANCE						
Output Current Settling Time (Notes 6, 7)	t_s	T_A = +25°C	—	0.25	1	µs
Feedthrough Error (V_{REF} to I_{OUT1}) (Note 6)	FT	V_{REF} = 20V_{p-p} @ f = 10kHz Digital Input = 0000 0000 0000 T_A = +25°C	—	0.45	1	mV_{p-p}
Digital to Analog Glitch Energy (Note 6)	Q	V_{REF} = 0V I_{OUT} Load = 100Ω C_{EXT} = 13pF DAC register loaded alternately with all 0s and all 1s	—	2	200	nVs
Total Harmonic Distortion (Note 6)	THD	V_{REF} = 6V RMS @ 1kHz DAC register loaded with all 1s	—	—	–92	dB
Output Noise Voltage Density (Notes 6, 14)	e_n	10Hz to 100kHz measured between R_{FB} and I_{OUT}	—	—	13	$nV/\sqrt{Hz}$
POWER SUPPLY						
Supply Voltage Range	V_{DD}		4.75	5	5.25	V
Supply Current	I_{DD}	All digital inputs = V_{IH} or V_{IL} All digital inputs = 0V or V_{DD}	— —	— —	2 0.1	mA
DIGITAL INPUTS						
Digital Input HIGH	V_{IH}		2.4	—	—	V
Digital Input LOW	V_{IL}		—	—	0.8	V
Input Leakage Current (Note 10)	I_{IL}	V_{IN} = 0V to +5V	—	—	±1	µA
Input Capacitance (Note 6)	C_{IN}	V_{IN} = 0V	—	—	8	pF
ANALOG OUTPUTS						
Output Capacitance (Note 6)	C_{OUT1} C_{OUT2}	Digital Inputs = V_{IH}	— —	30 65	60 90	pF
	C_{OUT1} C_{OUT2}	Digital Inputs = V_{IL}	— —	65 30	90 60	

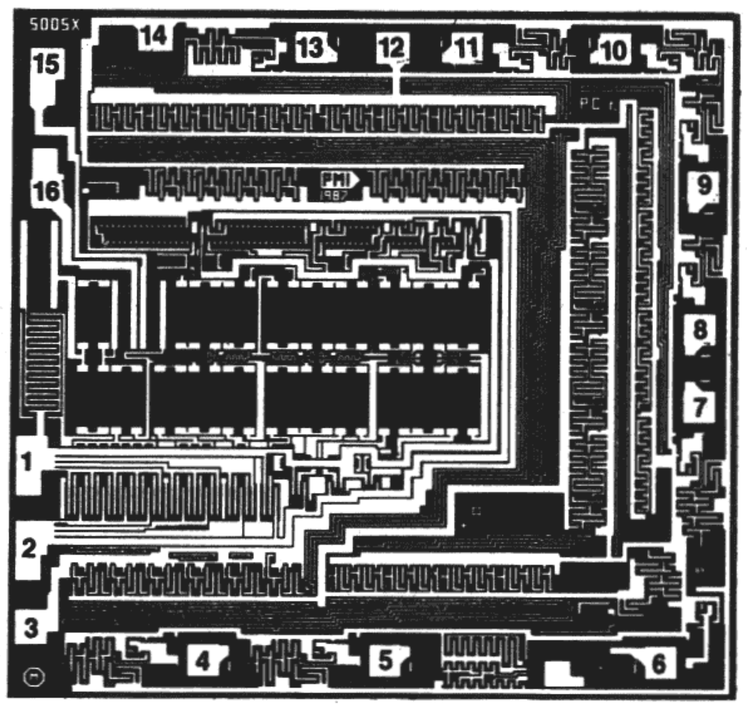
ELECTRICAL CHARACTERISTICS at V_{DD} = +5V; V_{REF} = +10V; V_{OUT1} = V_{OUT2} = V_{AGND} = V_{DGND} = 0V; T_A = –55°C to +125°C for PM-7542AQ/BQ; T_A = –40°C to +85°C for PM-7542EQ/FQ/FP/FS; and T_A = 0°C to +70°C for PM-7542GP, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	PM-7542 MIN	PM-7542 TYP	PM-7542 MAX	UNITS
TIMING CHARACTERISTICS (Note 6)						
WRITE Pulse Width	t_{WR}	T_A = +25°C	90	—	—	ns
		T_A = Full Temp. Range	120	—	—	
CLEAR Pulse Width	t_{CLR}	T_A = +25°C	70	—	—	ns
		T_A = Full Temp. Range	90	—	—	
Address Valid to WRITE Hold Time	t_{AWH}	T_A = +25°C	10	—	—	ns
		T_A = Full Temp. Range	10	—	—	
Chip Select to WRITE Hold Time	t_{CWH}	T_A = +25°C	0	—	—	ns
		T_A = Full Temp. Range	10	—	—	
Chip Select to WRITE Set-up Time	t_{CWS}	T_A = +25°C	0	—	—	ns
		T_A = Full Temp. Range	10	—	—	
Address Valid to WRITE Set-up Time	t_{AWS}	T_A = +25°C	0	—	—	ns
		T_A = Full Temp. Range	0	—	—	
Data Set-up Time	t_{DS}	T_A = +25°C	40	—	—	ns
		T_A = Full Temp. Range	40	—	—	
Data Hold Time	t_{DH}	T_A = +25°C	40	—	—	ns
		T_A = Full Temp. Range	40	—	—	

NOTES:

1. ±1/2 LSB = ±0.012% of Full Scale.
2. All grades are monotonic to 12-bits over temperature.
3. Using internal feedback resistor.
4. Applies to I_{OUT1}; all digital inputs = V_{IL}.
5. Specification also applies for I_{OUT2} when all digital inputs = V_{IH}.
6. Guaranteed by design and not tested.
7. I_{OUT1} Load = 100Ω, C_{EXT} = 13pF, digital input = 0V to V_{DD} or V_{DD} to 0V. Extrapolated to 1/2 LSB: t_s = Propagation Delay (t_{PD}) + 9τ, where τ = measured time constant of the final RC decay.
8. V_{REF} = +10V, all digital inputs = 0V.
9. Absolute temperature coefficient is less than +50 ppm/°C.
10. Digital inputs are CMOS gates; I_{IN} is typically 1nA at +25°C.
11. V_{REF} = 0V, all digital inputs = 0V to V_{DD} or V_{DD} to 0V.
12. All digital inputs = 0V.
13. Calculated from worst case R_{REF}:
    I_{ZSE} (in LSBs) = (R_{REF} × I_{LKG} × 4096)/V_{REF}.
14. Calculations from $e_n = \sqrt{4K\,TRB}$ where:
    K = Boltzmann constant, J/°K R = resistance Ω
    T = resistor temperature, °K B = bandwidth, Hz

DICE CHARACTERISTICS



DIE SIZE 0.116 × 0.109 inch, 12,644 sq. mils
(2.95 × 2.77 mm, 8.17 sq. mm)

1. I_{OUT1}
2. I_{OUT2}
3. AGND
4. DB_3 (MSB)
5. DB_2
6. DB_1
7. DB_0 (LSB)
8. $\overline{CS}$
9. $\overline{WR}$
10. A_0
11. A_1
12. DGND
13. $\overline{CLR}$
14. V_{DD} (Substrate)
15. V_{REF}
16. R_{FB}

For additional DICE ordering information, refer to 1990/91 Data Book, Section 2.

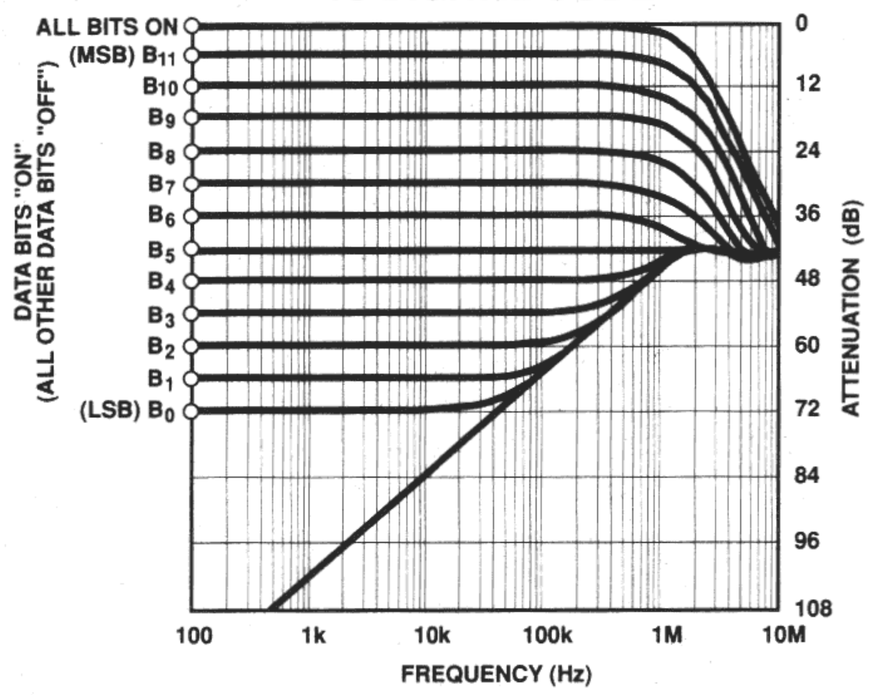
WAFER TEST LIMITS at V_{DD} = +5V, V_{REF} = +10V; V_{OUT1} = V_{OUT2} = V_{AGND} = V_{DGND} = 0V, T_A = +25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-7542GBC LIMIT	UNITS
STATIC ACCURACY				
Resolution	N		12	Bits MIN
Integral Nonlinearity	INL		±1	LSB MAX
Differential Nonlinearity	DNL		±1	LSB MAX
Gain Error	G_{FSE}	Using internal feedback resistor	±2	LSB MAX
Power Supply Rejection Ratio	PSRR	ΔV_{DD} = ±5%	±0.002	%/% MAX
Output Leakage Current (I_{OUT1})	I_{LKG}	Digital Inputs = V_{IL}	±5	nA MAX
REFERENCE INPUT				
Input Resistance	R_{REF}		7/15	kΩ MIN/MAX
DIGITAL INPUTS				
Digital Input HIGH	V_{IH}		2.4	V MIN
Digital Input LOW	V_{IL}		0.8	V MAX
Input Leakage Current	I_{IL}	V_{IN} = 0V to V_{DD}	±1	μA MAX
POWER SUPPLY				
Supply Current	I_{DD}	Digital Inputs = V_{IH} or V_{IL} Digital Inputs = 0V or V_{DD}	2 0.1	mA MAX

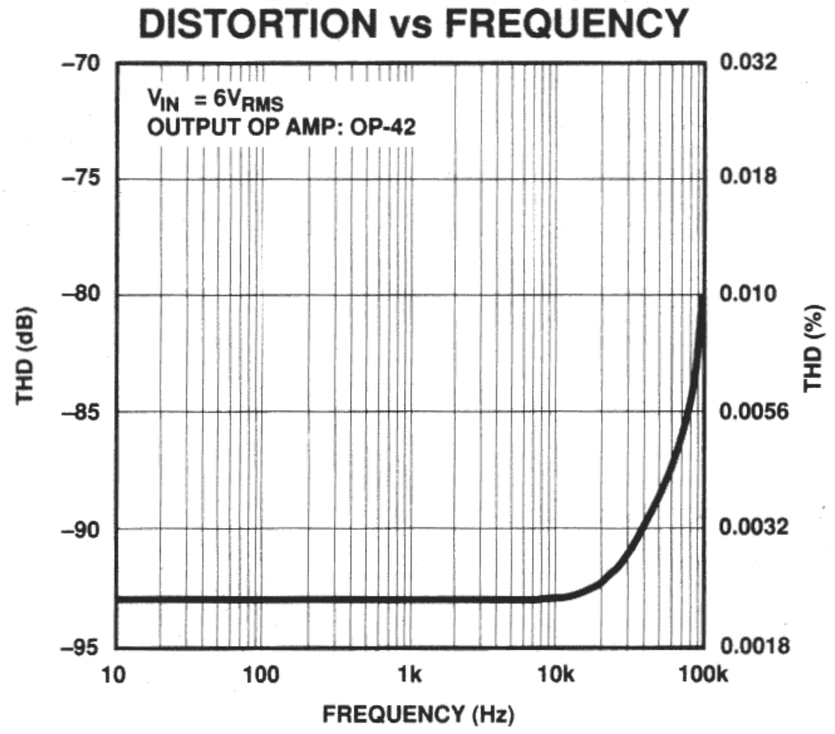
NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

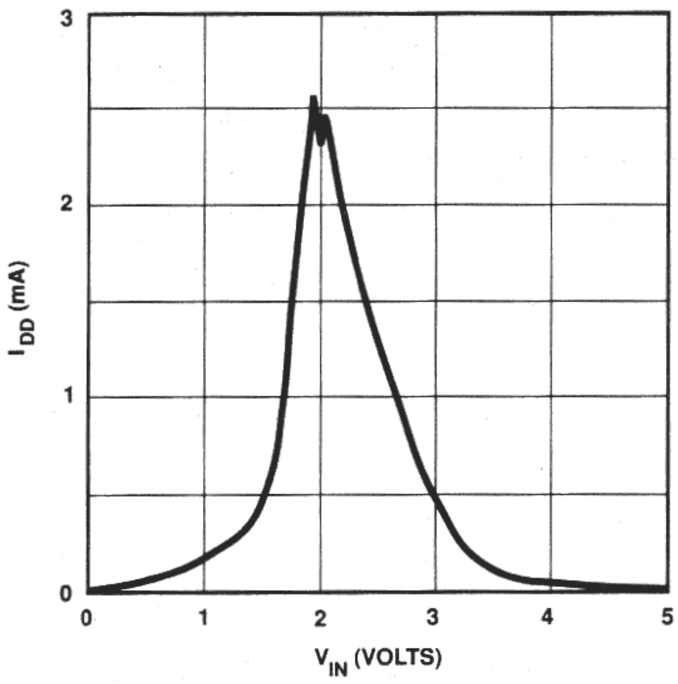
MULTIPLYING MODE FREQUENCY RESPONSE vs DIGITAL CODE



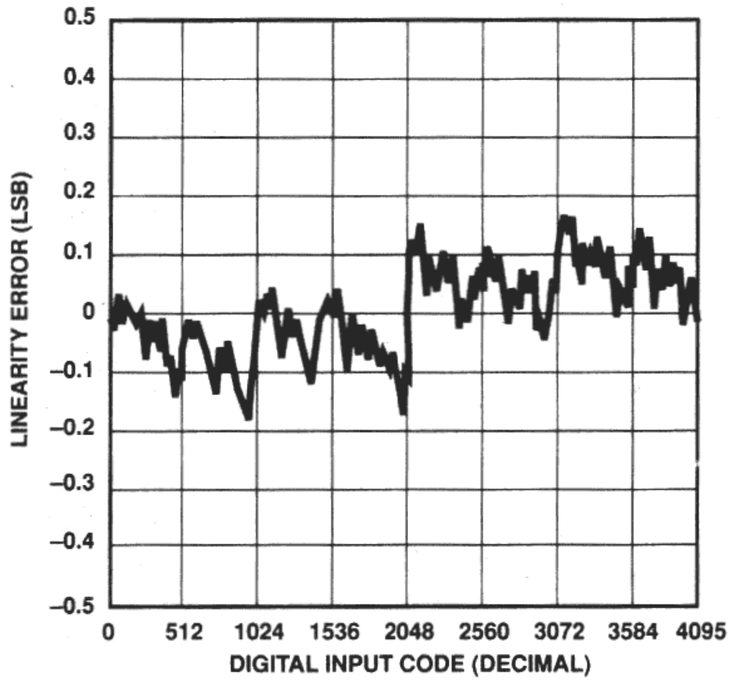
MULTIPLYING MODE TOTAL HARMONIC DISTORTION vs FREQUENCY



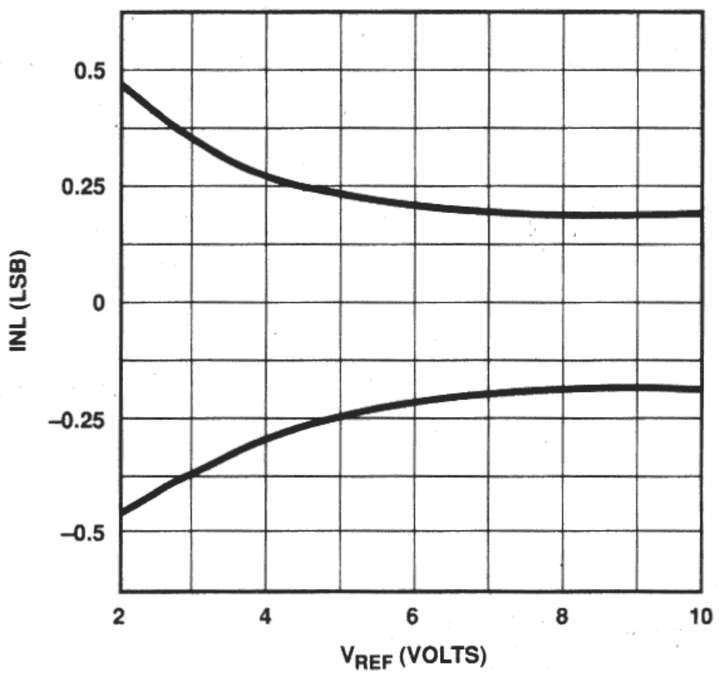
SUPPLY CURRENT vs LOGIC INPUT VOLTAGE



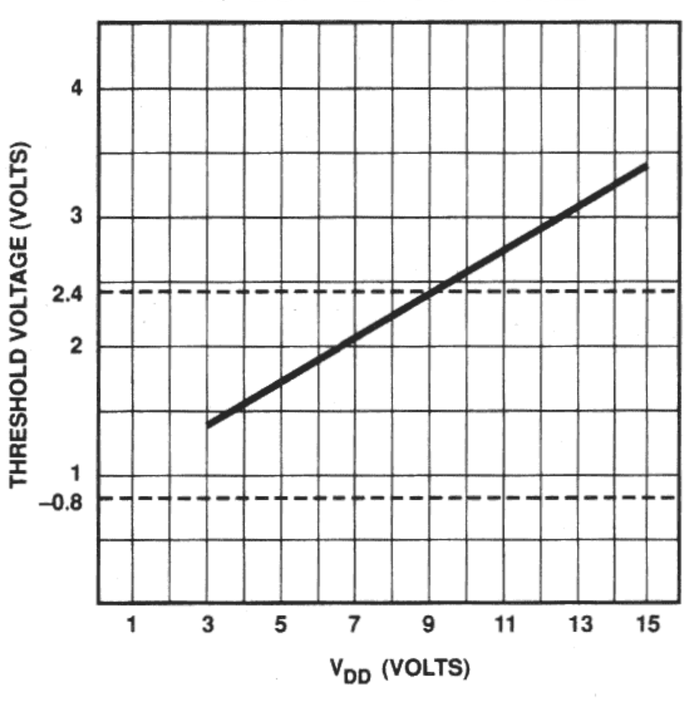
LINEARITY ERROR vs DIGITAL CODE



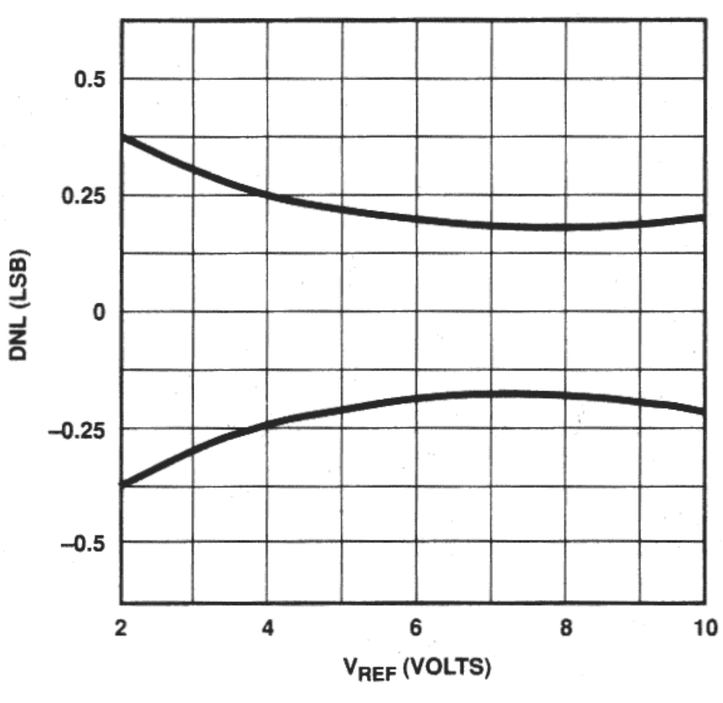
LINEARITY ERROR vs REFERENCE VOLTAGE



LOGIC THRESHOLD VOLTAGE vs SUPPLY VOLTAGE



DNL ERROR vs REFERENCE VOLTAGE



SPECIFICATION DEFINITIONS

RESOLUTION

The resolution of a DAC is the number of states (2^n) that the full-scale range (FSR) is divided (or resolved) into, where "n" is equal to the number of bits.

SETTLING TIME

Time required for the analog output of the DAC to settle to within 1/2 LSB of its final value for a given digital input stimulus; i.e. zero to full scale.

GAIN

Ratio of the DAC's external operational amplifier output voltage to the V_{REF} input voltage when all digital inputs are HIGH.

FEEDTHROUGH ERROR

Error caused by capacitive coupling from V_{REF} to output. Feedthrough error limits are specified with all switches OFF.

OUTPUT CAPACITANCE

Capacitance from I_{OUT1} terminal to ground with all digital inputs LOW, or from I_{OUT2} terminal to ground when all inputs are HIGH.

OUTPUT LEAKAGE CURRENT

Current appearing at I_{OUT1} when all digital inputs are LOW, or at I_{OUT2} terminal when all inputs are HIGH.

GENERAL CIRCUIT INFORMATION

The PM-7542 is a 12-bit multiplying D/A converter with a very low temperature coefficient, R-2R resistor ladder network, data input and control logic, and four data registers. The digital circuitry forms an interface between the 12-bit DAC and a four-bit data bus.

An asynchronous CLEAR function allows resetting the DAC register to a zero code (0000 0000 0000) without altering data stored in the registers.

A simplified circuit of the PM-7542 DAC is shown in Figure 1. An inverted R-2R ladder network consisting of silicon-chrome, thin-film resistor, and twelve pairs of NMOS current-steering switches steer binarily weighted currents into either I_{OUT1} or I_{OUT2}. Switching current to I_{OUT1} or I_{OUT2} yields a constant current in each ladder leg, regardless of digital input code. This constant current results in a constant input resistance at V_{REF} equal to R (typically 11kΩ). The V_{REF} input may be driven by any reference voltage or current, AC or DC, that is within the limits stated in the Absolute Maximum Ratings chart.

The twelve output current-steering switches are in series with the R-2R resistor ladder, and therefore, can introduce bit errors. It is essential then, that the switch "ON" resistance be binarily scaled so that the voltage drop across each switch remains constant. If, for example, switch 1 of Figure 1 was designed with an "ON" resistance of 10 ohms, switch 2 for 20 ohms, etc., a constant 5mV drop will then be maintained across each switch.

To further insure accuracy across the full temperature range, permanently "ON" MOS switches are included in series with the feedback resistor and the R-2R ladder's terminating resistor. The "Simplified DAC Circuit", Figure 1, shows the location of the series switches. These series switches are equivalently scaled to two times switch 1 (MSB) and to switch 12 (LSB) respectively to maintain constant relative voltage drops with varying temperature. During any testing of the resistor ladder or $R_{FEEDBACK}$ (such as incoming inspection), V_{DD} must be present to turn "ON" these series switches.

ESD PROTECTION

The PM-7542 data inputs have been designed with ESD resistance incorporated through careful layout and the inclusion of input protection circuitry.

Figure 2 shows the input protection diodes. High voltage static charges applied to the digital inputs are shunted to the supply and ground rails through forward biased diodes.

These protection diodes are designed to clamp the inputs well below dangerous levels during static discharge conditions.

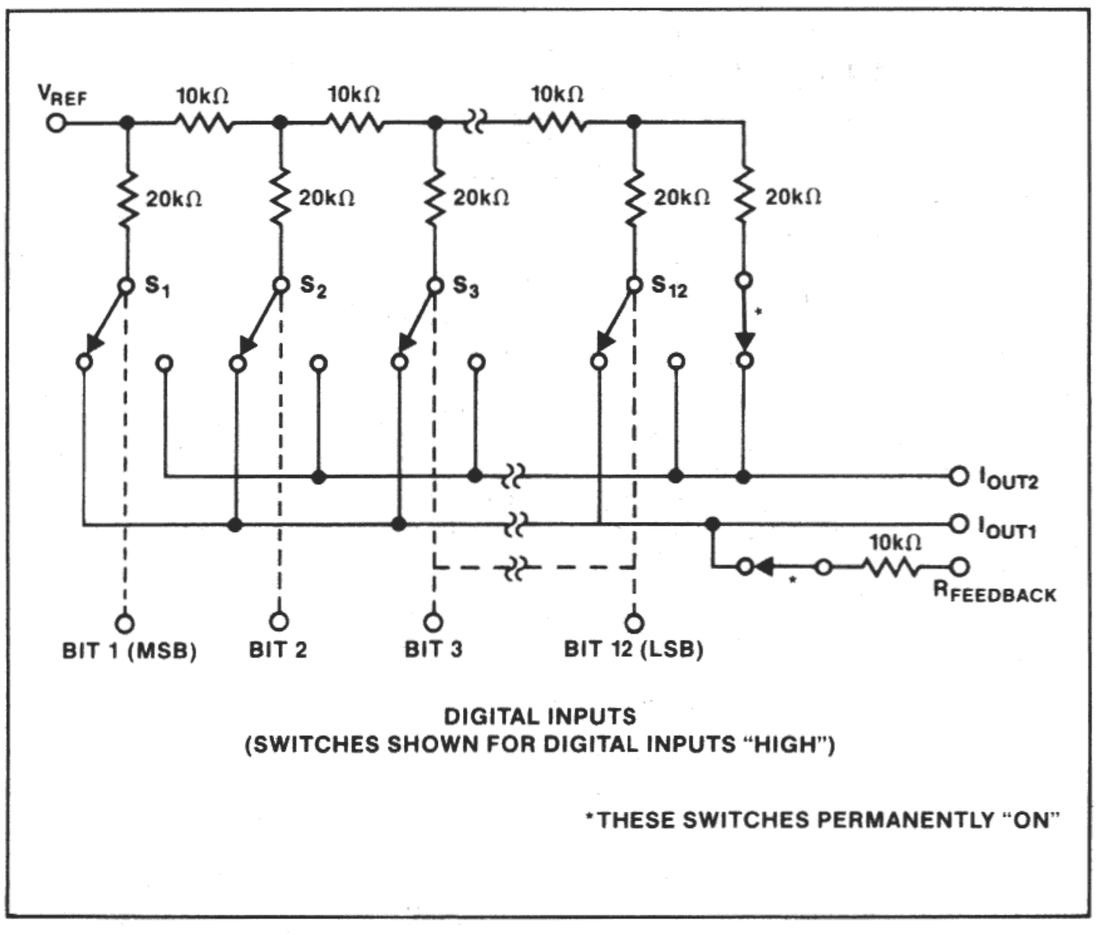


FIGURE 1: *Simplified DAC circuit*

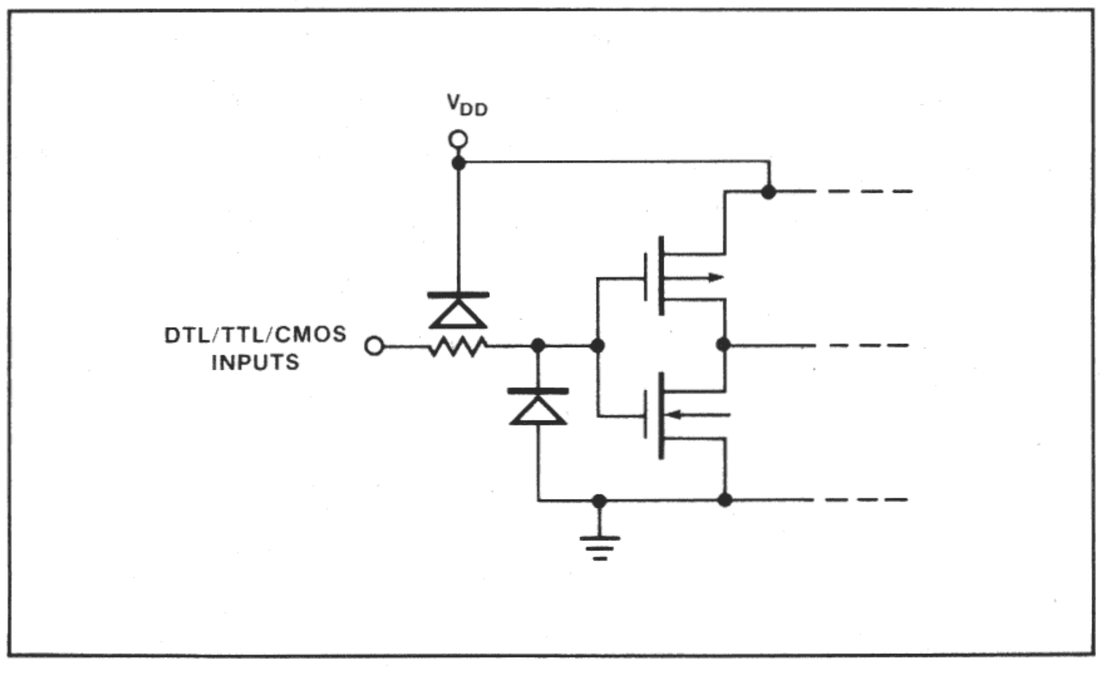


FIGURE 2: *Digital Input Protection*

EQUIVALENT CIRCUIT ANALYSIS

Figures 3 and 4 show equivalent circuits for the DAC with all bits LOW and HIGH, respectively. The reference current is switched to I_{OUT2} when all data bits are LOW and to I_{OUT1} when all bits are HIGH. The $I_{LEAKAGE}$ current source is the combination of surface and junction leakages to the substrate. The 1/4096 current source represents the constant 1-bit current drain through the ladder's terminating resistor.

Output capacitance is dependent upon the digital input code. This is because the gate capacitance of MOS transistors increases with applied gate voltage. This output capacitance varies between the low and high values.

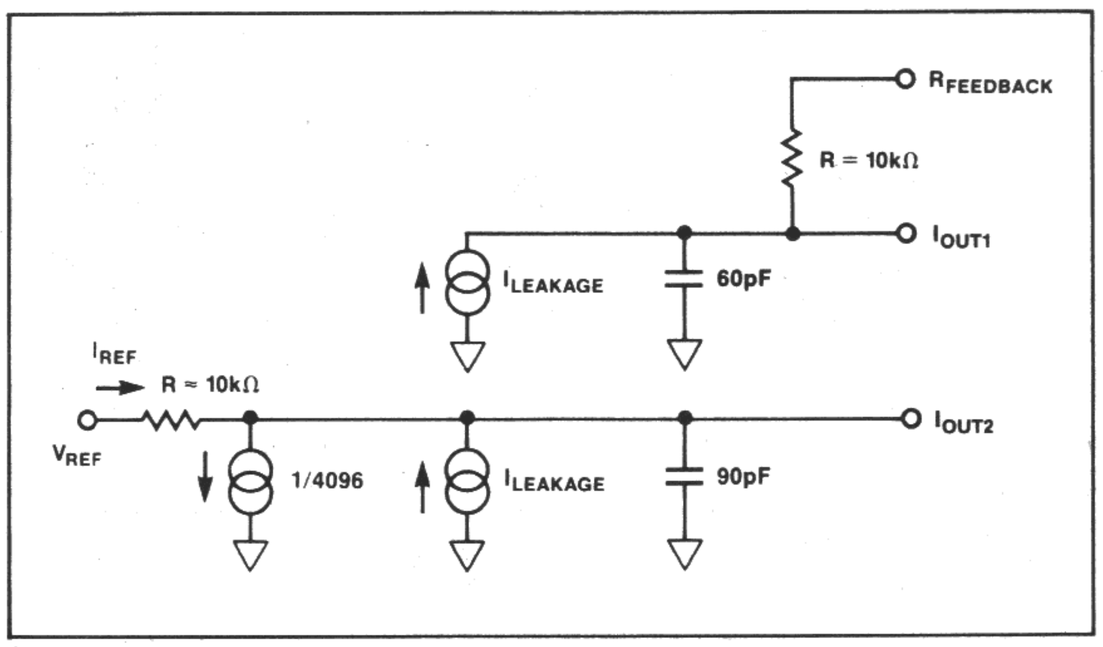


FIGURE 3: *PM-7542 Equivalent Circuit (All Inputs LOW)*

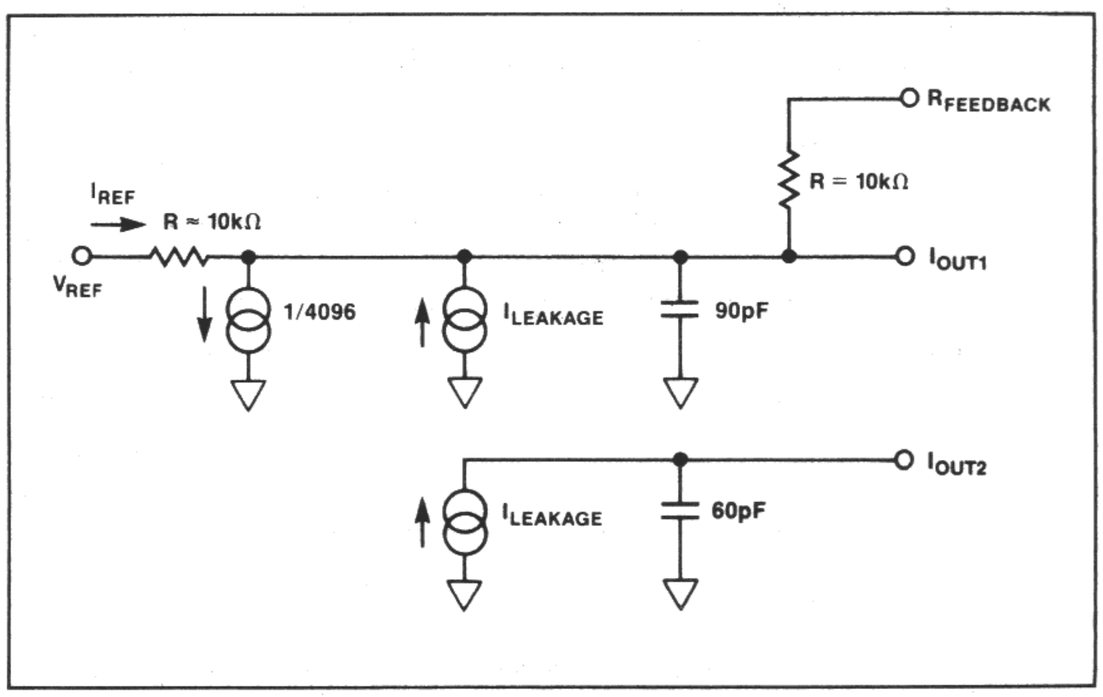


FIGURE 4: *PM-7542 Equivalent Circuits (All Digital Inputs HIGH)*

DYNAMIC PERFORMANCE

OUTPUT IMPEDANCE

The output resistance, as in the case of the output capacitance, varies with the digital input code. This resistance, looking back into the I_{OUT} terminal, may be between 11kΩ (the feedback resistor alone when all digital inputs are LOW) and 7.5kΩ (the feedback resistor in parallel with approximately 30kΩ of the R-2R ladder network resistance when any single bit logic is HIGH). Static accuracy and dynamic performance will be affected by these variations. The gain and phase stability of the output amplifier, board layout, and power supply decoupling will all affect the dynamic performance of the PM-7542. The use of a compensation capacitor may be required when high-speed operational amplifiers are used. It may be connected across the amplifier's feedback resistor to provide the necessary phase compensation to critically damp the output.

The considerations when using high-speed amplifiers are:

1. Phase compensation (see Figures 8 and 9).
2. Power supply decoupling at the device socket and use of proper grounding techniques.

APPLICATIONS INFORMATION

APPLICATION TIPS

In most applications, linearity depends upon the potential of I_{OUT1}, I_{OUT2}, and AGND (pins 1, 2, and 3) being exactly equal to each other. In most applications, the DAC is connected to an external op amp with its noninverting input tied to ground (see Figures 8 and 9). The amplifier selected should have a low input bias current and low drift over temperature. The amplifier's input offset voltage should be nulled to less than ±200μV (less than 10% of 1 LSB).

The operational amplifier's noninverting input should have a minimum resistance connection to ground; the usual bias current compensation resistor should not be used. This resistor can cause a variable offset voltage appearing as a varying output error. All grounded pins should tie to a single common ground point, avoiding ground loops. The V_{DD} power supply should have a low noise level with no transients greater than +17V.

Unused digital inputs must always be grounded or taken to V_{DD}; this will prevent noise from triggering the high impedance digital inputs resulting in output errors. It is also recommended that the used digital inputs be taken to ground or V_{DD} via a high value (1MΩ) resistor; this will prevent the accumulation of static charge if the PC card is disconnected from the system.

Peak supply current flows as the digital inputs pass through the transition voltage. The supply current decreases as the input voltage approaches the supply rails (V_{DD} or DGND), i.e. rapidly slewing logic signals that settle very near the supply rails will minimize supply current.

OUTPUT AMPLIFIER CONSIDERATIONS

When using high speed op amps, a small feedback capacitor (typically 15pF) should be used across the amplifier to minimize overshoot and ringing. For low speed or static applications, AC specifications of the amplifier are not very critical. In high-speed applications, slew rate, settling time, open-loop gain, and gain/phase margin specifications of the amplifier should be selected for the desired performance. It has already been noted that an offset can be caused by including the usual bias current compensation resistor in the amplifier's noninverting input terminal. This resistor should not be used. Instead, the amplifier should have a bias current which is low over the temperature range of interest.

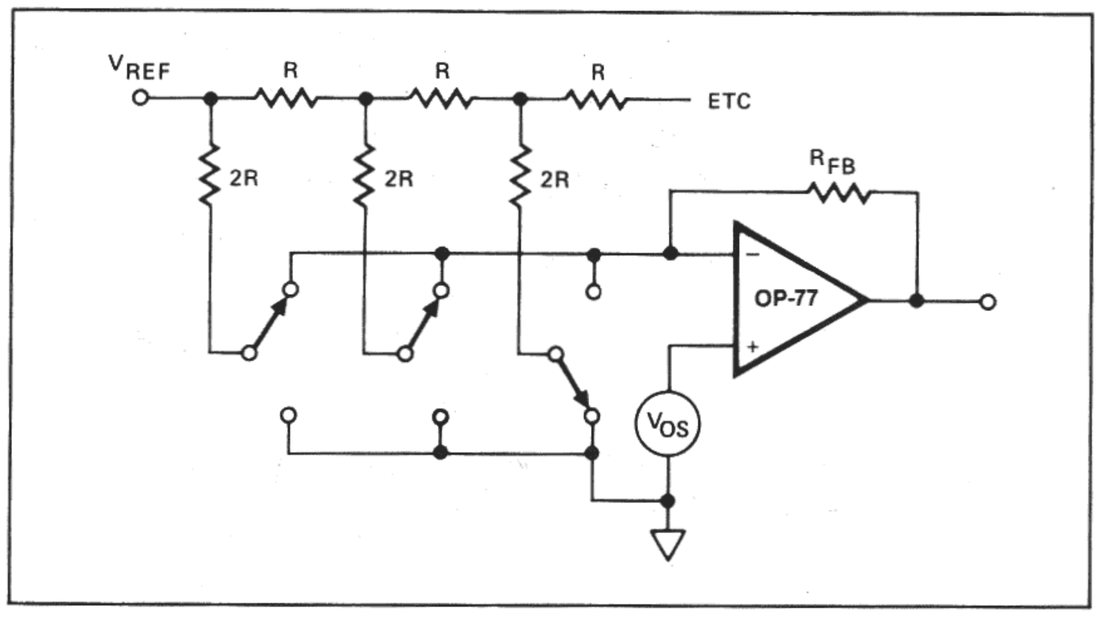


FIGURE 5: *Simplified Circuit*

Static accuracy is affected by the variation in the DAC's output resistance. This variation is best illustrated by using the circuit of Figure 5 and the equation:

$$V_{ERROR} = V_{OS}\left(1 + \frac{R_{FB}}{R_O}\right)$$

where R_O is a function of the digital code, and:
$R_O = 10k\Omega$ for more than four bits of logic 1,
$R_O = 30k\Omega$ for any single bit of logic 1.

Therefore, the offset gain varies as follows:
at code 0011 1111 1111,

$$V_{ERROR} = V_{OS}\left(1 + \frac{10k\Omega}{10k\Omega}\right) = 2V_{OS}$$

at code 0100 0000 0000,

$$V_{ERROR} = V_{OS}\left(1 + \frac{10k\Omega}{30k\Omega}\right) = 4/3V_{OS}$$

The error difference is 2/3 V_{OS}.

Since one LSB has a weight (for $V_{REF} = +10V$) of 2.4 mV for the PM-7542, it is clearly important that V_{OS} be minimized, either using the amplifier's nulling pins, an external nulling network, or by selection of an amplifier with inherently low V_{OS}. Amplifiers with sufficiently low V_{OS} include PMI's OP-77, OP-07, OP-27, and OP-42.

INTERFACE LOGIC OPERATION

The PM-7542 has been designed to be interfaced as a memory mapped output device as shown in Figure 6.

As shown in the device truth table, Table 1, $\overline{CS}$ is an externally decoded **device** address, selecting the device when needed.

A_0 and A_1 are internally decoded **operation** addresses. Each of these four available operations requires a memory location. Data operations are performed by executing a memory WRITE to the address for that operation. This WRITE cycle is identical to that of a RAM. Updating the entire 12-bit data word requires four WRITE cycles (three data nybble loads and one data word transfer). Timing for a WRITE cycle is shown in Figure 7.

The $\overline{CLR}$ input allows the asynchronous reset of the DAC register to 0000 0000 0000. This reset does not affect data held in the input registers. While in unipolar mode, a CLEAR will result in the analog output going to 0V. In bipolar mode, the output will go to $-V_{REF}$.

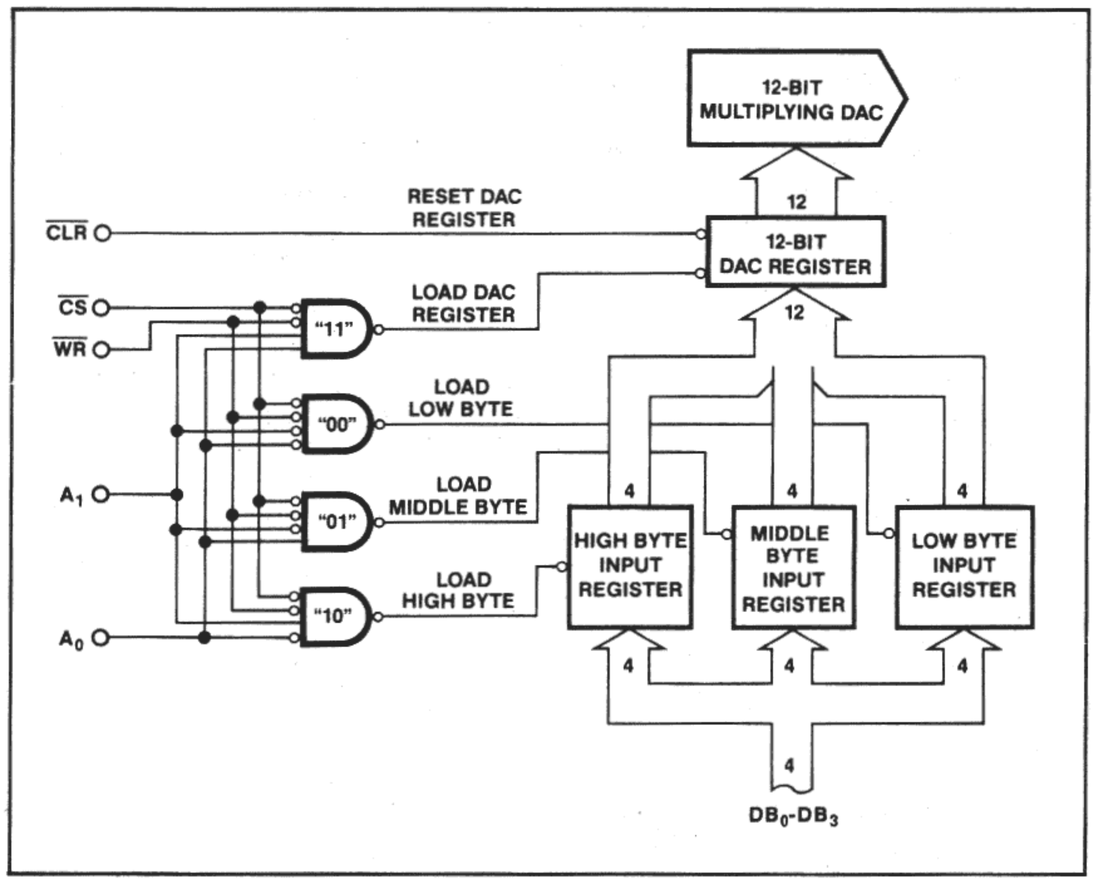


FIGURE 6: *Simplified Input Control Structure*

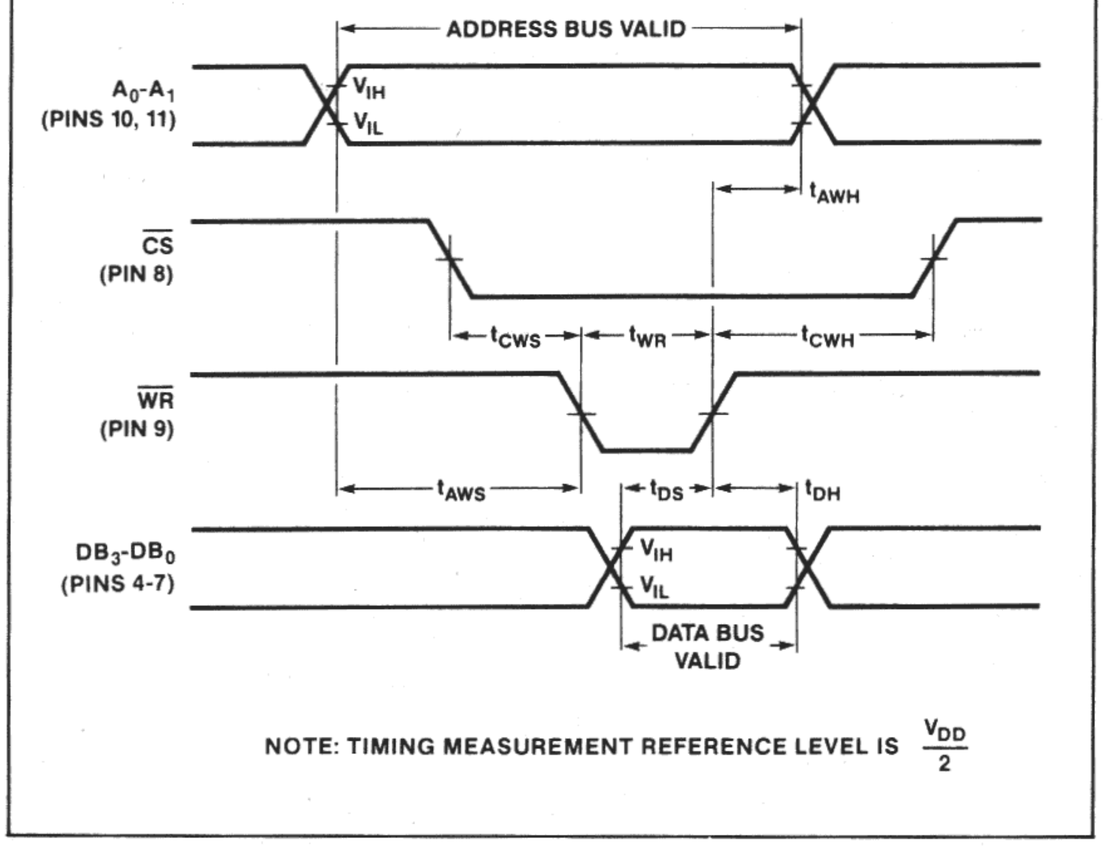


FIGURE 7: *PM-7542 Timing Diagram*

INTERFACE INPUT DESCRIPTION

$\overline{CS}$ (Pin 8)—Chip Select. Active Low.
Selected, with $\overline{WR}$, to load data into an input register or transfer data from input to DAC registers.

$\overline{WR}$ (Pin 9)—Write Input. Active Low.
Selected, with $\overline{CS}$ and appropriate address inputs, to load data into an input register or transfer data from input to DAC registers.

TABLE 1: PM-7542 Truth Table

CONTROL INPUTS					OPERATION	
A_1	A_0	$\overline{CS}$	$\overline{WR}$	$\overline{CLR}$		
X	X	X	X	0	Reset 12-bit DAC Register to Zero Code (Code = 0000 0000 0000). Does not affect Input Registers.	
X	X	1	X	1	No operation. Device not selected.	
0	0	0	↑	1	Load LOW Byte (Note 5) Data Register on Rising Edge.	Load Addressed Data Register With Data at DB_0-DB_3.
0	1	0	↑	1	Load MIDDLE Byte (Note 5) Data Register on Rising Edge.	
1	0	0	↑	1	Load HIGH Byte (Note 5) Data Register on Rising Edge.	
1	1	0	↓↑	1	Load DAC Register with 12-Bit Data in LOW, MIDDLE, and HIGH Byte Data Registers (Note 6).	

NOTES:
1. 1 indicates logic HIGH
2. 0 indicates logic LOW
3. X indicates don't care
4. ↑ indicates LOW to HIGH transition
5. Input

Data Bit	DB_3	DB_2	DB_1	DB_0	DB_3	DB_2	DB_1	DB_0	DB_3	DB_2	DB_1	DB_0	
MSB→	X	X	X	X	X	X	X	X	X	X	X	X	←LSB
	HIGH BYTE				MIDDLE BYTE				LOW BYTE				

6. These control signals are level triggered

A_0 (Pin 10), A_1 (Pin 11)—Address Inputs.
Addressed, with $\overline{CS}$ and $\overline{WR}$ selected, to perform data load or data transfer operations. See Table 1 for truth table.

$\overline{CLR}$ (Pin 13)—Clear Input. Active Low. Asynchronous.
When LOW, 12-bit DAC register is forced to a zero code (0000 0000 0000) regardless of other interface inputs.

UNIPOLAR OPERATION (2-QUADRANT)

The circuits shown in Figures 8 and 9 may be used with an AC or DC reference voltage. The circuits output will range between 0V and approximately $-V_{REF}$ (4095/4096) depending upon the digital input code. The relationship between the digital input and the analog output is shown in Table 2. The limiting parameters for the V_{REF} range are the maximum input voltage range of the op amp or ±25V, whichever is lowest.

Gain error may be trimmed by adjusting R_1 as shown in Figure 9. The DAC register must first be loaded with all 1s. R_1 may then be adjusted until $V_{OUT} = -V_{REF}$ (4095/4096). In the case of an adjustable V_{REF}, R_1 and $R_{FEEDBACK}$ may be omitted, with V_{REF} adjusted to yield the desired full-scale output.

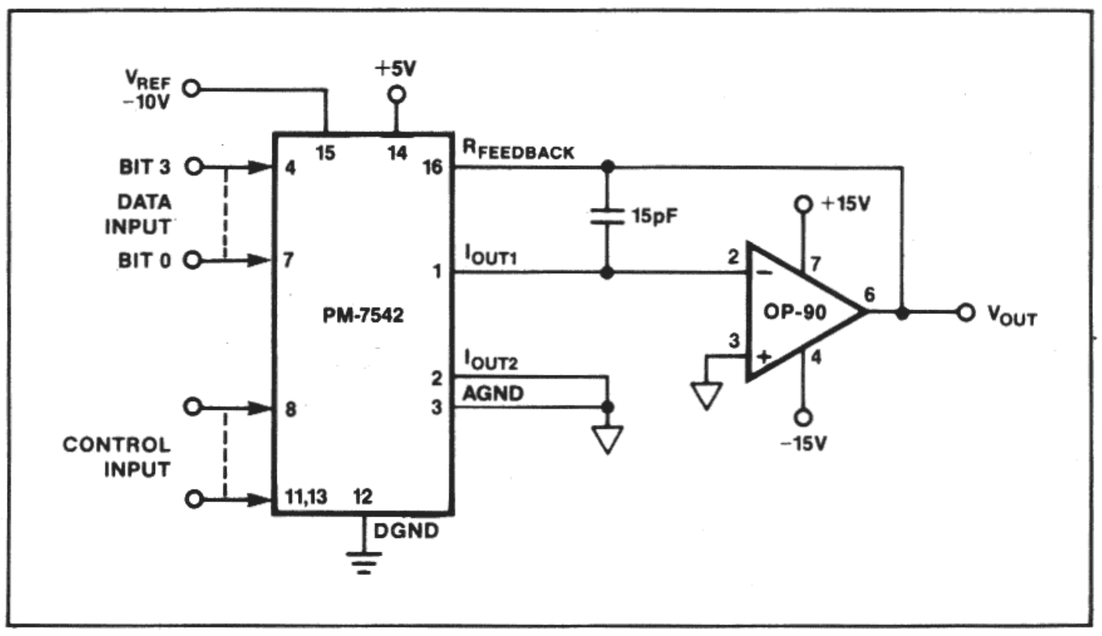


FIGURE 8: *Unipolar Operation with High Accuracy Micropower Op Amp (2-Quadrant)*

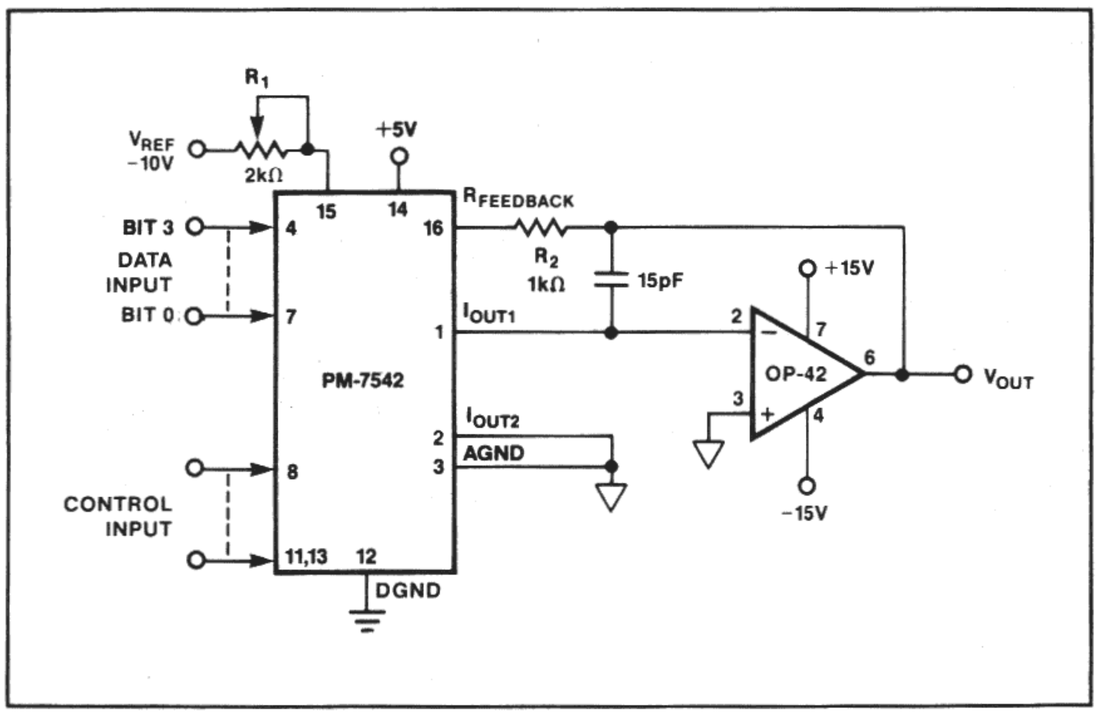


FIGURE 9: *Unipolar Operation with Fast Op Amp and Gain Error Trimming (2-Quadrant)*

In many applications the PM-7542's negligible zero scale error and very low gain error permit the elimination of the trimming components (R_1 and the external $R_{FEEDBACK}$) without adverse effects on circuit performance.

TABLE 2: Unipolar Code Table

DIGITAL INPUT MSB LSB	NOMINAL ANALOG OUTPUT (V_{OUT} as shown in Figures 8 and 9)
1 1 1 1 1 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{4095}{4096}\right)$
1 0 0 0 0 0 0 0 0 0 0 1	$-V_{REF}\left(\frac{2049}{4096}\right)$
1 0 0 0 0 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{2048}{4096}\right) = -\frac{V_{REF}}{2}$
0 1 1 1 1 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{2047}{4096}\right)$
0 0 0 0 0 0 0 0 0 0 0 1	$-V_{REF}\left(\frac{1}{4096}\right)$
0 0 0 0 0 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{0}{4096}\right) = 0$

NOTES:
1. Nominal full scale for the circuits of Figures 8 and 9 is given by $FS = V_{REF}\left(\frac{4095}{4096}\right)$.
2. Nominal LSB magnitude for the circuits of Figures 8 and 9 is given by $LSB = V_{REF}\left(\frac{1}{4096}\right)$ or $V_{REF}(2^{-n})$.

BIPOLAR OPERATION (4-QUADRANT)

Figure 10 details a suggested circuit for bipolar, or offset binary operation. Table 3 shows the digital input to analog output relationship. The circuit uses offset binary coding. Two's complement code can be converted to offset binary by software inversion of the MSB or by the addition of an external inverter to the MSB input.

Resistors R_3, R_4, and R_5 must be selected to match within 0.01% and must all be of the same (preferably metal foil) type to assure temperature coefficient matching. Mismatching between R_3 and R_4 causes offset and full scale errors while an R_5 to R_4 and R_3 mismatch will result in full-scale error.

Calibration is performed by loading the DAC register with 1000 0000 0000 and adjusting R_1 until $V_{OUT} = 0V$. R_1 and R_2 may be omitted, adjusting the ratio of R_3 to R_4 to yield $V_{OUT} = 0V$. Full scale can be adjusted by loading the DAC register with 1111 1111 1111 and either adjusting the amplitude of V_{REF} or the value of R_5 until the desired V_{OUT} is achieved.

TABLE 3: Bipolar (Offset Binary) Code Table

DIGITAL INPUT MSB LSB	NOMINAL ANALOG OUTPUT (V_{OUT} as shown in Figure 10)
1 1 1 1 1 1 1 1 1 1 1 1	$+V_{REF}\left(\frac{2047}{2048}\right)$
1 0 0 0 0 0 0 0 0 0 0 1	$+V_{REF}\left(\frac{1}{2048}\right)$
1 0 0 0 0 0 0 0 0 0 0 0	0
0 1 1 1 1 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{1}{2048}\right)$
0 0 0 0 0 0 0 0 0 0 0 1	$-V_{REF}\left(\frac{2047}{2048}\right)$
0 0 0 0 0 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{2048}{2048}\right)$

NOTES:
1. Nominal full scale for the circuit of Figure 10 is given by $FS = V_{REF}\left(\frac{2047}{2048}\right)$.
2. Nominal LSB magnitude for the circuit of Figure 10 is given by $LSB = V_{REF}\left(\frac{1}{2048}\right)$.

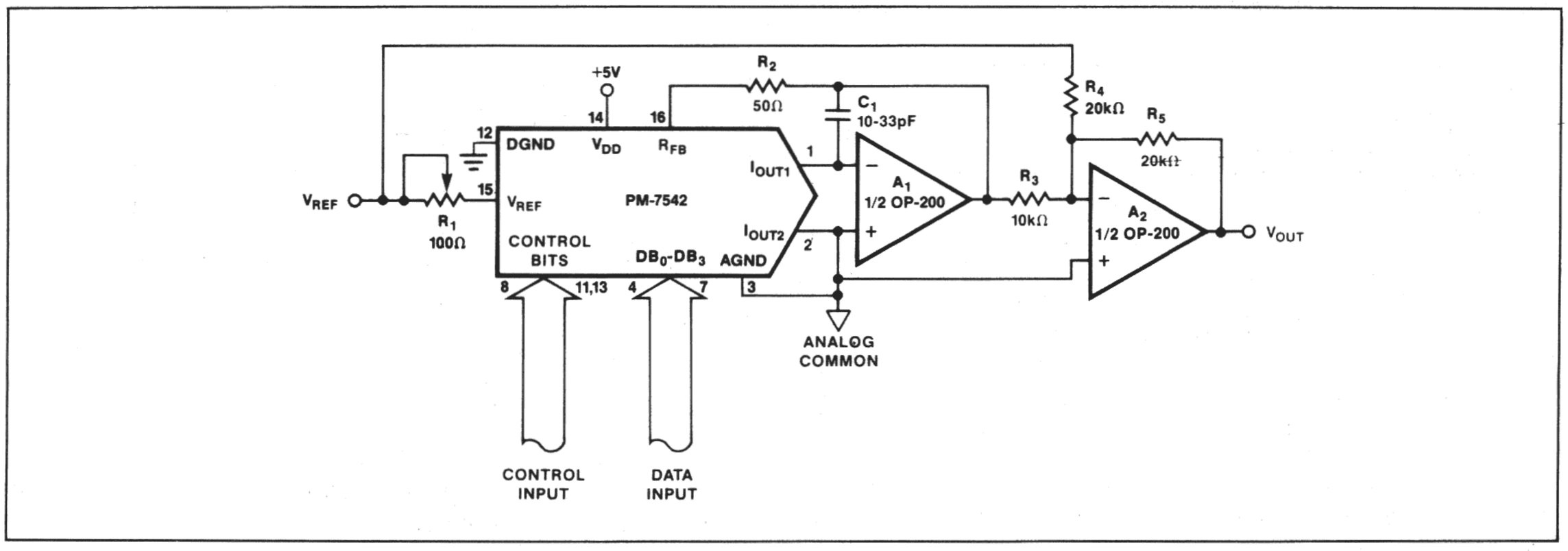


FIGURE 10: *Bipolar Operation (4-Quadrant, Offset Binary)*

ANALOG/DIGITAL DIVISION

The transfer function for the PM-7542 connected in the multiplying mode as shown in Figures 8 and 9 is:

$$V_O = -V_{IN}\left(\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \ldots \frac{A_{12}}{2^{12}}\right)$$

where A_X assumes a value of 1 for an "ON" bit and 0 for an "OFF" bit.

The transfer function is modified when the DAC is connected in the feedback of an operational amplifier as shown in Figure 11. It is now:

$$V_O = \frac{-V_{IN}}{\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \ldots \frac{A_{12}}{2^{12}}}$$

The above transfer function is the division of an analog voltage (V_{REF}) by a digital word. The amplifier goes to the rails with all bits "OFF" since division by zero is infinity. With all bits "ON", the gain is 1 (±1 LSB). The gain becomes 4096 with the LSB, bit 12, "ON".

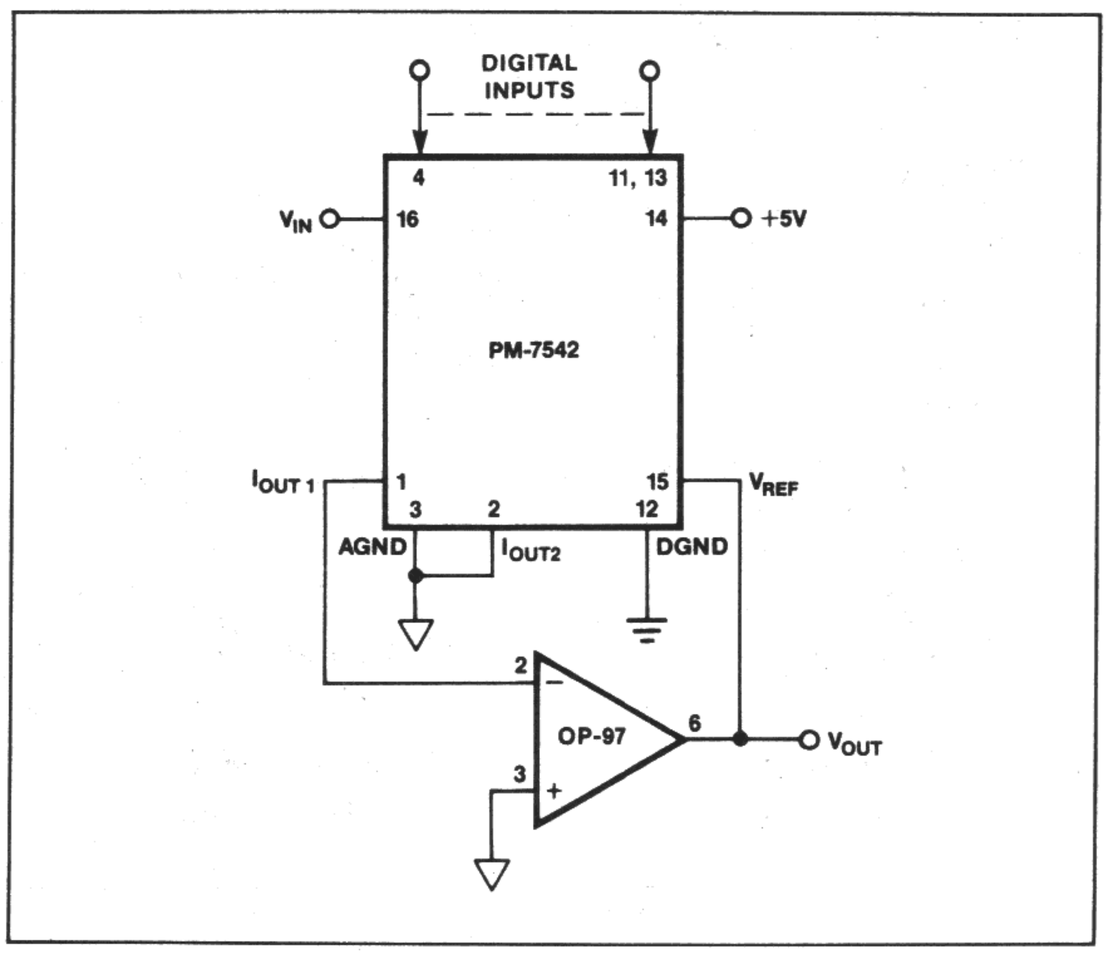


FIGURE 11: *Analog/Digital Divider*

INTERFACING TO THE MC6800

A typical interface configuration is shown in Figure 12. Data loading and transfer is performed by executing memory WRITE operations to the four operational addresses specified by A_1 and A_0.

Addresses AABB, AABB+1, and AABB+2 are assigned to load data into the low, middle, and high byte registers, respectively. Data transfer from input to DAC registers is assigned to address AABB+3. Eight bits of the full 12-bit data word are stored in memory location XXYY. The most significant data bits occupy the lower four bits of memory location XXYY+1.

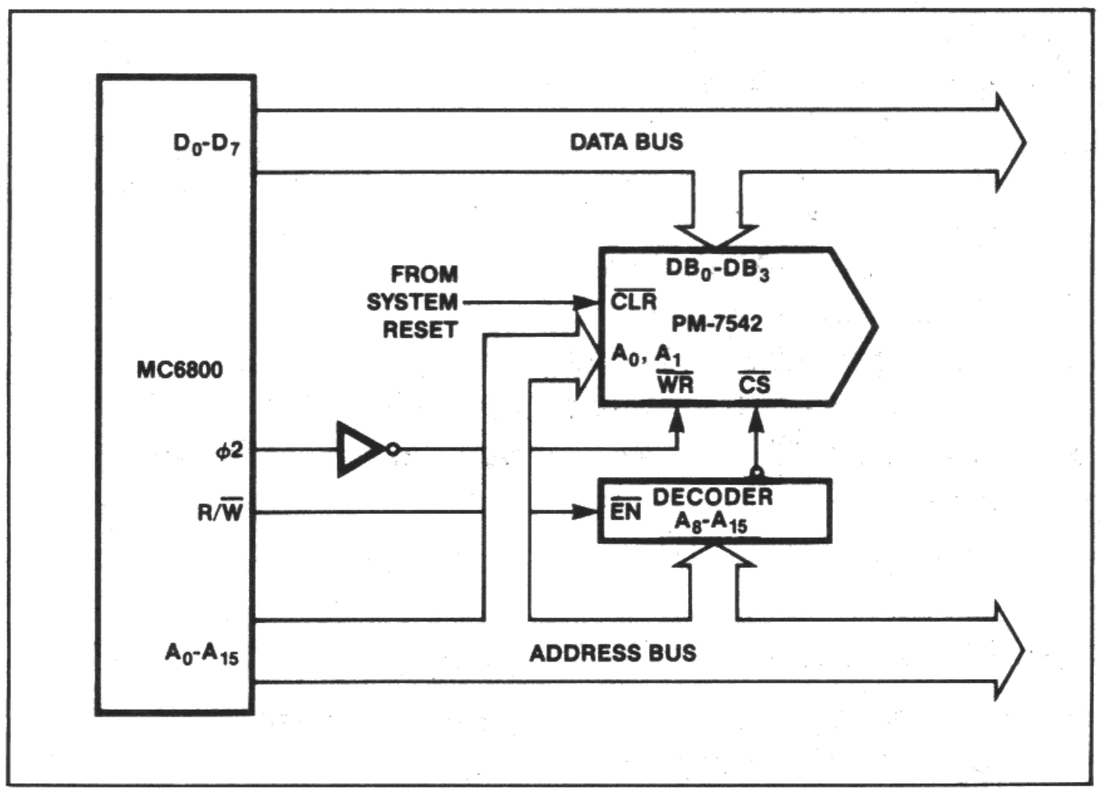


FIGURE 12: *Interfacing the PM-7542 to the MC6800*

DATA OPERATIONS SUBROUTINE

	JSR	WWZZ	Jump to Data Op Routine at WWZZ
WWZZ	PSH A		Push Acc. A Onto Stack
	TPA		
	PSH A		Push CCR Onto Stack
	LDA A	XXYY	Load Data to Acc.
	STA A	AABB	Load Low Byte
	ROR A		Rotate Right
	ROR A		
	ROR A		
	ROR A		
	STA A	AABB+1	Load Middle Byte
	LDA A	XXYY+1	Load Most Significant Byte to Acc.
	STA A	AABB+2	Load High Byte
	STA A	AABB+3	Transfer Data Word to DAC Register
	PUL A		
	TAP		Pop CCR From Stack
	PUL A		Pop Acc. A From Stack
	RTS		Return to Main Program

INTRODUCTION

A D/A converter accepts a digital input and produces an analog output. The basic DAC consists of a voltage or current reference, binary-weighted precision resistors, a set of electronic switches, and a means of summing the weighted currents.

Three important criteria for selecting a good DAC are resolution, accuracy, and speed. Other essential requirements to be considered are temperature stability, input coding, output format, reference requirements, and power consumption.

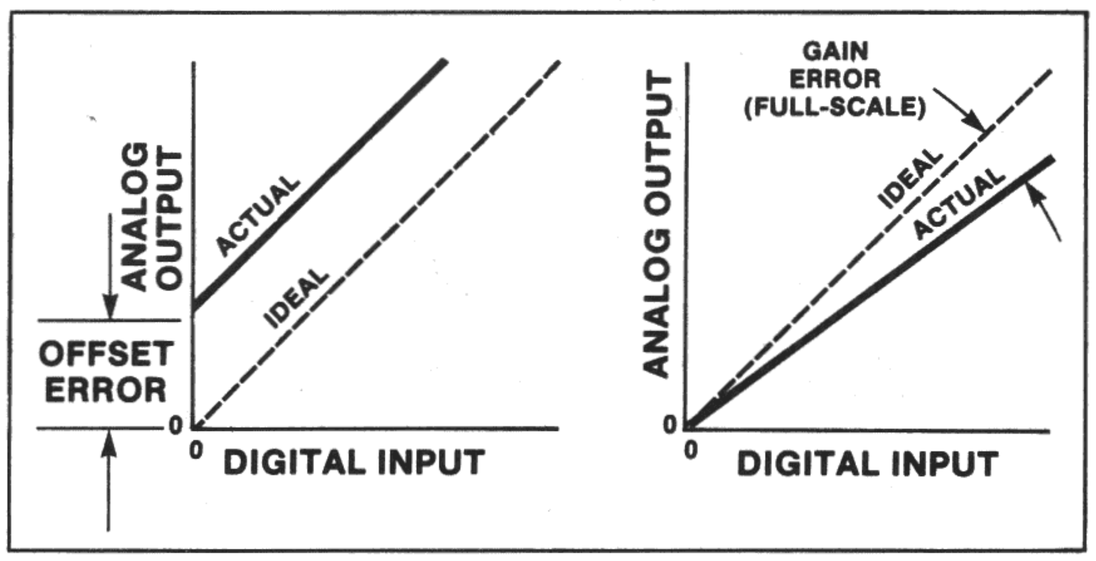
Since introducing the first monolithic D/A converter in 1970, PMI has continually improved and updated its DAC product line. Using bipolar GaAs and CMOS technologies, PMI offers complete selections of parametric trade-offs available from these technologies. Very high speed, internal references and amplifiers are key features of the bipolar technology DACs. The CMOS technology DACs offer a much higher degree of logic interface function, while maintaining absolute minimums in power dissipation. A wide offering of microprocessor-interfaceable DACs simplify connection to 4, 8, and 16-bit microprocessor systems. The DAC with "memory" is another first offered by PMI to simplify system self-diagnosis of data path integrity.

The selection guides following the definitions will aid you in quickly locating the appropriate DAC for your application.

DEFINITIONS — LINEAR DIGITAL-TO-ANALOG CONVERTERS

Absolute Accuracy — The absolute accuracy of a DAC is the difference between the actual unadjusted analog output and the ideal output that is expected when a given digital code is applied. Sources of error include full-scale error (gain error), zero-scale error (offset error), nonlinearity errors, and the drift of all of these. Therefore, absolute accuracy includes all deviations from the ideal. (See Figure 11.1)

Figure 11.1 Gain and Offset Error Defined



A.C. Feedthrough — The ratio of the amplitude of signal at the DAC output to the reference input with all DAC switches off. This parameter is expressed in dBs.

BCD — The abbreviation BCD stands for binary-coded decimal. It is a binary code used to represent decimal numbers in which the digits 0 through 9 are coded, using the 4-bit binary 8-4-2-1 code.

Binary — A positive-weighted code in which a number is represented by:

$$N = a_0 2^0 + a_1 2^1 + a_2 2^2 + \cdots + a_n 2^n$$

where each coefficient "a_i" has a value of zero or one. Data converters use this code in its fractional form where:

$$N = a_1 2^{-1} + a_2 2^{-2} + a_3 2^{-3} + \cdots + a_n 2^{-n}$$

and N has a fractional value between zero and one.

Bit — The unit of binary information. It can have the value of zero or one.

Bipolar Output — When the analog signal range includes both positive and negative values, the output is said to be bipolar. The transfer characteristic of an ideal 2-quadrant bipolar-output DAC is shown in Figure 11.2.

Differential Nonlinearity (DNL) — Differential nonlinearity is the worst case deviation of any adjacent analog outputs from the ideal 1 LSB step size. The deviation of the actual "step size" from the ideal step size of 1 LSB is called differential nonlinearity error or DNL. DACs with DNL greater than ±1 LSB may be nonmonotonic. Maximum DNL error is less than or equal to twice the maximum INL. (See Figure 11.3)

Figure 11.2 Bipolar Output Converter

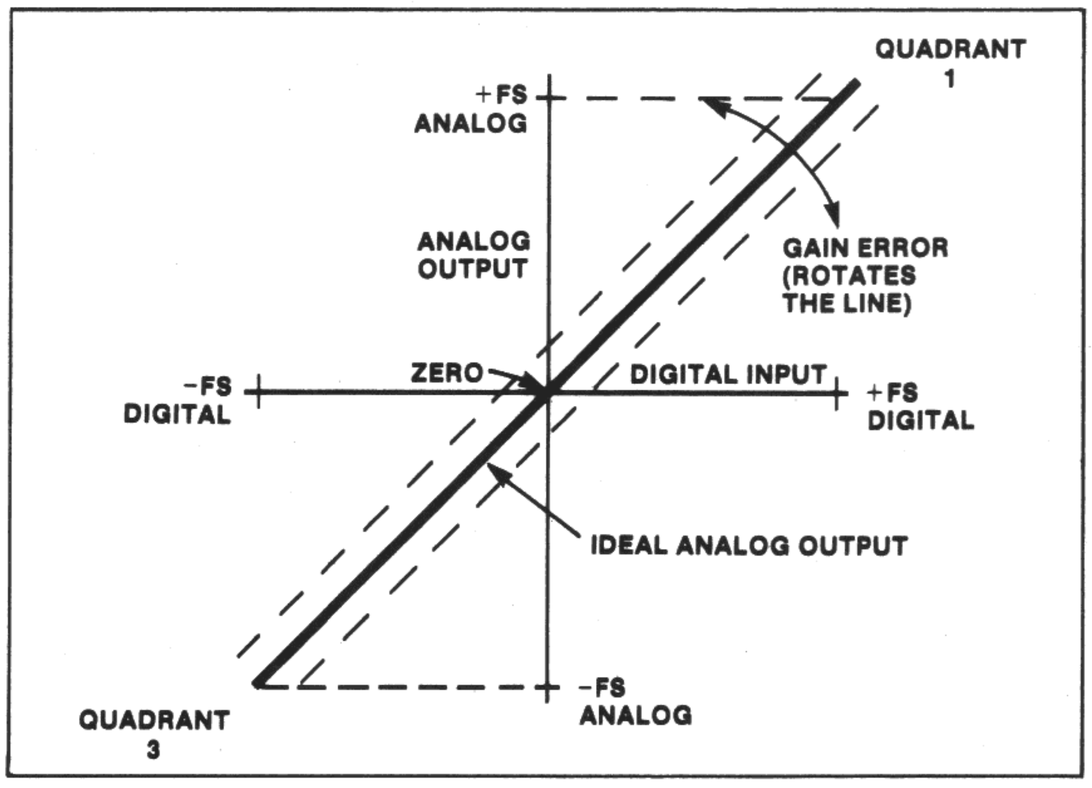
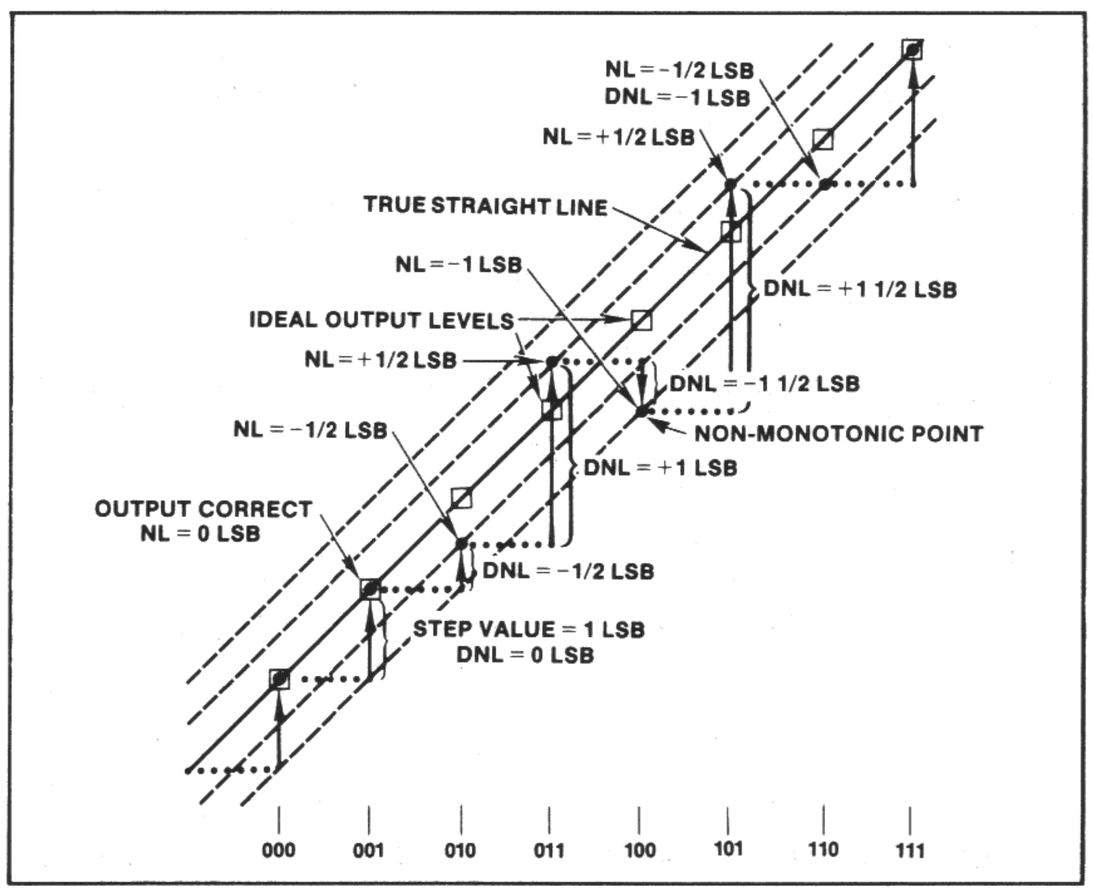


Figure 11.3 Nonlinearity (NL) and Differential Nonlinearity (DNL)



Digital Crosstalk (Q) — Digital crosstalk is a parameter that is used with multiple converters in a single package. It is the glitch impulse that is transferred from one converter that is being addressed to another converter that is not being addressed. It is specified in nV-secs and is measured with V_{REF} = 0V.

Digital Feedthrough (FT) — Digital feedthrough is the glitch-energy impulse transferred from the DAC's digital input to the analog output. It is specified in nV-secs and is measured with V_{REF} = 0V.

Dynamic Range (DR) — The dynamic range of a DAC is the ratio of the largest output to the smallest output (excluding zero) expressed in decibels (dB). For linear DACs, this ratio is 2^n, where n = number of bits of resolution.

DR (in dB) = 20 $Log_{10}2^n \simeq 6n$ for linear DACs; (COMDACs® are 66 or 72dB.)

Endpoint Linearity — See Integral Nonlinearity.

Functional Compliance — The functional compliance of a DAC is the voltage range over which the current output can be driven and for which the DAC output current will maintain the same relative accuracy (the output can change absolutely).

Full Scale (FS) — The full-scale output of a DAC is its maximum voltage or current. For a binary DAC, the full-scale output occurs when the digital inputs are all ones. The full-scale value is one LSB less than the reference value.

Full-Scale Gain Error (G_{FSE}) — See Gain Error.

Full-Scale Range (FSR) — The difference between the maximum analog output and the minimum analog output of a DAC.

Gain Drift (TCG_{FS}) — The variation of the full-scale value (voltage or current) measured over the operating temperature range is called gain drift. This parameter has units of %FS, ppmFS, or LSB. It may also be expressed % of FS/°C, ppmFS/°C, etc.

Gain Error (G_{FSE}) — The difference between the actual and the ideal analog output range, expressed as a percent of full-scale or in terms of LSB value (see Figure 11.1). It is the deviation in slope of the DAC transfer characteristic from ideal.

Glitch — A glitch is a switching transient appearing in the output during a code transition. Its value is expressed as a product of voltage (V × ns) or current (mA × ns) and time duration or charge transferred (in Picocoulombs).

Integral Nonlinearity (INL) or Nonlinearity (NL) — This is the single most important DAC specification. PMI measures INL as the maximum deviation of the analog output (from the ideal) from a straight line drawn between the

end points, expressed as a percent of full-scale range or in terms of LSBs. (See Figure 11.5)

For DACs, a specification of ±1/2 LSB INL guarantees monotonicity and ±1 LSB maximum differential nonlinearity.

Least Significant Bit (LSB) — The analog value of the LSB is the smallest change that can occur in the output of a DAC. It corresponds to a one-bit change in the binary input. The analog value will be either a voltage or current.

$$\text{LSB (Analog Value)} = \frac{\text{FSR}}{2^n}$$

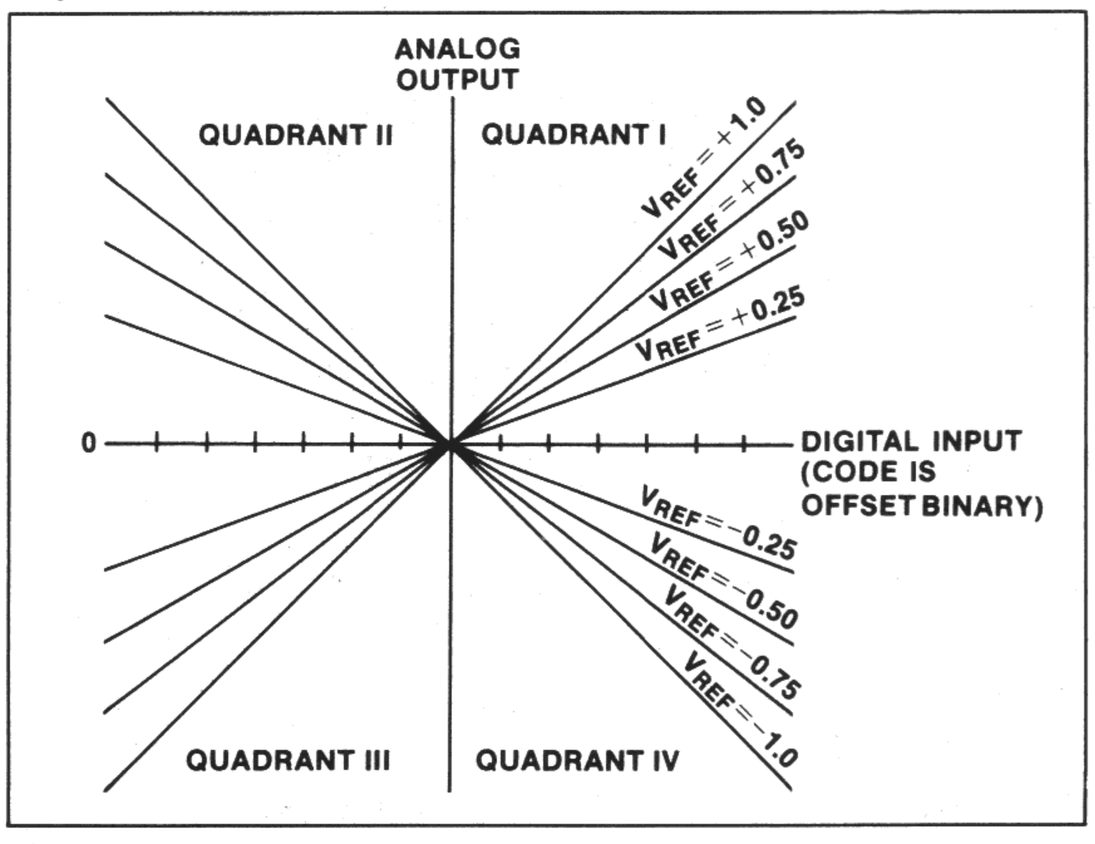
where FSR = Full-Scale Range
n = number of bits

Most Significant Bit (MSB) — The analog value of the MSB is the largest incremental output change obtainable by switching a single input bit. The analog value will be either a voltage or current.

$$\text{MSB (Analog Value)} = \frac{\text{FSR}}{2}$$

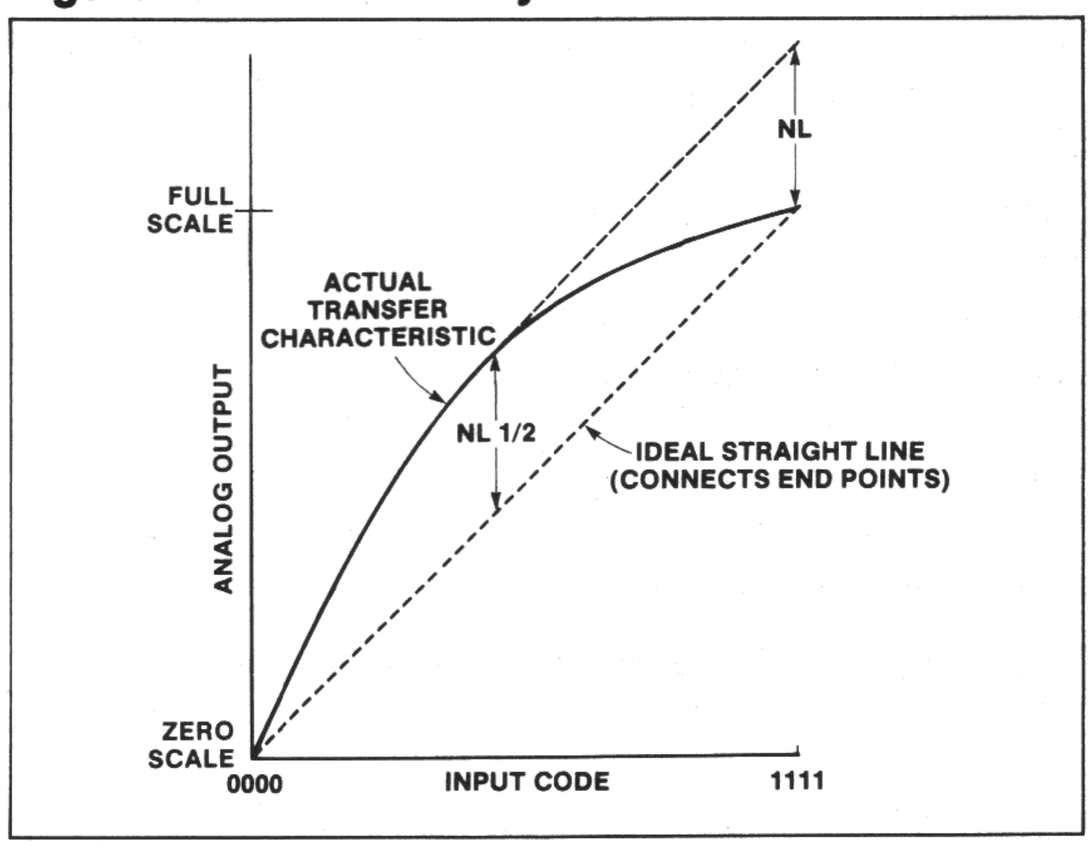
Monotonicity — A DAC is monotonic if the analog output either increases or remains the same for an increasing digital input code. If the DNL is less than ±1 LSB, monotonicity is guaranteed. (See Figure 11.3)

Figure 11.4 DAC Transfer Curves



Multiplying DACs — The DAC multiplies an analog reference by a digital word. Some DACs can multiply only positive digital words by a positive reference. This is known as single quadrant operation (Quadrant I, see Figure 11.4). Two quadrant operation (Quadrants I and III) can be performed by a DAC that usually operates in Quadrant I by configuring the output for bipolar output operation. This is accomplished by offsetting the output by a negative MSB (1/2 of FSR), so that the MSB becomes the sign bit. CMOS DACs provide four quadrant operation by allowing the use of both positive and negative references. (Quadrants I, II, III, IV).

Figure 11.5 Nonlinearity



Nonlinearity (NL) — See Integral Nonlinearity.

Offset Drift (TCV_{OS}, TCI_{OS}) — The variation of the offset (voltage or current) measured over the operating temperature range. The offset drift is divided by the temperature range over which it is measured, and expressed in ppm per degree centigrade or percent of full-scale range. This parameter applies to DACs operating in the bipolar output mode. See zero-scale drift for DACs operating in the unipolar output mode.

Offset Error (V_{OSE}, I_{OSE}) — The offset error is the error at analog zero for a data converter operating in the bipolar mode.

Output Resistance (R_O) — Output resistance is the equivalent internal resistance for a current output D/A converter as seen at its output. It is measured as the change in output current ΔI with the change in output voltage ΔV. It is a direct measure of the true compliance.

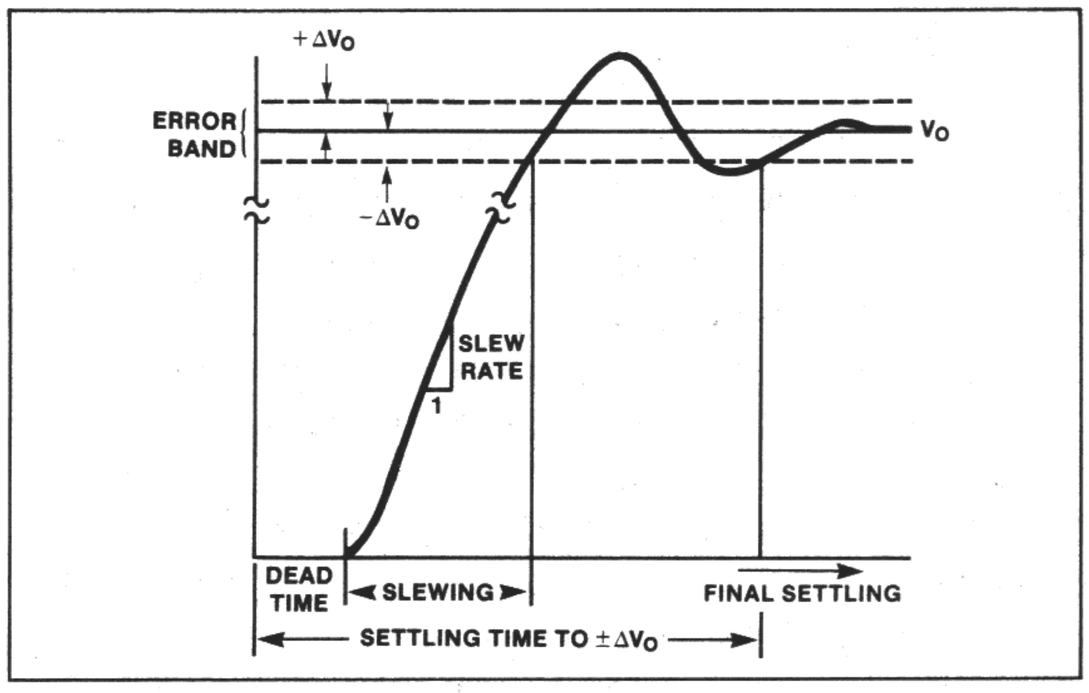
Power Supply Sensitivity (P_{SS}) — The change in the output of the converter due to a change in the power supply value. This may be expressed as a percent of full-scale range per one percent change in the power supply, or as a percent of full scale per volt of power supply change. Normally P_{SS} is specified at DC; it is sometimes specified over a given frequency range.

Relative Accuracy — See Integral Nonlinearity.

Resolution (n) — The resolution of a DAC is the number of states (2^n) that the FSR is divided (or resolved) into, where n is equal to the number of bits.

Settling Time — Settling time is the elapsed time for the analog output to reach its final value within a specified error band after a digital input code change. It is usually specified for a full-scale change and measured from the 50% point of the logic input change to the time the output reaches its final value within the specified error band. (See Figure 11.6)

Figure 11.6 Settling Time Measurement



Three-State Outputs — A digital output circuit that can be programmed to output a logic low, logic high, or a high output impedance state. These devices are generally connected to digital buses.

Total Unadjusted Error (TUE) — The total unadjusted error is a comprehensive specification which includes full scale error, relative accuracy, and zero code error. It is noted that the maximum ideal output voltage is V_{REF} – 1LSB, where 1LSB = $V_{REF}/2^n$, and n is the DAC resolution. This clearly indicates that the LSB voltage size is dependent on V_{REF}, and the zero code error will increase as V_{REF} decreases (in terms of LSB). The total unadjusted error then, will vary over the V_{REF} voltage range.

True Compliance — The true compliance of a DAC is the voltage range over which the current output can vary while the DAC maintains an absolute accuracy of ±1/2 LSB. The higher the DAC output impedance, the better the voltage compliance will be.

Unipolar Output — A DAC operates in the unipolar output mode when the analog output starts at zero, stopping at a full-scale positive or negative value, while the digital inputs are changed from zero to all-ones code. The analog output occurs in one quadrant.

Zero-Scale Error (V_{ZSE}, I_{ZSE}) — The zero-scale error is the error at analog zero for a data converter operating in the unipolar mode.

Zero-Scale Drift (TCV_{ZS}, TCI_{ZS}) — The variation of zero scale measured over the operating temperature. It is expressed in ppmFS/°C, or %FS/°C, etc.

Zero-Scale Symmetry Error (V_{ZSS}) — This definition applies only to sign-magnitude DACs. It is the change in the analog output produced by switching the sign bit with a zero-code input to the magnitude bits. It is expressed in units of voltage, current, or in fractions of an LSB.

DEFINITIONS — COMPANDING DACs

The companding (COMDAC®) DACs that PMI manufactures are the DAC-86, DAC-88, and the DAC-89. They are constructed such that the more significant bits of the digital input have a larger than binary relationship to the less significant bits. This decreases the resolution of the more significant bits, which increases the analog signal range. The effect of this is to compress more data into the more significant bits.

Chord — The mathematical formula, describing the DAC transfer function, is implemented by performing a piecewise linear approximation of the function. The straight line segments used in the approximation are called chords.

Chord Endpoints — The digital code corresponding to the maximum analog output for a given chord is called the chord endpoint.

Dynamic Range (DR) — The dynamic range of a DAC is the ratio of the largest output to the smallest output (excluding zero) expressed in decibels (dB). For the COMDACs® this would be output ($11_{7,15}$) divided by output ($I_{0,1}$). This is then converted to dB using the formula:

$$DR = 20\ Log_{10}\left(\frac{I_{7,15}}{I_{0,1}}\right)\ (dB)$$

Encode Current — The encode current is the difference between $I_{OE(+)}$ and $I_{OD\ (+)}$ or the difference between $I_{OE\ (-)}$ and $I_{OD\ (-)}$ at any code.

Full-Scale Symmetry Error — The full-scale symmetry error of a DAC is the difference between the maximum and the minimum analog output values. For the COMDACs® this is the difference between $I_{OD\ (-)}$ and $I_{OD\ (+)}$ or $I_{OE\ (+)}$ and $I_{OE\ (-)}$.

Output-Level Notation — Each output current level may be designated by the digital input code as $I_{c,s}$; where c = chord number and s = step number. For example, $I_{0,0}$ = zero scale current; $I_{0,1}$ = first step from zero; $I_{0,15}$ = endpoint of the first chord (C_0); and $I_{7,15}$ = full-scale current.

Steps — Each chord is divided into equal increments called steps.

Step Nonlinearity — This is the deviation of the actual step size from the ideal step size within a chord. In a linear DAC, it corresponds to differential nonlinearity.