

DRAM

64K x 1 DRAM

PAGE MODE

DRAM

FEATURES

- Industry standard pinout, functions and timing
- Single +5V ±10% power supply
- Low power, 15mW standby; 75mW active, typical
- Common I/O using EARLY-WRITE
- Q held indefinitely by $\overline{\text{CAS}}$
- 256-cycle refresh in 4ms
- Fully compatible with MT1259 (256K)
- Optional PAGE MODE access cycle

OPTIONS

- Timing
 - 100ns access
 - 120ns access
 - 150ns access
 - 200ns access
- Packages
 - Plastic DIP
 - Ceramic DIP

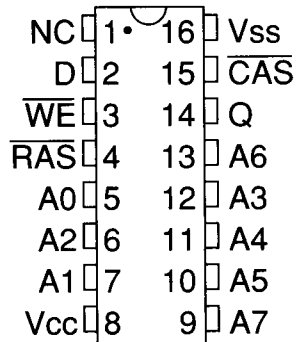
MARKING

-10
-12
-15
-20

None
C

PIN ASSIGNMENT (Top View)

16-Pin DIP
(A-1, B-1)



GENERAL DESCRIPTION

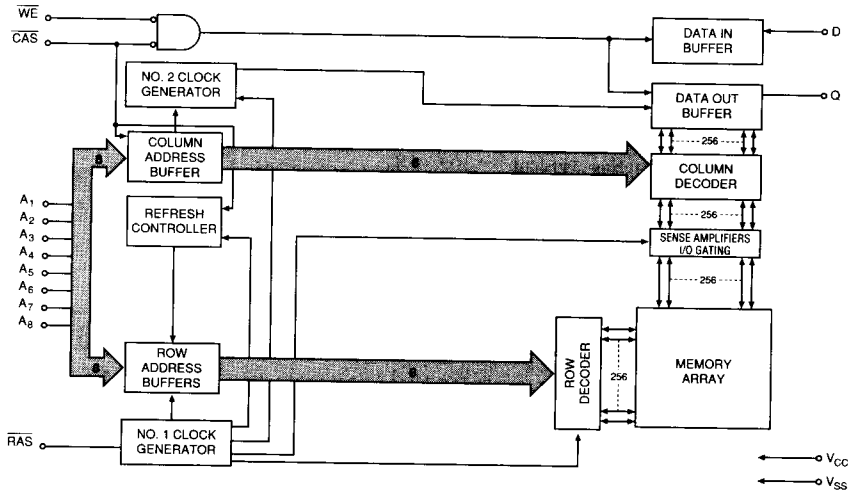
The MT4264 is a randomly accessed solid-state memory containing 65,536 bits organized in a x1 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 16 address bits, which are entered 8 bits (A0-A7) at a time. $\overline{\text{RAS}}$ is used to latch the first 8 bits and $\overline{\text{CAS}}$ the latter 8 bits. A READ or WRITE cycle is selected with the $\overline{\text{WE}}$ input. A logic HIGH on $\overline{\text{WE}}$ dictates READ mode while a logic LOW on $\overline{\text{WE}}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{\text{WE}}$ or $\overline{\text{CAS}}$, whichever occurs last. If $\overline{\text{WE}}$ goes LOW prior to $\overline{\text{CAS}}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{\text{CAS}}$ cycle. If $\overline{\text{WE}}$ goes LOW after data reaches the output pin(s), data out (Q) is activated and retains the selected cell data as long as $\overline{\text{CAS}}$ remains LOW (regardless of $\overline{\text{WE}}$ or $\overline{\text{RAS}}$). This late $\overline{\text{WE}}$ pulse results in a READ-WRITE cycle.

PAGE MODE operations allow faster data operations

(READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A7) defined page boundary. The PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{\text{RAS}}$ followed by a column address strobed-in by $\overline{\text{CAS}}$. $\overline{\text{CAS}}$ may be toggled-in by holding $\overline{\text{RAS}}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{\text{RAS}}$ HIGH terminates the PAGE MODE operation.

Returning $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{\text{RAS}}$ HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{\text{RAS}}$ cycle (READ, WRITE, $\overline{\text{RAS}}$ -ONLY or HIDDEN REFRESH) so that all 256 combinations of $\overline{\text{RAS}}$ addresses (A0-A7) are executed at least every 4ms, regardless of sequence.

**FUNCTIONAL BLOCK DIAGRAM
PAGE MODE**



TRUTH TABLE

Function	RAS	CAS	WE	Addresses		
				t _R	t _C	
Standby	H	X	X	X	X	High Impedance
READ	L	L	H	ROW	COL	Data Out
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In
READ-WRITE	L	L	H→L→H	ROW	COL	Valid Data Out, Valid Data In
PAGE-MODE READ	L	H→L→H	H	ROW	COL	Valid Data Out, Valid Data Out
PAGE-MODE WRITE	L	H→L→H	L	ROW	COL	Valid Data In, Valid Data In
PAGE-MODE READ-WRITE	L	H→L→H	H→L→H	ROW	COL	Valid Data Out, Valid Data In
RAS-ONLY REFRESH	L	H	X	ROW	n/a	High Impedance
HIDDEN REFRESH	L→H→L	L	H	ROW	COL	Valid Data Out
CAS-BEFORE-RAS REFRESH	H→L	L	X	X	X	High Impedance

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc supply relative to Vss	-1.0V to +7.0V
Operating Temperature, TA(Ambient)	0°C to +70°C
Storage Temperature (Ceramic)	-65°C to +150°C
Storage Temperature (Plastic)	-55°C to +150°C
Power Dissipation	1W
Short Circuit Output Current	50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 2, 3, 4, 6) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V _{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V _{IH}	2.4	V _{CC} +1	V	1
Input Low (Logic 0) Voltage, All Inputs	V _{IL}	-1.0	0.8	V	1
INPUT LEAKAGE Input leakage current, any input (0V ≤ V _{IN} ≤ V _{CC}); I all other pins not under test = 0V	I _I	-10	10	μA	
OUTPUT LEAKAGE Output leakage current (Q is disabled; 0V ≤ V _{OUT} ≤ V _{CC})	I _{OZ}	-10	10	μA	
OUTPUT LEVELS Output High (Logic 1) Voltage (I _{OUT} = -5mA)	V _{OH}	2.4		V	1
Output Low (Logic 0) Voltage (I _{OUT} = 5mA)	V _{OL}		0.4	V	

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
STANDBY CURRENT ($\overline{RAS} = \overline{CAS} = V_{IH}$ after 8 \overline{RAS} cycles)	I _{CC1}		4	mA	
OPERATING CURRENT (\overline{RAS} and \overline{CAS} Cycling)	I _{CC2}		30	mA	2
\overline{RAS}-ONLY REFRESH CURRENT ($\overline{CAS} = V_{IH}$)	I _{CC3}		20	mA	2
PAGE MODE CURRENT ($\overline{RAS} = V_{IL}$; $\overline{CAS} = \text{Cycling}$)	I _{CC4}		30	mA	2

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A7, D	C _{I1}		5	pF	18
Input Capacitance: RAS, CAS, WE	C _{I2}		8	pF	18
Output Capacitance: Q	C _O		8	pF	18

DRAM

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

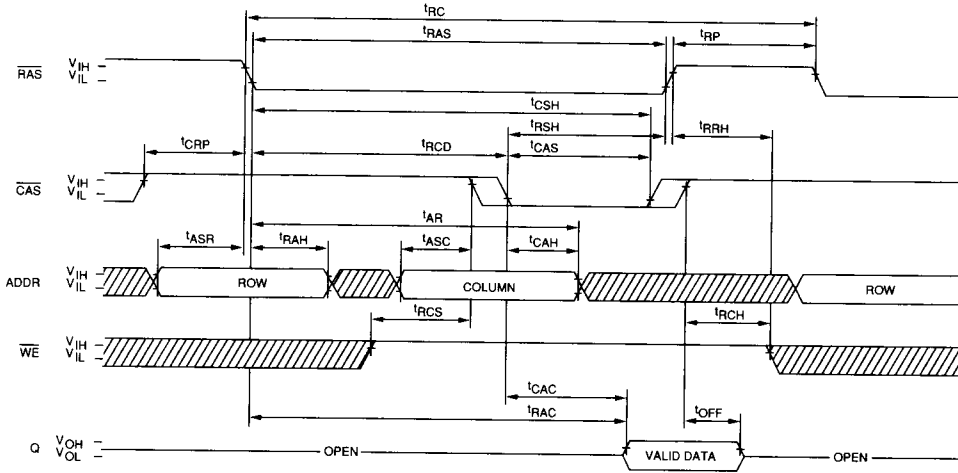
(Notes: 3, 4, 5, 10, 11, 17, 18) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5.0V ±10%)

A.C. CHARACTERISTICS		-10		-12		-15		-20		UNITS	NOTES
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Random READ or WRITE cycle time	¹ RC	195		230		260		330		ns	6, 7
READ-MODIFY-WRITE cycle time	¹ RWC	220		255		295		370		ns	
PAGE-MODE cycle time	¹ PC	90		100		120		170		ns	6, 7
Access time from $\overline{\text{RAS}}$	¹ RAC		100		120		150		200	ns	7, 8
Access time from $\overline{\text{CAS}}$	¹ CAC		50		60		75		120	ns	7, 9
RAS pulse width	¹ RAS	100	10,000	120	10,000	150	10,000	200	10,000	ns	
RAS hold time	¹ RSH	50		60		75		100		ns	
RAS precharge time	¹ RP	80	20,000	90	20,000	100	20,000	120	20,000	ns	
CAS pulse width	¹ CAS	50	10,000	60	10,000	75	10,000	120	10,000	ns	
CAS hold time	¹ CSH	100		120		150		200		ns	
CAS precharge time	¹ CPN	25		25		30		35		ns	19
CAS precharge time (PAGE MODE)	¹ CP	30		30		35		40		ns	
RAS to $\overline{\text{CAS}}$ delay time	¹ RCD	25	50	25	60	25	75	30	80	ns	13
Row address setup time	¹ ASR	0		0		0		0		ns	
Row address hold time	¹ RAH	15		15		20		25		ns	
Column address setup time	¹ ASC	0		0		0		0		ns	
Column address hold time	¹ CAH	20		20		25		50		ns	
Column address hold time referenced to $\overline{\text{RAS}}$	¹ AR	70		80		100		130		ns	
READ command setup time	¹ RCS	0		0		0		0		ns	
READ command hold time referenced to $\overline{\text{CAS}}$	¹ RCH	0		0		0		0		ns	14
READ command hold time referenced to $\overline{\text{RAS}}$	¹ RRH	0		0		0		0		ns	
Output buffer turn-off delay	¹ OFF	0	30	0	30	0	35	0	40	ns	12
$\overline{\text{WE}}$ command setup time	¹ WCS	0		0		0		0		ns	16
WRITE command hold time	¹ WCH	35		40		45		60		ns	
WRITE command hold time referenced to $\overline{\text{RAS}}$	¹ WCR	85		100		120		140		ns	
WRITE command pulse width	¹ WP	35		40		45		50		ns	
WRITE command to $\overline{\text{RAS}}$ lead time	¹ RWL	35		40		45		55		ns	
WRITE command to $\overline{\text{CAS}}$ lead time	¹ CWL	35		40		45		55		ns	
Data-in setup time	¹ DS	0		0		0		0		ns	15
Data-in hold time	¹ DH	35		40		45		55		ns	15
Data-in hold time referenced to $\overline{\text{RAS}}$	¹ DHR	85		100		120		135		ns	
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ delay	¹ CWD	40		50		60		100		ns	16
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ delay	¹ RWD	90		110		135		180		ns	16
Transition time (rise or fall)	¹ T	3	100	3	100	3	100	3	100	ns	5, 17
Refresh period (256 cycles)	¹ REF		4		4		4		4	ms	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ setup time	¹ CRP	10		15		20		20		ns	

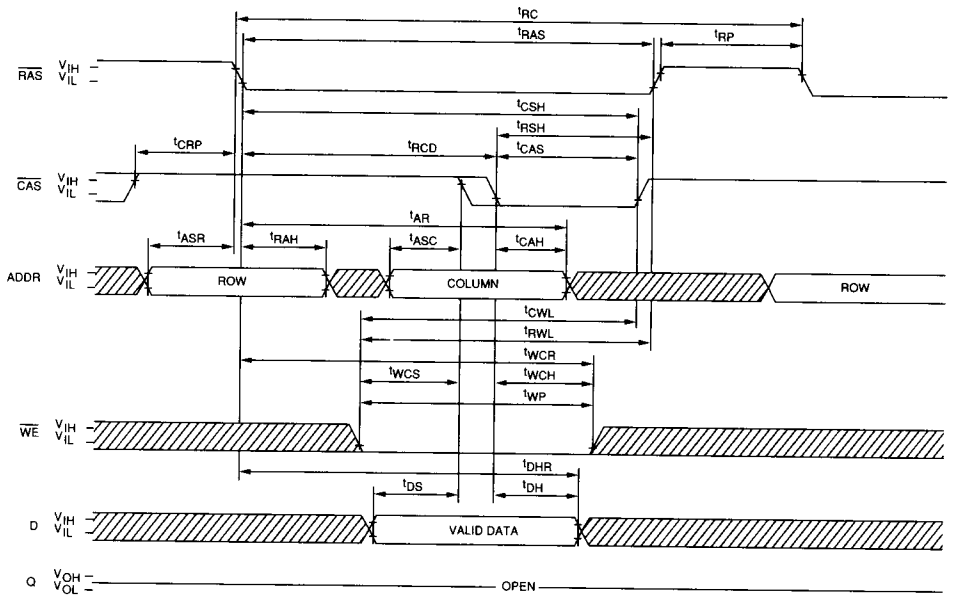
NOTES



1. All voltages referenced to Vss.
2. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any eight $\overline{\text{RAS}}$ cycles before proper device operation is assured. The eight $\overline{\text{RAS}}$ cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
4. AC characteristics assume $t_T = 5\text{ns}$.
5. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$) is assured.
7. Measured with a load equivalent to 2 TTL gates and 100pF.
8. Assumes that $t_{\text{RCD}} < t_{\text{RCD}}(\text{MAX})$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
9. Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{MAX})$.
10. If $\overline{\text{CAS}} = V_{IH}$, data output is high impedance.
11. If $\overline{\text{CAS}} = V_{IL}$, data output may contain data from the last valid READ cycle.
12. $t_{\text{OFF}}(\text{MAX})$ defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
13. Operation within the $t_{\text{RCD}}(\text{MAX})$ limit ensures that $t_{\text{RAC}}(\text{MAX})$ can be met. $t_{\text{RCD}}(\text{MAX})$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{\text{RCD}}(\text{MAX})$ limit, then access time is controlled exclusively by t_{CAC} .
14. t_{RCH} is referenced to the first rising edge of $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$.
15. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early WRITE cycles and $\overline{\text{WE}}$ leading edge in late WRITE or READ-WRITE cycles.
16. t_{WCS} , t_{RWD} and t_{CWD} are restrictive operating parameters in late READ-WRITE and READ-MODIFY-WRITE cycles only. If $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{MIN})$, the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{MIN})$ and $t_{\text{RWD}} \geq t_{\text{RWD}}(\text{MIN})$, the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of Q (at access time and until $\overline{\text{CAS}}$ goes back to V_{IH}) is indeterminate.
17. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
18. This parameter is sampled. Capacitance is calculated from the equation $C = I^{di}/dv$ with $dv = 3\text{V}$ and $V_{CC} = 5\text{V}$.
19. If $\overline{\text{CAS}}$ is LOW at the falling edge of $\overline{\text{RAS}}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{\text{CAS}}$ must be pulsed HIGH for t_{CPN} .

READ CYCLE

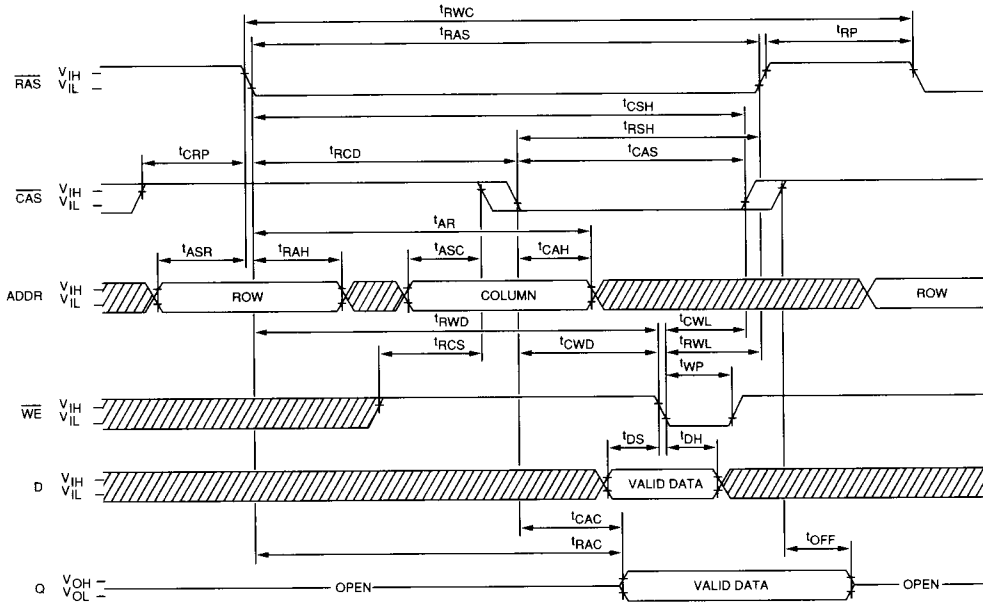


EARLY-WRITE CYCLE

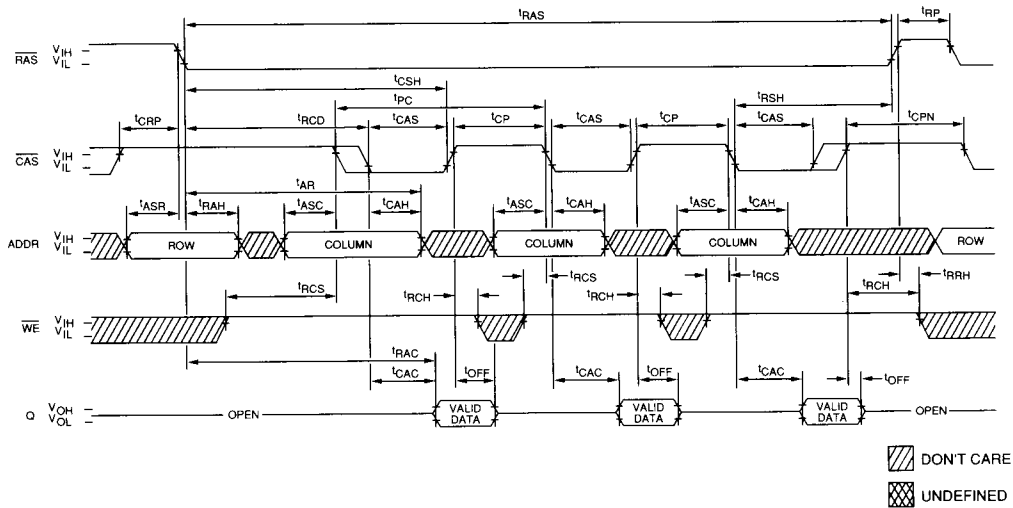


 DON'T CARE
 UNDEFINED

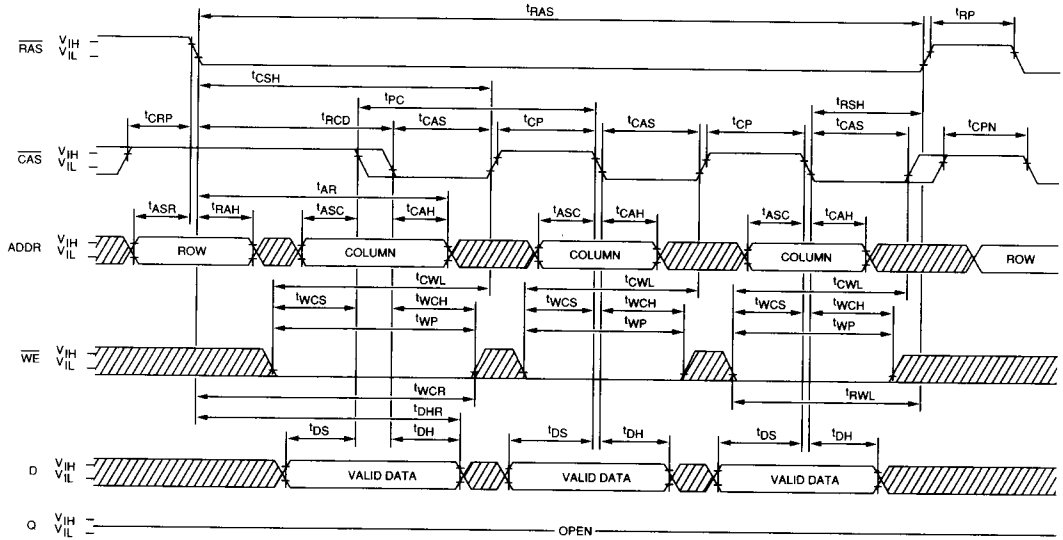
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



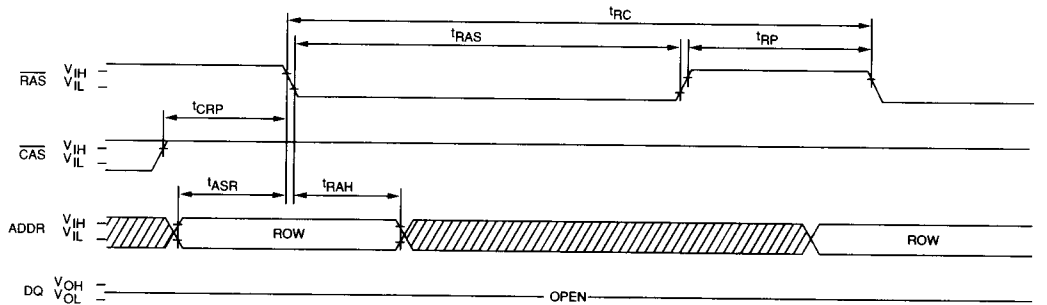
PAGE-MODE READ CYCLE



PAGE-MODE EARLY-WRITE CYCLE



RAS-ONLY REFRESH CYCLE
(ADDR = A₀ - A₇)



DON'T CARE
 UNDEFINED