**µPD23C8000**
**8,388,608-Bit**
**Mask-Programmable CMOS ROM**

## Description

The µPD23C8000 is a 8,388,608-bit ROM fabricated with CMOS silicon-gate technology. It is static in operation and has three-state outputs, fully TTL-compatible inputs and outputs, and an output enable pin which is mask-programmable and can be specified as active high, active low, or don't care.

The µPD23C8000 can be hardware-configured as either 512K x 16 bits or as 1M x 8 bits by tying the WORD/$\overline{BYTE}$ pin high or low, respectively. In the word configuration, pins $O_0$-$O_{15}$ are active. In the byte configuration, pins $O_0$-$O_7$ are active, pins $O_8$-$O_{14}$ are high impedance, and pin $O_{15}/A_{-1}$ becomes the additional bit required to address 1M bytes.

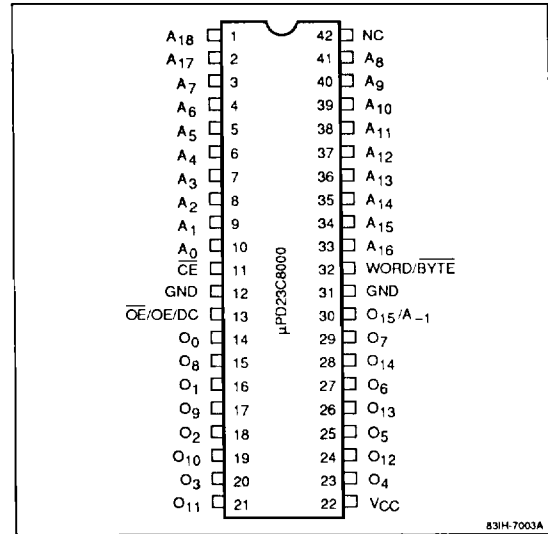The µPD23C8000 is available in a 42-pin plastic DIP.

## Features

□ Programmable organization
  — 524,288 words by 16 bits (word)
  — 1,048,576 words by 8 bits (byte)
□ Fast access time of 250 ns maximum
□ TTL-compatible inputs and outputs
□ Three-state outputs
□ Single + 5-volt power supply
□ CMOS technology
□ Fully static operation
□ Low power dissipation
□ 42-pin plastic DIP packaging

## Ordering Information

| Part Number | Access Time (max) | Package |
| --- | --- | --- |
| µPD23C8000CZ | 250 ns | 42-pin plastic DIP |

## Pin Configuration

### 42-Pin Plastic DIP



## Pin Identification

| Symbol | Function |
| --- | --- |
| $A_0$ - $A_{18}$ | Address inputs |
| $O_0$ - $O_{14}$ | Outputs |
| $O_{15}/A_{-1}$ | Output 15 (word)/LSB address (byte) |
| $\overline{CE}$ | Chip enable |
| $\overline{OE}$/OE/DC | Output enable/don't care (Note 1) |
| WORD/$\overline{BYTE}$ | Word/byte select |
| GND | Ground |
| $V_{CC}$ | + 5-volt power supply |
| NC | No connection |

**Notes:**

(1) This pin is user-definable as active low, active high, or "don't care."

## Absolute Maximum Ratings

| | |
|---|---|
| Supply voltage, $V_{CC}$ | $-0.3$ to $+7.0$ V |
| Input voltage, $V_I$ | $-0.3$ V to $V_{CC} + 0.3$ V |
| Output voltage, $V_O$ | $-0.3$ V to $V_{CC} + 0.3$ V |
| Operating temperature, $T_{OPR}$ | $-10$ to $+70°C$ |
| Storage temperature, $T_{STG}$ | $-65$ to $+150°C$ |

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.
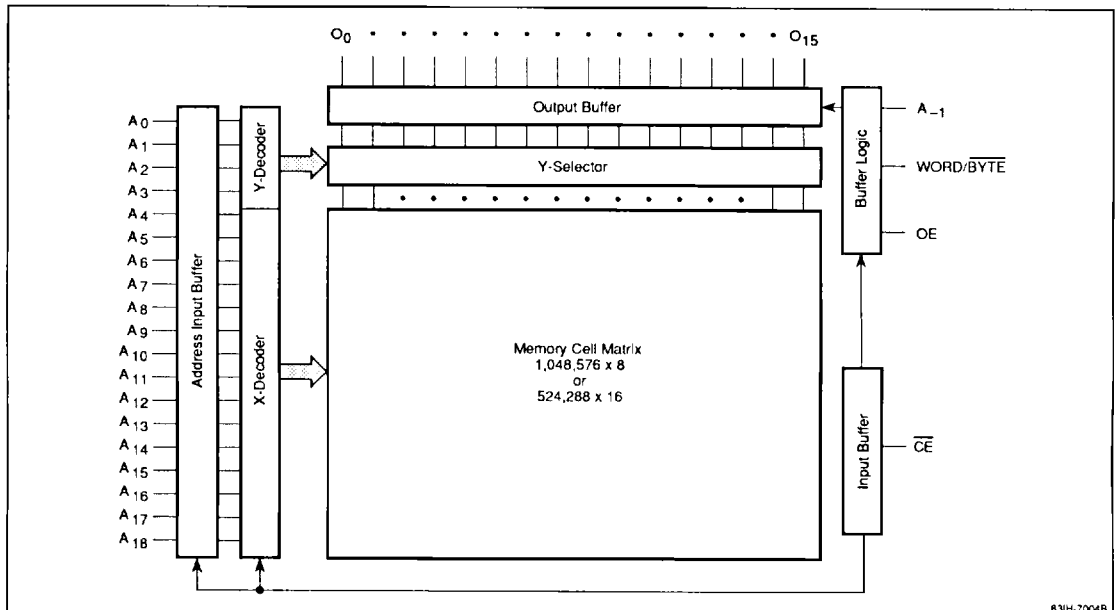
## Capacitance

$T_A = 25°C$; $f = 1$ MHz

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Input capacitance | $C_I$ | | | 15 | pF |
| Output capacitance | $C_O$ | | | 15 | pF |

## Recommended Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Input voltage, high | $V_{IH}$ | 2.2 | | $V_{CC} + 0.3$ | V |
| Input voltage, low | $V_{IL}$ | $-0.3$ | | 0.8 | V |
| Supply voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V |
| Ambient temperature | $T_A$ | $-10$ | | 70 | °C |

## Block Diagram



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## DC Characteristics

$T_A = -10$ to $+70°C$; $V_{CC} = +5.0$ V $\pm 10\%$

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Output voltage, high | $V_{OH}$ | 2.4 | | | V | $I_{OH} = -400\ \mu A$ |
| | $V_{OH2}$ | $V_{CC} - 0.5$ | | | V | $I_{OH} = -100\ \mu A$ |
| Output voltage, low | $V_{OL}$ | | | 0.4 | V | $I_{OL} = +2.1$ mA |
| Input leakage current | $I_{LI}$ | $-10$ | | 10 | $\mu A$ | $V_I = 0$ V to $V_{CC}$ |
| Output leakage current | $I_{LO}$ | $-10$ | | 10 | $\mu A$ | $V_O = 0$ V to $V_{CC}$; chip deselected |
| Power supply current | $I_{CC1}$ | | | 50 | mA | $\overline{CE} = V_{IL}$ |
| | $I_{CC2}$ | | | 1.5 | mA | $\overline{CE} = V_{IH}$; chip deselected |
| | $I_{CC3}$ | | | 100 | $\mu A$ | $\overline{CE} \geq V_{CC} - 0.2$ V; chip deselected |

## AC Characteristics

$T_A = -10$ to $+70°C$; $V_{CC} = +5.0$ V $\pm 10\%$

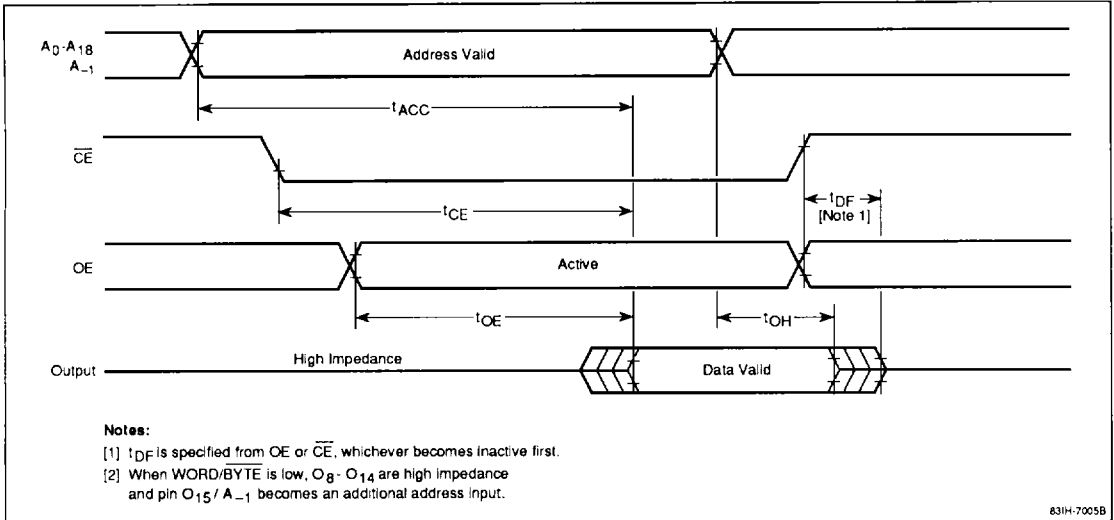| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Address access time | $t_{ACC}$ | | | 250 | ns | |
| Chip enable access time | $t_{CE}$ | | | 250 | ns | |
| Output enable access time | $t_{OE}$ | | | 100 | ns | |
| Output hold time | $t_{OH}$ | 0 | | | ns | |
| Output disable time | $t_{DF}$ | 0 | | 70 | ns | |
| Output enable access time referenced to WORD/$\overline{BYTE}$ | $t_{WB}$ | | | 250 | ns | |

**Notes:**

(1) Input voltage rise and fall times = 20 ns; input and output timing reference levels = 0.8 and 2.0 V; output load = 1 TTL + 100 pF.

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## Timing Waveforms

### Read Cycle

$A_0$-$A_{18}$
$A_{-1}$ — Address Valid

$t_{ACC}$

$\overline{CE}$

$t_{CE}$

$t_{DF}$
[Note 1]

OE — Active

$t_{OE}$

$t_{OH}$

Output — High Impedance — Data Valid

**Notes:**

[1] $t_{DF}$ is specified from OE or $\overline{CE}$, whichever becomes inactive first.

[2] When WORD/$\overline{BYTE}$ is low, $O_8$-$O_{14}$ are high impedance and pin $O_{15}$/$A_{-1}$ becomes an additional address input.

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### Word/Byte Selection Timing

$A_{-1}$ — High Impedance — Address Valid — High Impedance

WORD/$\overline{BYTE}$

$t_{ACC}$     $t_{OH}$

$C_0$-$O_7$ — Data Valid — Data Valid — Data Valid

$O_8$-$O_{15}$ — Data Valid — High Impedance — Data Valid

$t_{OH}$

$t_{DF}$

$t_{WB}$

**Notes:**

[1] $\overline{CE}$ = $V_{IL}$.

[2] OE is active.

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