Signetics

FAST 74F651, 74F652
Transceivers/Registers

'F651 Octal Transceiver/Register, Inverting (3-State)
'F652 Octal Transceiver/Register, Non-Inverting (3-State)
Product Specification

FAST Products

FEATURES

- **High-impedance NPN base inputs for reduced loading (70μA in High and Low states)**
- **Independent registers for A and B buses**
- **Multiplexed real-time and stored data**
- **Choice of non-inverting and inverting data paths**
- **3-State outputs**

DESCRIPTION

These devices consist of bus transceiver circuits with 3-State outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes High. Output Enable (OEAB, $\overline{OEBA}$) and Select (SAB, SBA) pins are provided for bus management.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F651	115MHz	140mA
74F652	115MHz	140mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
Cerdip (300mil)	N74F651F, N74F652F

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_0 - A_7$	A inputs	3.5/0.116	70μA/70μA
$B_0 - B_7$	B inputs	3.5/0.116	70μA/70μA
CPAB	A-to-B clock input	1.0/0.033	20μA/20μA
CPBA	B-to-A clock input	1.0/0.033	20μA/20μA
SAB	A-to-B select input	1.0/0.033	20μA/20μA
SBA	B-to-A select input	1.0/0.033	20μA/20μA
OEAB	Output Enable input	1.0/0.033	20μA/20μA
$\overline{OEBA}$	Output Enable input	1.0/0.033	20μA/20μA
$A_0 - A_7$	A outputs	750/106.7	15mA/64mA
$B_0 - B_7$	B outputs	750/106.7	15mA/64mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

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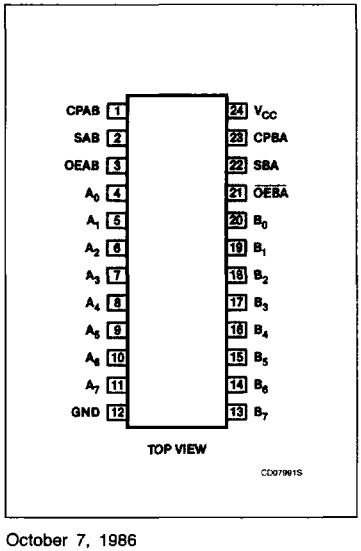
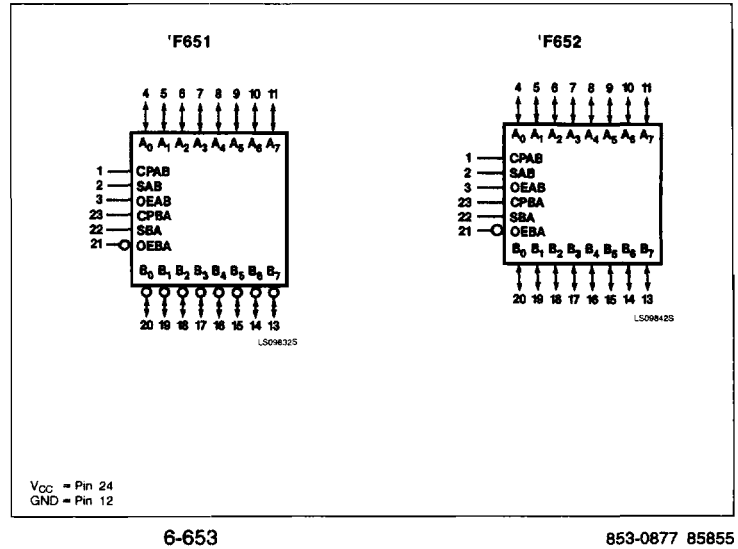
PIN CONFIGURATION



LOGIC SYMBOL

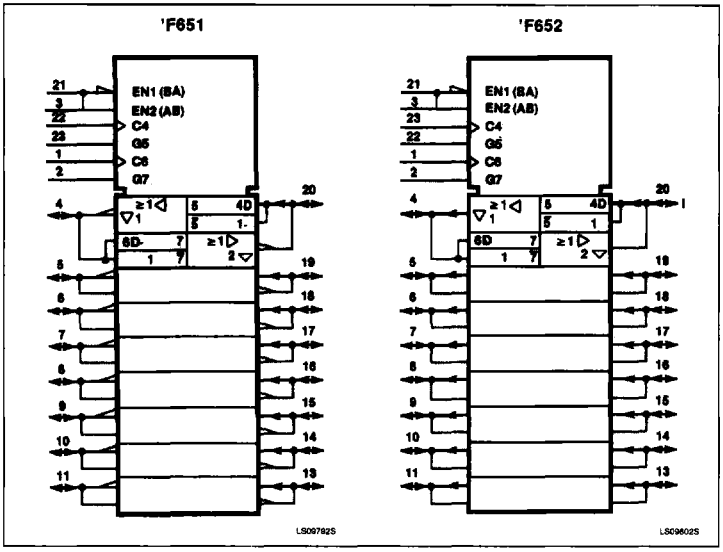


The following examples demonstrate the four fundamental bus-management functions that can be performed with the 'F651 and 'F652.

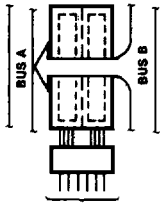
The select pins determine whether data is stored or transferred through the device in real-time.

The Output Enable pins determine the direction of the data flow.

SYMBOL (IEEE/IEC)

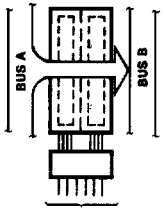


REAL-TIME TRANSFER BUS B TO BUS A



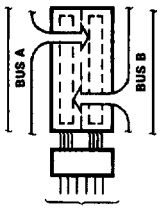
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER BUS A TO BUS B



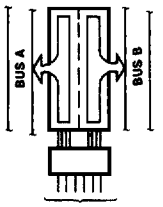
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
H	H	X	X	L	X

STORAGE FROM A, B, OR A AND B



OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

TRANSFER STORAGE DATA TO A OR B



OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
H	L	H or L	H or L	H	H

Figure 1

FUNCTION TABLE

OPERATING MODE		INPUTS						DATA I/O	
'F651	'F652	$\overline{OEBA}$	OEAB	CPAB	CPBA	SAB	SBA	A_n	B_n
Isolation Store A and B data	Isolation Store A and B data	L L	H H	H or L ↑	H or L ↑	X X	X X	Input	Input
Store A, Hold B Store A in both registers	Store A, Hold B Store A in both registers	X H	H H	↑ ↑	H or L ↑	X L	X X	Input Input	un* Output
Hold A, Store B Store B in both registers	Hold A, Store B Store B in both registers	L L	X L	H or L ↑	↑ ↑	X X	X L	un* Output	Input Input
Real time $\overline{B}$ data to A bus Stored $\overline{B}$ data to A bus	Real time B data to A bus Stored B data to A bus	L L	L L	X X	X H or L	X X	L H	Output	Input
Real time $\overline{A}$ data to B bus Stored $\overline{A}$ data to B bus	Real time A data to B bus Stored A data to B bus	H H	H H	X H or L	X X	L H	X X	Input	Output
Stored $\overline{A}$ data to B bus Stored $\overline{B}$ data to A bus	Stored A data to B bus Stored B data to A bus	H	L	H or L	H or L	H	H	Output	Output

NOTES:

* The data output function may be enabled or disabled by various signals at OEBA and OEAB inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.

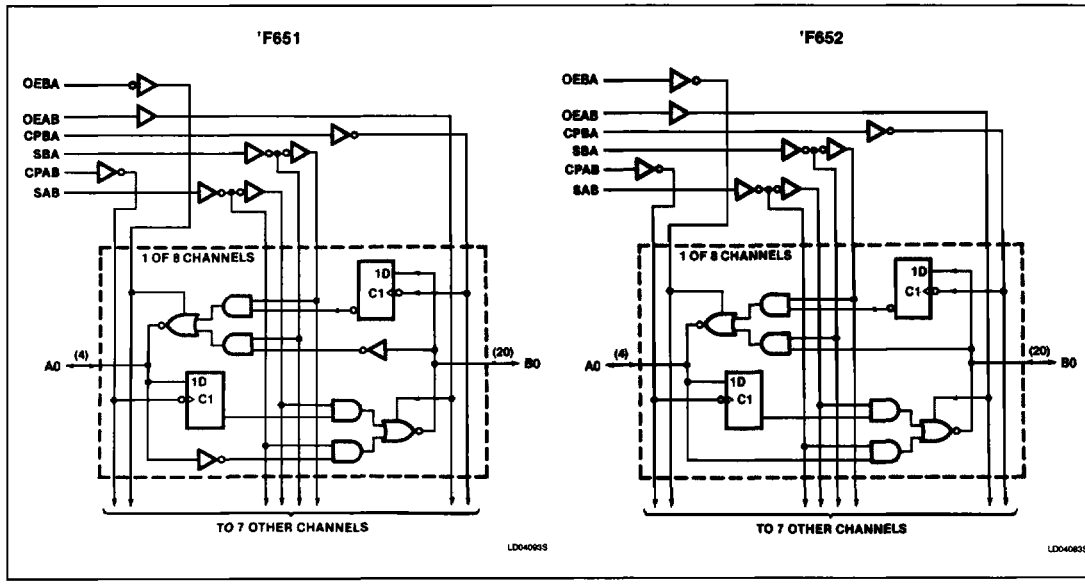
H = High voltage level

L = Low voltage level

X = Don't care

↑ = Low-to-High clock transition

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	128	V
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	High-level output current	V_{OH} = 2.4V or 2.7V			−3	mA
		V_{OH} = 2.0V			−15	mA
I_{OL}	Low-level output current				64	mA
T_A	Operating free-air temperature		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			74F651, 74F652			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
				I_{OH} = −15mA	±10%V_{CC}	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 48mA	±10%V_{CC}		0.35	0.50	V
				I_{OL} = 64mA	±5%V_{CC}		0.40	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_I	Input current at maximum input voltage	Others	V_{CC} = 0.0V, V_I = 7.0V					100	µA
		$A_0 - A_7$, $B_0 - B_7$	V_{CC} = 5.5V, V_I = 5.5V					1.0	mA
I_{IH}	High-level input current	CPAB, CPBA, SAB, SBA, OEAB, $\overline{OEBA}$	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					−20	µA
$I_{IH} + I_{OZH}$	High-level input current	$A_0 - A_7$, $B_0 - B_7$	V_{CC} = MAX, V_O = 2.7V					70	µA
$I_{IL} + I_{OZL}$	Low-level input current		V_{CC} = MAX, V_O = 0.5V					−70	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			−100		−225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				110 140[4]	155 185[4]	mA
		I_{CCL}					155 165[4]	200 240[4]	mA
		I_{CCZ}					130	175	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of High-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. These values are for worst case only. Worst case is defined as all (16) I/O pins selected as outputs. Thermal mounting is required when using worst case conditions.

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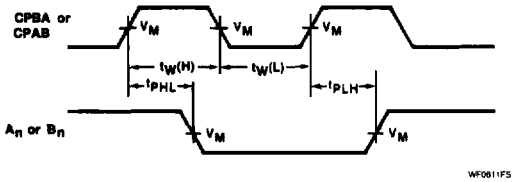
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F651, 74F652					UNIT
			$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	90	110		80		MHz
t_{PLH} t_{PHL}	Propagation delay CPAB or CPBA to A_n or B_n	Waveform 1	5.0 5.5	7.0 7.5	10.5 11.0	4.5 5.0	12.5 12.0	ns
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to B_n or A_n	Waveform 2, 3	3.0 3.0	6.0 6.0	10.0 9.0	2.5 3.0	12.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay SBA or SAB to A_n or B_n	Waveform 2, 3	4.0 4.0	7.0 6.5	10.0 9.5	4.0 4.0	12.5 10.0	ns
t_{PZH} t_{PZL}	Output Enable time OEAB or $\overline{OEBA}$ to A_n or B_n	Waveform 6 Waveform 7	4.0 6.0	7.0 10.5	10.0 12.0	3.5 5.5	11.0 13.0	ns
t_{PHZ} t_{PLZ}	Output Enable time OEAB or $\overline{OEBA}$ to A_n or B_n	Waveform 6 Waveform 7	4.5 4.5	9.5 9.0	13.0 13.0	4.0 4.0	14.5 15.5	ns

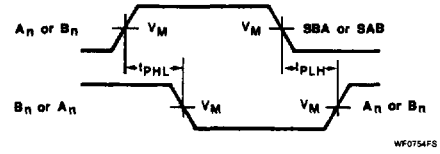
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	74F651, 74F652					UNIT
			$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n or B_n to CPAB or CPBA	Waveform 4	4.0 4.0			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n or B_n to CPAB or CPBA	Waveform 4	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{OEBA}$ to OEAB	Waveform 5	5.0 5.0			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{OEBA}$ to OEAB	Waveform 5	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	Pulse width, High or Low CPAB or CPBA	Waveform 1	4.5 6.5			4.5 6.5		ns

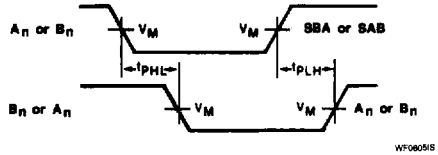
AC WAVEFORMS



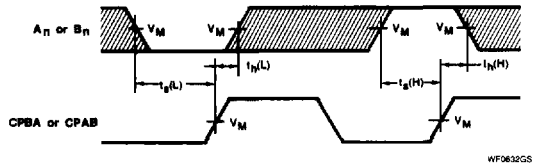
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width and Maximum Clock Frequency



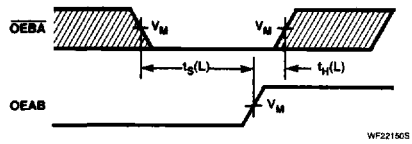
Waveform 2. Propagation Delay, A_n or B_n to B_n or A_n and SBA or SAB to A_n or B_n



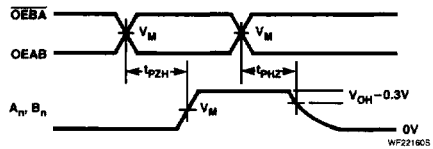
Waveform 3. Propagation Delay, A_n or B_n to B_n or A_n and SBA or SAB to A_n or B_n



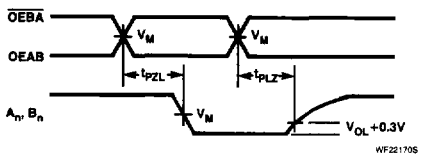
Waveform 4. Data Setup and Hold Times, and Clock Width



Waveform 5. OEBA to OEAB Setup and Hold Time



Waveform 6. 3-State Output Enable Time to High Level and Output Disable Time From High Level



Waveform 7. 3-State Output Enable Time to Low Level and Output Disable Time From Low Level

NOTE: $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output.

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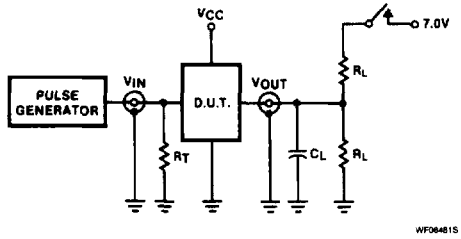
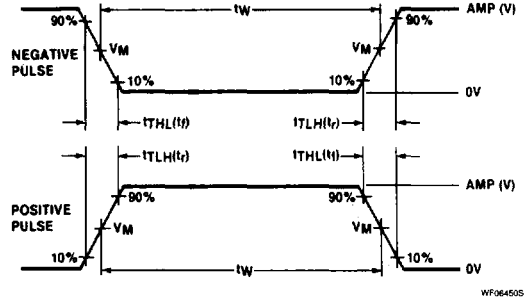
TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
OC	closed
All other	open

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.