

# TCA9554 Low Voltage 8-Bit I<sup>2</sup>C and SMBus Low-Power I/O Expander With Interrupt Output and Configuration Registers

## 1 Features

- I<sup>2</sup>C to Parallel Port Expander
- Open-Drain Active-Low Interrupt Output
- Operating Power-Supply Voltage Range of 1.65 V to 5.5 V
- 5-V Tolerant I/O Ports
- 400-kHz Fast I<sup>2</sup>C Bus
- Three Hardware Address Pins Allow up to Eight Devices on the I<sup>2</sup>C/SMBus
- Input/Output Configuration Register
- Polarity Inversion Register
- Internal Power-On Reset
- Low Standby Current Consumption
- Power-Up With All Channels Configured as Inputs
- No Glitch on Power Up
- Noise Filter on SCL/SDA Inputs
- Latched Outputs With High-Current Drive  
Maximum Capability for Directly Driving LEDs
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 1000-V Charged-Device Model (C101)

## 2 Applications

- Servers
- Routers (Telecom Switching Equipment)
- Personal Computers
- Personal Electronics (e.g. Gaming Consoles)
- Industrial Automation
- Products With GPIO-Limited Processors

## 3 Description

The TCA9554 is a 16-pin device that provides 8 bits of general purpose parallel input/output (I/O) expansion for the two-line bidirectional I<sup>2</sup>C bus (or SMBus) protocol. The device can operate with a power supply voltage ranging from 1.65 V to 5.5 V. The device supports both 100-kHz (Standard-mode) and 400-kHz (Fast-mode) clock frequencies. I/O expanders such as the TCA9554 provide a simple solution when additional I/Os are needed for switches, sensors, push-buttons, LEDs, fans, and other similar devices.

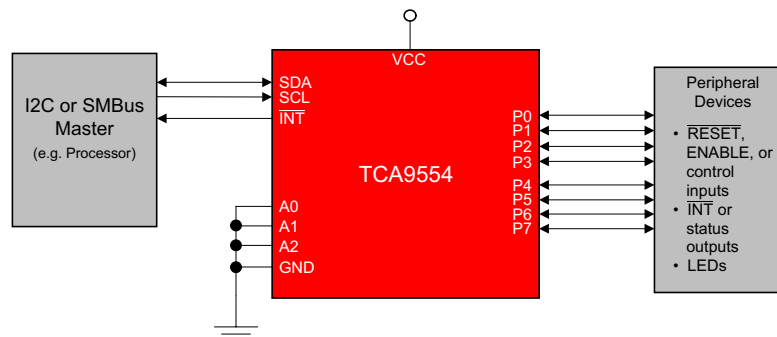
The features of the TCA9554 include an interrupt that is generated on the INT pin whenever an input port changes state. The A0, A1, and A2 hardware selectable address pins allow up to eight TCA9554 devices on the same I<sup>2</sup>C bus. The device can also be reset to its default state by cycling the power supply and causing a power-on reset.

### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TCA9554	TSSOP (16)	5.00 mm × 4.40 mm
	SSOP (16)	4.90 mm × 3.90 mm
	SSOP (16)	6.20 mm × 5.30 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

### Simplified Block Diagram



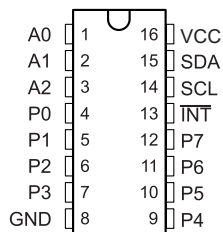
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## 4 Revision History

<b>Changes from Revision C (May 2015) to Revision D</b>	<b>Page</b>
• Added DB package.....	<b>1</b>
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<b>Changes from Revision B (October 2014) to Revision C</b>	<b>Page</b>
• Added standby mode current for $V_I = V_{CC}$ test condition.....	<b>6</b>
• Changed $\Delta I_{CC}$ for one P-port input at $V_I = V_{CC} - 0.6$ , and other P-port I/O at $V_I = V_{CC}$ or GND.....	<b>6</b>
• Added clarification in datasheet that raising voltage above $V_{CC}$ on P-port I/O will result in current flow from P-port to $V_{CC}$ . .....	<b>15</b>
<hr/>	
<b>Changes from Revision A (March 2012) to Revision B</b>	<b>Page</b>
• Added Handling Rating table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section. ....	<b>1</b>
• Updated $I_{OL}$ PARAMETER in the Electrical Characteristics table. ....	<b>5</b>
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<b>Changes from Original (September 2014) to Revision A</b>	<b>Page</b>
• Initial release of full version. ....	<b>1</b>

## 5 Pin Configuration and Functions

**PW, DB, OR DBQ PACKAGE  
(TOP VIEW)**

**Pin Functions**

PIN		I/O	DESCRIPTION
NAME	NO.		
A0	1	I	Address input. Connect directly to V <sub>CC</sub> or ground.
A1	2	I	Address input. Connect directly to V <sub>CC</sub> or ground.
A2	3	I	Address input. Connect directly to V <sub>CC</sub> or ground.
P0	4	I/O	P-port input/output. Push-pull design structure. At power on, P0 is configured as an input.
P1	5	I/O	P-port input/output. Push-pull design structure. At power on, P1 is configured as an input.
P2	6	I/O	P-port input/output. Push-pull design structure. At power on, P2 is configured as an input.
P3	7	I/O	P-port input/output. Push-pull design structure. At power on, P3 is configured as an input.
GND	8	–	Ground
P4	9	I/O	P-port input/output. Push-pull design structure. At power on, P4 is configured as an input.
P5	10	I/O	P-port input/output. Push-pull design structure. At power on, P5 is configured as an input.
P6	11	I/O	P-port input/output. Push-pull design structure. At power on, P6 is configured as an input.
P7	12	I/O	P-port input/output. Push-pull design structure. At power on, P7 is configured as an input.
INT	13	O	Interrupt output. Connect to V <sub>CC</sub> through a pull-up resistor.
SCL	14	I	Serial clock bus. Connect to V <sub>CC</sub> through a pull-up resistor.
SDA	15	I/O	Serial data bus. Connect to V <sub>CC</sub> through a pull-up resistor.
VCC	16	–	Supply voltage

## 6 Specifications

### 6.1 Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	-0.5	6	V
V <sub>I</sub>	Input voltage range <sup>(2)</sup>	-0.5	6	V
V <sub>O</sub>	Output voltage range <sup>(2)</sup>	-0.5	6	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0	-20	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0	-20	mA
I <sub>IOK</sub>	Input/output clamp current	V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub>	±20	mA
I <sub>OL</sub>	Continuous output low current through a single P-port	V <sub>O</sub> = 0 to V <sub>CC</sub>	50	mA
I <sub>OH</sub>	Continuous output high current through a single P-port	V <sub>O</sub> = 0 to V <sub>CC</sub>	-50	mA
I <sub>CC</sub>	Continuous current through GND by all P-ports, $\overline{\text{INT}}$ , and SDA		250	mA
	Continuous current through V <sub>CC</sub> by all P-ports		-160	
T <sub>stg</sub>	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

### 6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	1.65	5.5	V
V <sub>IH</sub>	High-level input voltage	SCL, SDA	V <sub>CC</sub> = 1.65 V to 5.5 V	0.7 × V <sub>CC</sub> V <sub>CC</sub> <sup>(1)</sup>
		A0, A1, A2, P7-P0	V <sub>CC</sub> = 1.65 V to 2.7 V	0.7 × V <sub>CC</sub> 5.5
			V <sub>CC</sub> = 3.0 V to 5.5 V	0.8 × V <sub>CC</sub> 5.5
V <sub>IL</sub>	Low-level input voltage	SCL, SDA	V <sub>CC</sub> = 1.65 V to 5.5 V	-0.5 0.3 × V <sub>CC</sub>
		A0, A1, A2, P7-P0	V <sub>CC</sub> = 1.65 V to 2.7 V	-0.5 0.3 × V <sub>CC</sub>
			V <sub>CC</sub> = 3.0 V to 5.5 V	-0.5 0.2 × V <sub>CC</sub>
I <sub>OL</sub>	Low-level output current	Any P-port, P7-P0		25 mA
I <sub>OH</sub>	High-level output current	Any P-port, P7-P0		-10 mA
I <sub>CC</sub>	Continuous current through GND	All P-ports P7-P0, $\overline{\text{INT}}$ , and SDA		200 mA
	Continuous current through V <sub>CC</sub>	All P-ports P7-P0		-80
T <sub>A</sub>	Operating free-air temperature	-40	85	°C

- (1) The SCL and SDA pins shall not be at a higher potential than the supply voltage V<sub>CC</sub> in the application, or an increase in leakage current, I<sub>I</sub>, will result.

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TCA9554			UNIT
		PW (TSSOP)	DBQ (SSOP)	DB (SSOP)	
		16 PINS	16 PINS	16 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	122.0	121.7	113.2	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	56.4	72.9	63.6	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	67.1	64.2	64.0	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	10.8	24.4	21.2	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	66.5	63.8	63.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>IK</sub>	Input diode clamp voltage	I <sub>I</sub> = -18 mA	1.65 V to 5.5 V	-1.2			V
V <sub>PORR</sub>	Power-on reset voltage, V <sub>CC</sub> rising	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0			1.2	1.5	V
V <sub>PORF</sub>	Power-on reset voltage, V <sub>CC</sub> falling	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0		0.75	1.0		V
V <sub>OH</sub>	P-port high-level output voltage <sup>(2)</sup>	I <sub>OH</sub> = -8 mA	1.65 V	1.2			V
			2.3 V	1.8			
			3 V	2.6			
			4.5 V	4.1			
		I <sub>OH</sub> = -10 mA	1.65 V	1.1			
			2.3 V	1.7			
			3 V	2.5			
			4.5 V	4.0			
I <sub>OL</sub>	SDA <sup>(3)</sup>	V <sub>OL</sub> = 0.4 V	1.65 V to 5.5 V	3	11		mA
	P port <sup>(4)</sup>	V <sub>OL</sub> = 0.5 V	1.65 V	8	10		
			2.3 V	8	13		
			3 V	8	15		
			4.5 V	8	17		
		V <sub>OL</sub> = 0.7 V	1.65 V	10	14		
			2.3 V	10	17		
			3 V	10	20		
			4.5 V	10	24		
	$\overline{\text{INT}}$ <sup>(5)</sup>	V <sub>OL</sub> = 0.4 V	1.65 V to 5.5 V	3	7		
I <sub>I</sub>	SCL, SDA	V <sub>I</sub> = V <sub>CC</sub> or GND	1.65 V to 5.5 V			±1	μA
	A0, A1, A2					±1	
I <sub>IH</sub>	P port	V <sub>I</sub> = V <sub>CC</sub>	1.65 V to 5.5 V			1	μA
I <sub>IL</sub>	P port	V <sub>I</sub> = GND	1.65 V to 5.5 V			-100	μA

(1) All typical values are at nominal supply voltage (1.8-V, 2.5-V, 3.3-V, or 5-V V<sub>CC</sub>) and T<sub>A</sub> = 25°C.

(2) Each P-port I/O configured as a high output must be externally limited to a maximum of 10 mA, and the total current sourced by all I/Os (P-ports P7-P0) through V<sub>CC</sub> should be limited to a maximum current of 80 mA.

(3) The SDA pin must be externally limited to a maximum of 12 mA, and the total current sunk by all I/Os (P-ports P7-P0,  $\overline{\text{INT}}$ , and SDA) through GND should be limited to a maximum current of 200 mA.

(4) Each P-port I/O configured as a low output must be externally limited to a maximum of 25 mA, and the total current sunk by all I/Os (P-ports P7-P0,  $\overline{\text{INT}}$ , and SDA) through GND should be limited to a maximum current of 200 mA.

(5) The  $\overline{\text{INT}}$  pin must be externally limited to a maximum of 7 mA, and the total current sunk by all I/Os (P-ports P7-P0,  $\overline{\text{INT}}$ , and SDA) through GND should be limited to a maximum current of 200 mA.

### Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT
I <sub>CC</sub>	Operating mode	All P-port I/O at V <sub>I</sub> = V <sub>CC</sub> or GND <sup>(6)</sup> , I <sub>O</sub> = 0, I/O = inputs, f <sub>scI</sub> = 400 kHz, No load t <sub>r</sub> = 3 ns	1.65 V to 5.5 V		18	30	μA
			5.5 V		34		
		All P-port I/O at V <sub>I</sub> = V <sub>CC</sub> or GND <sup>(6)</sup> , I <sub>O</sub> = 0, I/O = inputs, f <sub>scI</sub> = 400 kHz, No load t <sub>r,max</sub> = 300 ns	3.6 V		15		
			2.7 V		9		
			1.65 V		5		
			5.5 V		20		
		All P-port I/O at V <sub>I</sub> = V <sub>CC</sub> or GND <sup>(6)</sup> , I <sub>O</sub> = 0, I/O = inputs, f <sub>scI</sub> = 100 kHz, No load t <sub>r,max</sub> = 1 μs	3.6 V		8		
			2.7 V		5		
	1.65 V			3			
	Standby mode		All P-port I/O at V <sub>I</sub> = V <sub>CC</sub> , I <sub>O</sub> = 0, I/O = inputs, f <sub>scI</sub> = 0 kHz, No load	5.5 V	1.9	3.5	
				3.6 V	1.1	1.8	
				2.7 V	1.0	1.6	
		1.65 V		0.4	1.0		
	All P-port I/O at V <sub>I</sub> = GND, I <sub>O</sub> = 0, I/O = inputs, f <sub>scI</sub> = 0 kHz	5.5 V	450	700			
3.6 V		300	600				
2.7 V		225	500				
1.95 V		225	500				
ΔI <sub>CC</sub>	Supply current increase (in standby mode) with one I/O input at specified voltage level, rather than GND or V <sub>CC</sub>	One P-port I/O at V <sub>I</sub> = V <sub>CC</sub> – 0.6 V, Other P-port I/O at V <sub>I</sub> = V <sub>CC</sub> or GND	1.65 V to 5.5 V			70	μA
C <sub>i</sub>	SCL	V <sub>I</sub> = V <sub>CC</sub> or GND	1.65 V to 5.5 V		4	5	pF
	C <sub>iO</sub>	SDA	V <sub>IO</sub> = V <sub>CC</sub> or GND	1.65 V to 5.5 V	5.5	6.5	pF
P port		8			9.5		

(6) The current through the integrated pull-up resistor has been subtracted from the I<sub>CC</sub> operating mode current for V<sub>I</sub> = GND condition.

## 6.6 I<sup>2</sup>C Interface Timing Requirements

over operating free-air temperature range (unless otherwise noted) (see [Figure 10](#))

		STANDARD MODE I <sup>2</sup> C BUS		FAST MODE I <sup>2</sup> C BUS		UNIT
		MIN	MAX	MIN	MAX	
f <sub>scl</sub>	I <sup>2</sup> C clock frequency	0	100	0	400	kHz
t <sub>sch</sub>	I <sup>2</sup> C clock high time	4		0.6		μs
t <sub>scl</sub>	I <sup>2</sup> C clock low time	4.7		1.3		μs
t <sub>sp</sub>	I <sup>2</sup> C spike time		50		50	ns
t <sub>sds</sub>	I <sup>2</sup> C serial-data setup time	250		100		ns
t <sub>sdh</sub>	I <sup>2</sup> C serial-data hold time	0		0		ns
t <sub>icr</sub>	I <sup>2</sup> C input rise time		1000	20	300	ns
t <sub>icf</sub>	I <sup>2</sup> C input fall time		300	20 × (V <sub>DD</sub> / 5.5 V)	300	ns
t <sub>ocf</sub>	I <sup>2</sup> C output fall time	10-pF to 400-pF bus	300	20 × (V <sub>DD</sub> / 5.5 V)	300	ns
t <sub>buf</sub>	I <sup>2</sup> C bus free time between Stop and Start	4.7		1.3		μs
t <sub>sts</sub>	I <sup>2</sup> C Start or repeated Start condition setup	4.7		0.6		μs
t <sub>sth</sub>	I <sup>2</sup> C Start or repeated Start condition hold	4		0.6		μs
t <sub>sps</sub>	I <sup>2</sup> C Stop condition setup	4		0.6		μs
t <sub>vd(data)</sub>	Valid data time	SCL low to SDA output valid	3.45		0.9	μs
t <sub>vd(ack)</sub>	Valid data time of ACK condition	ACK signal from SCL low to SDA (out) low	3.45		0.9	μs
C <sub>b</sub>	I <sup>2</sup> C bus capacitive load		400		400	pF

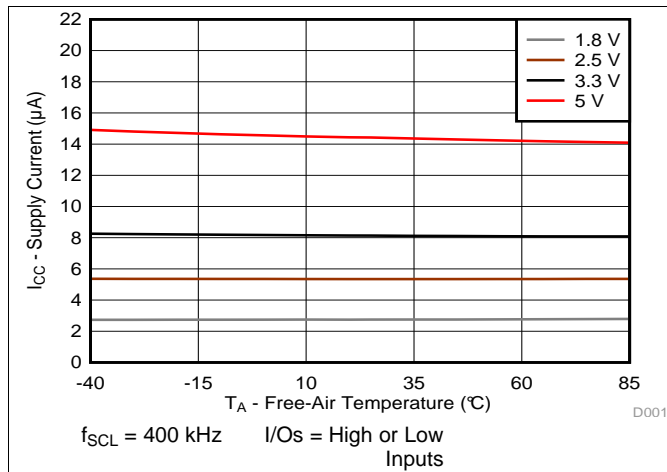
## 6.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted) (see [Figure 11](#) and [Figure 12](#))

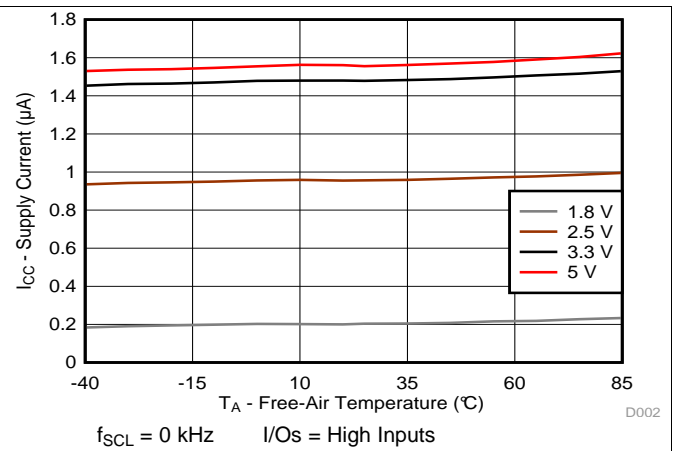
PARAMETER		FROM (INPUT)	TO (OUTPUT)	STANDARD MODE I <sup>2</sup> C BUS		FAST MODE I <sup>2</sup> C BUS		UNIT
				MIN	MAX	MIN	MAX	
t <sub>iv</sub>	Interrupt valid time	P port	$\overline{\text{INT}}$	4		4		μs
t <sub>ir</sub>	Interrupt reset delay time	SCL	$\overline{\text{INT}}$	4		4		μs
t <sub>pv</sub>	Output data valid	SCL	P7–P0	350		350		ns
t <sub>ps</sub>	Input data setup time	P port	SCL	100		100		ns
t <sub>ph</sub>	Input data hold time	P port	SCL	1		1		μs

## 6.8 Typical Characteristics

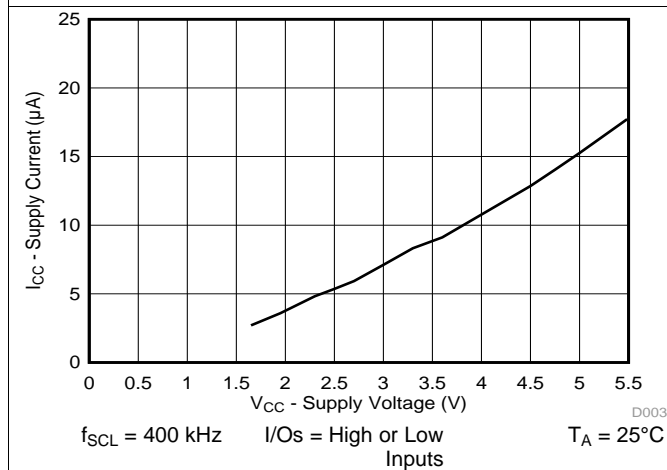
$T_A = 25^\circ\text{C}$  (unless otherwise noted)



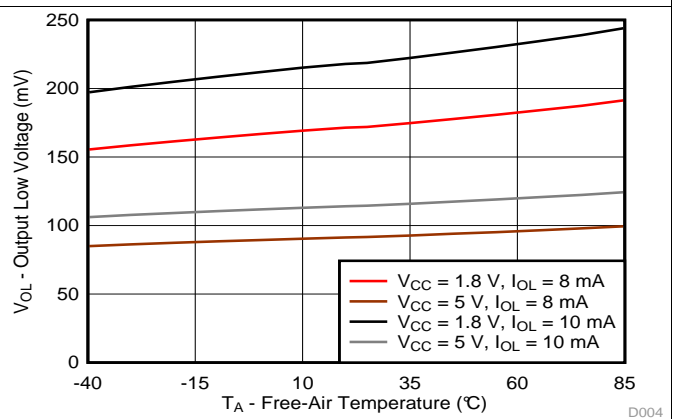
**Figure 1. Supply Current ( $I_{CC}$ , Operating Mode) vs. Temperature ( $T_A$ ) at Four Supply Voltages**



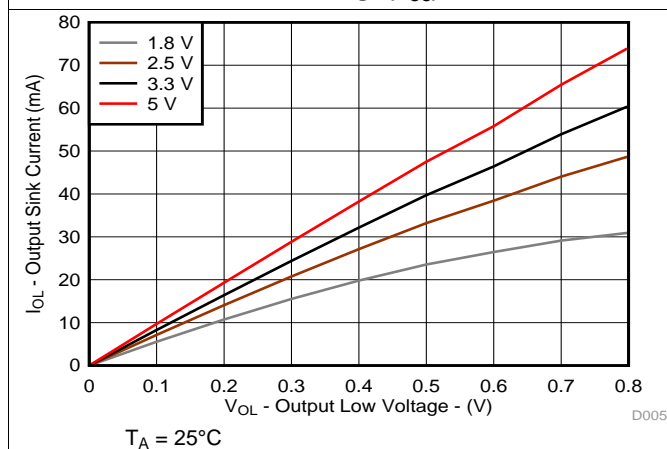
**Figure 2. Supply Current ( $I_{CC}$ , Standby Mode) vs. Temperature ( $T_A$ ) at Four Supply Voltages**



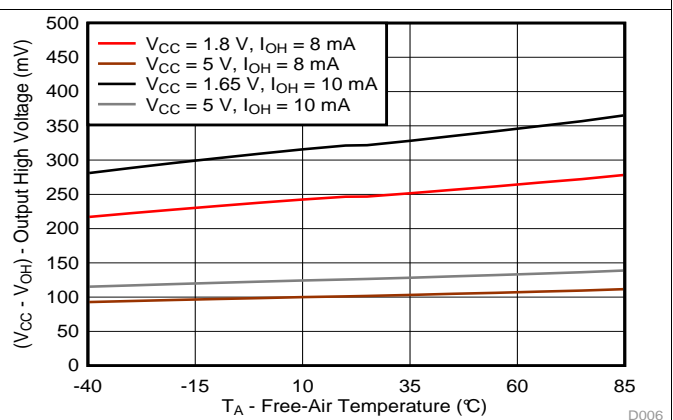
**Figure 3. Supply Current ( $I_{CC}$ , Operating Mode) vs. Supply Voltage ( $V_{CC}$ )**



**Figure 4. Output Low Voltage ( $V_{OL}$ ) vs. Temperature ( $T_A$ ) for P-Port I/Os**



**Figure 5. Sink Current ( $I_{OL}$ ) vs. Output Low Voltage ( $V_{OL}$ ) for P-Ports at Four Supply Voltages**

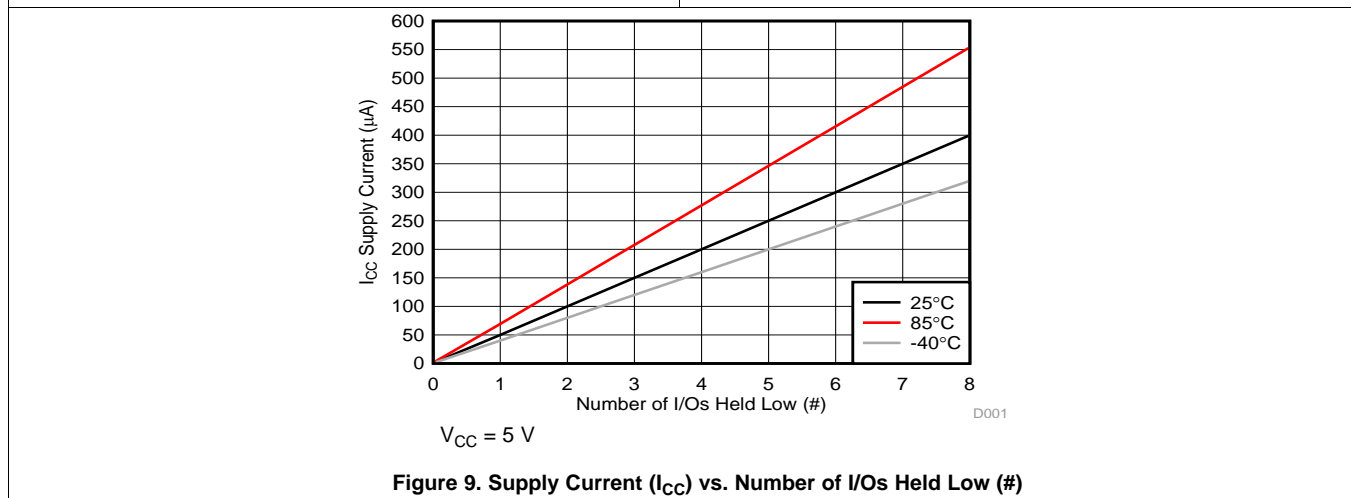
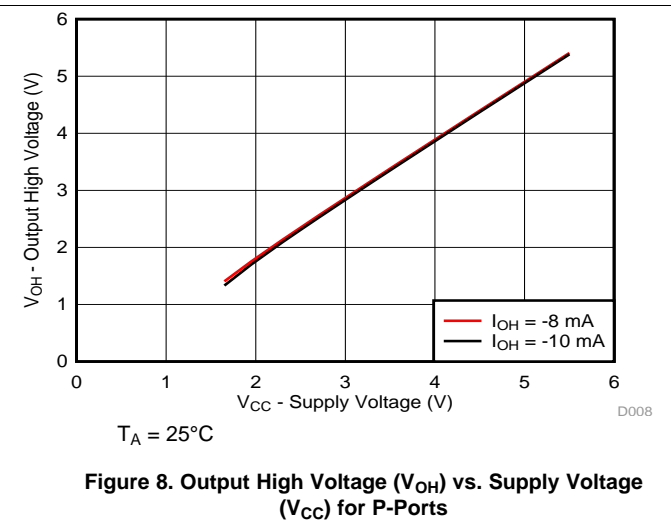
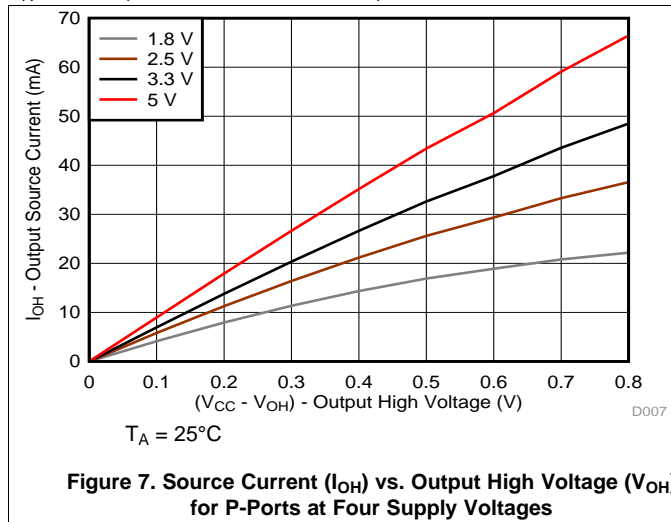


**Figure 6. Output High Voltage ( $V_{CC} - V_{OH}$ ) vs. Temperature ( $T_A$ ) for P-Ports**

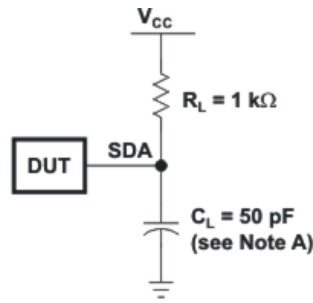


Typical Characteristics (continued)

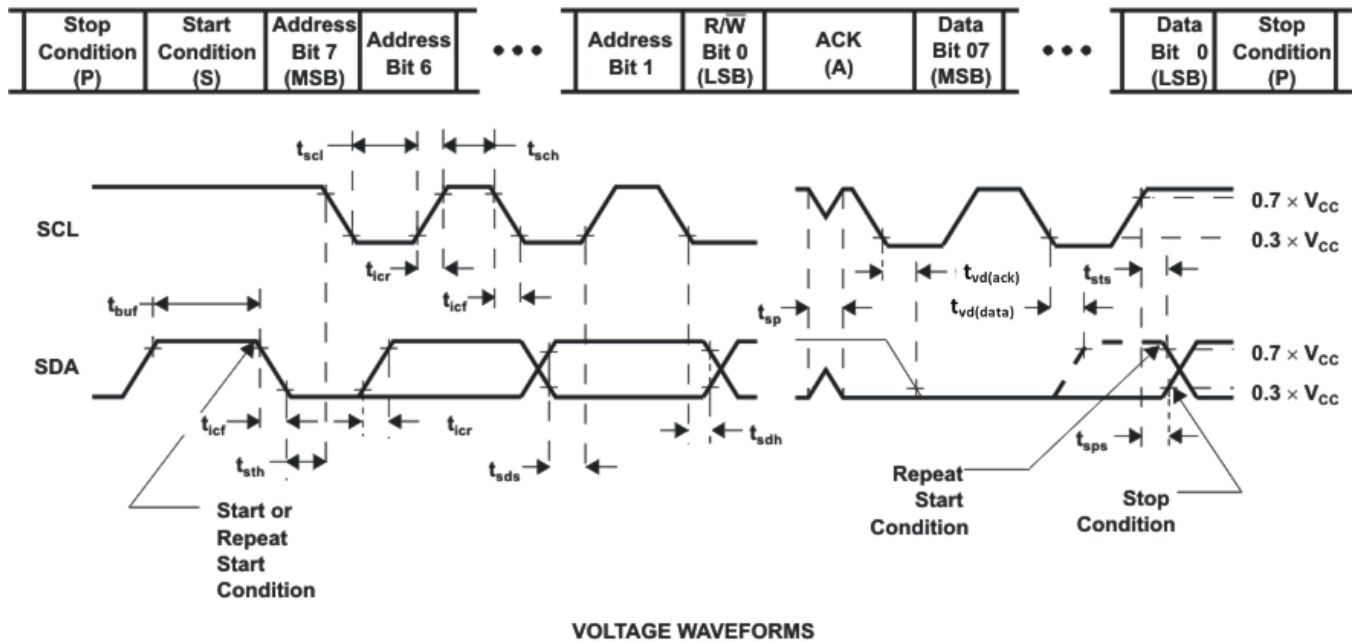
T<sub>A</sub> = 25°C (unless otherwise noted)



## 7 Parameter Measurement Information



SDA LOAD CONFIGURATION



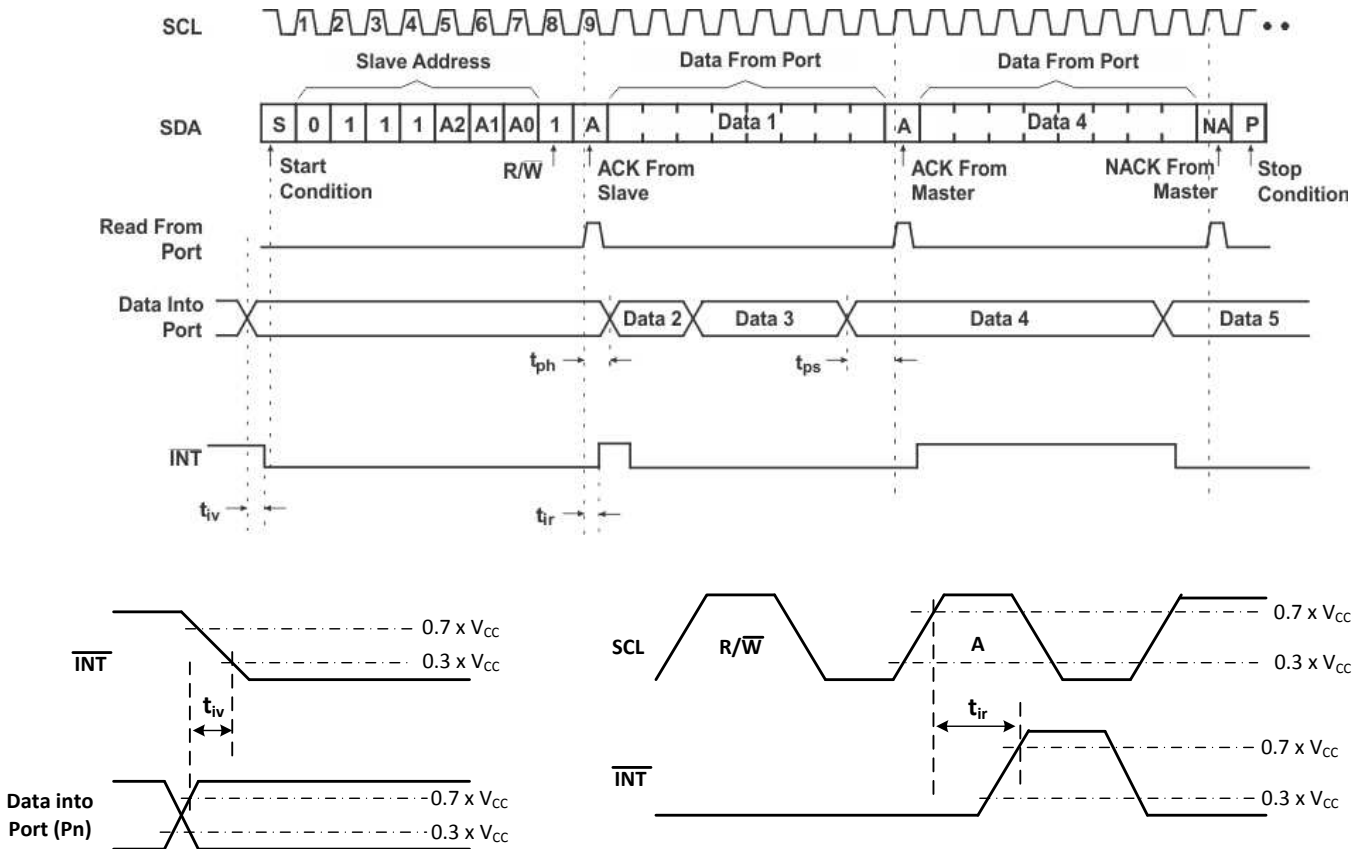
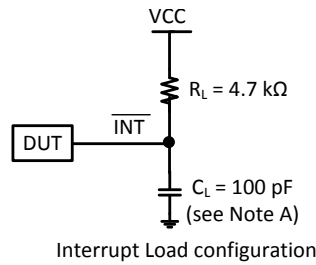
VOLTAGE WAVEFORMS

BYTE	DESCRIPTION
1	I <sup>2</sup> C address
2, 3	P-port data

- A.  $C_L$  includes probe and jig capacitance.
- B. All inputs are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r/t_f \leq 30$  ns.
- C. All parameters and waveforms are not applicable to all devices.

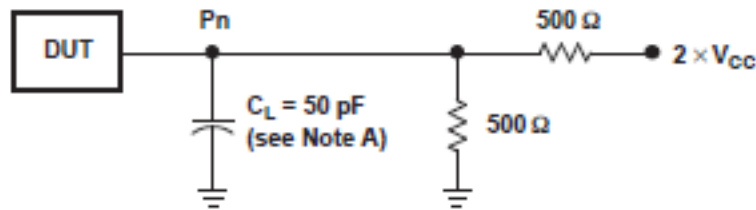
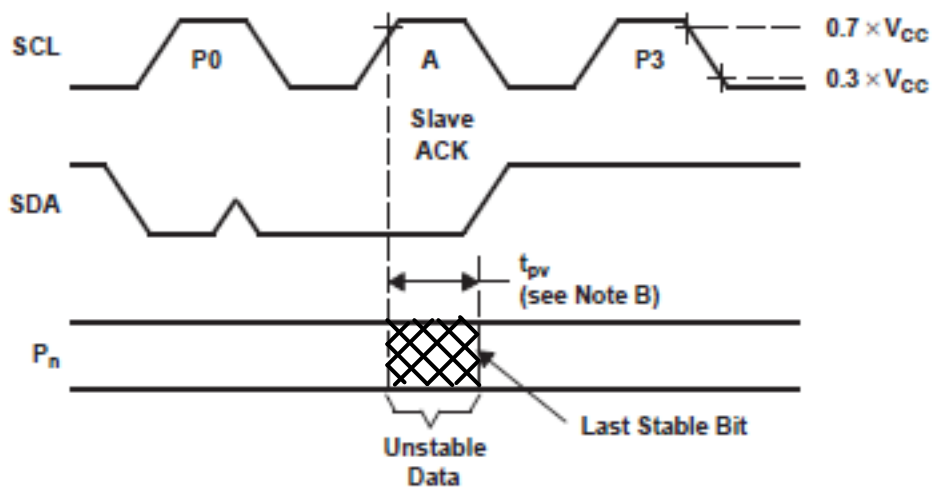
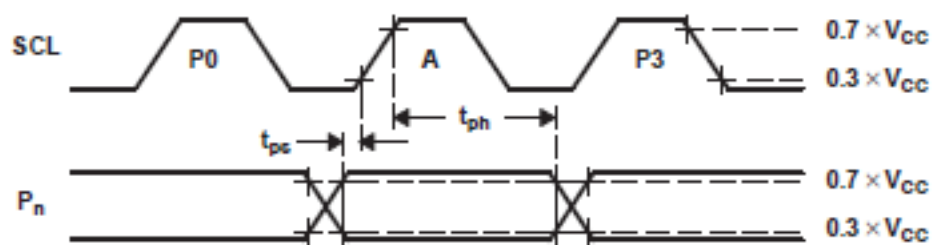
Figure 10. I<sup>2</sup>C Interface Load Circuit And Voltage Waveforms

Parameter Measurement Information (continued)



- A.  $C_L$  includes probe and jig capacitance.
- B. All inputs are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_r/t_f \leq 30$  ns.
- C. All parameters and waveforms are not applicable to all devices.

Figure 11. Interrupt Load Circuit And Voltage Waveforms

**Parameter Measurement Information (continued)**

**P-PORT LOAD CONFIGURATION**

**WRITE MODE (R/W = 0)**

**READ MODE (R/W = 1)**

- A.  $C_L$  includes probe and jig capacitance.
- B.  $t_{pv}$  is measured from  $0.7 \times V_{CC}$  on SCL to 50% I/O ( $P_n$ ) output.
- C. All inputs are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r/t_f \leq 30$  ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

**Figure 12. P-Port Load Circuit And Voltage Waveforms**

## 8 Detailed Description

### 8.1 Overview

The TCA9554 is an 8-bit I/O expander for the two-line bidirectional bus (I<sup>2</sup>C) is designed for 1.65-V to 5.5-V V<sub>CC</sub> operation. It provides general-purpose remote I/O expansion for most micro-controller families via the I<sup>2</sup>C interface (serial clock, SCL, and serial data, SDA, pins).

The TCA9554 open-drain interrupt ( $\overline{\text{INT}}$ ) output is activated when any input state differs from its corresponding Input Port register state and is used to indicate to the system master that an input state has changed. The INT pin can be connected to the interrupt input of a micro-controller. By sending an interrupt signal on this line, the remote I/O can inform the micro-controller if there is incoming data on its ports without having to communicate via the I<sup>2</sup>C bus. Thus, the TCA9554 can remain a simple slave device. The device outputs (latched) have high-current drive capability for directly driving LEDs.

Three hardware pins (A0, A1, and A2) are used to program and vary the fixed I<sup>2</sup>C slave address and allow up to eight devices to share the same I<sup>2</sup>C bus or SMBus.

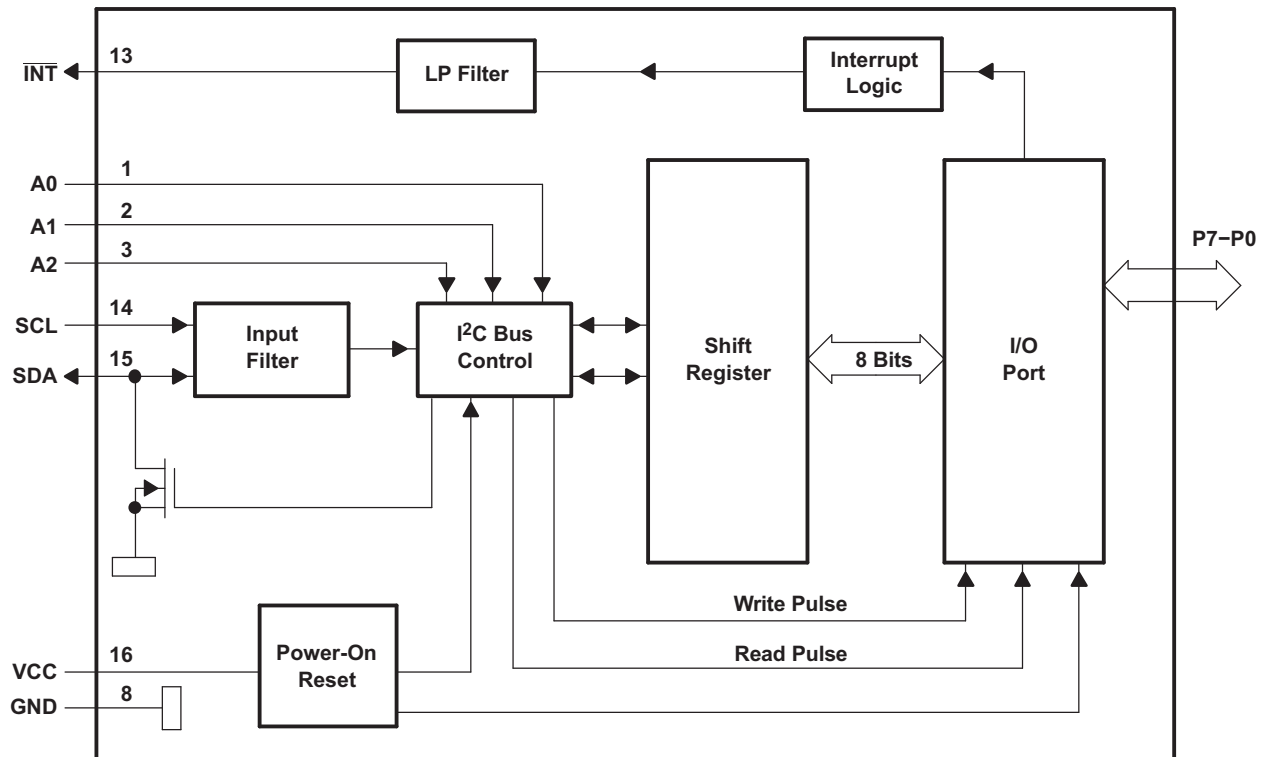
The system master can reset the TCA9554 in the event of a timeout or other improper operation by cycling the power supply and causing a power-on reset (POR). A reset puts the registers in their default state and initializes the I<sup>2</sup>C /SMBus state machine.

The TCA9554 consists of one 8-bit Configuration (input or output selection), Input Port, Output Port, and Polarity Inversion (active high or active low) registers. At power on, the I/Os are configured as inputs. However, the system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each input or output is kept in the corresponding Input Port or Output Port register. The polarity of the Input Port register can be inverted with the Polarity Inversion register. All registers can be read by the system master.

The TCA9554 and TCA9554A are identical except for their fixed I<sup>2</sup>C address. This allows for up to 16 of these devices (8 of each) on the same I<sup>2</sup>C/SMBus.

The TCA9554 is identical to the TCA9534 except for the addition of the internal I/O pull-up resistors, which keeps P-ports from floating when configured as inputs.

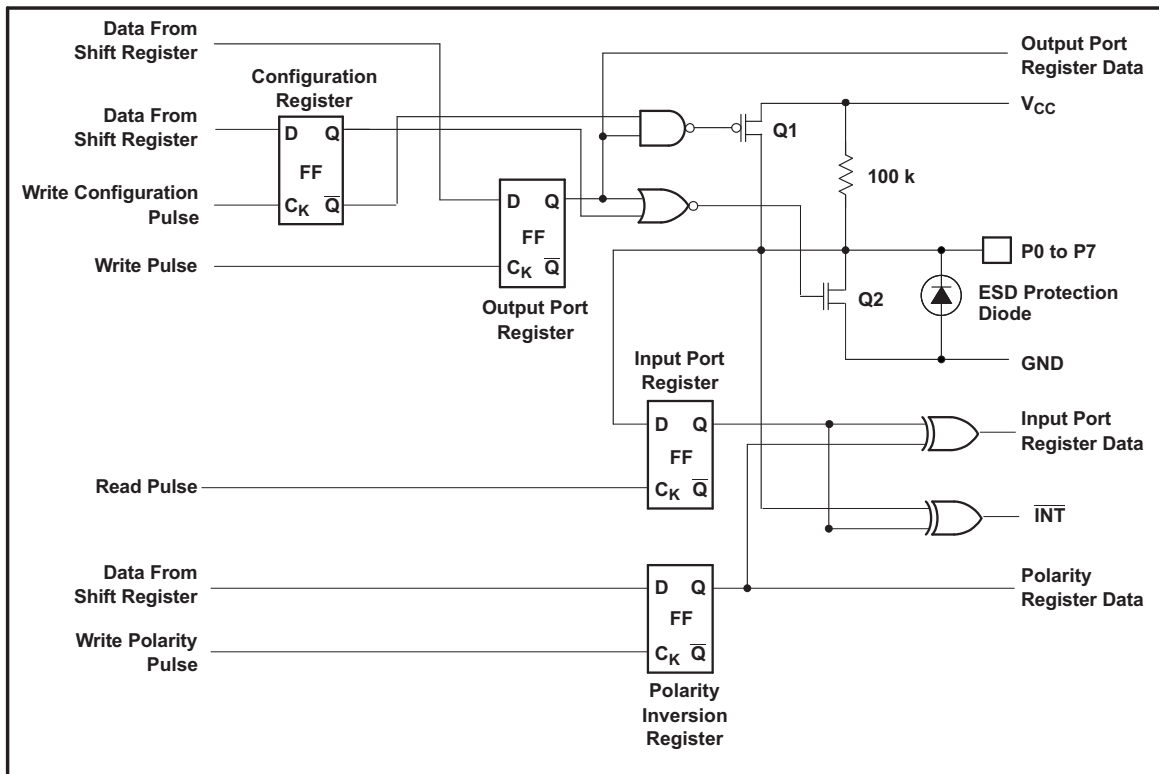
## 8.2 Functional Block Diagram



A. Pin numbers shown are for the PW package.

**Figure 13. Functional Block Diagram**

Functional Block Diagram (continued)



A. At power-on reset, all registers return to default values.

Figure 14. Simplified Schematic Of P0 To P7

8.3 Feature Description

8.3.1 I/O Port

When an I/O is configured as an input, FETs Q1 and Q2 are off, creating a high-impedance input with a weak pull-up (100 kΩ typ) to V<sub>CC</sub>. The input voltage may be raised above V<sub>CC</sub> to a maximum of 5.5 V, however it must be noted that because of the integrated 100 kΩ pull-up resistor it may result in current flow from I/O to V<sub>CC</sub> pin (Figure 14).

If the I/O is configured as an output, Q1 or Q2 is enabled depending on the state of the output port register. In this case, there are low impedance paths between the I/O pin and either V<sub>CC</sub> or GND. The external voltage applied to this I/O pin should not exceed the recommended levels for proper operation.

8.3.2 Interrupt Output (INT̄)

An interrupt is generated by any rising or falling edge of any P-port I/O configured as an input. After time t<sub>IV</sub>, the signal INT̄ is valid. Resetting the interrupt circuit is achieved when data on the ports is changed back to the original state or when data is read from the Input Port register. Resetting occurs in the read mode at the acknowledge (ACK) bit after the rising edge of the SCL signal. Interrupts that occur during the ACK clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and is transmitted as an interrupt on the INT̄ pin.

Reading from or writing to another device does not affect the interrupt circuit, and a pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the Input Port register.

The INT̄ output has an open-drain structure and requires pull-up resistor to V<sub>CC</sub>.

## 8.4 Device Functional Modes

### 8.4.1 Power-On Reset

When power (from 0 V) is applied to V<sub>CC</sub>, an internal power-on reset holds the TCA9554 in a reset condition until V<sub>CC</sub> has reached V<sub>PORR</sub>. At that point, the reset condition is released and the TCA9554 registers and SMBus/I<sup>2</sup>C state machine will initialize to their default states. After that, V<sub>CC</sub> must be lowered to below V<sub>PORF</sub> and then back up to the operating voltage for a power-on reset cycle.

## 8.5 Programming

### 8.5.1 I<sup>2</sup>C Interface

The bidirectional I<sup>2</sup>C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply through a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I<sup>2</sup>C communication with this device is initiated by a master sending a Start condition, a high-to-low transition on the SDA input/output while the SCL input is high (see Figure 15). After the Start condition, the device address byte is sent, most significant bit (MSB) first, including the data direction bit (R/W).

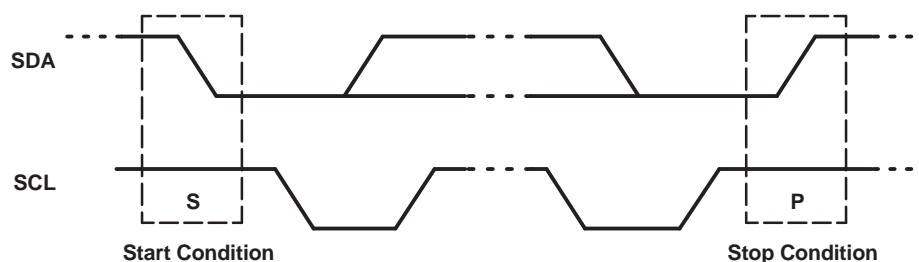
After receiving the valid address byte, this device responds with an acknowledge (ACK), a low on the SDA input/output during the high of the ACK-related clock pulse. The address inputs (A0–A2) of the slave device must not be changed between the Start and the Stop conditions.

On the I<sup>2</sup>C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (Start or Stop) (see Figure 16).

A Stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master (see Figure 15).

Any number of data bytes can be transferred from the transmitter to receiver between the Start and the Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period (see Figure 17). When a slave receiver is addressed, it must generate an ACK after each byte is received. Similarly, the master must generate an ACK after each byte that it receives from the slave transmitter. Setup and hold times must be met to ensure proper operation.

A master receiver will signal an end of data to the slave transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a Stop condition.



**Figure 15. Definition of Start and Stop Conditions**



Programming (continued)

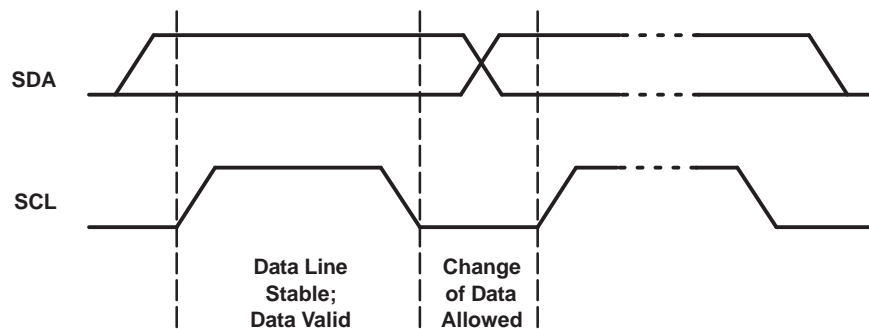


Figure 16. Bit Transfer

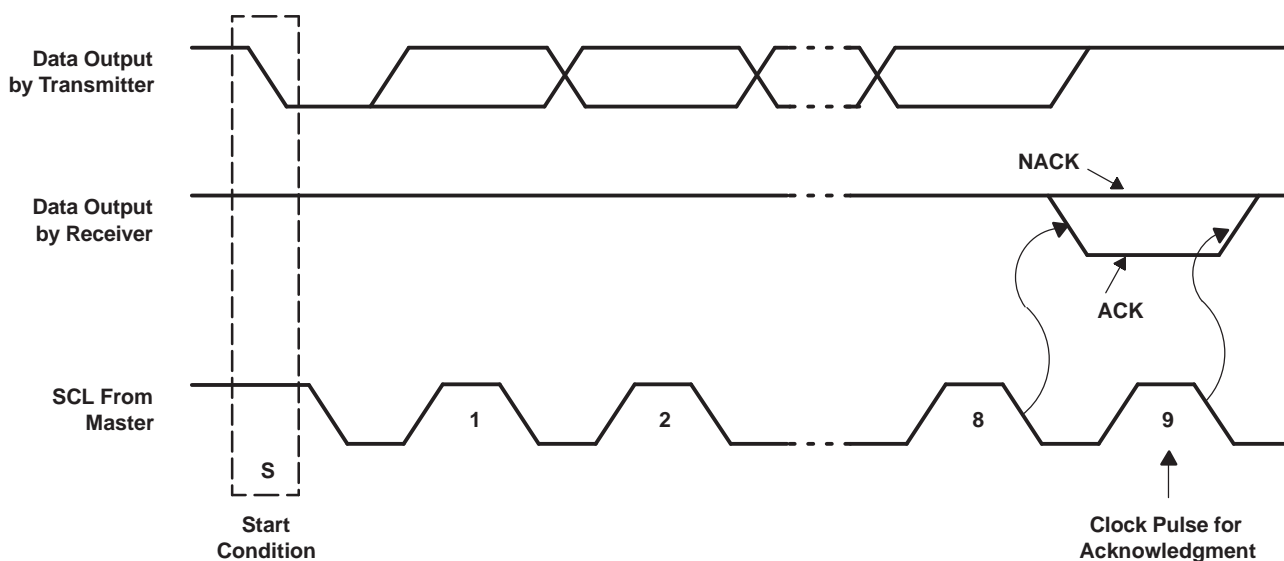


Figure 17. Acknowledgment on I<sup>2</sup>C Bus

Table 1. Interface Definition Table

BYTE	BIT							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I <sup>2</sup> C slave address	L	H	L	L	A2	A1	A0	R/W
Px I/O data bus	P7	P6	P5	P4	P3	P2	P1	P0

## 8.6 Register Map

### 8.6.1 Device Address

Figure 18 shows the address byte of the TCA9554.

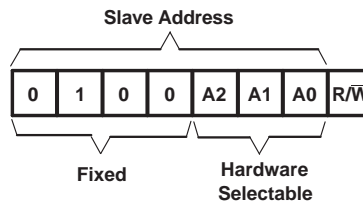


Figure 18. TCA9554 Address

Table 2. Address Reference

INPUTS			I <sup>2</sup> C BUS SLAVE ADDRESS
A2	A1	A0	
L	L	L	32 (decimal), 20 (hexadecimal)
L	L	H	33 (decimal), 21 (hexadecimal)
L	H	L	34 (decimal), 22 (hexadecimal)
L	H	H	35 (decimal), 23 (hexadecimal)
H	L	L	36 (decimal), 24 (hexadecimal)
H	L	H	37 (decimal), 25 (hexadecimal)
H	H	L	38 (decimal), 26 (hexadecimal)
H	H	H	39 (decimal), 27 (hexadecimal)

The last bit of the slave address defines the operation (read or write) to be performed. When it is high (1), a read is selected, while a low (0) selects a write operation.

### 8.6.2 Control Register and Command Byte

Following the successful Acknowledgment of the address byte, the bus master sends a command byte that is stored in the control register in the TCA9554 (see Figure 19). Two bits of this command byte state the operation (read or write) and the internal register (input, output, polarity inversion or configuration) that will be affected. This register can be written or read through the I<sup>2</sup>C bus. The command byte is sent only during a write transmission.

Once a command byte has been sent, the register that was addressed continues to be accessed by reads until a new command byte has been sent.

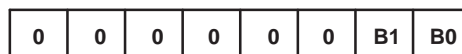


Figure 19. Control Register Bits

Table 3. Command Byte Table

CONTROL REGISTER BITS		COMMAND BYTE (HEX)	REGISTER	PROTOCOL	POWER-UP DEFAULT
B1	B0				
0	0	0x00	Input Port	Read byte	XXXX XXXX
0	1	0x01	Output Port	Read/write byte	1111 1111
1	0	0x02	Polarity Inversion	Read/write byte	0000 0000
1	1	0x03	Configuration	Read/write byte	1111 1111

### 8.6.3 Register Descriptions

The Input Port register (register 0) reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration register. It only acts on read operation. Writes to these registers have no effect. The default value, X, is determined by the externally applied logic level.

Before a read operation, a write transmission is sent with the command byte to indicate to the I<sup>2</sup>C device that the Input Port register is accessed next.

**Table 4. Register 0 (Input Port Register) Table**

BIT	I7	I6	I5	I4	I3	I2	I1	I0
DEFAULT	X	X	X	X	X	X	X	X

The Output Port register (register 1) shows the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, not the actual pin value.

**Table 5. Register 1 (Output Port Register) Table**

BIT	O7	O6	O5	O4	O3	O2	O1	O0
DEFAULT	1	1	1	1	1	1	1	1

The Polarity Inversion register (register 2) allows polarity inversion of pins defined as inputs by the Configuration register. If a bit in this register is set (written with 1), the corresponding port pin polarity is inverted. If a bit in this register is cleared (written with a 0), the corresponding port pin original polarity is retained.

**Table 6. Register 2 (Polarity Inversion Register) Table**

BIT	N7	N6	N5	N4	N3	N2	N1	N0
DEFAULT	0	0	0	0	0	0	0	0

The Configuration register (register 3) configures the directions of the I/O pins. If a bit in this register is set to 1, the corresponding port pin is enabled as an input with a high-impedance output driver. If a bit in this register is cleared to 0, the corresponding port pin is enabled as an output.

**Table 7. Register 3 (Configuration Register) Table**

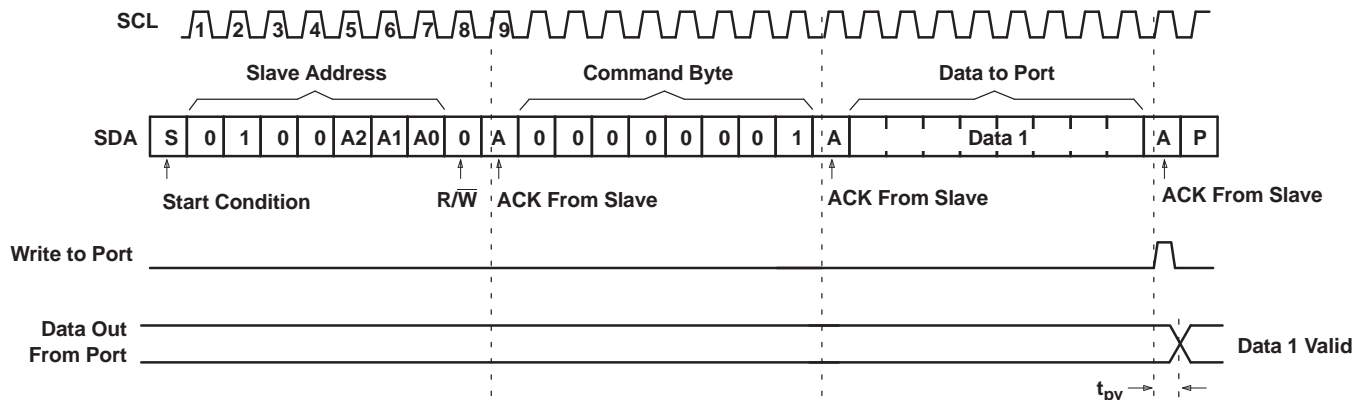
BIT	C7	C6	C5	C4	C3	C2	C1	C0
DEFAULT	1	1	1	1	1	1	1	1

### 8.6.3.1 Bus Transactions

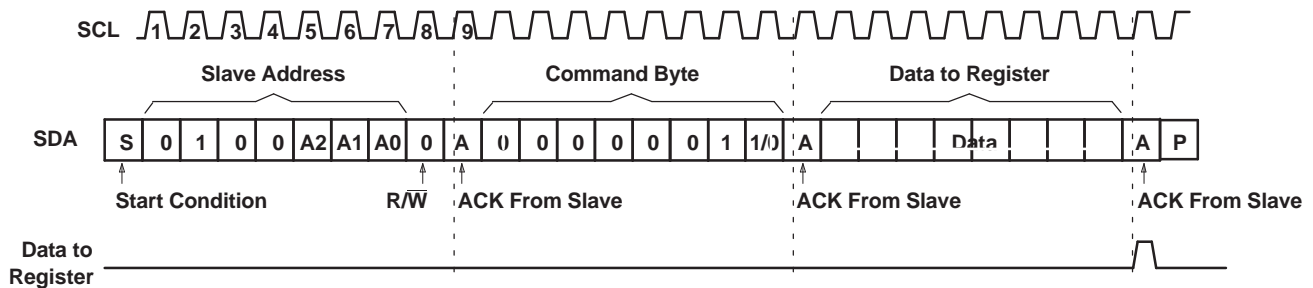
Data is exchanged between the master and TCA9554 through write and read commands.

#### 8.6.3.1.1 Writes

Data is transmitted to the TCA9554 by sending the device address and setting the least-significant bit (LSB) to a logic 0 (see Figure 18 for device address). The command byte is sent after the address and determines which register receives the data that follows the command byte (see Figure 20 and Figure 21). There is no limitation on the number of data bytes sent in one write transmission.



**Figure 20. Write to Output Port Register**



**Figure 21. Write to Configuration or Polarity Inversion Registers**

8.6.3.1.2 Reads

The bus master first must send the TCA9554 address with the LSB set to a logic 0 (see Figure 18 for device address). The command byte is sent after the address and determines which register is accessed. After a restart, the device address is sent again but, this time, the LSB is set to a logic 1. Data from the register defined by the command byte then is sent by the TCA9554 (see Figure 22 and Figure 23). After a restart, the value of the register defined by the command byte matches the register being accessed when the restart occurred. Data is clocked into the register on the rising edge of the ACK clock pulse. There is no limitation on the number of data bytes received in one read transmission, but when the final byte is received, the bus master must not acknowledge the data.

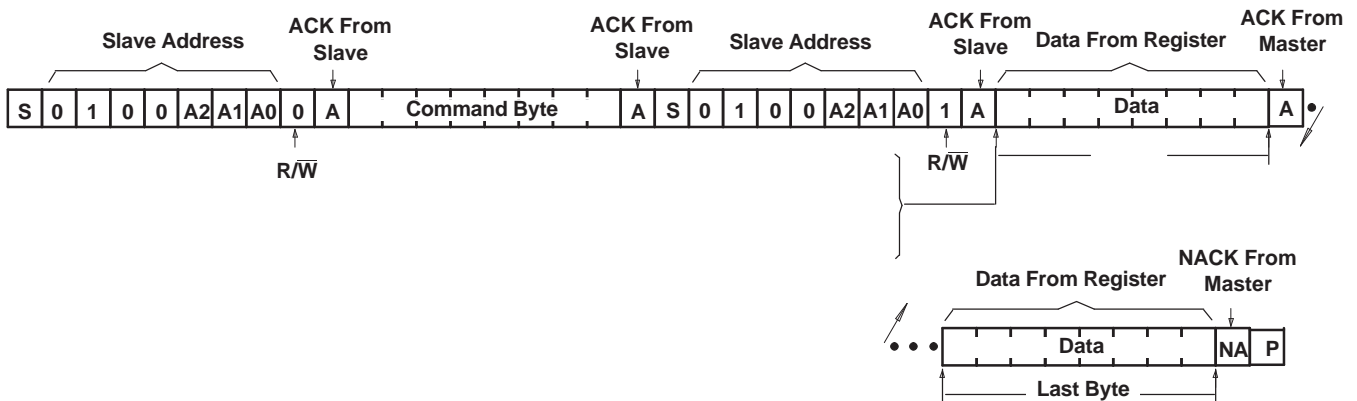
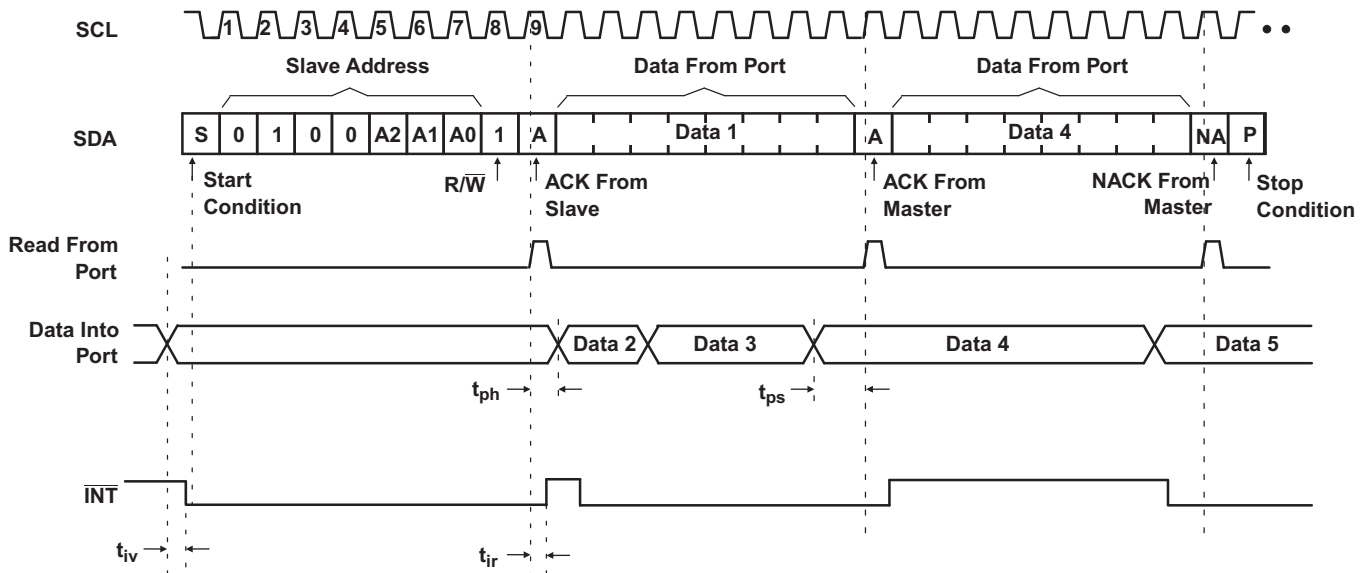


Figure 22. Read From Register



- A. This figure assumes the command byte has previously been programmed with 00h.
- B. Transfer of data can be stopped at any moment by a Stop condition.
- C. This figure eliminates the command byte transfer, a restart, and slave address call between the initial slave address call and actual data transfer from the P port. See Figure 22 for these details.

Figure 23. Read From Input Port Register

## 9 Application and Implementation

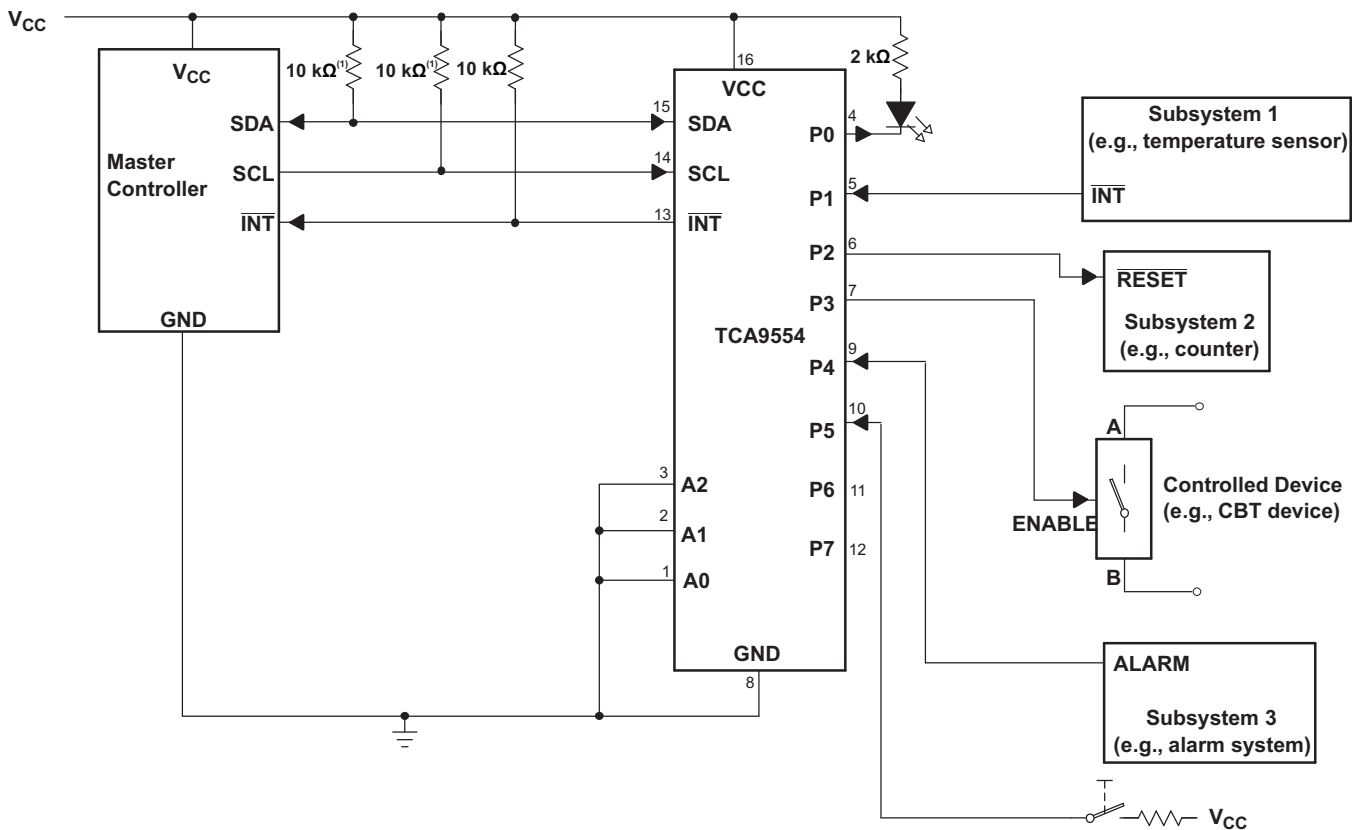
### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

Figure 24 shows an application in which the TCA9554 can be used.

### 9.2 Typical Application



(1) The SCL and SDA pins must be tied directly to VCC because if SCL and SDA are tied to an auxiliary power supply that could be powered on while VCC is powered off, then the supply current, ICC, will increase as a result.

- A. Device address is configured as 0100000 for this example.
- B. P0, P2, and P3 are configured as outputs.
- C. P1, P4, and P5 are configured as inputs.
- D. P6 and P7 are not used and have internal 100-kΩ pullup resistors to protect them from floating.

**Figure 24. Application Schematic**

## Typical Application (continued)

### 9.2.1 Design Requirements

#### 9.2.1.1 Minimizing $I_{CC}$ When I/Os Control LEDs

When the I/Os are used to control LEDs, normally they are connected to  $V_{CC}$  through a resistor as shown in Figure 24. For a P-port configured as an input,  $I_{CC}$  increases as  $V_I$  becomes lower than  $V_{CC}$ . The LED is a diode, with threshold voltage  $V_T$ , and when a P-port is configured as an input the LED will be off but  $V_I$  is a  $V_T$  drop below  $V_{CC}$ .

For battery-powered applications, it is essential that the voltage of P-ports controlling LEDs is greater than or equal to  $V_{CC}$  when the P-ports are configured as input to minimize current consumption. Figure 25 shows a high-value resistor in parallel with the LED. Figure 26 shows  $V_{CC}$  less than the LED supply voltage by at least  $V_T$ . Both of these methods maintain the I/O  $V_I$  at or above  $V_{CC}$  and prevents additional supply current consumption when the P-port is configured as an input and the LED is off.

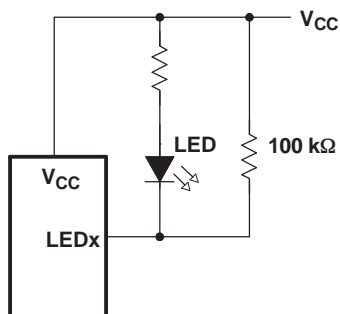


Figure 25. High-Value Resistor in Parallel With LED

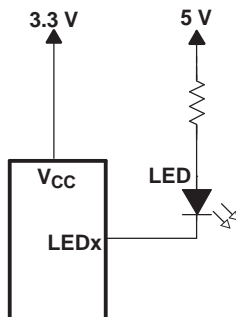


Figure 26. Device Supplied by a Lower Voltage

## Typical Application (continued)

### 9.2.2 Detailed Design Procedure

The pull-up resistors,  $R_p$ , for the SCL and SDA lines need to be selected appropriately and take into consideration the total capacitance of all slaves on the I<sup>2</sup>C bus. The minimum pull-up resistance is a function of  $V_{CC}$ ,  $V_{OL(max)}$ , and  $I_{OL}$ :

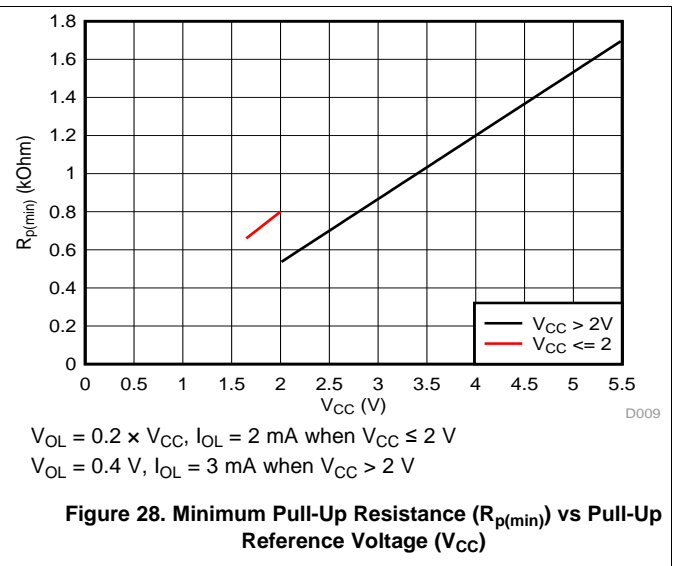
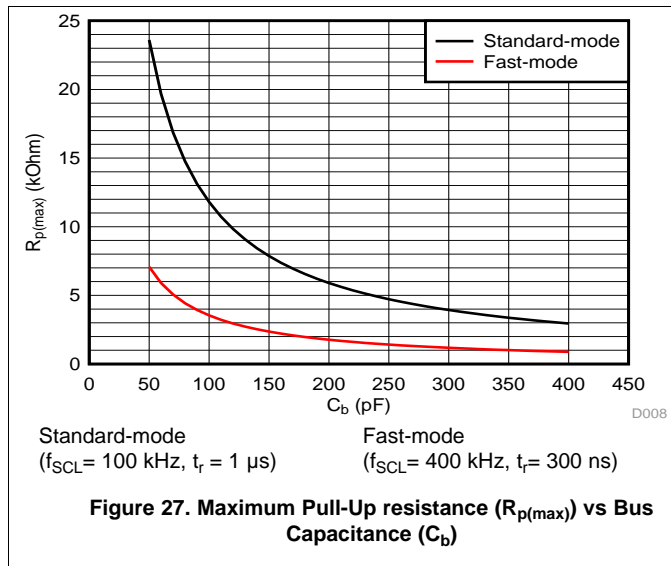
$$R_{p(min)} = \frac{V_{CC} - V_{OL(max)}}{I_{OL}} \tag{1}$$

The maximum pull-up resistance is a function of the maximum rise time,  $t_r$  (300 ns for fast-mode operation,  $f_{SCL} = 400$  kHz) and bus capacitance,  $C_b$ :

$$R_{p(max)} = \frac{t_r}{0.8473 \times C_b} \tag{2}$$

The maximum bus capacitance for an I<sup>2</sup>C bus must not exceed 400 pF for standard-mode or fast-mode operation. The bus capacitance can be approximated by adding the capacitance of the TCA9554,  $C_i$  for SCL or  $C_{io}$  for SDA, the capacitance of wires/connections/traces, and the capacitance of additional slaves on the bus.

### 9.2.3 Application Curves



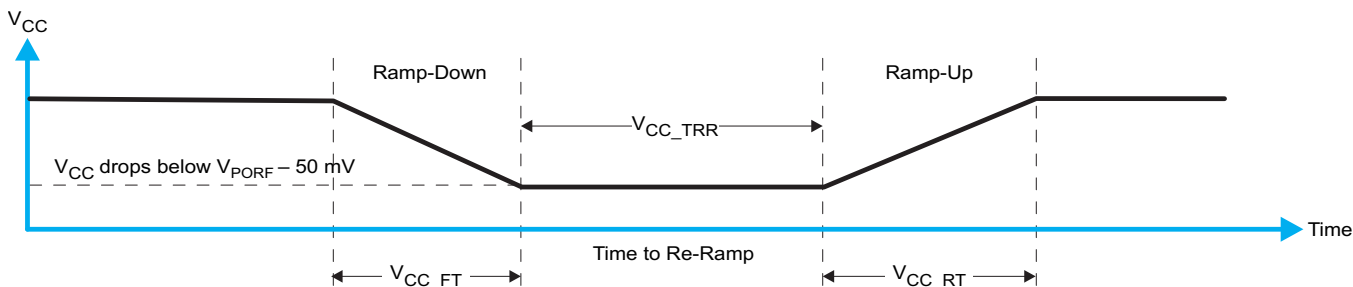


## 10 Power Supply Recommendations

### 10.1 Power-On Reset Requirements

In the event of a glitch or data corruption, TCA9554 can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The two types of power-on reset are shown in and [Figure 29](#).



**Figure 29.  $V_{CC}$  is Lowered Below the POR Threshold, Then Ramped Back Up to  $V_{CC}$**

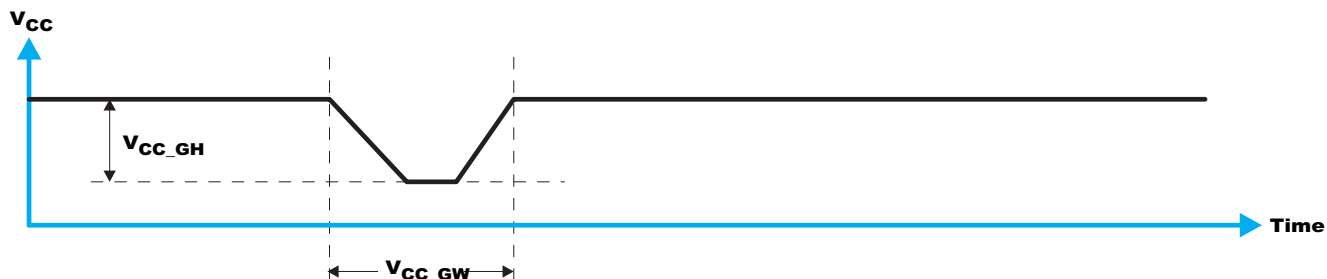
[Table 8](#) specifies the performance of the power-on reset feature for TCA9554 for both types of power-on reset.

**Table 8. Recommended Supply Sequencing And Ramp Rates<sup>(1)</sup>**

PARAMETER			MIN	TYP	MAX	UNIT
$V_{CC\_FT}$	Fall rate	See <a href="#">Figure 29</a>	1			ms
$V_{CC\_RT}$	Rise rate	See <a href="#">Figure 29</a>	0.1			ms
$V_{CC\_TRR}$	Time to re-ramp (when $V_{CC}$ drops to $V_{POR\_MIN} - 50$ mV or when $V_{CC}$ drops to GND)	See <a href="#">Figure 29</a>	2			$\mu$ s
$V_{CC\_GH}$	Level that $V_{CCP}$ can glitch down to, but not cause a functional disruption when $V_{CC\_GW} = 1$ $\mu$ s	See <a href="#">Figure 30</a>			1.2	V
$V_{CC\_GW}$	Glitch width that will not cause a functional disruption when $V_{CC\_GH} = 0.5 \times V_{CC}$	See <a href="#">Figure 30</a>			10	$\mu$ s

(1) All supply sequencing and ramp rate values are measured at  $T_A = 25^\circ\text{C}$

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width ( $V_{CC\_GW}$ ) and height ( $V_{CC\_GH}$ ) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. [Figure 30](#) and [Table 8](#) provide more information on how to measure these specifications.



**Figure 30. Glitch Width and Glitch Height**

$V_{PORR}$  is critical to the power-on reset.  $V_{PORR}$  is the voltage level at which the reset condition is released and all the registers and the I<sup>2</sup>C/SMBus state machine are initialized to their default states. The value of power-on-reset voltage differs based on the  $V_{CC}$  being lowered to or from 0 ( $V_{PORR}$  or  $V_{PORF}$ ). [Figure 31](#) and [Table 8](#) provide more details on this specification.

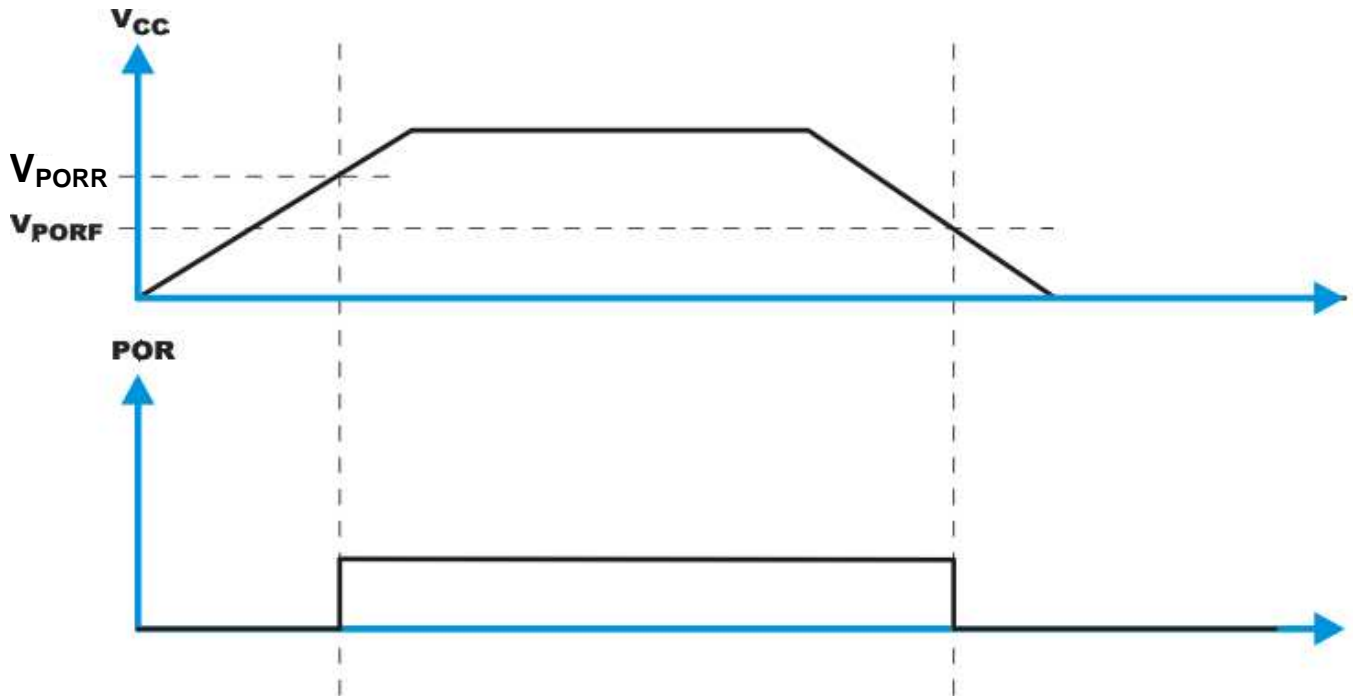


Figure 31. Waveform describing  $V_{CC}$  voltage level at which power-on-reset (POR) occurs

## 11 Layout

### 11.1 Layout Guidelines

For printed circuit board (PCB) layout of the TCA9554, common PCB layout practices should be followed but additional concerns related to high-speed data transfer such as matched impedances and differential pairs are not a concern for I<sup>2</sup>C signal speeds.

In all PCB layouts, it is a best practice to avoid right angles in signal traces, to fan out signal traces away from each other upon leaving the vicinity of an integrated circuit (IC), and to use thicker trace widths to carry higher amounts of current that commonly pass through power and ground traces. By-pass and de-coupling capacitors are commonly used to control the voltage on the VCC pin, using a larger capacitor to provide additional power in the event of a short power supply glitch and a smaller capacitor to filter out high-frequency ripple. These capacitors should be placed as close to the TCA9554 as possible. These best practices are shown in Figure 32.

For the layout example provided in Figure 32, it would be possible to fabricate a PCB with only 2 layers by using the top layer for signal routing and the bottom layer as a split plane for power (V<sub>CC</sub>) and ground (GND). However, a 4 layer board is preferable for boards with higher density signal routing. On a 4 layer PCB, it is common to route signals on the top and bottom layer, dedicate one internal layer to a ground plane, and dedicate the other internal layer to a power plane. In a board layout using planes or split planes for power and ground, vias are placed directly next to the surface mount component pad which needs to attach to V<sub>CC</sub> or GND and the via is connected electrically to the internal layer or the other side of the board. Vias are also used when a signal trace needs to be routed to the opposite side of the board, but this technique is not demonstrated in Figure 32.

### 11.2 Layout Example

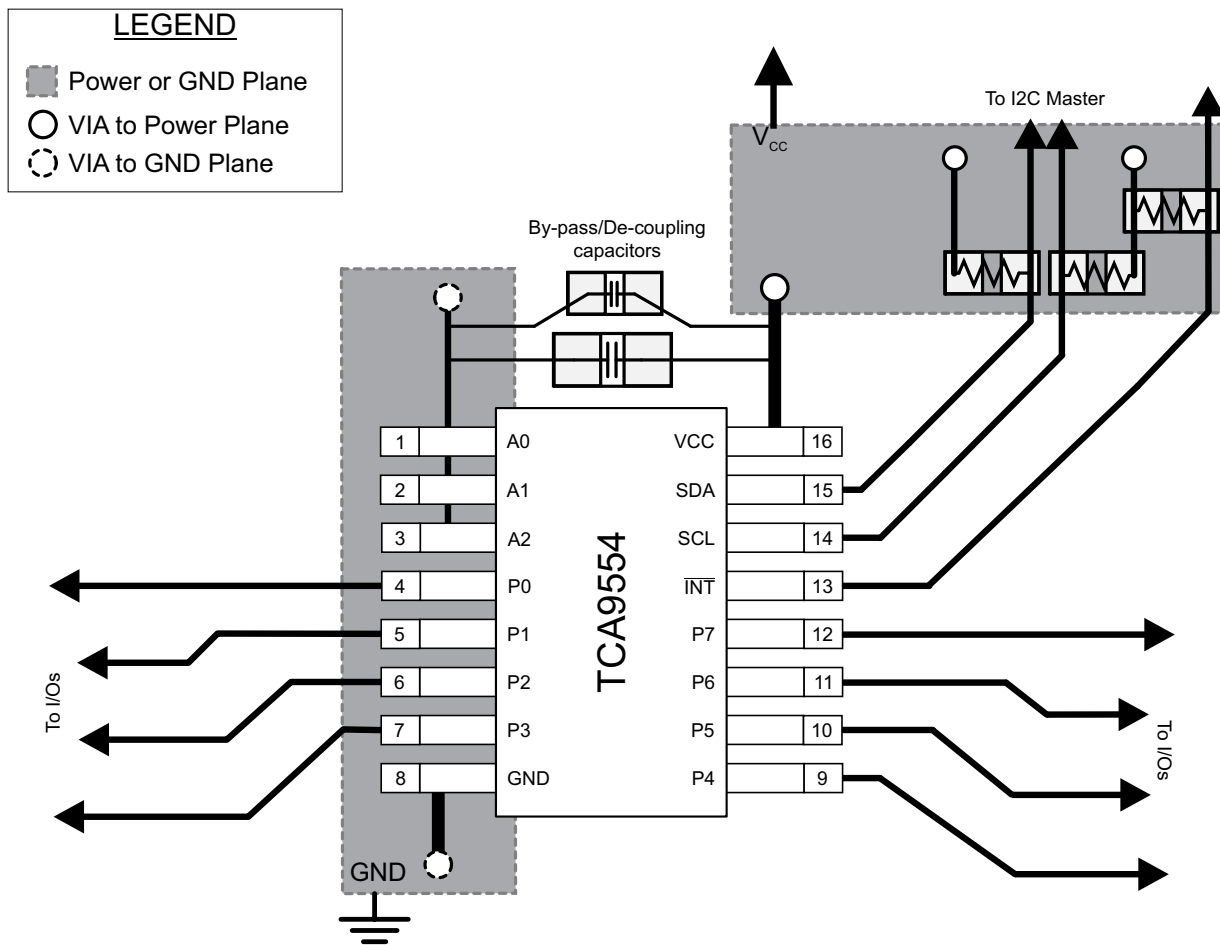


Figure 32. TCA9554 Layout

## 12 Device and Documentation Support

### 12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.2 Trademarks

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 12.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.4 Glossary




[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TCA9554DBQR	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	9554	
TCA9554DBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TD554	
TCA9554DWR	PREVIEW	SOIC	DW	16	2000	TBD	Call TI	Call TI	-40 to 85	TCA9554	
TCA9554DWT	PREVIEW	SOIC	DW	16	250	TBD	Call TI	Call TI	-40 to 85		
TCA9554PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PW554	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCA9554DBQR	SSOP	DBQ	16	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
TCA9554DBR	SSOP	DB	16	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
TCA9554PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

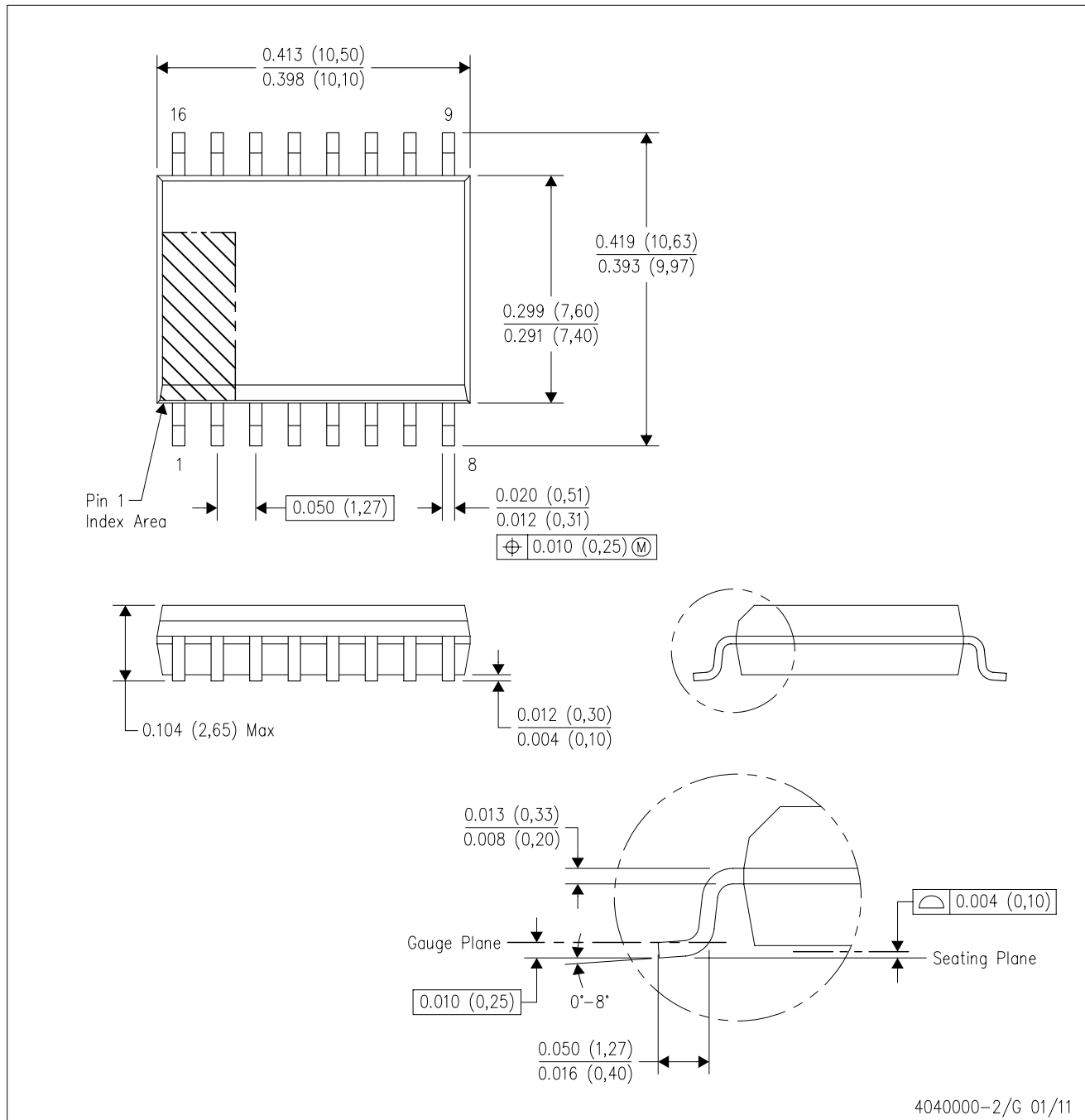

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCA9554DBQR	SSOP	DBQ	16	2500	340.5	338.1	20.6
TCA9554DBR	SSOP	DB	16	2000	367.0	367.0	38.0
TCA9554PWR	TSSOP	PW	16	2000	367.0	367.0	35.0



DW (R-PDSO-G16)

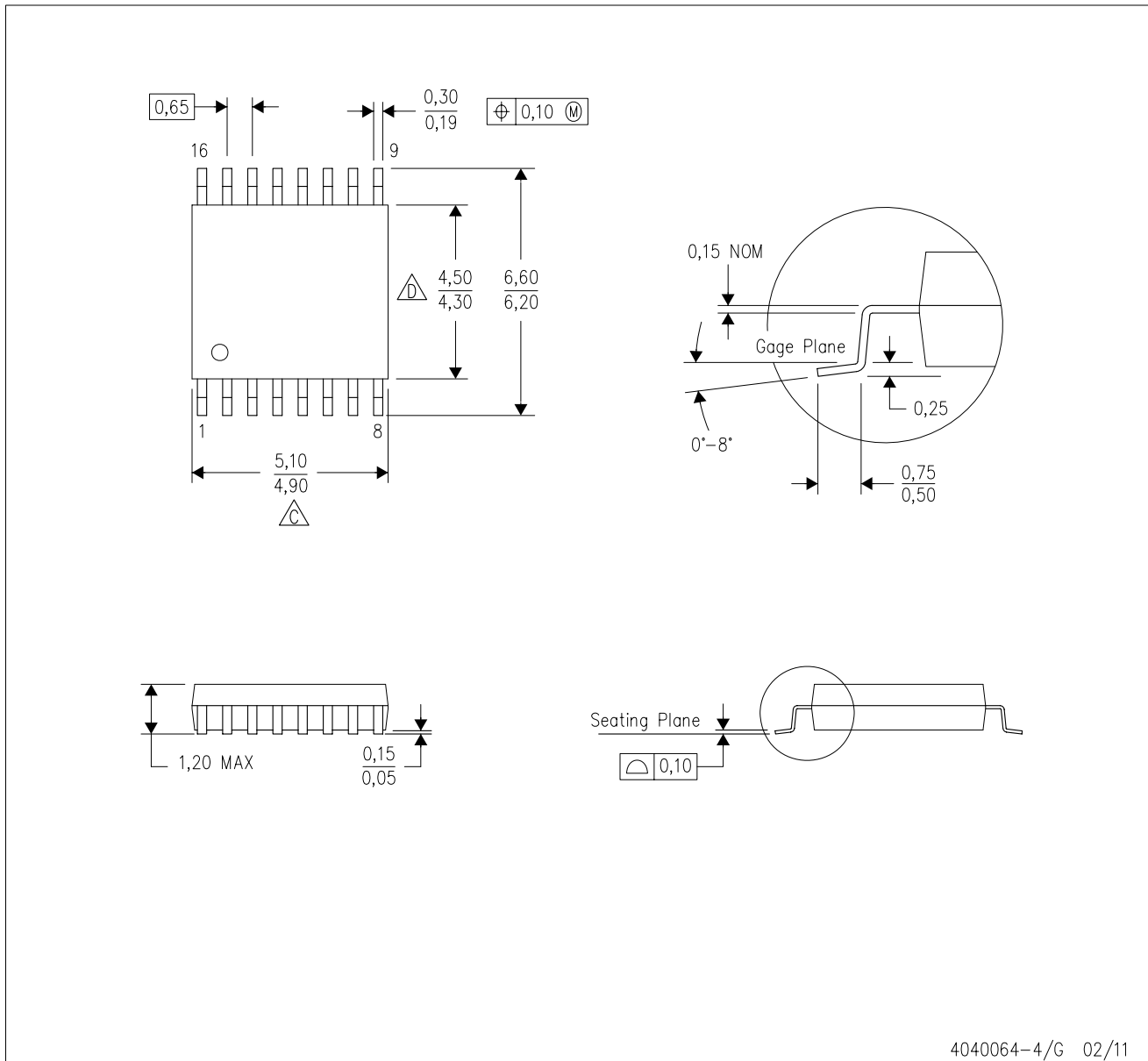
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MS-013 variation AA.

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE

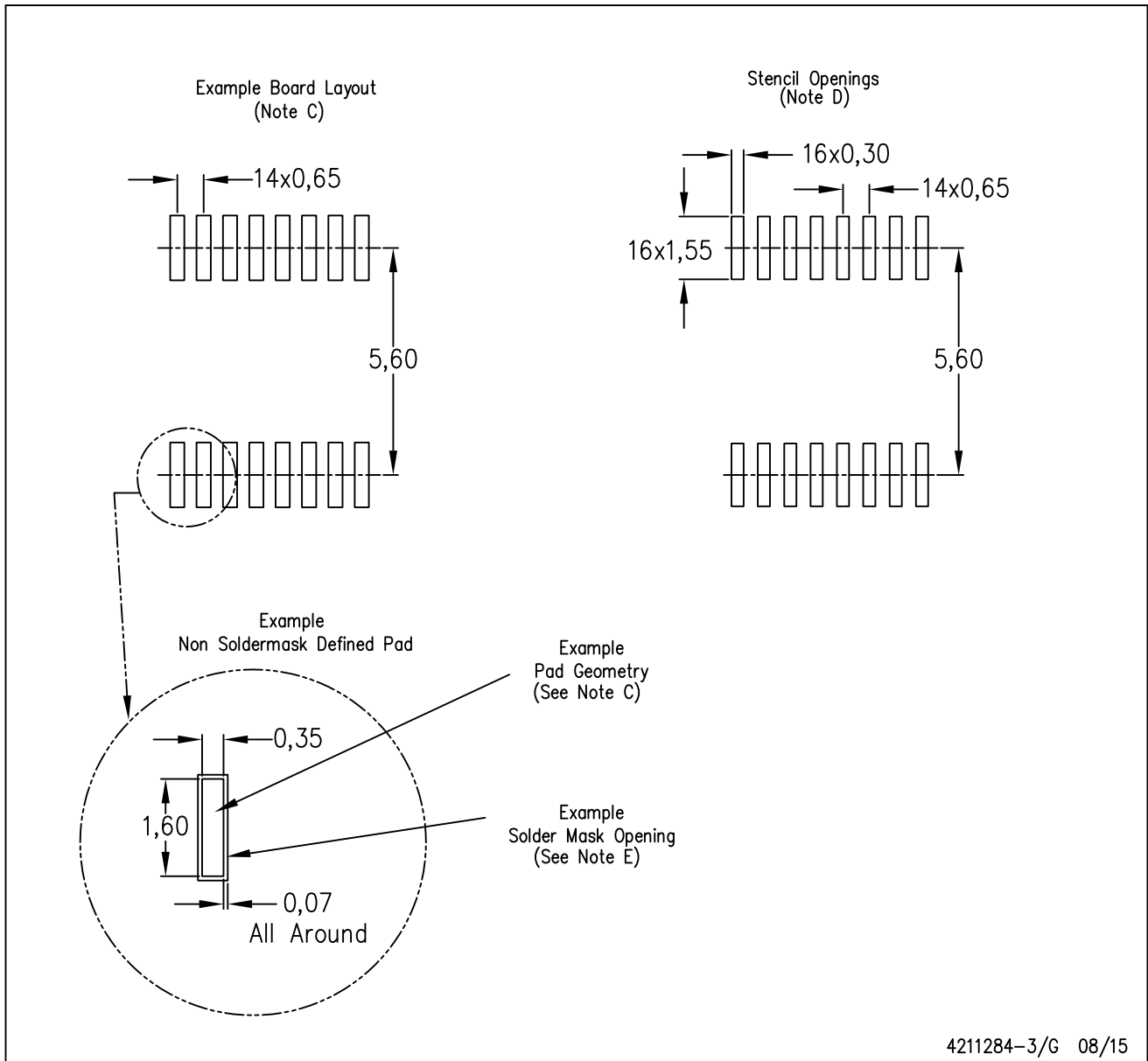


4040064-4/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

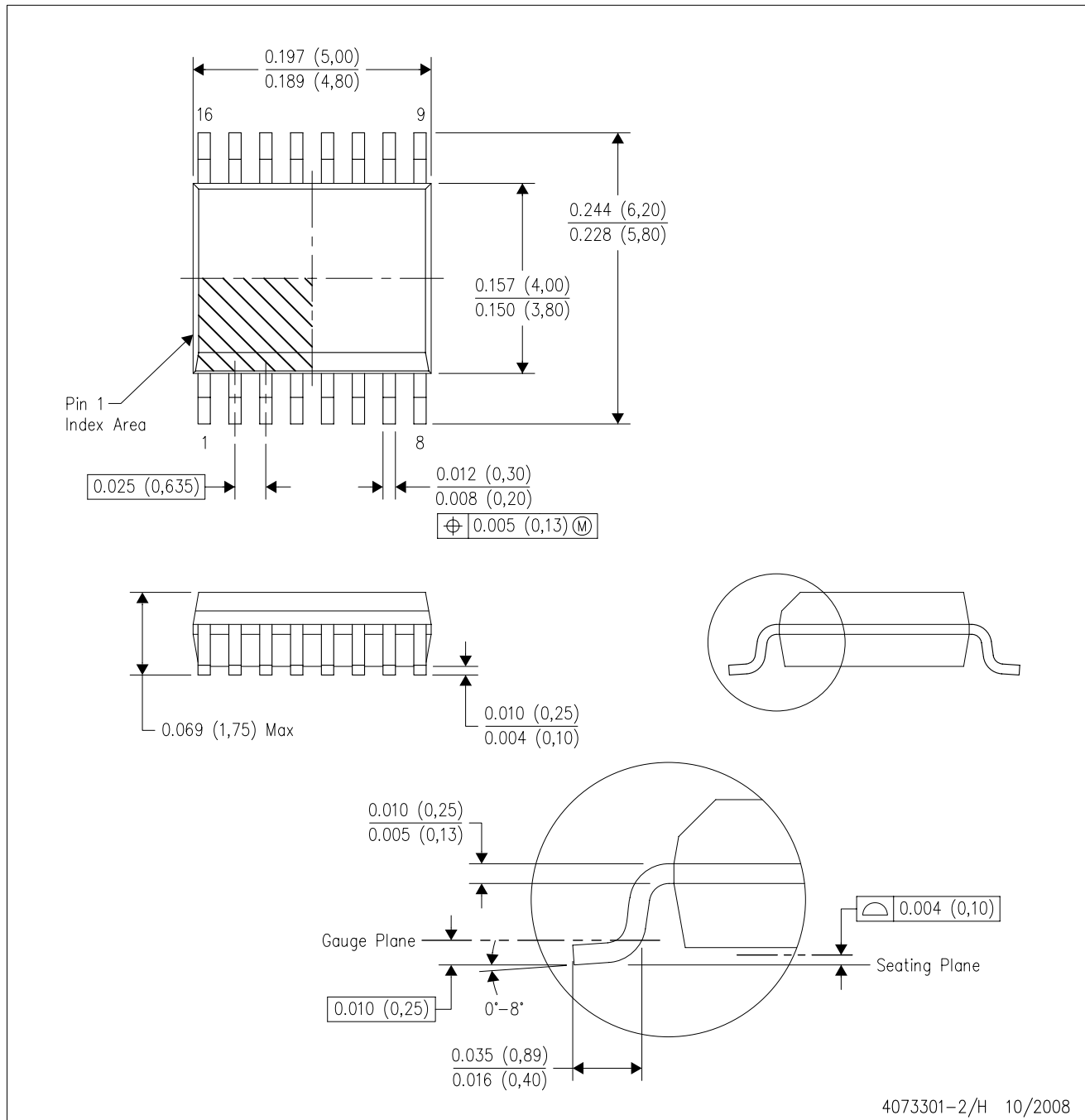
28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

DBQ (R-PDSO-G16)

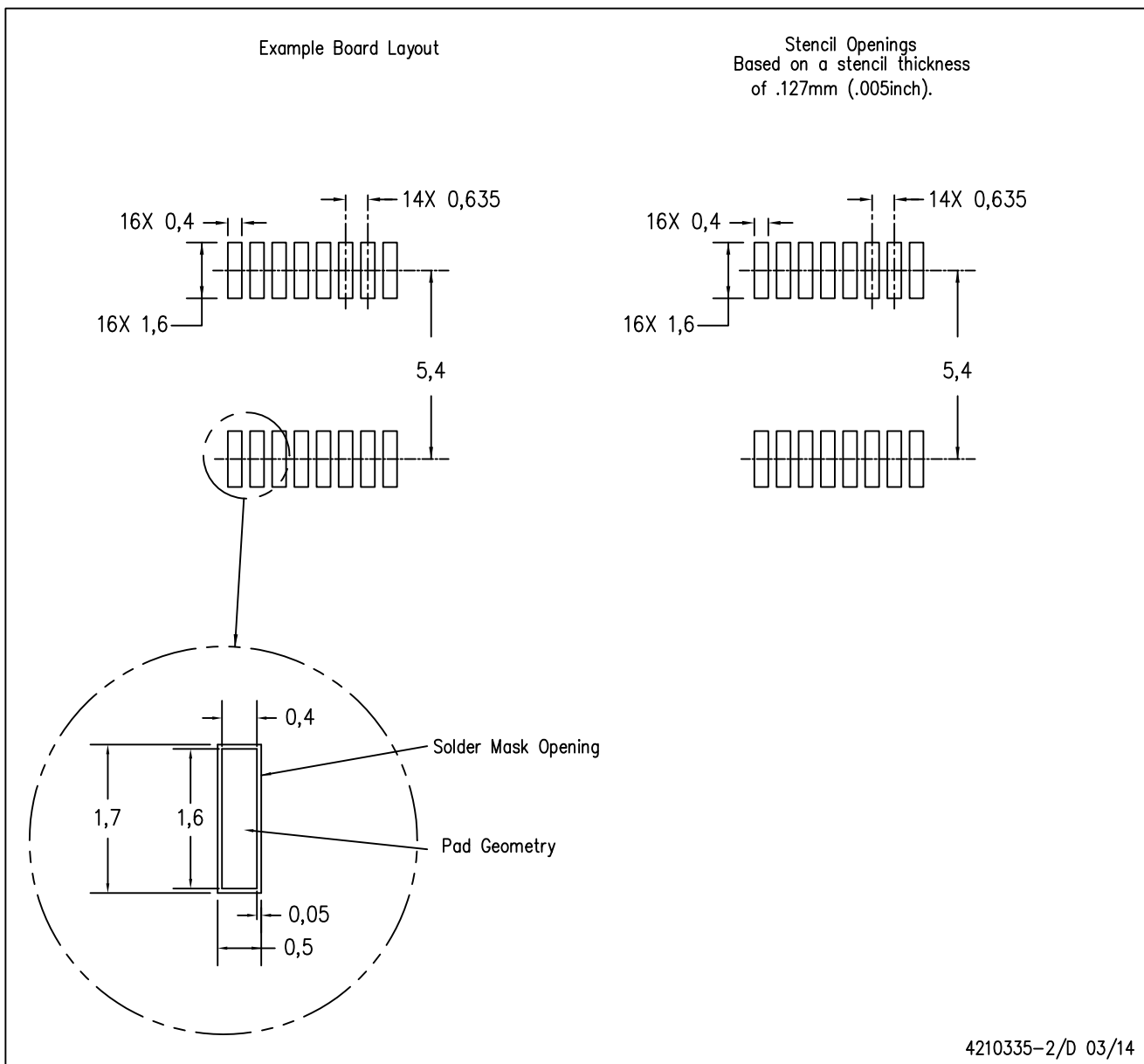
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
  - D. Falls within JEDEC MO-137 variation AB.

DBQ (R-PDSO-G16)

PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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