

MITSUBISHI LSTTLs M74LS669P

SYNCHRONOUS PRESETTABLE UP/DOWN 4-BIT BINARY COUNTER

DESCRIPTION

The M74LS669P is a semiconductor integrated circuit containing a synchronous 4-bit binary counter function with an up/down control input and preset input.

FEATURES

- Fully synchronous operation for counting and programming
- Integral look-ahead for counting
- Carry output for n bit cascading
- Fully independent clock circuit
- Up/down control input provided
- Preset input provided

APPLICATION

General purpose, for use in industrial and consumer equipment

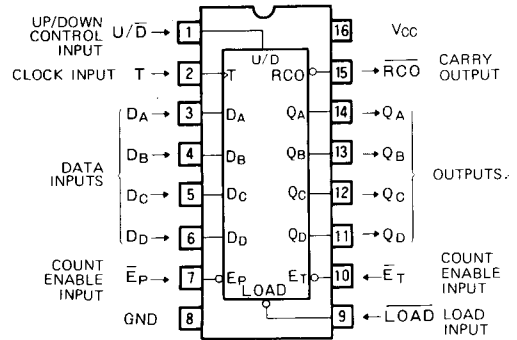
FUNCTIONAL DESCRIPTION

This device operates with the preset, up/down control and enable function synchronized to the rising edge of the clock pulse.

Data is acquisitioned from outputs Q_A thru Q_D on the rising edge of clock input T, synchronized with (and in response to) data input at D_A thru D_D ; and occurs after preset is initiated by dropping load input (\overline{LOAD}) to a low-level.

Up/down counter operations are initiated when \overline{LOAD} is high-level, and the count enable input ($\overline{E_P}$ and $\overline{E_T}$) is low-

PIN CONFIGURATION (TOP VIEW)



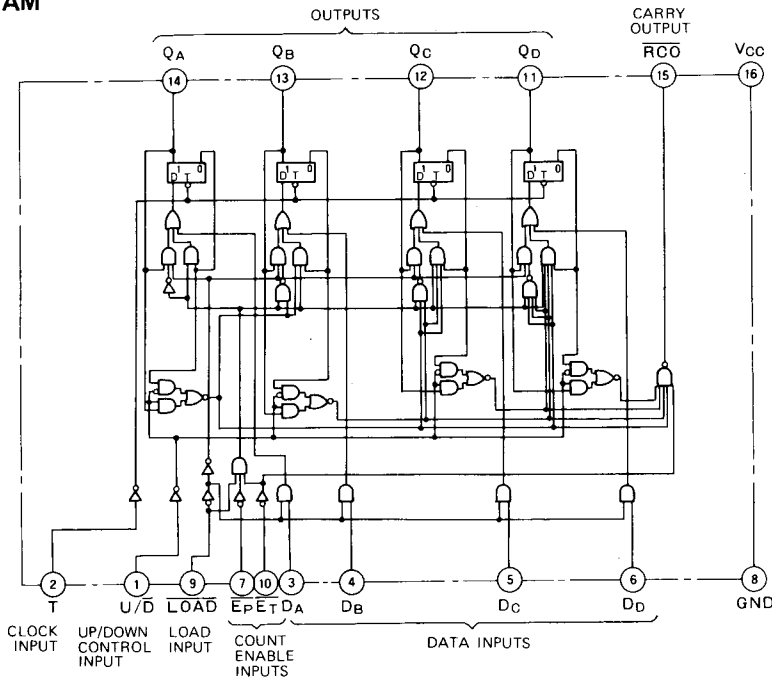
Outline 16P4

level. The counter increments (up) when control input U/\overline{D} is high-level, and decrements (down) at low-level.

Carry output (\overline{RCO}) goes low-level (active) at 15_2 during up operations, and at 0_2 while the count is going down. The synchronous feature of the counter permits it to be cascaded for use as a binary counter. (See the application example given for M74LS668P.)

Counter operations are inhibited when \overline{LOAD} and ($\overline{E_P}$ or $\overline{E_T}$) are all high-level.

BLOCK DIAGRAM



SYNCHRONOUS PRESETTABLE UP/DOWN 4-BIT BINARY COUNTER

FUNCTION TABLE (Note 1)

LOAD	$\overline{E_P}$	$\overline{E_T}$	U/D	T	Q _A	Q _B	Q _C	Q _D	RCO*
L	X	X	X	↑	D _A	D _B	D _C	D _D	H
H	L	L	H	↑	COUNT UP				H
H	L	L	L	↑	COUNT DOWN				H
H	H	X	X	X	COUNT INHIBIT				H
H	X	H	X	X					

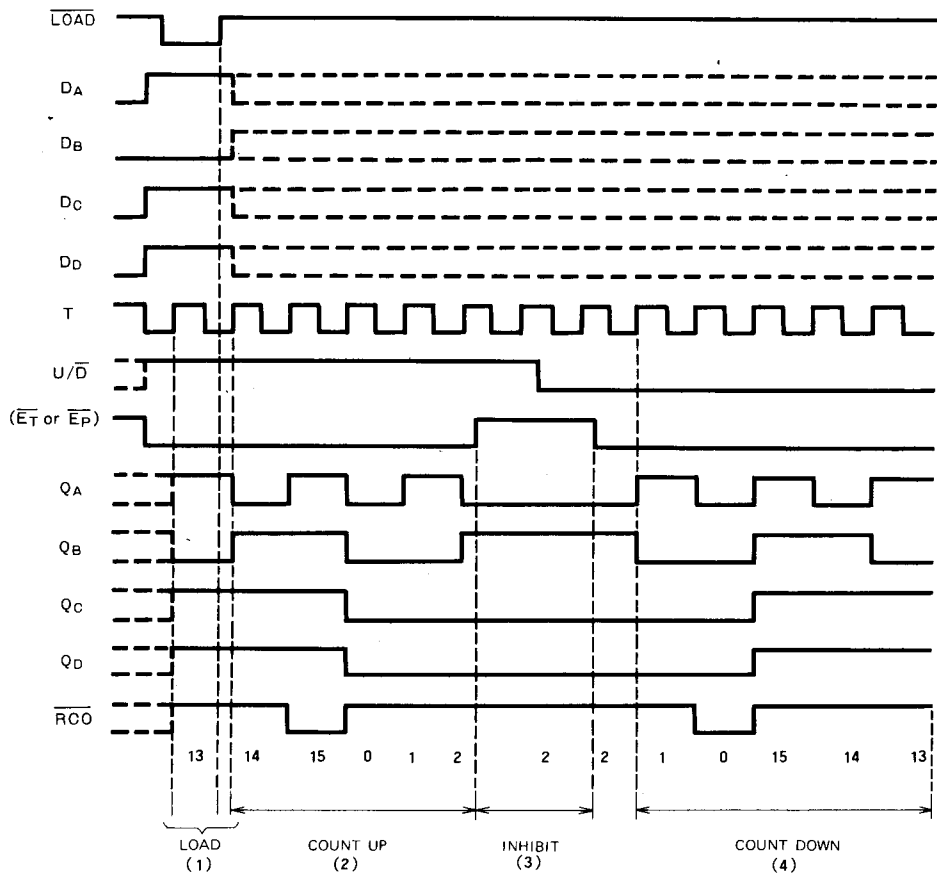
Note 1. ↑ : Transition from low to high
X : Irrelevant

* : RCO is normally at high-level, however, when $\overline{E_T}$ is low and the counter is incrementing, Q_A, Q_B, Q_C and Q_D will be high, and RCO will be low. Also, when the counter is decrementing, Q_A, Q_B, Q_C and Q_D will be low, and RCO will also be low.

$$\overline{RCO} = Q_A \cdot Q_B \cdot Q_C \cdot Q_D \cdot (U/\overline{D}) \cdot \overline{E_T}$$

$$\overline{RCO} = \overline{Q_A} \cdot \overline{Q_B} \cdot \overline{Q_C} \cdot \overline{Q_D} \cdot (U/\overline{D}) \cdot \overline{E_T}$$

TIMING DIAGRAM



Timing diagram notes:
 (1) Preset at 13
 (2) Increment at 14, 15, 0, 1, 2
 (3) Count inhibit
 (4) Decrement at 1, 0, 15, 14, 13

SYNCHRONOUS PRESETTABLE UP/DOWN 4-BIT BINARY COUNTER

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		$-0.5 \sim +7$	V
V_I	Input voltage		$-0.5 \sim +15$	V
V_O	Output voltage	High-level state	$-0.5 \sim V_{CC}$	V
T_{opr}	Operating free-air ambient temperature range		$-20 \sim +75$	$^\circ\text{C}$
T_{stg}	Storage temperature range		$-65 \sim +150$	$^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geq 2.7\text{V}$	0		-400	μA
I_{OL}	Low-level output current	$V_{OL} \leq 0.4\text{V}$	0		4	mA
		$V_{OL} \leq 0.5\text{V}$	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage		$V_{CC} = 4.75\text{V}$, $I_{IC} = -18\text{mA}$			-1.5	V
V_{OH}	High-level output voltage		$V_{CC} = 4.75\text{V}$, $V_I = 0.8\text{V}$ $V_I = 2\text{V}$, $I_{OH} = -400\mu\text{A}$	2.7	3.4		V
V_{OL}	Low-level output voltage		$V_{CC} = 4.75\text{V}$ $V_I = 0.8\text{V}$, $V_I = 2\text{V}$	$I_{OL} = 4\text{mA}$	0.25	0.4	V
				$I_{OL} = 8\text{mA}$	0.35	0.5	V
I_{IH}	High-level input current	$D_A, D_B, D_C, D_D, \overline{E_P}, U/\overline{D}$	$V_{CC} = 5.25\text{V}$, $V_I = 2.7\text{V}$			20	μA
		$T, \overline{E_T}$				20	
		LOAD				40	
I_{IH}	High-level input current	$D_A, D_B, D_C, D_D, \overline{E_P}, U/\overline{D}$	$V_{CC} = 5.25\text{V}$, $V_I = 10\text{V}$			0.1	mA
		$T, \overline{E_T}$				0.1	
		LOAD				0.2	
I_{IL}	Low-level input current	$D_A, D_B, D_C, D_D, \overline{E_P}, U/\overline{D}$	$V_{CC} = 5.25\text{V}$, $V_I = 0.4\text{V}$			-0.4	mA
		$T, \overline{E_T}$				-0.4	
		LOAD				-0.8	
I_{OS}	Short-circuit output current (Note 2)		$V_{CC} = 5.25\text{V}$, $V_O = 0\text{V}$	-20		-100	mA
I_{CC}	Supply current		$V_{CC} = 5.25\text{V}$ (Note 3)		20	34	mA

* All typical values are at $V_{CC} = 5\text{V}$, $T_a = 25^\circ\text{C}$.

Note 2. All measurements should be done quickly, and not more than one output should be shorted at a time.

3. I_{CC} is measured after applying a momentary 4.5V, then ground, to the clock input with all other inputs grounded.

SYNCHRONOUS PRESETTABLE UP/DOWN 4-BIT BINARY COUNTER

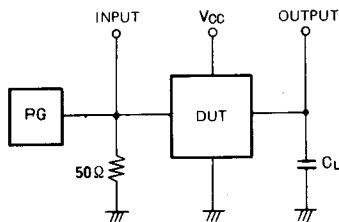
SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25^\circ C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	$C_L = 15pF$ (Note 4)	25	30		MHz
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input T to output \overline{RCO}			24	40	ns
t_{PHL}				32	60	
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input T to outputs Q_A , Q_B , Q_C , and Q_D			20	27	ns
t_{PHL}				15	27	
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{E_T}$ to output \overline{RCO}			10	17	ns
t_{PHL}				28	45	
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input U/\overline{D} to output \overline{RCO}			25	35	ns
t_{PHL}				20	40	

TIMING REQUIREMENTS ($V_{CC}=5V$, $T_a=25^\circ C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_w	Clock T pulse width		25	12		ns
$t_{su(D)}$	Setup time $D_A \sim D_D$ to T		20	18		ns
$t_{su(E)}$	Setup time $\overline{E_T}$, $\overline{E_P}$ to T		35	26		ns
$t_{su(LOAD)}$	Setup time \overline{LOAD} to T		25	15		ns
$t_{su(U/\overline{D})}$	Setup time U/\overline{D} to T		30	20		ns
t_h	Setup time of all inputs to T		0	-15		ns

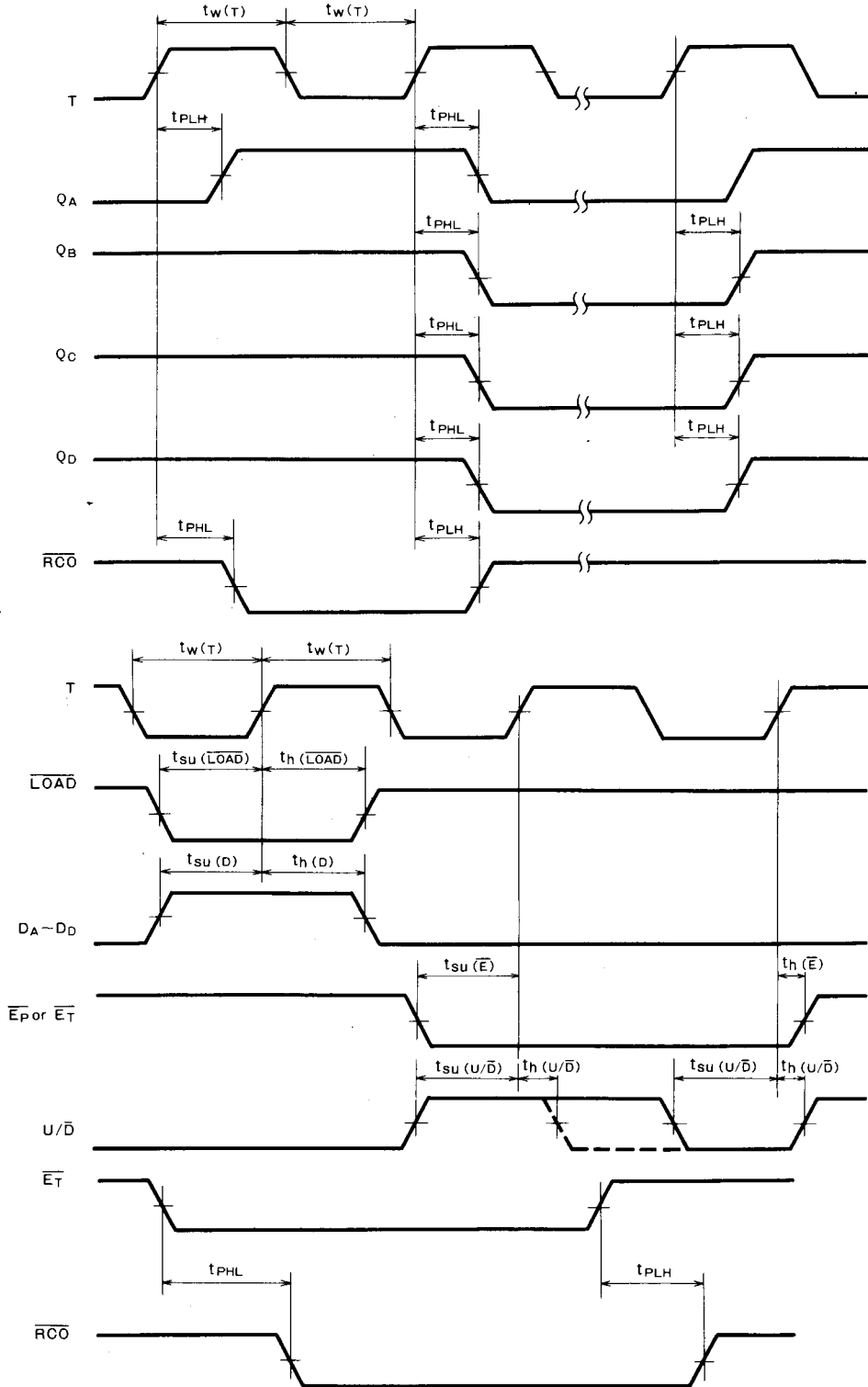
Note 4. Measurement Circuit



- (1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, $t_r = 6ns$, $t_f = 6ns$, $t_w = 500ns$, $V_p = 3V_{p-p}$, $Z_o = 50\Omega$.
- (2) C_L includes probe and jig capacitance.

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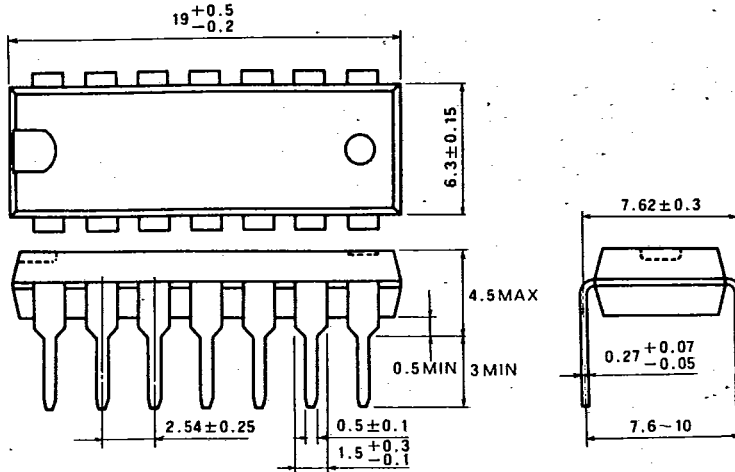
TIMING DIAGRAM (Reference level = 1.3V)



T-90-20

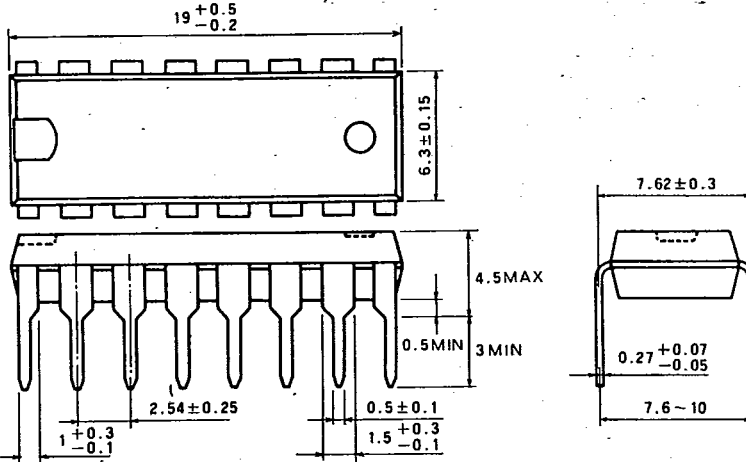
TYPE 14P4 14-PIN MOLDED PLASTIC DIL

Dimension in mm



TYPE 16P4 16-PIN MOLDED PLASTIC DIL

Dimension in mm



TYPE 20P4 20-PIN MOLDED PLASTIC DIL

Dimension in mm

