



### FEATURES

- Fully integrated, single-lead ECG front end
- Low quiescent supply current: 50  $\mu$ A (typical)
- Leads on/off detection while in shutdown (<1  $\mu$ A)
- Common-mode rejection ratio: 80 dB (dc to 60 Hz)
- 2 electrode and 3 electrode configurations
- High signal gain ( $G = 100$ ) with dc blocking capabilities
- 2-pole adjustable high-pass filter
- Accepts up to  $\pm 300$  mV of half cell potential
- Fast restore feature improves filter settling
- Uncommitted op amp
- 3-pole adjustable low-pass filter with adjustable gain
- Integrated RLD amplifier with shutdown
- Single-supply operation: 1.7 V to 3.5 V
- Integrated reference buffer generates virtual ground
- Rail-to-rail output
- Internal RFI filter
- 8 kV HBM ESD rating
- Shutdown pin
- 2 mm  $\times$  1.7 mm WLCSP package

### APPLICATIONS

- Fitness and activity heart rate monitors
- Portable ECG
- Wearable and remote health monitors
- Gaming peripherals
- Biopotential signal acquisition, such as EMG or EEG

### GENERAL DESCRIPTION

The AD8233 is an integrated signal conditioning block for electrocardiogram (ECG) and other biopotential measurement applications. It is designed to extract, amplify, and filter small biopotential signals in the presence of noisy conditions, such as those created by motion or remote electrode placement. This design allows an ultralow power analog-to-digital converter (ADC) or an embedded microcontroller to easily acquire the output signal.

The AD8233 implements a two-pole, high-pass filter for eliminating motion artifacts and the electrode half cell potential. This filter is tightly coupled with the instrumentation amplifier architecture to allow both large gain and high-pass filtering in a single stage, thereby saving space and cost.

An uncommitted operational amplifier enables the AD8233 to create a three-pole, low-pass filter to remove additional noise. The user can select the frequency cutoff of all filters to suit different types of applications.

### FUNCTIONAL BLOCK DIAGRAM

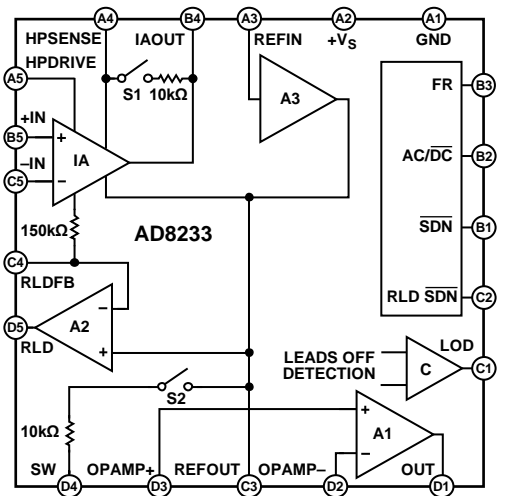


Figure 1. 20-Ball WLCSP

To improve the common-mode rejection of the line frequencies in the system and other undesired interferences, the AD8233 includes a right leg drive (RLD) amplifier for driven electrode applications.

The AD8233 includes a fast restore function that reduces the duration of the otherwise long settling tails of the high-pass filters. After an abrupt signal change that rails the amplifier (such as a leads off condition), the AD8233 automatically adjusts to a higher filter cutoff. This feature allows the AD8233 to recover quickly, and therefore, to take valid measurements soon after connecting the electrodes to the subject.

The AD8233 is available in a 2 mm  $\times$  1.7 mm, 20-ball WLCSP package and a 150  $\mu$ m thin die for height constrained applications. Performance is specified from 0°C to 70°C and is operational from -40°C to +85°C.

The AD8233 has several improvements over the AD8232, which are detailed in Table 1.

Table 1. AD8232 vs. AD8233 Comparison

Parameter	AD8232	AD8233
Supply Current	170 $\mu$ A	50 $\mu$ A
Peak-to-Peak Voltage Noise (f = 0.5 Hz to 40 Hz)	14 $\mu$ V p-p	8.5 $\mu$ V
Leads On or Off Detection in Shutdown	Not included	Included
Right Leg Drive Shutdown	Not included	Included
Package Size	4 mm $\times$ 4 mm $\times$ 0.75 mm	2 mm $\times$ 1.7 mm $\times$ 0.5 mm or 0.15 mm

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## REVISION HISTORY

### 10/2018—Rev. 0 to Rev. A

Added 20-Pad Bare Die .....	Universal
Changes to Features Section and General Description Section.....	1
Change to Table 1 .....	1
Changes to Specifications Section and Table 2.....	3
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Added Measuring Surface Electromyography (EMG) or Electroencephalography (EEG) Section .....	26
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Renamed Synchronized ECG and PPG Measurement Section to Synchronous ECG and Photoplethysmography (PPG) Measurement Using Transimpedance Amplifier (TIA) ADC Mode Using the ADPD1080 Section .....	29
Changes to Synchronous ECG and Photoplethysmography (PPG) Measurement Using Transimpedance Amplifier (TIA) ADC Mode Using the ADPD1080 Section .....	29
Changes to Figure 79 Caption .....	29
Added Die Information Section, Figure 80, and Table 8, Renumbered Sequentially .....	30
Updated Outline Dimensions.....	31
Changes to Ordering Guide .....	32

### 8/2016—Revision 0: Initial Version

## SPECIFICATIONS

+V<sub>S</sub> = 1.8 V to 3 V ± 5.5%, voltage at REFIN pin (V<sub>REF</sub>) = +V<sub>S</sub>/2, V<sub>CM</sub> = +V<sub>S</sub>/2, T<sub>A</sub> = 25°C, FR = low,  $\overline{\text{SDN}}$  = high, AC/DC = low, RLD  $\overline{\text{SDN}}$  = low, unless otherwise noted. The AD8233C-DF is only characterized at 25°C.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
<b>INSTRUMENTATION AMPLIFIER</b>						
Common-Mode Rejection Ratio, DC to 60 Hz	CMRR	Input common-mode voltage (V <sub>CM</sub> ) = 0.35 V to +V <sub>S</sub> – 150 mV, dc differential input range (V <sub>DIFF</sub> ) = 0 V V <sub>CM</sub> = 0.35 V to +V <sub>S</sub> – 150 mV, V <sub>DIFF</sub> = ±0.3 V	80	86		dB
Power Supply Rejection Ratio	PSRR	+V <sub>S</sub> = 1.8 V to 3.5 V	76	80		dB
Offset Voltage (Referred to Input (RTI))	V <sub>OS</sub>			90		dB
Instrumentation Amplifier Inputs				1	6	mV
DC Blocking Input <sup>1</sup>				25		μV
Average Offset Drift				2		μV/°C
Instrumentation Amplifier Inputs				0.05		μV/°C
DC Blocking Input <sup>1</sup>						
Input Bias Current	I <sub>B</sub>	T <sub>A</sub> = 0°C to 70°C		50	200	pA
Input Offset Current	I <sub>OS</sub>	T <sub>A</sub> = 0°C to 70°C		1		nA
Input Impedance				25	100	pA
Differential				1		nA
Common Mode						
Input Voltage Noise (RTI)				10  7.5		GΩ  pF
Spectral Noise Density		f = 1 kHz		5  15		GΩ  pF
Peak-to-Peak Voltage Noise		f = 0.1 Hz to 10 Hz				
		f = 0.5 Hz to 40 Hz				
Input Voltage Range		T <sub>A</sub> = 0°C to 70°C	0.2		+V <sub>S</sub>	V
DC Differential Input Range	V <sub>DIFF</sub>		–300		+300	mV
Output						
Output Swing		Output load resistor (R <sub>L</sub> ) = 50 kΩ	0.1		+V <sub>S</sub> – 0.1	V
Short-Circuit Current	I <sub>OUT</sub>			6.3		mA
Gain	A <sub>V</sub>			100		V/V
Gain Error		V <sub>DIFF</sub> = 0 V		0.4		%
		V <sub>DIFF</sub> = –300 mV to +300 mV		1	4	%
Average Gain Drift		T <sub>A</sub> = 0°C to 70°C		12		ppm/°C
Bandwidth	BW			1		kHz
Radio Frequency Interference (RFI) Filter Cutoff (Each Input)				1		MHz
<b>OPERATIONAL AMPLIFIER (A1)</b>						
Offset Voltage	V <sub>OS</sub>			1	5	mV
Average Temperature Coefficient	TC	T <sub>A</sub> = 0°C to 70°C		1		μV/°C
Input Bias Current	I <sub>B</sub>	T <sub>A</sub> = 0°C to 70°C		100		pA
Input Offset Current	I <sub>OS</sub>	T <sub>A</sub> = 0°C to 70°C		1		nA
Input Offset Current	I <sub>OS</sub>	T <sub>A</sub> = 0°C to 70°C		100		pA
Input Offset Current	I <sub>OS</sub>	T <sub>A</sub> = 0°C to 70°C		1		nA
Input Voltage Range			0.1		+V <sub>S</sub> – 0.1	V
Common-Mode Rejection Ratio	CMRR	V <sub>CM</sub> = 0.5 V to +V <sub>S</sub> – 0.5 V		100		dB
Power Supply Rejection Ratio	PSRR			100		dB
Large Signal Voltage Gain	A <sub>VO</sub>			110		dB
Output Voltage Range		R <sub>L</sub> = 50 kΩ	0.1		+V <sub>S</sub> – 0.1	V
Short-Circuit Current Limit	I <sub>OUT</sub>			12		mA

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Gain Bandwidth Product	GBP			15		kHz
Slew Rate	SR			0.01		V/ $\mu$ s
Voltage Noise Density (RTI)	$e_n$	$f = 1$ kHz		120		nV/ $\sqrt{\text{Hz}}$
Peak-to-Peak Voltage Noise (RTI)	$e_{n\text{ p-p}}$	$f = 0.1$ Hz to 10 Hz $f = 0.5$ Hz to 40 Hz		7 9		$\mu$ V p-p $\mu$ V p-p
<b>RIGHT LEG DRIVE AMPLIFIER (A2)</b>						
Quiescent Supply Current		$R_L = 50$ k $\Omega$		7.5	10	$\mu$ A
Output Swing			0.1		$+V_S - 0.1$	V
Short-Circuit Current	$I_{\text{OUT}}$			11		mA
Integrator Input Resistor			120	150	180	k $\Omega$
Gain Bandwidth Product	GDP			20		kHz
<b>REFERENCE BUFFER (A3)</b>						
Offset Error	$V_{\text{OS}}$	$R_L > 50$ k $\Omega$		1		mV
Input Bias Current	$I_B$			100		pA
Short-Circuit Current Limit	$I_{\text{OUT}}$			12		mA
Voltage Range		$R_L = 50$ k $\Omega$	0.1		$+V_S - 0.7$	V
<b>DC LEADS OFF COMPARATORS</b>						
Threshold Voltage				$+V_S - 0.27$		V
Hysteresis				125		mV
Propagation Delay				1.5		$\mu$ s
<b>AC LEADS OFF DETECTOR</b>						
Square Wave Frequency	$f_{\text{AC}}$		50	100	175	kHz
Square Wave Amplitude	$I_{\text{AC}}$			200		nA p-p
Input Currents in Shutdown Mode <sup>2</sup>	$I_{\text{DC}}$	$+IN, \overline{SDN} = \text{low}$ $-IN, \overline{SDN} = \text{low}$		250 -300		nA nA
Impedance Threshold		Between $+IN$ and $-IN, \overline{SDN} = \text{high}$	10	20		M $\Omega$
Detection Delay				100		$\mu$ s
<b>FAST RESTORE CIRCUIT</b>						
Switches		S1 and S2				
On Resistance	$R_{\text{ON}}$		8	10	12	k $\Omega$
Off Leakage				100		pA
Window Comparator						
Threshold Voltage		From either rail		100		mV
Propagation Delay				2		$\mu$ s
Switch Timing Characteristics						
Feedback Recovery Switch On Time	$t_{\text{S1}}$	$+V_S = 3$ V $+V_S = 1.8$ V		160 80		ms
Filter Recovery Switch On Time	$t_{\text{S2}}$	$+V_S = 3$ V $+V_S = 1.8$ V		80 40		ms
Fast Restore Reset	$t_{\text{RST}}$	$+V_S = 3$ V $+V_S = 1.8$ V		3 1.5		$\mu$ s

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
<b>LOGIC INTERFACE</b>						
Input Characteristics						
Input Voltage ( $\overline{AC/DC}$ , FR, and RLD $\overline{SDN}$ )						
Low	$V_{IL}$			$0.41 \times +V_S$		V
High	$V_{IH}$			$0.45 \times +V_S$		V
Input Voltage ( $\overline{SDN}$ )						
Low	$V_{IL}$			$0.6 \times +V_S$		V
High	$V_{IH}$			$0.3 \times +V_S$		V
Output Characteristics						
Output Voltage						
Low	$V_{OL}$	LOD terminal $R_L = 100 \text{ k}\Omega$		0.05		V
High	$V_{OH}$			$+V_S - 0.05$		V
<b>SYSTEM SPECIFICATIONS</b>						
Quiescent Supply Current				50	70	$\mu\text{A}$
		$T_A = 0^\circ\text{C to } 70^\circ\text{C}$		60		$\mu\text{A}$
Wakeup Current		$\overline{SDN} = \text{low}, \text{LOD} = \text{low}$		0.65	1.5	$\mu\text{A}$
		$T_A = 0^\circ\text{C to } 70^\circ\text{C}$		0.75		$\mu\text{A}$
Shutdown Current		$\overline{SDN} = \text{low}, \text{LOD} = \text{high}$		0.5	1	$\mu\text{A}$
		$T_A = 0^\circ\text{C to } 70^\circ\text{C}$		0.6		$\mu\text{A}$
Peak-to-Peak Voltage Noise (RTI)						
		$V_{\text{DIFF}} = 0 \text{ V}$				
		$f = 0.5 \text{ Hz to } 40 \text{ Hz}$		9		$\mu\text{V p-p}$
		$f = 0.05 \text{ Hz to } 150 \text{ Hz}$		15		$\mu\text{V p-p}$
		$V_{\text{DIFF}} = \pm 0.3 \text{ V}$				
		$f = 0.5 \text{ Hz to } 40 \text{ Hz}$		11		$\mu\text{V p-p}$
		$f = 0.05 \text{ Hz to } 150 \text{ Hz}$		21		$\mu\text{V p-p}$
Supply Range			1.7		3.5	V
Specified Temperature Range			0		70	$^\circ\text{C}$
Operational Temperature Range			-40		+85	$^\circ\text{C}$

<sup>1</sup> Offset is referred to the input of the instrumentation amplifier inputs.

<sup>2</sup> In ac leads off and shutdown mode, the dc leads off comparator at the +IN pin trips the LOD pin.

## ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	3.6V
Output Short-Circuit Current Duration	Indefinite
Maximum Voltage, Any Terminal <sup>1</sup>	+Vs + 0.3 V
Minimum Voltage, Any Terminal <sup>1</sup>	-0.3 V
Storage Temperature Range	-65°C to +125°C
Operating Temperature Range	-40°C to +85°C
Maximum Junction Temperature	140°C
Electrostatic Discharge (ESD) Rating	
Human Body Model (HBM)	8 kV
Field Induced Charged Device Model (FICDM)	1 kV

<sup>1</sup> This level or the maximum specified supply voltage, whichever is the lesser, indicates the superior voltage limit for any terminal. If input voltages beyond the specified minimum or maximum voltages are expected, place resistors in series with the inputs to limit the current to less than 5 mA.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Table 4. Thermal Resistance

Package Type	PCB	Power (W)	$\theta_{JA}$ (°C/W)			$\theta_{JC}$ (°C/W)
			0 ms	1 ms	2 ms	
CP-20-13	1S0P <sup>1</sup>	0.25	108.5	89.0	82.3	0.6
		1.25	101.1	87.3	87.3	0.6
	2S2P <sup>2</sup>	0.25	47.9	43.4	42.1	0.7
		1.25	46.8	43.3	42.1	0.7

<sup>1</sup> Simulated thermal numbers per JE51-9: 1-layer PCB (1S0P), low effective thermal conductivity test board.

<sup>2</sup> 4-layer PCB (2S2P), high effective thermal conductivity test board.

## ESD CAUTION



### ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

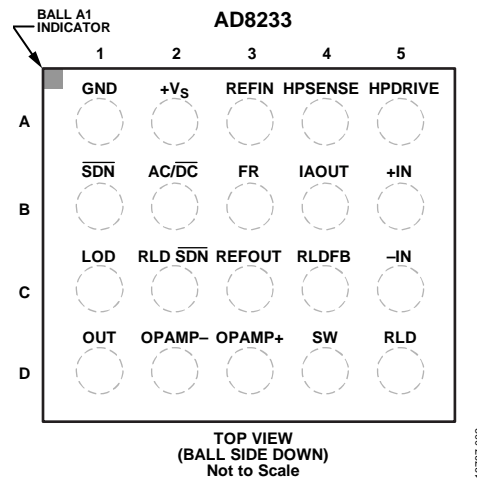


Figure 2. 20-Ball WLCSP Pin Configuration

Table 5. 20-Ball WLCSP Pin Function Descriptions

Ball No.	Mnemonic	Description
A1	GND	Power Supply Ground.
A2	+Vs	Power Supply Terminal.
A3	REFIN	Reference Buffer Input. Use REFIN, a high impedance input terminal, to set the level of the reference buffer.
A4	HPSENSE	High-Pass Sense Input for Instrumentation Amplifier. Connect HPSENSE to the junction of R and C that sets the corner frequency of the dc blocking circuit.
A5	HPDRIVE	High-Pass Driver Output. Connect HPDRIVE to the capacitor in the first high-pass filter. The AD8233 drives this pin to keep HPSENSE at the same level as the reference voltage.
B1	$\overline{\text{SDN}}$	Shutdown Control Input. Drive $\overline{\text{SDN}}$ low to enter the low power shutdown mode.
B2	$\overline{\text{AC/DC}}$	Leads Off Mode Control Input. Drive the $\overline{\text{AC/DC}}$ pin low for dc leads off mode. Drive the $\overline{\text{AC/DC}}$ pin high for ac leads off mode.
B3	FR	Fast Restore Control Input. Drive FR high to enable fast recovery mode. Otherwise, drive it low.
B4	IAOUT	Instrumentation Amplifier Output Terminal.
B5	+IN	Instrumentation Amplifier, Positive Input. +IN is typically connected to the left arm (LA) electrode.
C1	LOD	Leads Off Detection Comparator Output.
C2	$\overline{\text{RLD SDN}}$	Right Leg Drive Shutdown Control Input. Drive $\overline{\text{RLD SDN}}$ low to power down the RLD amplifier.
C3	REFOUT	Reference Buffer Output. The instrumentation amplifier output is referenced to this potential. Use REFOUT as a virtual ground for any point in the circuit that requires a signal reference.
C4	RLDFB	Right Leg Drive Feedback Input. RLDFB is the feedback terminal for the right leg drive circuit.
C5	-IN	Instrumentation Amplifier, Negative Input. -IN is typically connected to the right arm (RA) electrode.
D1	OUT	Operational Amplifier Output. The fully conditioned heart rate signal is present at this output. OUT can be connected to the input of an ADC.
D2	OPAMP-	Operational Amplifier Inverting Input.
D3	OPAMP+	Operational Amplifier Noninverting Input.
D4	SW	Fast Restore Switch Terminal. Connect this terminal to the output of the second high-pass filter.
D5	RLD	Right Leg Drive Output. Connect the driven electrode (typically right leg) to the RLD pin.

# TYPICAL PERFORMANCE CHARACTERISTICS

+V<sub>S</sub> = 3 V, V<sub>REF</sub> = 1.5 V, V<sub>CM</sub> = 1.5 V, T<sub>A</sub> = 25°C, unless otherwise noted. All typical performance characteristics are measured for the WLCSP package.

## INSTRUMENTATION AMPLIFIER PERFORMANCE CHARACTERISTICS

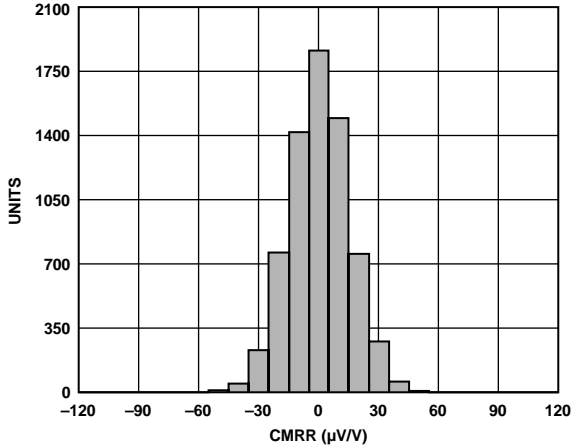


Figure 3. CMRR Distribution

13737-003

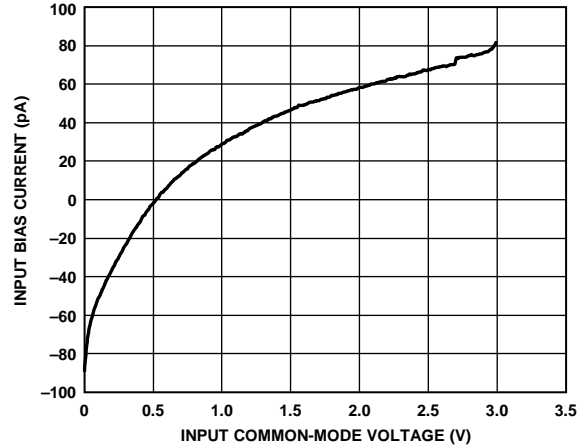


Figure 6. Input Bias Current vs. Input Common-Mode Voltage

13737-006

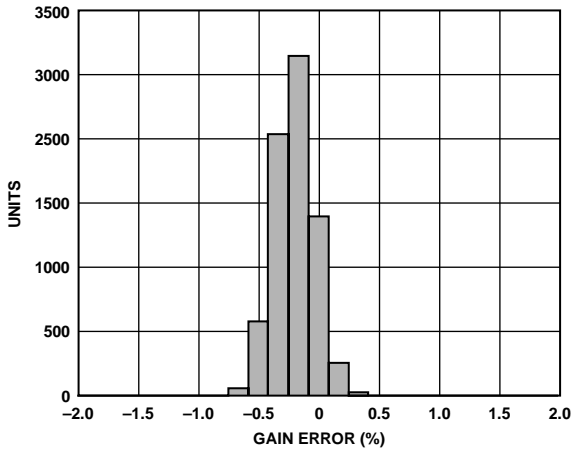


Figure 4. Gain Error Distribution

13737-004

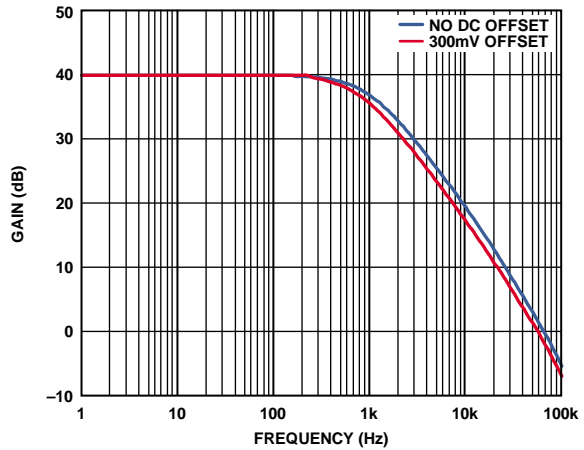


Figure 7. Gain vs. Frequency

13737-007

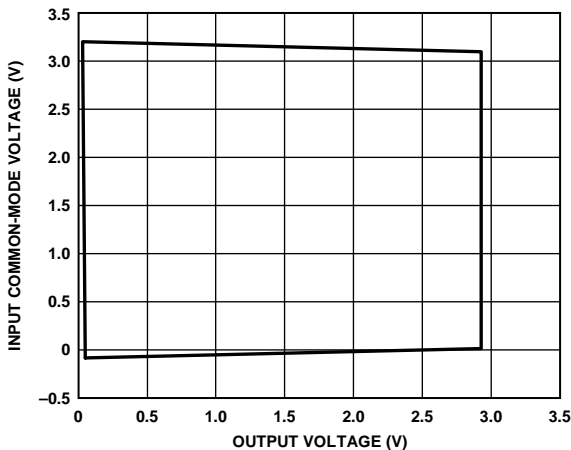


Figure 5. Input Common-Mode Voltage vs. Output Voltage

13737-005

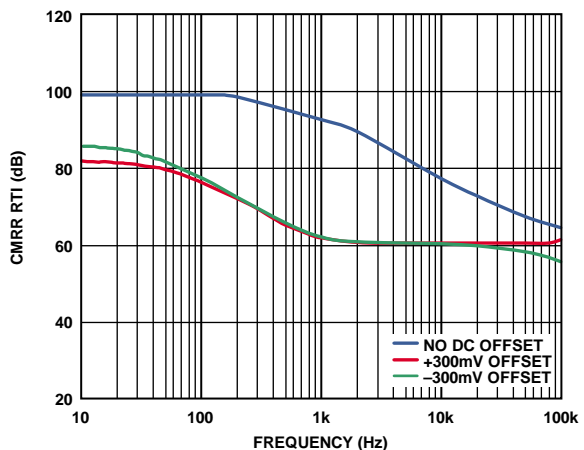


Figure 8. CMRR RTI vs. Frequency

13737-008



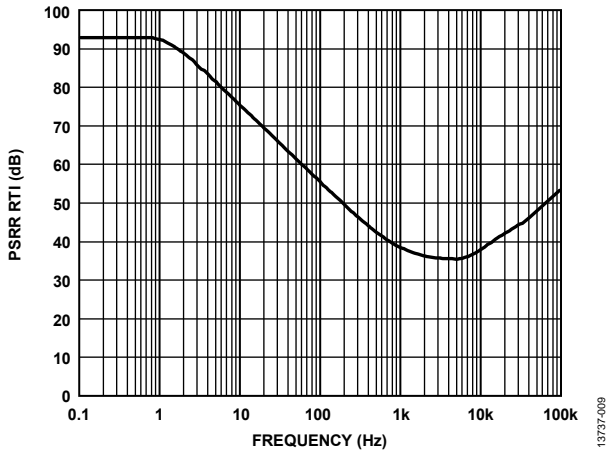


Figure 9. PSRR RTI vs. Frequency

13737-009

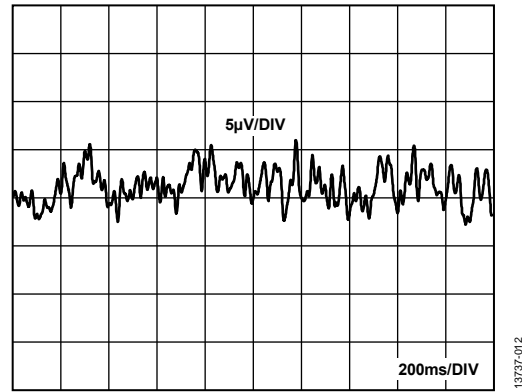


Figure 12. 0.5 Hz to 40 Hz Noise (RTI)

13737-012

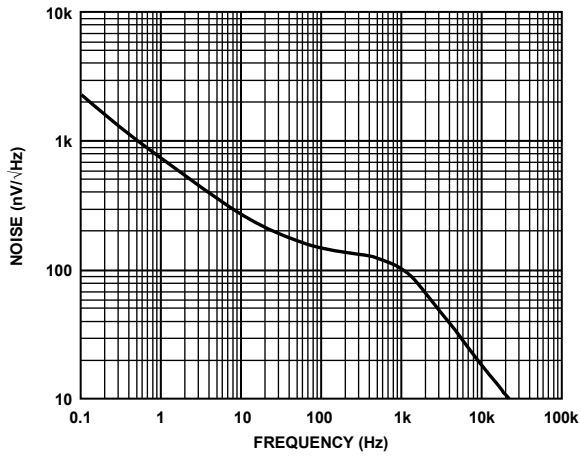


Figure 10. Voltage Noise Spectral Density (RTI)

13737-010

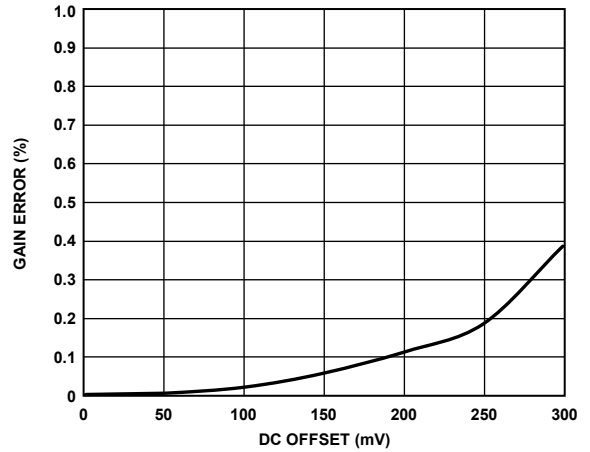


Figure 13. Gain Error vs. DC Offset

13737-013

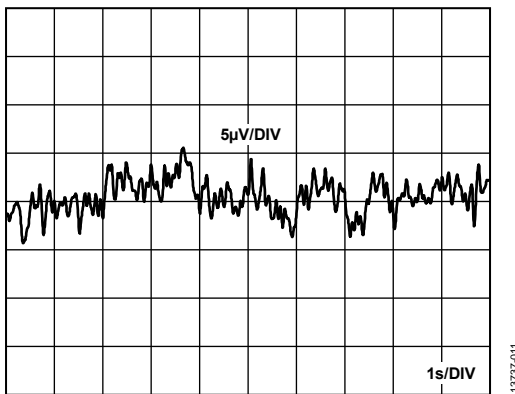


Figure 11. 0.1 Hz to 10 Hz Noise (RTI)

13737-011

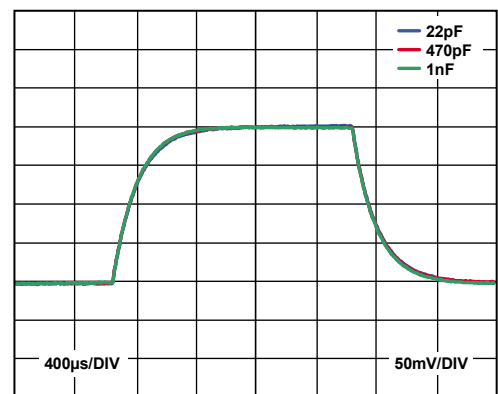


Figure 14. Small Signal Pulse Response

13737-014

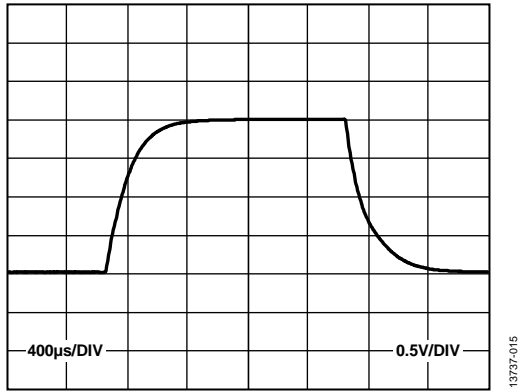


Figure 15. Large Signal Pulse Response

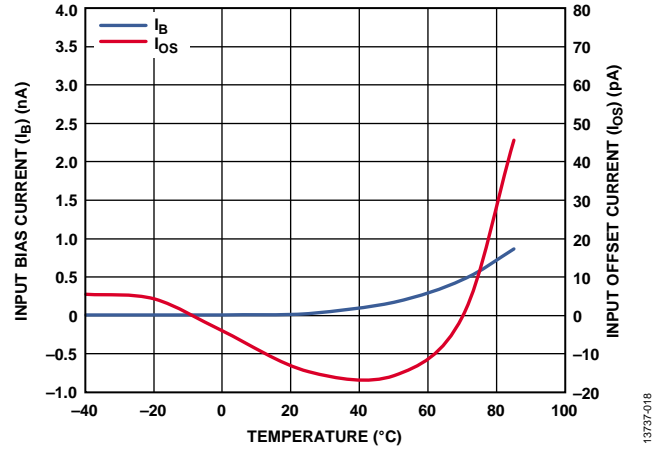


Figure 18. Input Bias Current ( $I_b$ ) and Input Offset Current ( $I_{os}$ ) vs. Temperature

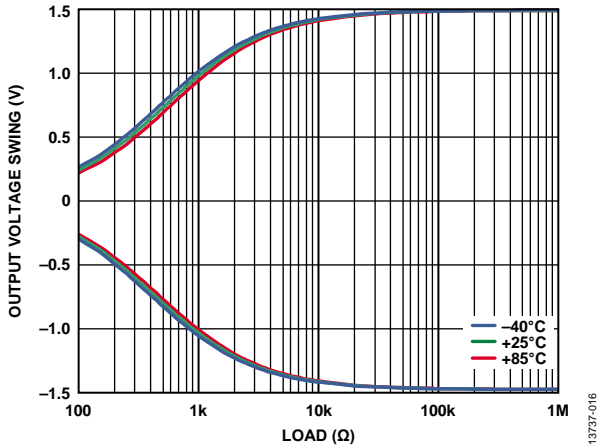


Figure 16. Output Voltage Swing vs. Load

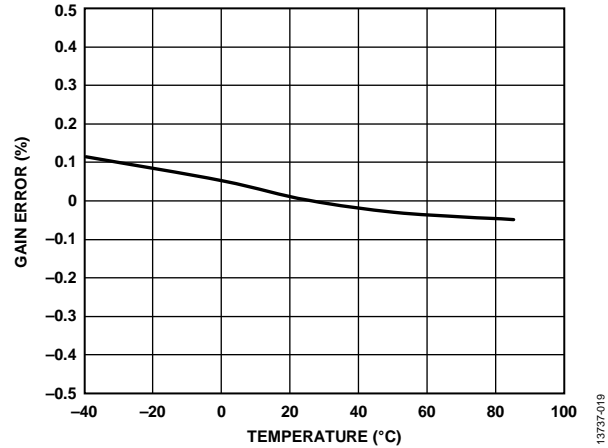


Figure 19. Gain Error vs. Temperature

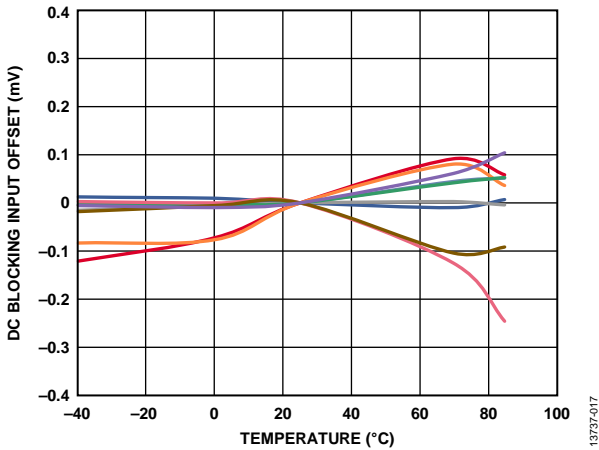


Figure 17. DC Blocking Input Offset Drift on Multiple Parts

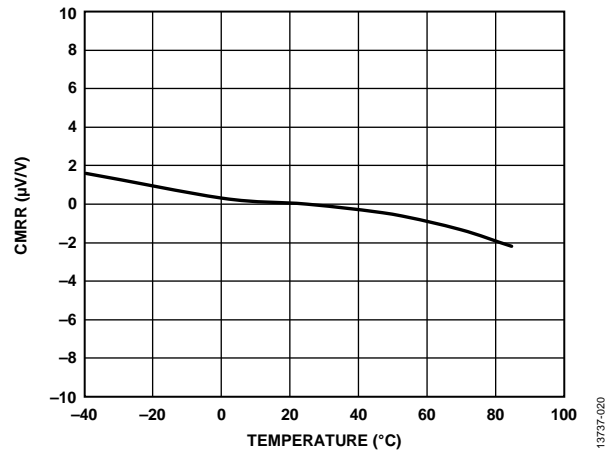


Figure 20. CMRR vs. Temperature

OPERATIONAL AMPLIFIER PERFORMANCE CHARACTERISTICS

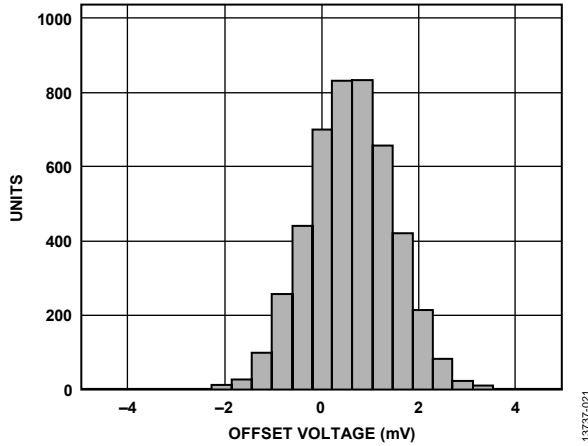


Figure 21. Offset Distribution

13737-021

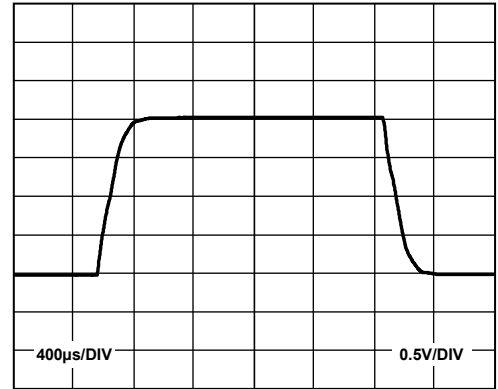


Figure 24. Large Signal Transient Response

13737-024

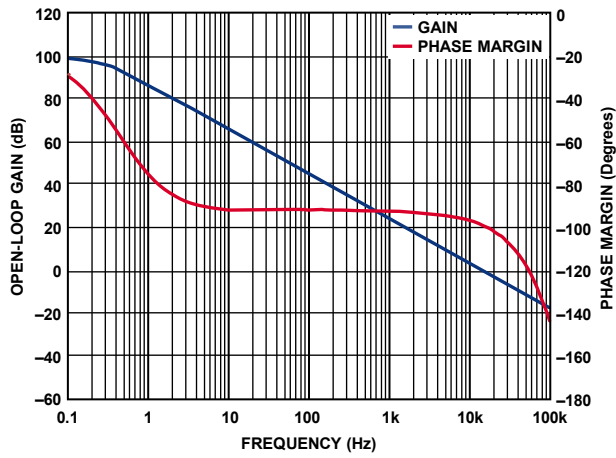


Figure 22. Open-Loop Gain and Phase Margin vs. Frequency

13737-022

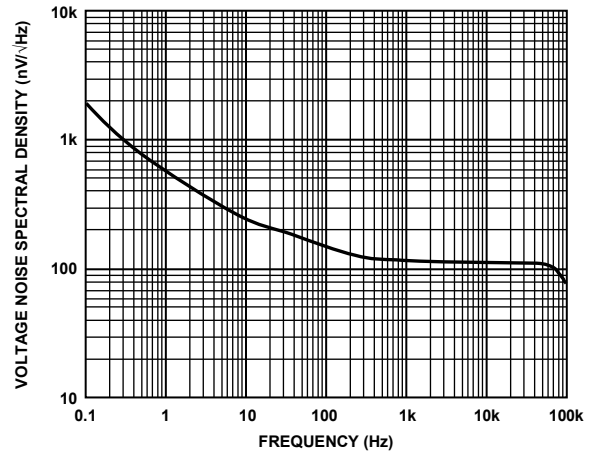


Figure 25. Voltage Noise Spectral Density vs. Frequency

13737-025

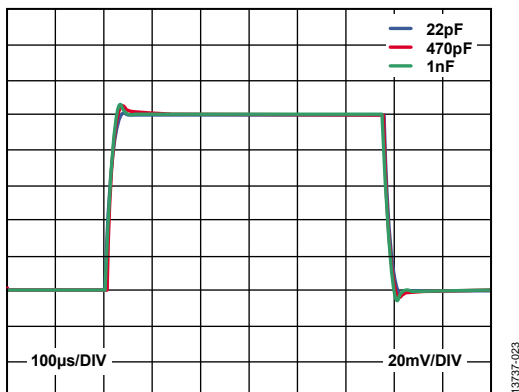


Figure 23. Small Signal Response for Various Capacitive Loads

13737-023

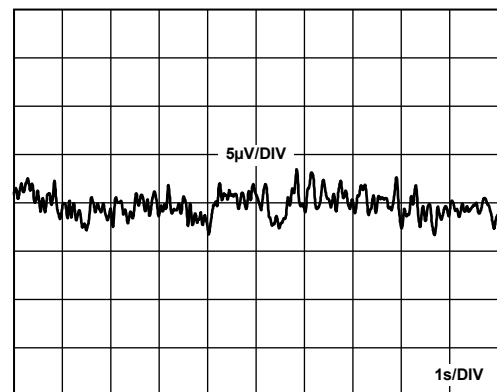


Figure 26. 0.1 Hz to 10 Hz Noise

13737-026

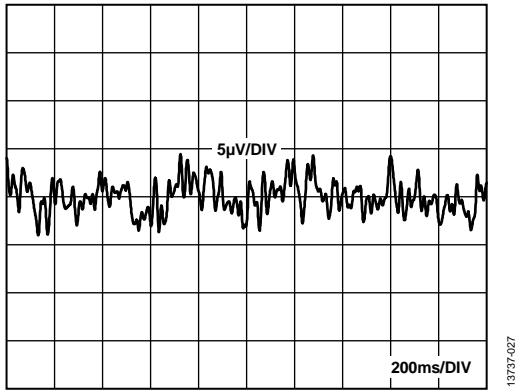


Figure 27. 0.5 Hz to 40 Hz Noise

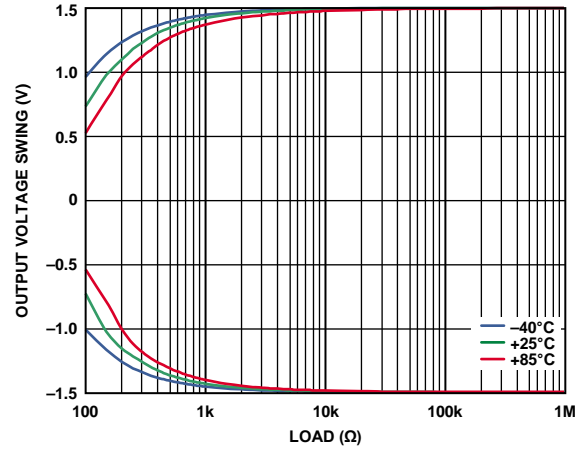


Figure 29. Output Voltage Swing vs. Load

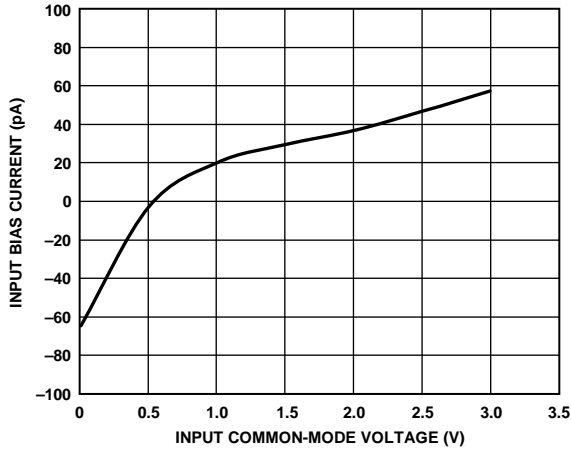


Figure 28. Input Bias Current vs. Input Common-Mode Voltage

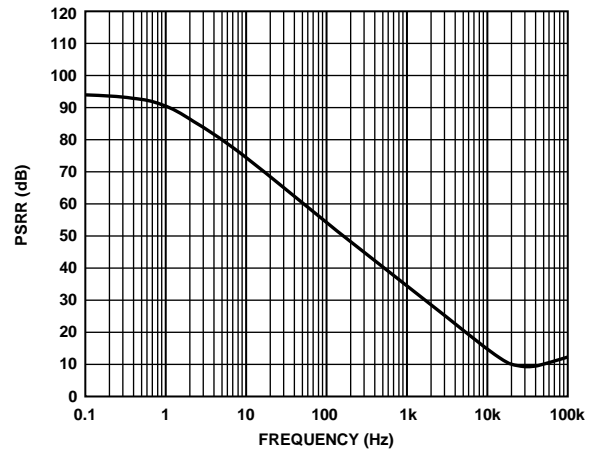


Figure 30. Power Supply Rejection Ratio vs. Frequency

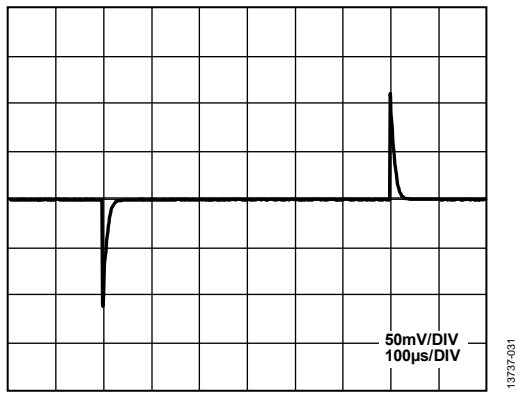


Figure 31. Load Transient Response (100  $\mu$ A Load Change)

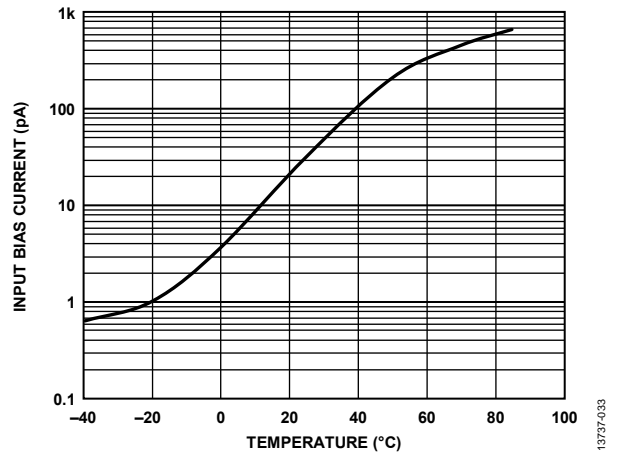


Figure 33. Input Bias Current vs. Temperature

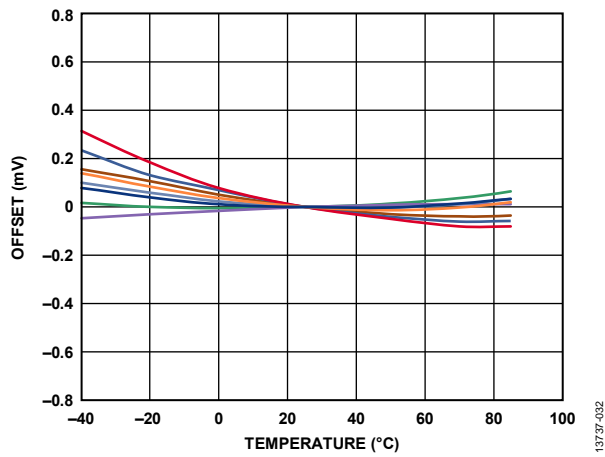


Figure 32. Offset vs. Temperature on Multiple Parts

RLD AMPLIFIER PERFORMANCE CHARACTERISTICS

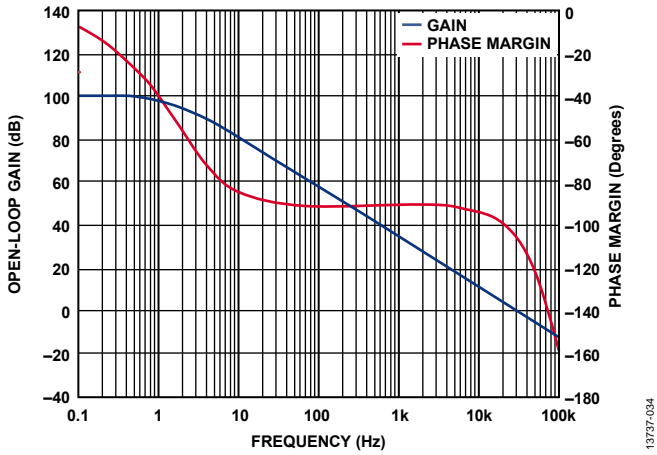


Figure 34. Open-Loop Gain and Phase Margin vs. Frequency

13737-034

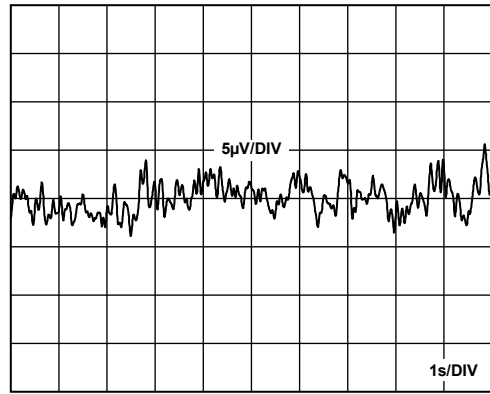


Figure 37. 0.1 Hz to 10 Hz Noise

13737-037

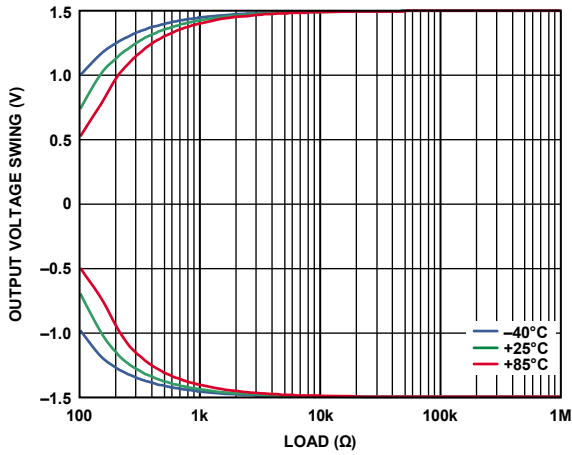


Figure 35. Output Voltage Swing vs. Load

13737-035

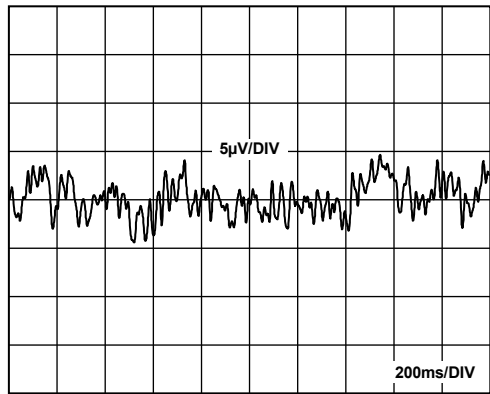


Figure 38. 0.5 Hz to 40 Hz Noise

13737-038

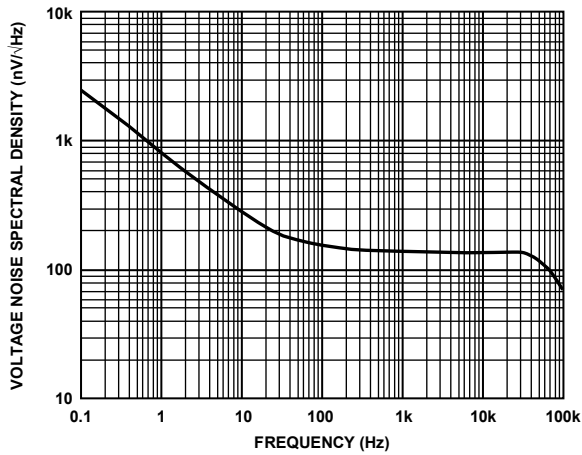


Figure 36. Voltage Spectral Noise Density vs. Frequency

13737-036

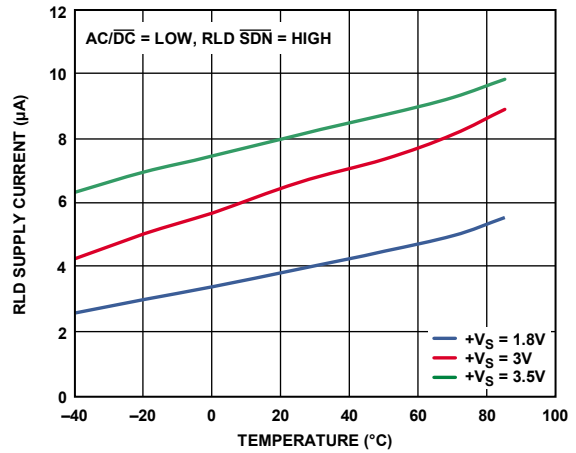


Figure 39. RLD Supply Current vs. Temperature

13737-039

REFERENCE BUFFER PERFORMANCE CHARACTERISTICS

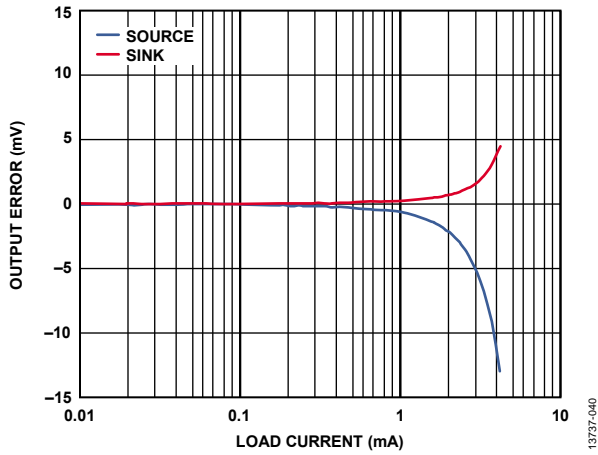


Figure 40. Load Regulation

13737-040

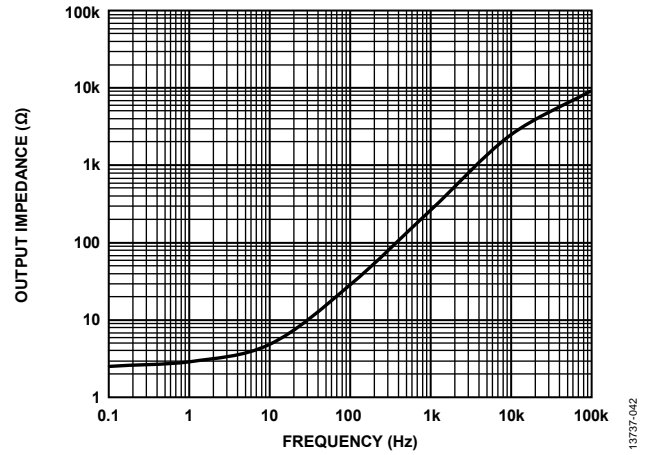


Figure 42. Output Impedance vs. Frequency

13737-042

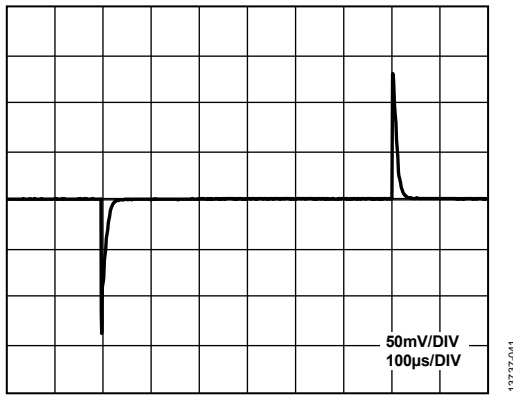


Figure 41. Load Transient Response (100 μA Load Change)

13737-041

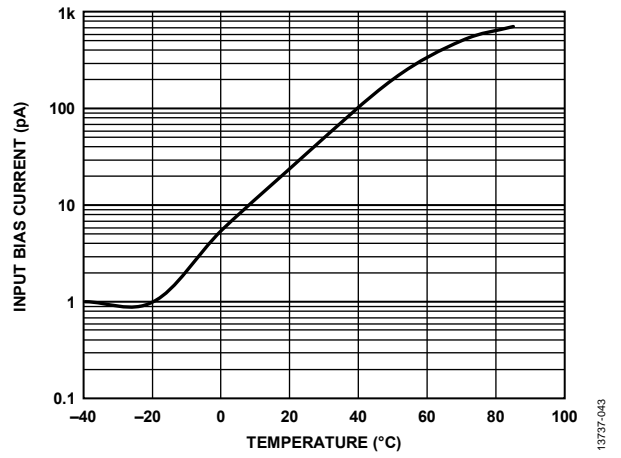


Figure 43. Input Bias Current vs. Temperature

13737-043

SYSTEM PERFORMANCE CHARACTERISTICS

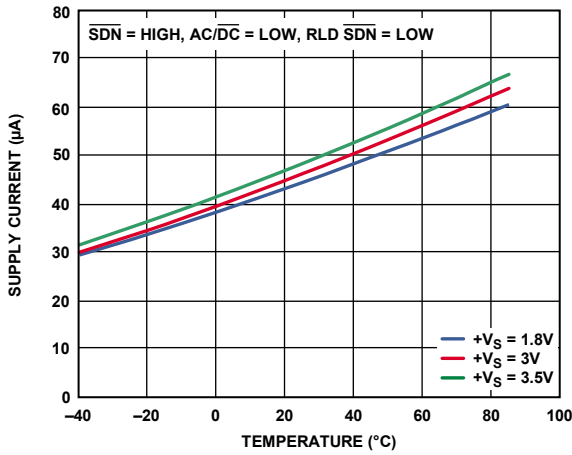


Figure 44. Supply Current vs. Temperature

13737-044

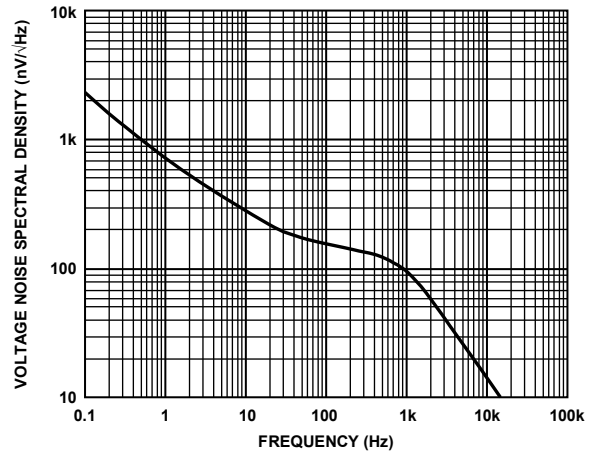


Figure 47. Voltage Noise Spectral Density (RTI), Measured at IAOUT

13737-047

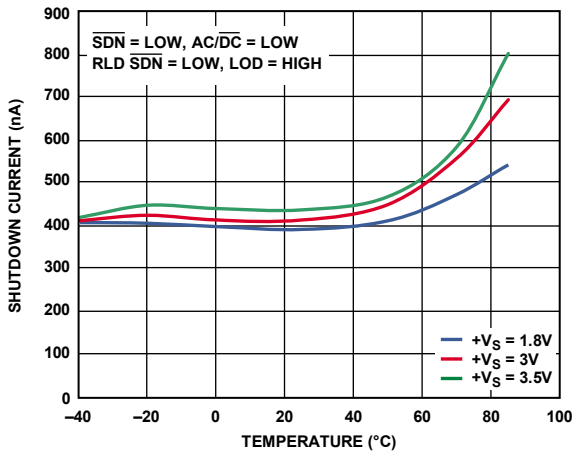


Figure 45. Shutdown Current vs. Temperature

13737-045

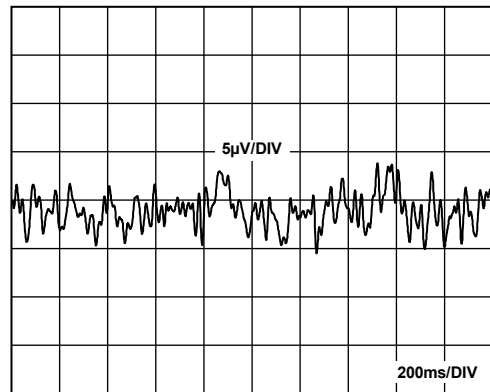


Figure 48. 0.5 Hz to 40 Hz Noise (RTI), Measured at IAOUT

13737-048

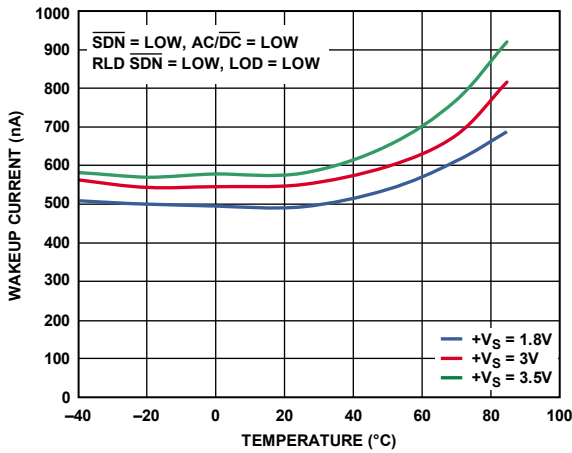


Figure 46. Wakeup Current vs. Temperature

13737-046

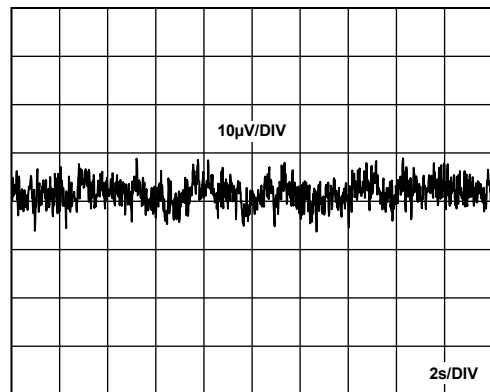


Figure 49. 0.05 Hz to 150 Hz Noise (RTI), Measured at IAOUT

13737-049



# THEORY OF OPERATION

## ARCHITECTURE OVERVIEW

The AD8233 is an integrated front end for signal conditioning of cardiac biopotentials for heart rate monitoring. It consists of a specialized instrumentation amplifier (IA), an operational amplifier (A1), a right leg drive amplifier (A2), and a midsupply reference buffer (A3). In addition, the AD8233 includes leads on or off detection circuitry and an automatic fast restore circuit that restores the signal shortly after leads are reconnected.

The AD8233 contains a specialized instrumentation amplifier that amplifies the ECG signal while rejecting the electrode half cell potential on the same stage. The amplification of the ECG signal and the rejection of the electrode half cell potential are possible with an indirect current feedback architecture, which reduces size and power compared with traditional implementations.

## INSTRUMENTATION AMPLIFIER

The instrumentation amplifier shown in Figure 50 is composed of two well matched transconductance amplifiers (GM1 and GM2), the dc blocking amplifier (HPA), and an integrator formed by C1 and an op amp. The transconductance amplifier, GM1, generates a current that is proportional to the voltage present at its inputs. When the feedback is satisfied, an equal voltage appears across the inputs of the transconductance amplifier, GM2, thereby matching the current generated by GM1. The difference generates an error current that is integrated across Capacitor C1. The resulting voltage appears at the output of the instrumentation amplifier.

The feedback of the amplifier is applied via GM2 through two separate paths: the two resistors divide the output signal to set an overall gain of 100, whereas the dc blocking amplifier integrates any deviation from the reference level. Consequently, dc offsets as large as  $\pm 300$  mV across the GM1 inputs appear inverted and with the same magnitude across the inputs of GM2, all without saturating the signal of interest.

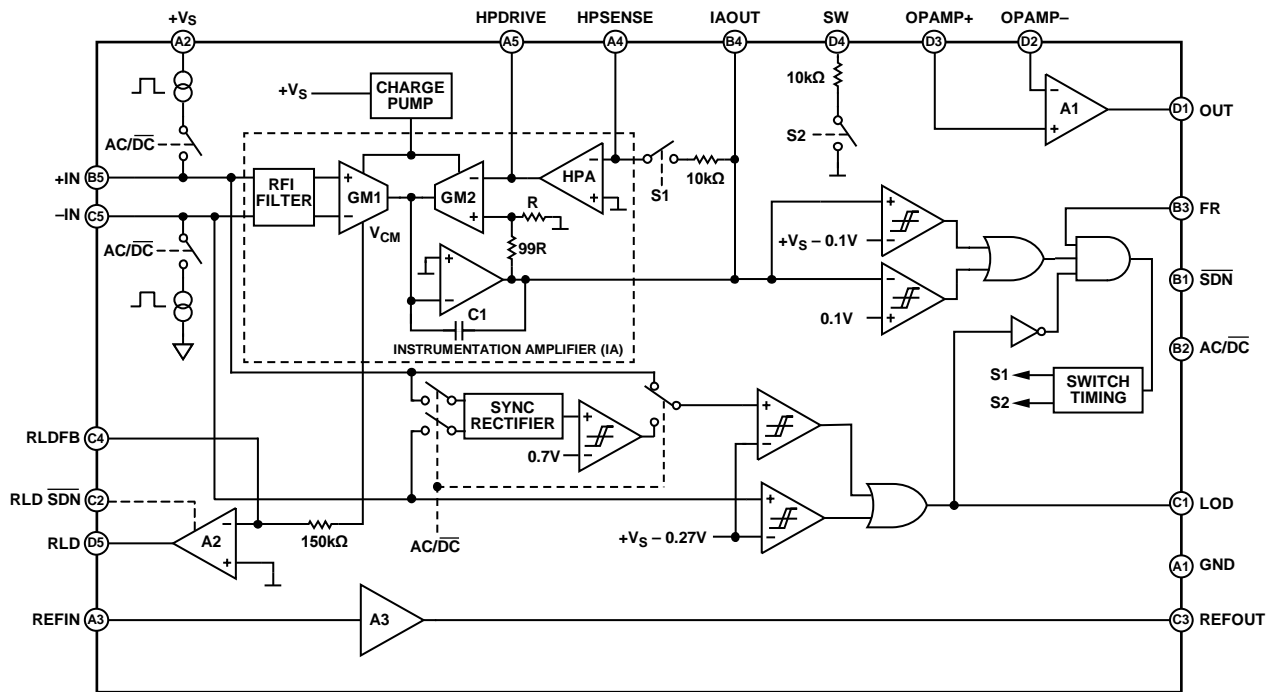
To increase the common-mode voltage range of the instrumentation amplifier, a charge pump boosts the supply voltage for the two transconductance amplifiers. This boost in supply voltage further prevents saturation of the amplifier in the presence of large common-mode signals, such as line interference. The charge pump runs from an internal oscillator, the frequency of which is set around 500 kHz.

## OPERATIONAL AMPLIFIER

The general-purpose operational amplifier (A1) is a rail-to-rail device that can be used for low-pass filtering and to add additional gain. The following sections provide details and example circuits that use this amplifier.

## RLD AMPLIFIER

The RLD amplifier inverts the common-mode signal that is present at the instrumentation amplifier inputs. When the right leg drive output current is injected into the subject, it counteracts common-mode voltage variations, thus improving the common-mode rejection of the system.



\*ALL SWITCHES SHOWN IN DC LEADS OFF DETECTION POSITION AND FAST RESTORE DISABLED  
 ⊥ = REFOUT

Figure 50. Simplified Schematic Diagram  
 Rev. A | Page 17 of 31

The common-mode signal that is present across the inputs of the instrumentation amplifier is derived from the transconductance amplifier, GM1. It is then connected to the inverting input of A2 through a 150 kΩ resistor.

An integrator can be built by connecting a capacitor between the RLD FB and RLD terminals. A good starting point is a 1 nF capacitor, which places the crossover frequency at about 1 kHz (the frequency at which the amplifier has an inverting unity gain). This configuration results in about 26 dB of loop gain available at a frequency range from 50 Hz to 60 Hz for common-mode line rejection. Higher capacitor values reduce the crossover frequency, thereby reducing the gain that is available for rejection and, consequently, increasing the line noise. Lower capacitor values move the crossover frequency to higher frequencies, allowing increased gain. However, when using higher gain, the system can become unstable and saturate the output of the right leg amplifier.

When using this amplifier to drive an electrode, place a resistor in series with the output to limit the current to be always less than 10 μA, even in fault conditions. For example, if the supply used is 3.0 V, ensure that the resistor is greater than 330 kΩ to account for component and supply variations.

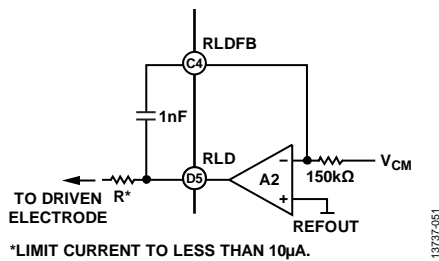


Figure 51. Typical Configuration of Right-Leg Drive Circuit

In two electrode configurations, A2 can be shut down by setting RLD SDN low for additional power savings. If left in shutdown, it is recommended to leave both RLD and RLDFB floating. Alternatively, RLD can be used to bias the inputs through 10 MΩ resistors, as described in the Leads On or Off Detection section. When the AD8233 is in shutdown and dc leads off detection mode, RLD pulls down towards ground. This pull-down acts as an LOD wake-up function, pulling the inputs down when the electrodes are reconnected.

## REFERENCE BUFFER

The AD8233 operates from a single supply. To simplify the design of single-supply applications, the AD8233 includes a reference buffer to create a virtual ground between the supply voltage and the system ground. The signals present at the output of the instrumentation amplifier are referenced around this voltage. For example, if there is zero differential input voltage, the voltage at the output of the instrumentation amplifier is this reference voltage.

The reference voltage level is set at the REFIN pin. It can be set with a voltage divider or by driving the REFIN pin from some other point in the circuit (for example, from the ADC reference). The voltage is available at the REFOUT pin for the filtering circuits or for an ADC input.

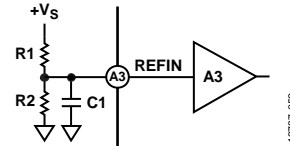


Figure 52. Setting the Internal Reference

To limit the power consumption of the voltage divider, the use of large resistors is recommended, such as 10 MΩ. The designer must keep in mind that high resistor values make it easier for interfering signals to appear at the input of the reference buffer. To minimize noise pickup, it is recommended to place the resistors close to each other and as near as possible to the REFIN terminal. Furthermore, use a capacitor in parallel with the lower resistor on the divider for additional filtering, as shown in Figure 52. A large capacitor results in better noise filtering but takes longer to settle the reference after power-up. The total time the reference takes to settle within 1% can be estimated with the formula

$$t_{\text{SETTLE\_REFERENCE}} = 5 \times \frac{R1 \times R2 \times C1}{R1 + R2}$$

Disabling the AD8233 with the shutdown terminal does not discharge this capacitor.

## FAST RESTORE CIRCUIT

Because of the low cutoff frequency used in high-pass filters in ECG applications, signals may require several seconds to settle. This settling time can result in a delay for the user after a step response, such as when the electrodes are first connected.

This fast restore function is implemented internally, as shown in Figure 53. The output of the instrumentation amplifier is connected to a window comparator. The window comparator detects a saturation condition at the output of the instrumentation amplifier when its voltage approaches 0.1 V from either supply rail.

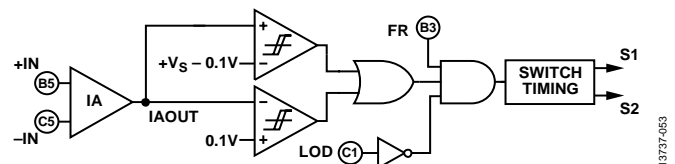


Figure 53. Fast Restore Circuit

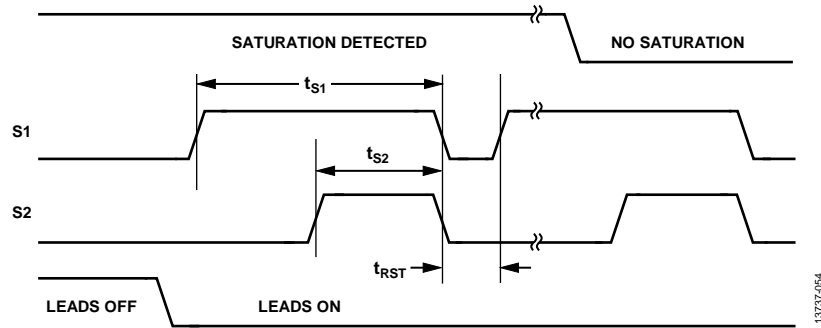


Figure 54. Timing Diagram for Fast Restore Switches (Time Base Not to Scale)

If this saturation condition is present when both input electrodes are attached to the subject, the comparator triggers a timing circuit that automatically closes Switch S1 and Switch S2. See Figure 54 for the fast restore switches timing diagram.

These two switches (S1 and S2) enable two different 10 k $\Omega$  resistor paths: one between HPSENSE and IAOUT, and another between SW and REFOUT. During the time Switch S1 and Switch S2 are enabled, the internal resistors appear in parallel with their corresponding external resistors, forming high-pass filters. The result is that the equivalent lower resistance shifts the pole to a higher frequency, delivering a quicker settling time. The fast restore settling time depends on how quickly the internal 10 k $\Omega$  resistors of the AD8233 can drain the capacitors in the high-pass circuit. Smaller capacitor values result in a shorter settling time.

If, by the end of the timing, the saturation condition persists, the cycle repeats. Otherwise, the AD8233 returns to its normal operation. If either of the leads off comparator outputs indicates that an electrode is disconnected, the timing circuit is prevented from triggering because it is assumed that no valid signal is present. To disable fast restore, drive the FR pin low or tie it permanently to GND.

### LEADS ON OR OFF DETECTION

The AD8233 includes leads off detection. The AD8233 features ac and dc detection modes that both work with two and three electrode configurations. Ultralow power comparators allow the leads on or off detection to remain functional in shutdown mode, creating power savings at the system level when the LOD output is used as a wake-up signal for the microcontroller.

#### DC Leads On or Off Detection

The dc leads off detection mode can be used in two or three electrode configurations. This mode works by sensing when either instrumentation amplifier input voltage is within 0.27 V from the positive rail. The lowest power use case for the AD8233 is two electrode dc mode. A pull-up resistor on +IN and a pull-down resistor on -IN create a voltage divider when the electrodes are connected, setting the input common mode to midsupply. When the electrodes disconnect, the comparator monitoring +IN sets LOD high when the input pulls to +V<sub>s</sub>.

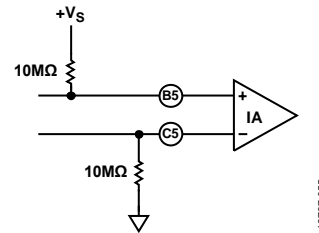


Figure 55. Circuit Configuration for Two Electrode DC Leads Off Detection

For three electrode dc mode, each input must have a pull-up resistor connected to the positive supply. During normal operation, the potential of the subject must be inside the common-mode range of the instrumentation amplifier, which is only possible if a third electrode is connected to the output of the right leg drive amplifier.

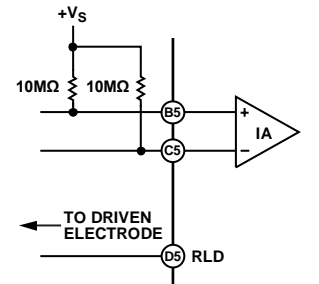


Figure 56. Circuit Configuration for Three Electrode DC Leads Off Detection

The AD8233 indicates when any electrode is disconnected by setting the LOD pin high. To use this mode, connect the AC/DC pin to ground.

#### AC Leads On or Off Detection

The ac leads off detection mode is useful when using two electrodes. A conduction path must exist between the two electrodes, which is usually formed by two resistors, as shown in Figure 57.

These resistors also provide a path for bias return on each input. Connect each resistor to REFOUT or RLD to maintain the inputs within the common-mode range of the instrumentation amplifier.

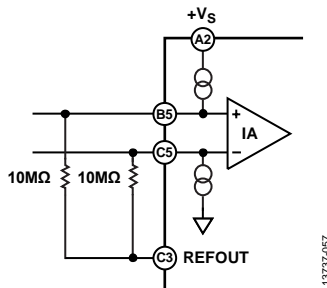


Figure 57. Circuit Configuration for Two Electrode AC Leads Off Detection

The AD8233 detects when an electrode is disconnected by forcing a 100 kHz current into the input terminals. This current flows through the external resistors from IN+ to IN- and develops a differential voltage across the inputs, which is then synchronously detected and compared to an internal threshold. The recommended value for these external resistors is 10 MΩ. Low resistance values make the differential drop too low to be detected and lower the input impedance of the amplifier. When the electrodes are attached to the subject, the impedance of this path must be less than 3 MΩ to maintain the drop below the threshold of the comparator.

To use the ac leads off mode, tie the AC/DC pin to the positive supply rail. Although REFOUT is at a constant voltage value, using the RLD output as the input bias may be more effective in rejecting common-mode interference at the expense of additional power.

In three electrode ac leads off detection mode, shown in Figure 58, pull-up resistors are not required, which improves the input impedance of the circuit. This mode is beneficial for dry electrode applications. The ac mode currents contribute flicker noise (1/f noise) to the system. Depending on the application, use ac leads off detection as a spot check and then switching to dc mode for improved ECG acquisition.

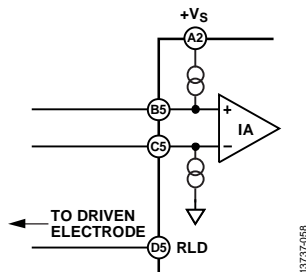


Figure 58. Circuit Configuration for Three Electrode AC Leads Off Detection

The ac leads off detection mode continues to function in shutdown mode as well. To keep the power under 1 μA, the clock is disabled and the ac currents become dc currents. The current source on +IN is 250 nA, while the current sink on -IN is -300 nA. The stronger pull-down current on -IN acts as a wake-up function, pulling LOD low when the electrodes are reconnected.

## STANDBY OPERATION

The AD8233 includes a shutdown pin ( $\overline{\text{SDN}}$ ) that further enhances the flexibility and ease of use in portable applications where low power consumption is critical. A logic level signal can be applied to this pin to switch to shutdown mode.

Driving the  $\overline{\text{SDN}}$  pin low places the AD8233 in shutdown mode and draws less than 1 μA of supply current, offering considerable power savings. To enter normal operation, drive  $\overline{\text{SDN}}$  high. When not using this feature, permanently tie  $\overline{\text{SDN}}$  to +Vs.

During shutdown operation, the AD8233 cannot maintain the REFOUT voltage, but it does not drain the REFIN voltage, thereby maintaining this additional conduction path from the supply to ground.

When emerging from a shutdown condition, the charge stored in the capacitors on the high-pass filters can saturate the instrumentation amplifier and subsequent stages. The use of the fast restore feature helps reduce the recovery time and, therefore, minimize the amount of time powered on in power sensitive applications.

Using leads on or off detection in shutdown mode allows system level power saving. The microcontroller enters sleep mode when the electrodes are disconnected, and the LOD signal acts as an interrupt to wake up the microcontroller. An example of this functionality is shown in Figure 59.

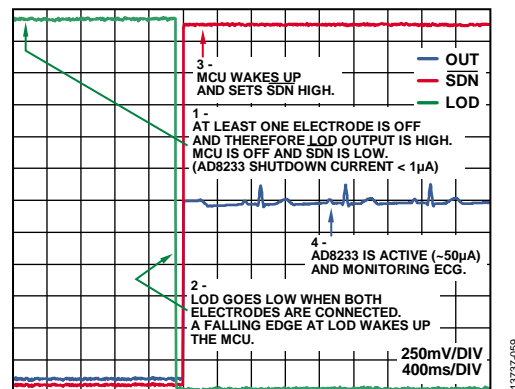


Figure 59. Electrode Connection and System Wakeup Sequence

## INPUT PROTECTION

All terminals of the AD8233 are protected against ESD. In addition, the input structure allows dc overload conditions that are a diode drop above the positive supply and a diode drop below the negative supply. Voltages beyond a diode drop of the supplies cause the ESD diodes to conduct and enable current to flow through the diode. Use an external resistor in series with each of the inputs to limit current for voltages beyond the supplies. In either scenario, the AD8233 safely handles a continuous 5 mA current at room temperature.

For applications where the AD8233 encounters extreme overload voltages, such as in cardiac defibrillators, use external series resistors and gas discharge tubes (GDTs). Neon lamps are commonly used as an inexpensive alternative to GDTs. These

devices can handle the application of large voltages but do not maintain the voltage below the absolute maximum ratings for the AD8233. A complete solution includes further clamping to either supply using additional resistors and low leakage diode clamps, such as BAV199 or FJH1100.

As a safety measure, place a resistor between the input pin and the electrode that is connected to the subject to ensure that the current flow never exceeds  $10\ \mu\text{A}$ . Calculate the value of this resistor to be equal to the supply voltage across the AD8233 divided by  $10\ \mu\text{A}$ .

### RADIO FREQUENCY INTERFERENCE

Radio frequency (RF) rectification is often a problem in applications where there are large RF signals. The problem appears as a dc offset voltage at the output. The AD8233 has a  $15\ \text{pF}$  gate capacitance and  $10\ \text{k}\Omega$  resistors at each input. This forms a low-pass filter on each input that reduces rectification at high frequency (see Figure 60) without the addition of external elements.

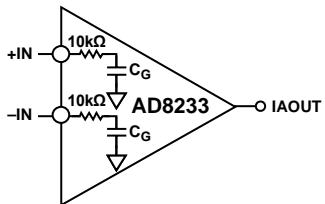


Figure 60. RFI Filter Without External Capacitors

For increased filtering, additional resistors can be added in series with each input. They must be placed as close as possible to the instrumentation amplifier inputs. These can be the same resistors used for overload and patient protection.

### POWER SUPPLY REGULATION AND BYPASSING

The AD8233 is designed to be powered directly from a single  $3\ \text{V}$  battery, such as a CR2032. The AD8233 can also operate from rechargeable Li-Ion batteries, but the designer must take into account that the voltage during a charge cycle may exceed the absolute maximum ratings of the AD8233. To avoid damage to the device, use a power switch or a low power, low dropout regulator, such as the [ADP150](#) or [ADP160](#).

In addition, excessive noise on the supply pins can adversely affect performance. As in all linear circuits, bypass capacitors must be used to decouple the chip power supplies. Place a  $0.1\ \mu\text{F}$  capacitor close to the supply pin. A  $1\ \mu\text{F}$  capacitor can be used farther away from the device. In most cases, the capacitor can be shared by other integrated circuits. Excessive decoupling capacitance increases power dissipation during power cycling.

### INPUT REFERRED OFFSETS

Because of its internal architecture, the instrumentation amplifier must always be used with the dc blocking amplifier, labeled HPA in Figure 50.

The dc blocking amplifier attenuates the input referred offsets present at the inputs of the instrumentation amplifier, as described in the Theory of Operation section. However, this attenuation only occurs when the dc blocking amplifier is used as an integrator. In this case, the input offsets from the dc blocking amplifier are dominant and appear directly at the output of the instrumentation amplifier.

If the dc blocking amplifier is used as a follower instead of its intended function as an integrator, the input referred offsets of the in-amp are amplified by a factor of 100.

### LAYOUT RECOMMENDATIONS

It is important to follow good layout practices to optimize system performance. In low power applications, most resistors are of a high value to minimize additional supply current. The challenge of using high value resistors is that high impedance nodes become even more susceptible to noise pickup and board parasitics, such as capacitance and surface leakages. Keep all of the connections between high impedance nodes as short as possible to avoid introducing additional noise and errors from corrupting the signal.

To maintain high CMRR over frequency, keep the input traces symmetrical and length matched. Place safety and input bias resistors in the same position relative to each input. In addition, the use of a ground plane significantly improves the noise rejection of the system.

For WLCSP layout best practices, refer to the [AN-617 Application Note](#).

## APPLICATION INFORMATION

### ELIMINATING ELECTRODE OFFSETS

The instrumentation amplifier in the AD8233 is designed to apply gain and to filter out near dc signals simultaneously. This capability allows the device to amplify a small ECG signal by a factor of 100 while rejecting electrode offsets as large as  $\pm 300$  mV.

To achieve offset rejection, connect a resistor/capacitor (RC) network between the output of the instrumentation amplifier (HPSENSE) and HPDRIVE, as shown in Figure 61.

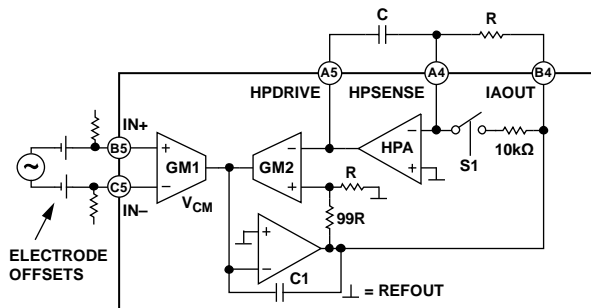


Figure 61. Eliminating Electrode Offsets

This RC network forms an integrator that feeds any dc signals that are not filtered back into the instrumentation amplifier, thus eliminating the offsets without saturating any node and maintaining high signal gain.

In addition to blocking offsets present across the inputs of the instrumentation amplifier, this integrator also works as a high-pass filter that minimizes the effect of slow moving signals, such as baseline wander. The cutoff frequency of the filter is given by the following equation:

$$f_c = \frac{100}{2\pi RC}$$

where:

R is in  $\Omega$ .

C is in farads.

The filter cutoff is 100 times higher than is typically expected from a single-pole filter. Because of the feedback architecture of the instrumentation amplifier, the typical filter cutoff equation is modified by a gain of 100 from the instrumentation amplifier.

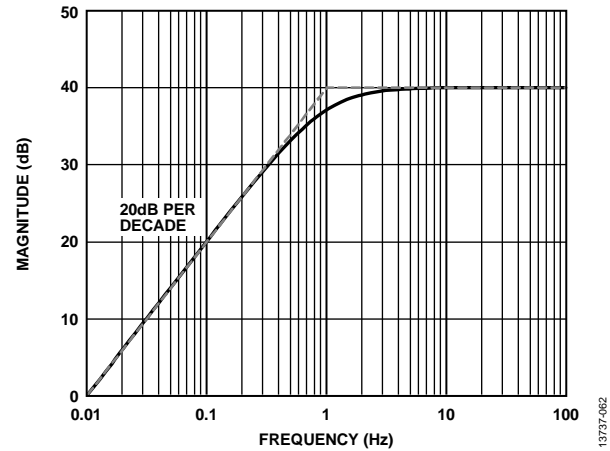


Figure 62. Frequency Response of a Single-Pole DC Blocking Circuit

As with any high-pass filter with low frequency cutoff, a fast change in dc offset requires a long time to settle. If such a change saturates the instrumentation amplifier output, the S1 switch briefly enables the 10 k $\Omega$  resistor path, thus moving the cutoff frequency to

$$f_c = \frac{100(R + 10^4)}{2\pi RC(10^4)}$$

For values of R greater than 100 k $\Omega$ , this expression can be approximated by

$$f_c = \frac{1}{200\pi C}$$

This higher cutoff frequency reduces the settling time and enables faster recovery of the ECG signal. For more information, see the Fast Restore Circuit section.

### HIGH-PASS FILTERING

The AD8233 can implement higher order high-pass filters. A higher filter order yields better artifact rejection, but increased signal distortion and more passive components on the PCB.

#### Two-Pole High-Pass Filter

A two-pole architecture can be implemented by adding a simple ac coupling RC at the output of the instrumentation amplifier, as shown in Figure 63.

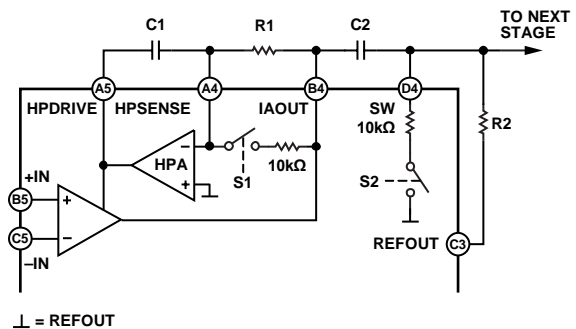


Figure 63. Schematic for a Two-Pole High-Pass Filter



The right side of C2 connects to the SW terminal. As with S1, S2 reduces the recovery time for the ac coupling network by placing 10 kΩ in parallel with R2. See the Fast Restore Circuit section for additional details on switch timing and trigger conditions.

If the passive network is not buffered, the network exhibits higher output impedance at the input of a subsequent low-pass filter, as with Sallen-Key filter topologies. Careful component selection results in reliable performance without a buffer. See the Low-Pass Filtering and Gain section for additional information on component selection.

**Additional High-Pass Filtering Options**

In addition to the topologies explained in previous sections, an additional pole may be added to the dc blocking circuit for the rejection of low frequency signals. This configuration is shown in Figure 64.

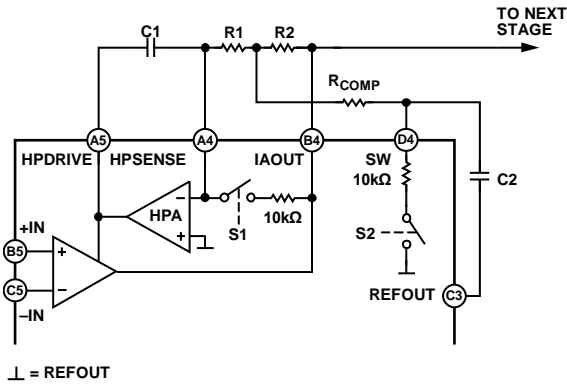


Figure 64. Schematic for an Alternative Two-Pole, High-Pass Filter

An extra benefit of this circuit topology is that it allows a lower cutoff frequency with lower R and C values. The resistor, R<sub>COMP</sub>, can also be used to control the quality factor (Q) of the filter to achieve narrow band-pass filters (for heart rate detection) or maximum pass-band flatness (for cardiac monitoring).

With this circuit topology, the filter attenuation reverts to a single-pole roll-off at very low frequencies. Because the initial roll-off is 40 dB per decade, this reversion to 20 dB per decade has little impact on the ability of the filter to reject out-of-band low frequency signals.

The designer may choose different values to achieve the desired filter performance. To simplify the design process, use the following recommendations as a starting point for component value selection.

- R1 = R2 ≥ 100 kΩ
- C1 = C2
- R<sub>COMP</sub> = 0.14 × R1

The cutoff frequency is located at

$$f_c = \frac{10}{2\pi\sqrt{R1 \times C1 \times R2 \times C2}}$$

The selection of R<sub>COMP</sub> to be 0.14 times the value of the other two resistors optimizes the filter for a maximally flat pass band. Reduce the value of R<sub>COMP</sub> to increase the Q and, consequently, the peaking of the filter. A very low R<sub>COMP</sub> value may result in an unstable circuit. The selection of values based on these criteria results in a transfer function similar to what is shown in Figure 66. When additional low frequency rejection is desired, a high-order, high-pass filter can be implemented by adding an ac coupling network at the output of the instrumentation amplifier, as shown in Figure 65. The SW terminal is connected to the ac coupling network to obtain the best settling time response when fast restore engages.

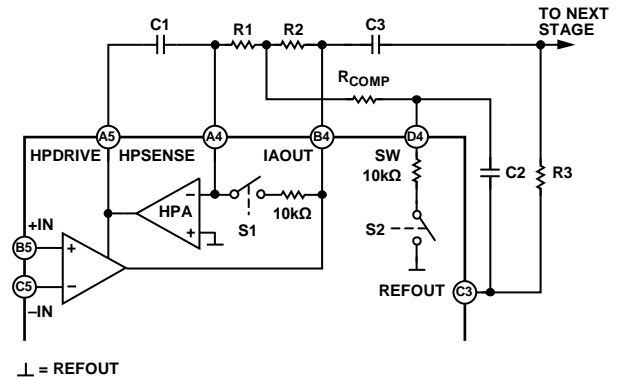


Figure 65. Schematic for a Three-Pole, High-Pass Filter

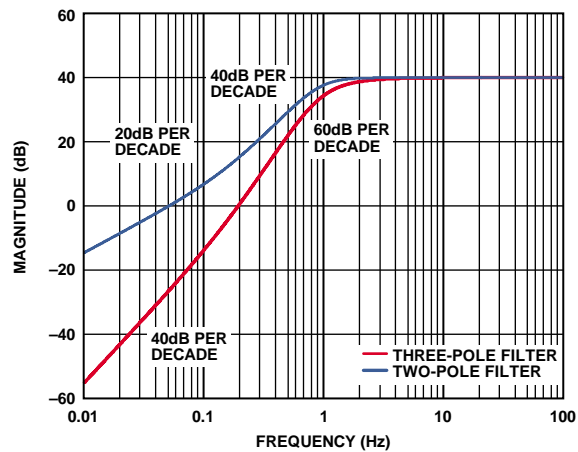


Figure 66. Frequency Response of the Circuits Shown in Figure 64 and Figure 65

Careful analysis and adjustment of all of the component values in practice is recommended to optimize the filter characteristics. To reduce the value of R<sub>COMP</sub>, increase the peaking of the active filter to overcome the additional roll-off introduced by the ac coupling network. Proper adjustment yields the best pass-band flatness.

Table 6. Comparison of High-Pass Filtering Options

Figure to Reference	Filter Order	Component Count	Low Frequency Rejection	Capacitor Sizes/Values	Signal Distortion <sup>1</sup>	Output Impedance <sup>2</sup>
Figure 61	1	2	Good	Large	Low	Low
Figure 63	2	4	Better	Large	Medium	Higher
Figure 64	2	5	Better	Smaller	Medium	Low
Figure 65	3	7	Best	Smaller	Highest	Higher

<sup>1</sup> The signal distortion is for the equivalent corner frequency location.

<sup>2</sup> Output impedance refers to the drive capability of the high-pass filter before the low-pass filter. Low output impedance is desirable to allow flexibility in the selection of values for a low-pass filter, as explained in the Low-Pass Filtering and Gain section.

The design of the high-pass filter involves trade-offs between signal distortion, component count, low frequency rejection, and component size. For example, a single-pole, high-pass filter results in the least distortion to the signal, but the associated rejection of low frequency artifacts is the lowest of the available filter options. Table 6 compares the recommended filtering options.

### LOW-PASS FILTERING AND GAIN

The AD8233 includes an uncommitted op amp that can be used for extra gain and filtering. For applications that do not require a high order filter, a simple RC low-pass filter is sufficient, and the op amp can buffer or further amplify the signal.

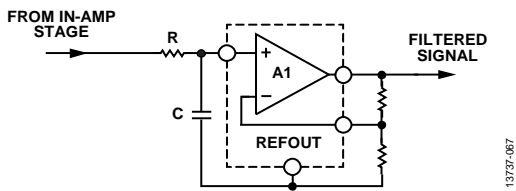


Figure 67. Schematic for a Single-Pole, Low-Pass Filter and Additional Gain

A Sallen-Key filter topology can be implemented for applications that require a steeper roll-off or a sharper cutoff frequency, as shown in Figure 68.

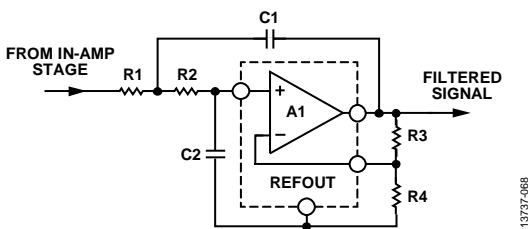


Figure 68. Schematic for a Two-Pole, Low-Pass Filter

The following equations describe the low-pass cutoff frequency ( $f_c$ ), gain, and Q:

$$f_c = \frac{1}{2\pi\sqrt{R1 \times C1 \times R2 \times C2}}$$

$$\text{Gain} = 1 + R3/R4$$

$$Q = \frac{\sqrt{R1 \times C1 \times R2 \times C2}}{R1 \times C2 \times R2 \times C2 + R1 \times C1(1 - \text{Gain})}$$

Changing the gain has an effect on Q and vice versa. Common values for Q are 0.5, to avoid peaking, or 0.7 for maximum flatness and a sharp cutoff frequency. Use a high Q value in narrow-band applications to increase peaking and the selectivity of the band-pass filter.

A common design procedure is to set  $R1 = R2 = R$  and  $C1 = C2 = C$ , simplifying the expressions for the cutoff frequency and Q to

$$f_c = 1/(2\pi RC)$$

$$Q = \frac{1}{3 - \text{Gain}}$$

Q can be controlled by setting the gain with R3 and R4, but this setting limits the gain to be less than 3. The circuit becomes unstable for gain values equal to or greater than 3. A simple modification that allows higher gains is to make the value of C2 at least four times larger than C1.

These design equations only hold true in a case where the output impedance of the previous stage is much lower than the input impedance of the Sallen-Key filter. The design equations do not hold true when using an ac coupling network between the instrumentation amplifier output and the input of the low-pass filter without a buffer.

To connect these two filtering stages properly without a buffer, make the value of R1 at least 10 times larger than the resistor of the ac coupling network (labeled as R2 in Figure 63).

### Driving ADCs

The ability of AD8233 to drive capacitive loads makes it ideal for driving an ADC without an additional buffer. However, depending on the input architecture of the ADC, a simple, low-pass RC network may be required to decouple the transients from the switched capacitor input that are typical of modern ADCs. This RC network also acts as an additional filter that can help reduce noise and aliasing. Follow the recommended guidelines from the ADC in use for the selection of proper R and C values. Table 7 lists compatible ADCs by category.

Table 7. Compatible ADCs by Category

ADCs	Microcontrollers	Optical Sensors	Accelerometers
AD7091	ADuCM350	ADPD103	ADXL363
AD7988-1	ADuCM3029	ADPD105	
AD7682	ADuCM4050	ADPD1080	
AD7689			



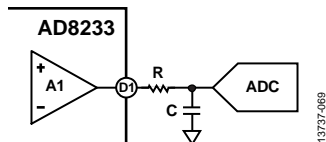


Figure 69. Driving an ADC

## DRIVEN ELECTRODE

A driven electrode (or reference electrode) is often used to minimize the effects of common-mode voltages induced by the power line and other interfering sources. The AD8233 extracts the common-mode voltage from the instrumentation amplifier inputs and makes it available through the RLD amplifier to drive an opposing signal into the patient. This functionality maintains the voltage between the patient and the AD8233 at a near constant, greatly improving the CMRR.

As a safety measure, place a resistor between the RLD pin and the electrode connected to the subject to ensure that current flow never exceeds 10  $\mu\text{A}$ . Calculate the value of this resistor to be equal to the supply voltage across the AD8233 divided by 10  $\mu\text{A}$ .

The AD8233 implements an integrator formed by an internal 150 k $\Omega$  resistor and an external capacitor to drive this electrode. The choice of the integrator capacitor is a trade-off between line rejection capability and stability. It is recommended that the capacitor be small to maintain as much loop gain as possible, around 50 Hz and 60 Hz, which is typical for line frequencies. For stability, it is recommended that the gain of the integrator be less than unity gain at the frequency of any other poles in the loop, such as those formed by the capacitance and the safety resistors of the patient. The suggested application circuits use a 1 nF capacitor, which results in a loop gain of about 20 at line frequencies, with a crossover frequency of about 1 kHz.

In a 2-lead configuration, the RLD pin amplifier can be shut down or used to drive the bias current resistors on the inputs. Although not as effective as a true driven electrode, this configuration can provide some common-mode rejection improvement if the sense electrode impedance is small and well matched.

## MEASURING SURFACE ELECTROMYOGRAPHY (EMG) OR ELECTROENCEPHALOGRAPHY (EEG)

Due to its flexible architecture, the AD8233 filters can be configured to measure other biopotential signals, such as surface EMG or nondiagnostic EEG (alpha or beta waves). The frequency range of signals for surface EMG is typically 2 Hz to 500 Hz for skeletal muscles and 0.01 Hz to 1 Hz for smooth muscles. When measuring wider bandwidth signals inclusive of 50 Hz or 60 Hz, consider lower gain settings. EEG signals have a shared frequency range with ECG signals. However, the amplitude for EEG signals is about 10 times smaller than those for ECG, and as such, require a lower noise solution. Alpha waves (8 Hz to 13 Hz) and beta waves (14 Hz to 40 Hz) can be measured with the AD8233 by setting the high-pass filter at 7 Hz, similar to ECG measurement at the hands (see Figure 72). The 7 Hz cutoff frequency helps remove additional 1/f noise, which lowers the noise floor for the EEG measurement.

## APPLICATION CIRCUITS

### Heart Rate Measurement (HRM) Next to the Heart

For wearable exercise devices, the AD8233 is typically placed in a pod near the heart. The two sense electrodes are placed under the pectoral muscles, and no driven electrode is used. Because the distance from the heart to the AD8233 is small, the heart signal is strong and there is less muscle artifact interference.

In this wearable device configuration, space is at a premium. By using as few external components as possible, the circuit shown in Figure 70 is optimized for size.

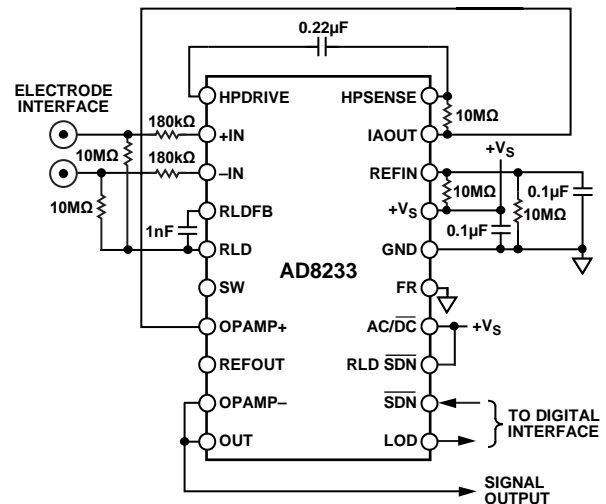


Figure 70. Circuit for HRM Next to the Heart

A shorter distance from the AD8233 to the heart makes this application less vulnerable to common-mode interference. However, because RLD is not used to drive an electrode, it can be used to improve the common-mode rejection by maintaining the midscale voltage through the 10 M $\Omega$  bias resistors. Alternatively, tie RLD SDN low to save power, and tie the bias resistors to REFOUT.

A single-pole, high-pass filter is set at 7 Hz, and there is no low-pass filter. No gain is used on the output op amp, which reduces the number of resistors for a total system gain of 100, as shown in Figure 71.

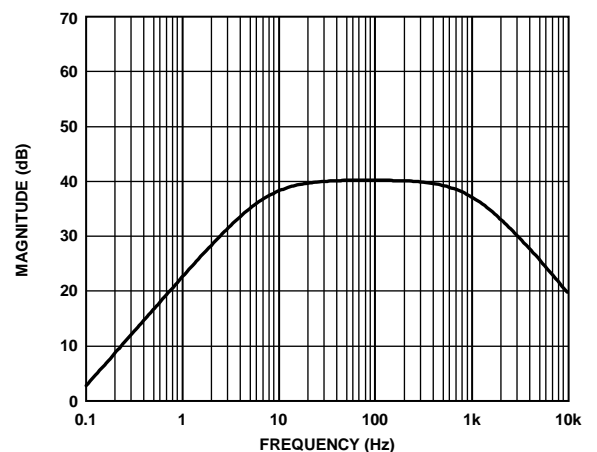


Figure 71. Frequency Response for HRM Next to the Heart Circuit

The input terminals in this configuration use two 180 kΩ resistors to protect the user from fault conditions. Two 10 MΩ resistors provide input bias. Use higher values for electrodes with high output impedance, such as cloth electrodes.

Figure 70 also shows two 10 MΩ resistors to set the midscale reference voltage. If there is already a reference voltage available, it can be driven into the REFIN input to eliminate these two 10 MΩ resistors.

**Exercise Application, HRM at the Hands**

In this application, the heart rate signal is measured at the hands with stainless steel electrodes. The arm and upper body movement of the user create large motion artifacts, and the long lead length makes the system susceptible to common-mode interference. A very narrow band-pass characteristic is required to separate the heart signal from interference.

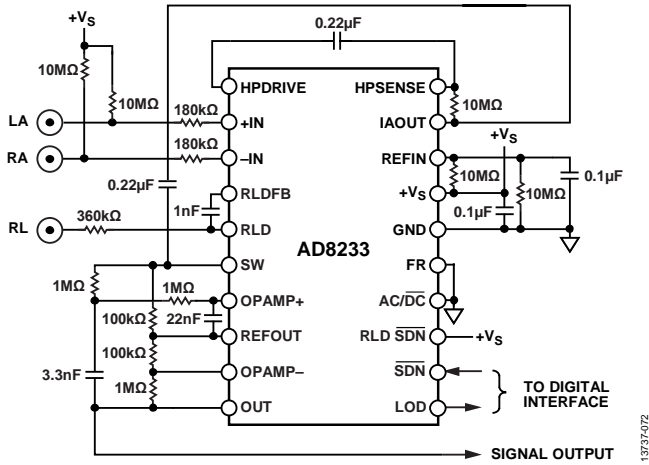


Figure 72. Circuit for HRM at Hands

The circuit shown in Figure 72 uses a two-pole, high-pass filter set at 7 Hz. A two-pole, low-pass filter at 24 Hz follows the high-pass filters to eliminate any other artifacts and line noise.

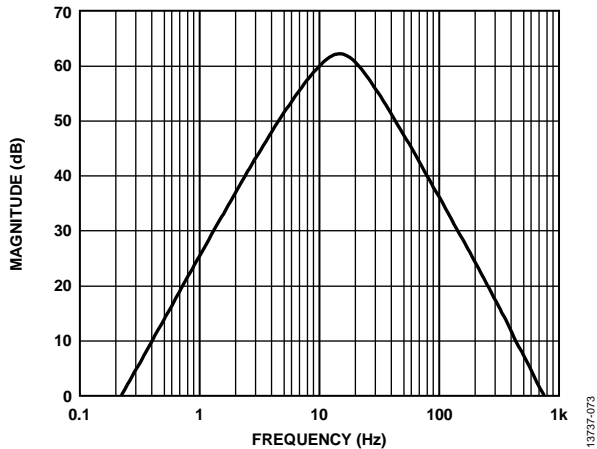


Figure 73. Frequency Response for HRM Circuit Taken at the Hands

The overall narrow-band nature of the two-pole, low-pass filter combination distorts the ECG waveform significantly. Therefore, it is only suitable to determine the heart rate, and not to analyze the ECG signal characteristics.

The low-pass filter stage also includes a gain of 11, bringing the total system gain close to 1100. Because the ECG signal is measured at the hands, it is weaker than when measured closer to the heart.

The RLD circuit drives to the third electrode, which can also be located at the hands, to cancel common-mode interference.

**Holter Monitor Configuration**

The circuit in Figure 75 is designed for monitoring the shape of the ECG waveform.

To obtain an ECG waveform with minimal distortion, the AD8233 is configured with a 0.5 Hz, single-pole, high-pass filter, followed by a two-pole, 40 Hz, low-pass filter. A third electrode is driven for optimum common-mode rejection.

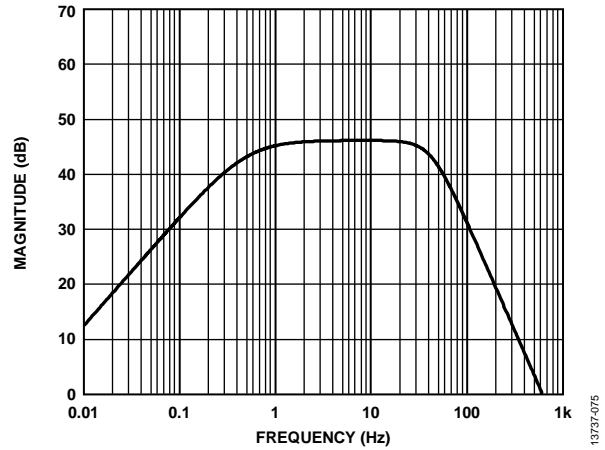


Figure 74. Frequency Response of Holter Monitor Circuit

In addition to 40 Hz filtering, the op amp stage is configured for a gain of 2, resulting in a total system gain of 200. Keeping the gain lower helps with any motion artifacts picked up in band. To optimize the dynamic range of the system, the gain level is adjustable, depending on the input signal amplitude (which may vary with electrode placement) and ADC input range.

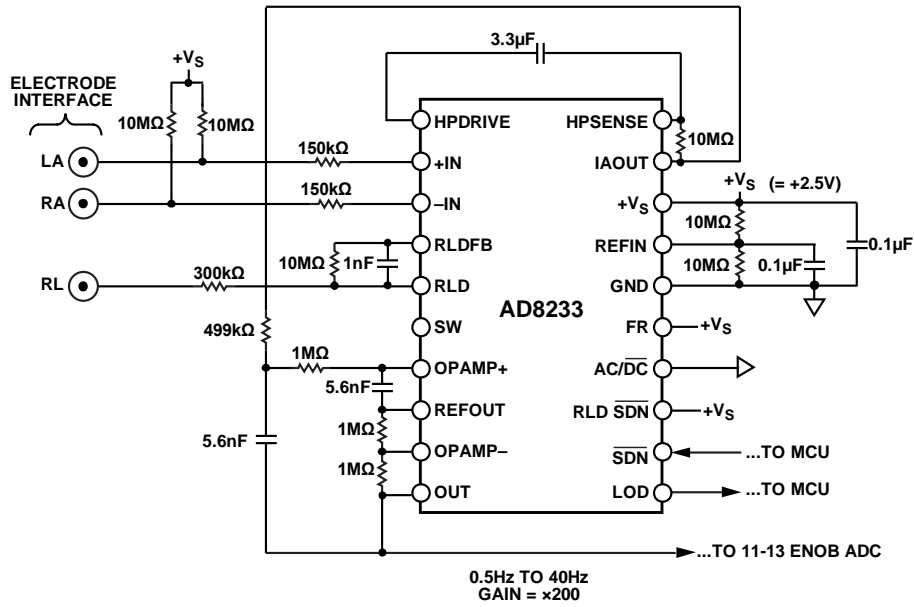


Figure 75. Holter Monitor Circuit

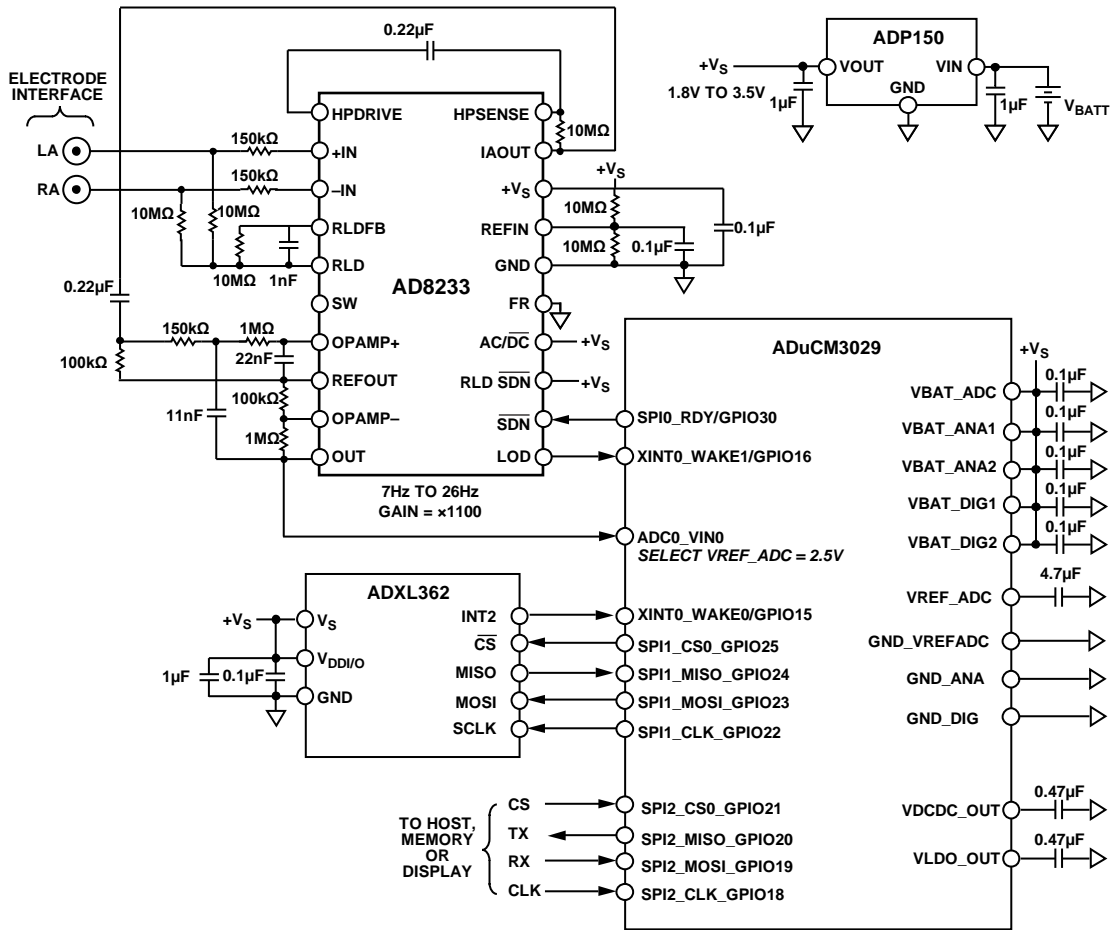


Figure 76. Portable Heart Rate and Activity Monitor Circuit

**Portable Heart Rate and Activity Monitor System**

The circuit in Figure 76 shows the AD8233 configured as an HRM circuit for two electrode applications. The AD8233 implements a two-pole, low-pass filter with a cutoff frequency of 7 Hz, and a two-pole, low-pass filter with a cutoff frequency of 26 Hz. The total signal gain in the pass band is 1,100.

The output of this HRM circuit is sampled by the 12-bit ADC embedded in the ADuCM3029, an ultralow power (<38  $\mu$ A/MHz, <750 nA in hibernate mode) Arm® Cortex™ M3 microcontroller.

The ADXL362 is a micropower (1.8  $\mu$ A at 100 SPS), 3-axis accelerometer that monitors user activity and features an output that serves as the basis for motion-based applications, such as pedometers, calorie burn estimation, and activity tracking. The ADXL362 also features a deep first in, first out (FIFO) that stores samples and allows the system to sleep for long periods of time, minimizing the system power.

**Synchronous ECG and Photoplethysmography (PPG) Measurement Using Transimpedance Amplifier (TIA) ADC Mode Using the ADPD1080**

In wearable devices developed for monitoring the health care of patients, it is often necessary to have synchronized measurements of biomedical signals. For example, a synchronous measurement of patient ECG and PPG can determine the pulse wave transit time (PWTT), which can then estimate blood pressure.

The circuit shown in Figure 78 shows a synchronous ECG and PPG measurement using the AD8233 and the ADPD1080. The AD8233 implements a two-pole high-pass filter (HPF) with a cutoff frequency at 0.3 Hz, and a two-pole low-pass filter (LPF) with a cutoff frequency of 37 Hz. The output of the AD8233 is fed

to one of the current inputs of the ADPD1080 through a 200 k $\Omega$  resistor to convert the voltage output of the AD8233 into a current.

The ADPD1080 is configured to alternately measure the photodiode signal and the ECG signal from the AD8233 on consecutive timeslots to provide fully synchronized PPG and ECG measurements. Data can be read out of the on-chip FIFO or straight from data registers. The ADPD1080 channel used to process the ECG signal is set up in TIA ADC mode, and the input bias voltage must be set to the 0.90 V setting using Bits[5:4] of Register 0x42 if the ECG signal is on Time Slot A, or Register 0x44 on Time Slot B. The TIA gain setting can be set to optimize the dynamic range of the signal path. The channel used to process the PPG signal is configured in its normal operating mode. Figure 77 shows a plot of a synchronized ECG and PPG measurement using the AD8233 with the ADPD1080.

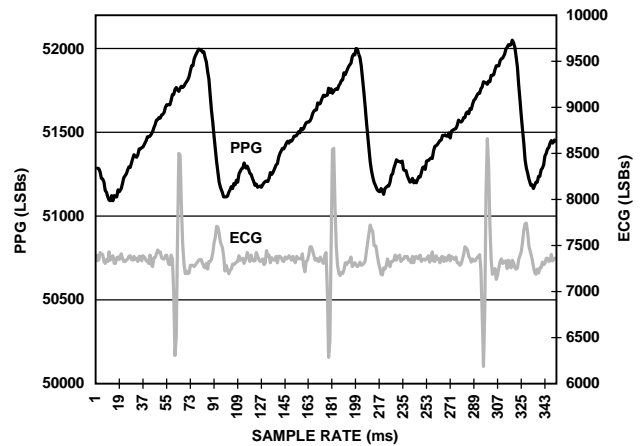


Figure 77. Plot of Synchronized ECG and PPG Waveforms

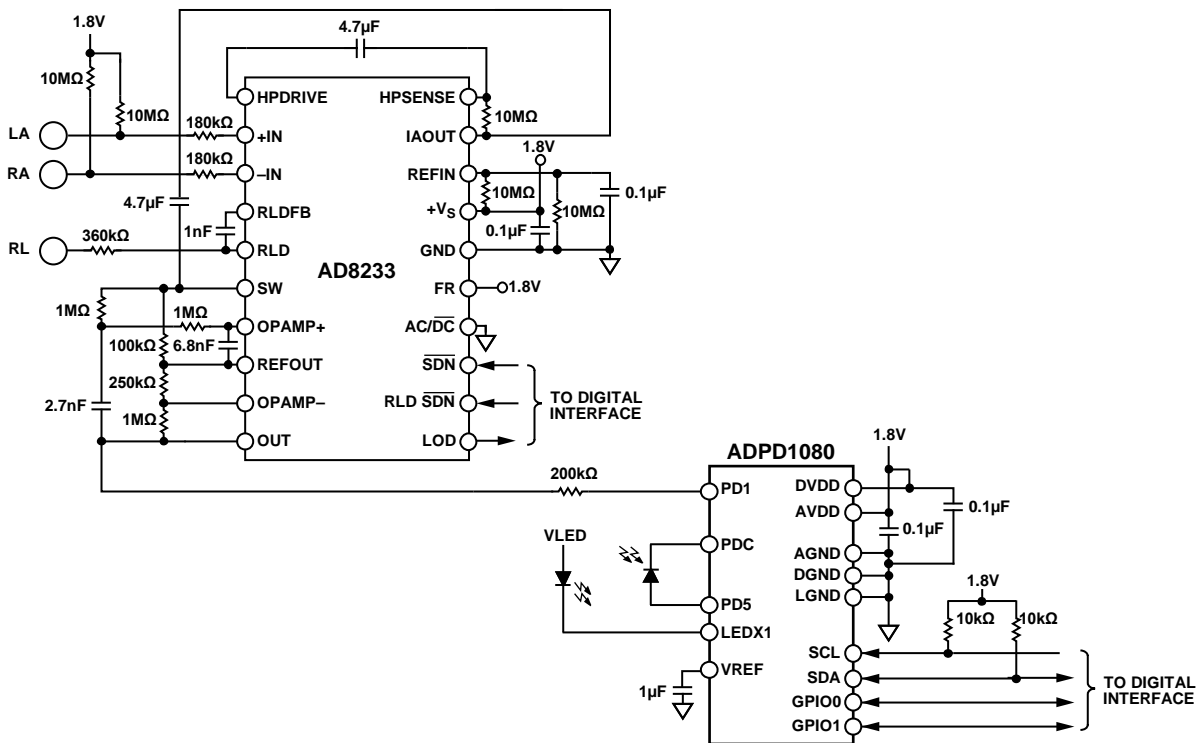


Figure 78. Synchronized PPG and ECG Measurement Using the ADPD1080 with the AD8233

## DIE INFORMATION

Die size: 2.080 mm × 1.745 mm

Die thickness: 150 μm

Bond Pad 16A and Pad 16B to GND. Bond Pad 17A and Pad 17B to +V<sub>s</sub>.

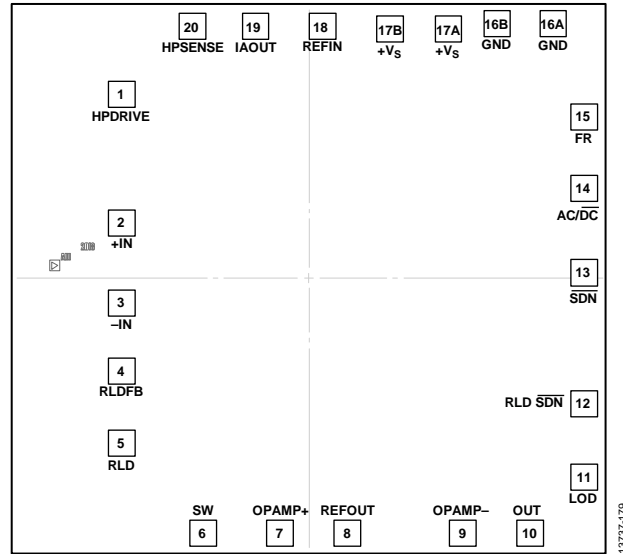


Figure 79. 20-Pad Bare Die Bond Pad Diagram

Table 8. Bond Pad Information

Pad No.	Mnemonic	Pad Coordinates <sup>1</sup>	
		X (μm)	Y (μm)
1	HPDRIVE	-630.5	+557
2	+IN	-630.5	+176.4
3	-IN	-630.5	-62.8
4	RLDFB	-630.5	-261.2
5	RLD	-630.5	-475.1
6	SW	-356	-758
7	OPAMP+	-98.45	-758
8	REFOUT	+127.95	-758
9	OPAMP-	+515.95	-758
10	OUT	+742.35	-758
11	LOD	+925.5	-575.45
12	RLD $\overline{\text{SDN}}$	+925.5	-359.05
13	$\overline{\text{SDN}}$	+925.5	+28
14	AC/DC	+925.5	+279.7
15	FR	+925.5	+490.6
16A	GND	+821.9	+765.5
16B	GND	+631.9	+765.5
17A	+V <sub>s</sub>	+467.8	+752.5
17B	+V <sub>s</sub>	+272.9	+752.5
18	REFIN	+45.35	+758
19	IAOUT	-181.05	+758
20	HPSENSE	-391.95	+758

<sup>1</sup> The pad coordinates indicate the center of each pad, referenced to the center of the die. The die orientation is indicated by the logo, as shown in Figure 79.

OUTLINE DIMENSIONS

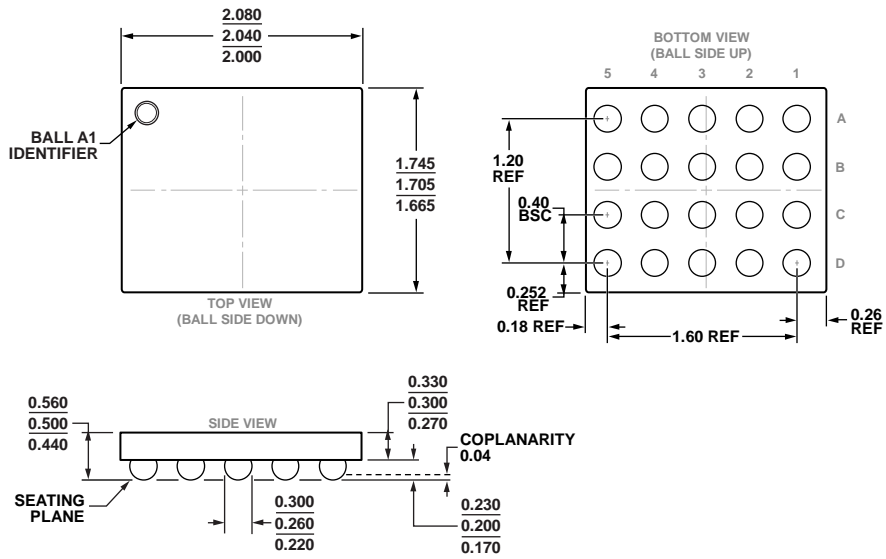


Figure 80. 20-Ball, Backside-Coated, Wafer Level Chip Scale Package [WLCSP] (CB-20-13)  
Dimensions shown in millimeters

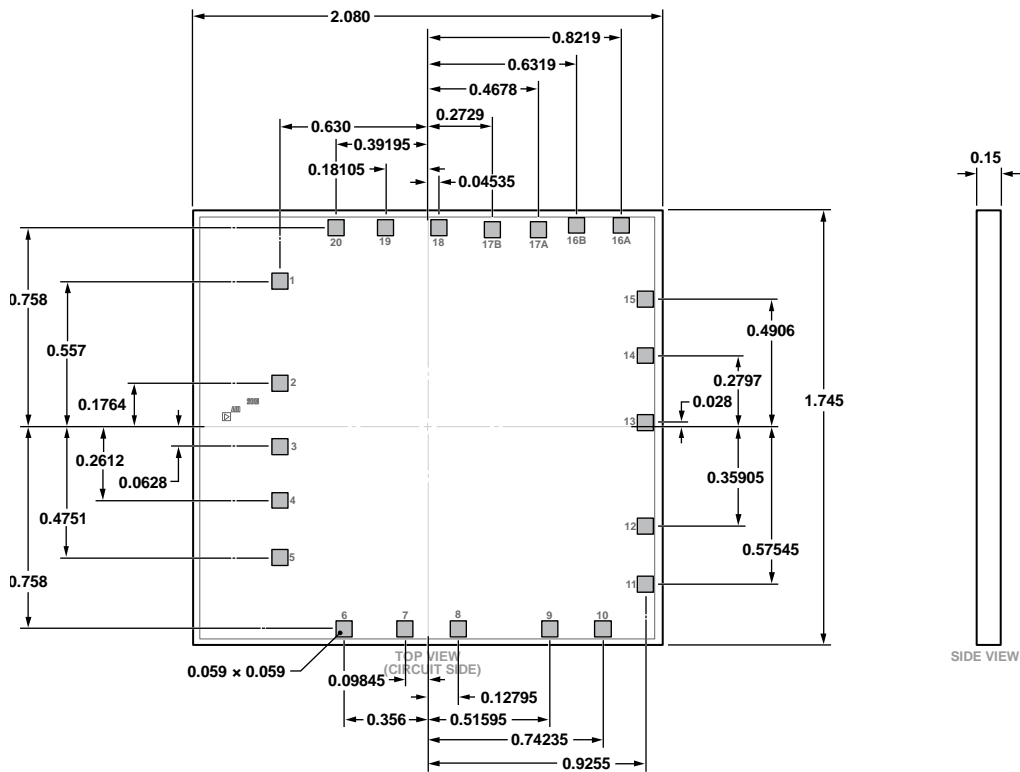


Figure 81. 20-Pad Bare Die [CHIP] (C-20-3)  
Dimensions shown in millimeters

**ORDERING GUIDE**

Model <sup>1</sup>	Temperature Range	Package Description	Package Option
AD8233ACBZ-R7	-40°C to +85°C	20-Ball, Backside-Coated, Wafer Level Chip Scale Package [WLCSP]	CP-20-13
AD8233C-DF	25°C	20-Pad Bare Die [CHIP], Die on Film Frame	C-20-3
AD8233CB-EBZ		Evaluation Board	

<sup>1</sup> Z = RoHS Compliant Part.