QUALCOMM®
CDMA Technologies

PM7540™ Power Management IC

Device Specification (Preliminary Information)

80-VD691-1 Rev. B

February 26, 2007

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Revision history

Bars appearing in the left margin of the document (as shown here) indicate changes made to this document since the last revision issued.

Revision	Date	Description
A	November 2006	Initial release
B	February 2007	Updated Table 3-25 for parameter for efficiency I_{load} Updated Table 3-37 for maximum short circuit current for vibration motor driver Updated Table 3-38 for: ■ Minimum input resistance ■ Minimum output voltage ■ Maximum output voltage ■ Minimum mute suppression rating

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1 Introduction

1.1 Documentation overview

Technical information for the PM7540 IC is contained in the four documents listed in Table 1-1. Each document is a self-contained document that describes certain IC functions and/or specifications. Therefore, for a thorough understanding of the IC and its applications you will need to study all four documents. The device description given in the next section is a good place to begin learning about the PM7540 IC. All PM7540 documents are available for downloading for the QUALCOMM CDMA Tech Support website (https://support.cdmatech.com).

Table 1-1 PM7540 documentation

Document #	Title / description
80-VD691-1 (this document)	*PM7540 Power Management IC Device Specification* The primary objective of this document is to convey all PM7540 electrical and mechanical specifications. Additional material includes pin assignment definitions, PCB mounting specifications, packing methods and materials, and part reliability. This document can be used by company purchasing departments to facilitate procurement.
80-VD691-3	*PM7540 Power Management IC User Guide* This document provides detailed descriptions of all PM75402 functions and interfaces, defining how to control the IC and explaining the resulting operating modes.
80-VD691-4	*PM7540 Power Management IC Revision Guide* This document provides a history of PM7540 IC revisions and changes to its device specification. It explains how to identify the various IC revisions, discusses known issues for each revision and how to work around them, and lists performance specification changes between each revision of the *PM7540 Power Management IC Device Specification* (80-VD691-1).
80-VD691-5	*PM7540 Power Management IC Design Guidelines* This document tries to anticipate and answer questions hardware engineers might have when incorporating the PM7540 IC into their wireless product designs. An example application is presented, then specific design topics, such as layout guidelines, power distribution recommendations, external component recommendations, troubleshooting techniques, (and more) are addressed.

This PM7540 Device Specification is organized as follows:

- Chapter 1 Provides an overview of PM7540 documentation, gives a high-level functional description of the PM7540 IC, lists the device features, and lists terms and acronyms used throughout this document.
- Chapter 2 Defines the IC pin assignments.
- Chapter 3 Defines the IC electrical performance specifications, including absolute maximum ratings and recommended operating conditions.
- Chapter 4 Defines the IC mechanical specifications, including dimensions, thermal characteristics, moisture sensitivity, and markings.
- Chapter 5 Presents procedures and specifications for mounting PM7540 ICs onto printed circuit boards (PCBs).
- Chapter 6 Discusses packing methods and materials for PM7540 shipments.
- Chapter 7 Presents PM7540 IC reliability data, including definition of the qualification samples and a summary of qualification test results.

1.2 Concise device description

The PM7540 device (Figure 1-1) integrates all wireless handset power management, general housekeeping, and user interface support functions into a single mixed signal IC. Its versatile design is suitable for CDMA and non-CDMA handsets, and other wireless products such as PC PDAs.

The power management portion accepts power from common sources—battery, external charger, adapter, USB_VBUS, coin cell backup—and generates all the regulated voltages needed to power the appropriate handset electronics. It monitors and controls the power sources, detecting which sources are applied, verifying that they are within acceptable operational limits, and coordinates battery and coin cell recharging while maintaining the handset electronics supply voltages.

On-chip voltage regulators generate 24 programmable output voltages using a combination of switched-mode power supplies and low-dropout voltage regulators, all derived from a common trimmed voltage reference. One regulator is dedicated for generating microphone bias voltages.

The device's general housekeeping functions include a 16-position analog multiplexer that has five internal connections, six hardwired external connections, and supports an additional 22 external connections. The internal connections are used to monitor on-chip functions such as the temperature sensor. The hardwired external connections access input power nodes such as VCHG, VBAT, etc. The 22 additional external connections are made using the IC's multipurpose pins that are configured as analog inputs and are routed through switch circuits to create five multiplexer inputs; these are available to monitor system parameters such as temperature and battery ID.

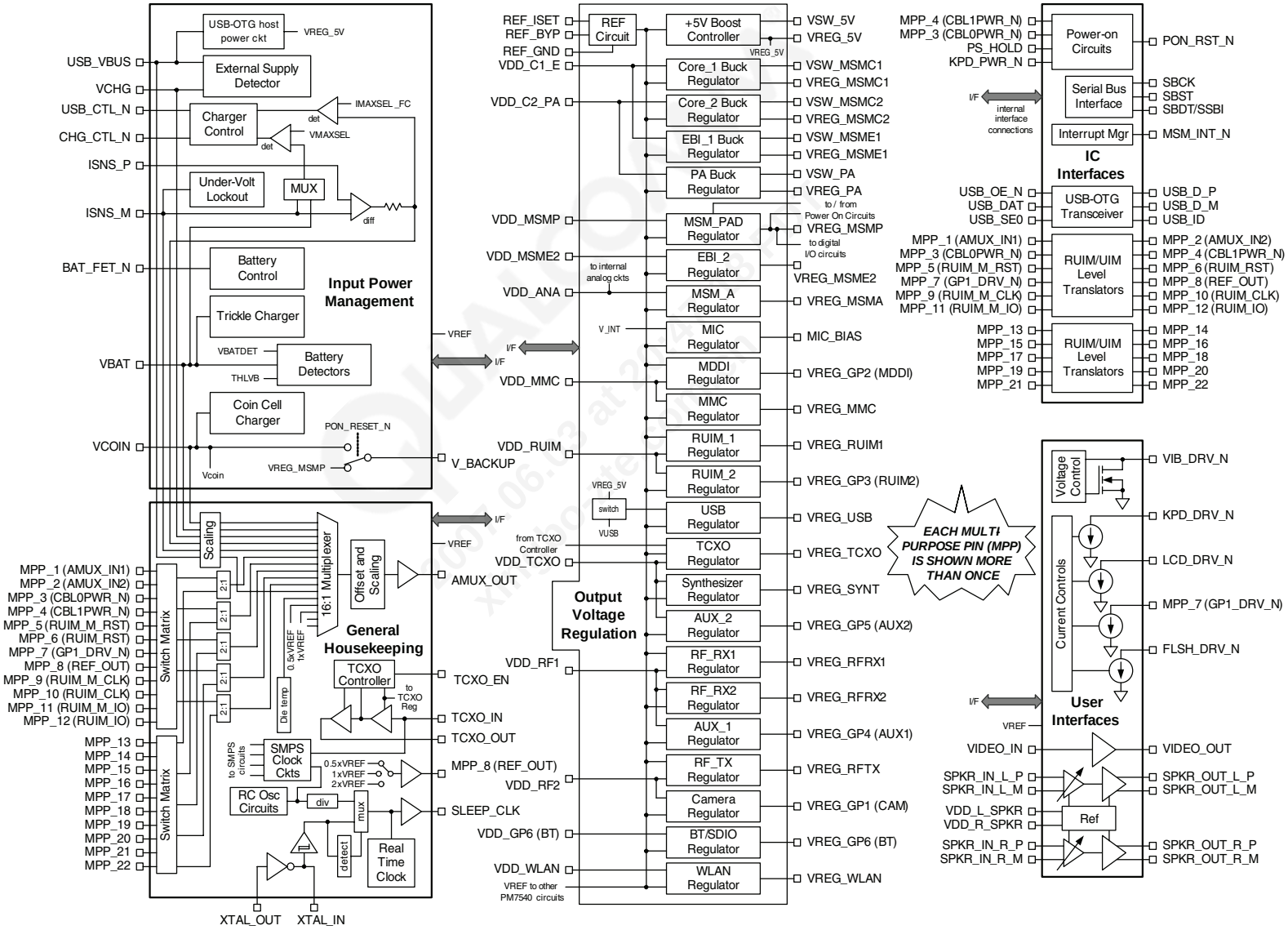

Figure 1-1 PM7540 functional block diagram

The multiplexer output signal's offset and gain is adjusted, then buffered and routed to the Mobile Station Modem™ (MSM™) device for analog-to-digital conversion. Various oscillator, clock, and counter circuits are provided to initialize and maintain valid pulse waveforms and measure time intervals for higher-level handset functions. A dedicated controller manages the TCXO warm-up and signal buffering, and key parameters are monitored to protect against detrimental conditions.

Handset-level user interfaces are also supported. The IC includes four backlight or LED drivers with brightness (current) control that could be used for keypad, LCD, camera flash, and general-purpose drivers. A vibration motor driver alerts handset users of incoming calls, and a two-channel speaker driver with volume control can be used for audio alerts or speakerphone and melody-ringer applications. The speaker circuits accept stereo differential, stereo single-ended, and mono differential inputs, and can be configured for stereo or mono outputs. A video amplifier is included that allows the handset to be used as a camcorder or for slide presentations.

IC-level interfaces include the configurable serial bus interface (SBI) used by the MSM device to control and status the PM7540 IC. This bus is supplemented by an interrupt manager for time-critical information. Another dedicated IC interface circuit monitors multiple trigger events and controls the power-on/power-off sequences. A universal serial bus/on-the-go (USB-OTG) transceiver is included for interfacing the MSM device to computers as a USB peripheral, or connecting the MSM device to other peripherals. Removable user identity module (RUIM) level translators enable MSM device interfacing with external modules.

The PM7540 IC is a mixed signal BiCMOS device and is available in the 137-pin chip scale package (137 CSP) that includes several center ground pins for electrical ground and thermal relief.

Because the PM7540 IC includes so many diverse functions, its operation is more easily understood by considering major functional blocks individually. Therefore, this document (and all PM7540 documents within the set) is organized by the following device functionality:

- Input power management
- Output voltage regulation
- General housekeeping
- User interfaces
- IC interfaces
- Multipurpose pins (which can be configured to function within some of the other categories)

Most of the information contained in this device specification is organized accordingly, including the circuit groupings within the block diagram (Figure 1-1), pin descriptions (Chapter 2), and detailed electrical specifications (Chapter 3).

See *PM7540 Power Management IC User Guide* (80-VD691-3) for much more detailed descriptions of each PM7540 function and interface.

1.3 IC features

- Complete power management, housekeeping, and user interface functions for wireless devices (CDMA, non-CDMA handsets, and PDAs)
- Input power management
  - Valid external supply attachment and removal detection
  - Supports unregulated (closed-loop) external charger supplies and USB supplies as input power sources
  - Supports lithium-ion main batteries
  - Trickle, constant current, constant voltage, and pulsed charging of the main battery
  - Supports coin cell backup battery (including charging)
  - Battery voltage detectors with programmable thresholds
  - VDD collapse protection
  - Charger current regulation and real-time monitoring for over-current protection
  - Charger transistor protection by power limit control
  - Control drivers for two external pass transistors and one external battery MOSFET (MOSFET is optional)
  - Voltage, current, and power control loops
  - Automated recovery from sudden momentary power loss
- Output voltage regulation
  - One boost (step-up) switched-mode power supply (SMPS) for driving white LEDs and hosting USB-OTG
  - Four buck (step-down), switched-mode power supplies for efficiently generating MSMC1, MSMC2, MSME, and PA supply voltages
  - Supports dynamic voltage scaling (DVS) for MSMC1, MSMC2, and PA outputs
  - 18 low-dropout regulator circuits with programmable output voltages, implemented using three different current ratings: 300 mA (four), 150 mA (ten), and 50 mA (four). These can be used to power MSMA, MSMP, MSME2, MMC, RFRX1, RFRX2, RFTX, TCXO, SYNT, RUIM1, RUIM2, USB, WLAN, MDDI, CAM, BT, AUX1, and AUX2 circuits.
  - One MIC bias regulator circuit
  - All regulators can be individually enabled/disabled for power savings
  - Low power mode available on most regulators
  - All regulated outputs are derived from a common bandgap reference (close tracking)

- Integrated handset-level housekeeping functions reduces external parts count, size, and cost
  - Analog multiplexer selects from five internal and up to 28 external inputs
  - Multiplexer output's offset and gain are adjusted, increasing the effective ADC resolution
  - Adjusted multiplexer output is buffered and routed to an MSM device ADC
  - Dual oscillators: a 32.768 kHz off-chip crystal and an on-chip RC assure MSM device sleep clock
  - Crystal oscillator detector and automated switch-over upon lost oscillation
  - Real-time clock for tracking time and generating associated alarms
  - On-chip adjustments minimize crystal oscillator frequency errors
  - Control TCXO warm-up and synchronize, deglitch, and buffer the TCXO signal
  - TCXO buffer control for optimal QPH/catnap timing
  - Multistage over temperature protection (smart thermal control)
- Integrated handset-level user interfaces
  - Four programmable current sinks recommended as keypad backlight, LCD backlight, camera flash, and general-purpose drivers
  - Vibration motor driver programmable from 1.2 to 3.1 V in 100 mV increments
  - Two-channel speaker driver with programmable gain, turn-on time, and muting; configurable inputs and outputs capable of stereo or mono operation (drives external 8-Ω speakers with volume controlled 500 mW, each channel)
  - Video (TV) amplifier allows use as a camcorder or for slide presentations
- IC-level interfaces
  - Configurable SBI (three-wire or single-wire) for efficient initialization, status, and control
  - Supports MSM interrupt processing with an internal interrupt manager
  - Many functions monitored and reported through real-time and interrupt status signals
  - Dedicated circuits for controlled power-on sequencing, including the MSM device's reset signal
  - Several events continuously monitored for triggering poweron/poweroff sequences
  - Supports and orchestrates soft resets
  - USB-OTG transceiver for full-speed (12 Mb/s) and low-speed (1.5 Mb/s) interfacing of the MSM device to computers as a USB peripheral, or connecting the MSM device to other peripherals
  - Two sets of RUIM level translators enable MSM device interfacing with external modules

- 22 multipurpose pins that can be configured as digital or analog I/Os, bidirectional I/Os, or current sinks; default functions support the two sets of RUIM level translators, power-on circuits, analog multiplexer inputs, an LED driver, and a selectable reference voltage output
- Highly integrated functionality in a small package - 137-pin CSP with a several center ground pins for electrical ground, mechanical stability, and thermal relief

1.4 Terms and acronyms

The following table defines terms and acronyms used throughout this document.

Table 1-2 Terms and acronyms

Term or acronym	Definition
ADC	Analog-to-digital converter
API	Application programming interface
CDMA	Code Division Multiple Access
CSP	Chip scale package
EBI	External bus interface
HAST	Highly accelerated stress test
HIC	Humidity indicator card
HTOL	High-temperature operating life
ID	Identification
Li	Lithium
MBB	Moisture barrier bag
MPP	Multipurpose pin
MSL	Moisture sensitivity level
MSM	Mobile Station Modem (trademarked by QUALCOMM)
MUX	Multiplexer
OTG	On-the-go
PA	Power amplifier
PBM	Pulse burst modulation
PCB	Printed circuit board
PDA	Personal digital assistant
PFM	Pulse frequency modulation
PLL	Phase-locked loop
PM	Power management
PWM	Pulse width modulation
QCT	QUALCOMM CDMA Technologies division
RUIM	Removable user identity module

Table 1-2 Terms and acronyms (continued)

Term or acronym	Definition
SBI	Serial bus interface (3-wire unless designated as SSBI)
SiGe	Silicon germanium
SMPS	Switched-mode power supply (DC-to-DC converter)
SMT	Surface mount technology
SnPb	Tin/lead
SSBI	Single-wire serial bus interface
support.cdmatech.com	QCT website address for technical assistance
TCXO	Temperature-compensated crystal oscillator
USB	Universal serial bus
VCO	Voltage-controlled oscillator
VCTCXO	Voltage-controlled temperature-compensated crystal oscillator
Zero-IF or ZIF	Zero intermediate frequency; a radio architecture that converts received signals directly from RF to baseband, thereby eliminating the intermediate frequency necessary in super-heterodyne receivers. The transmit signals likewise eliminate the Tx IF, upconverting directly from baseband to RF.

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2 Pin Definitions

The PM7540 IC is available in the 137-pin chip-scale package (137 CSP) that includes several center ground pins for electrical grounding, mechanical strength, and thermal continuity. Pin assignments are illustrated in Figure 2-1, listed in Table 2-1, and described in Table 2-2 through Table 2-9.

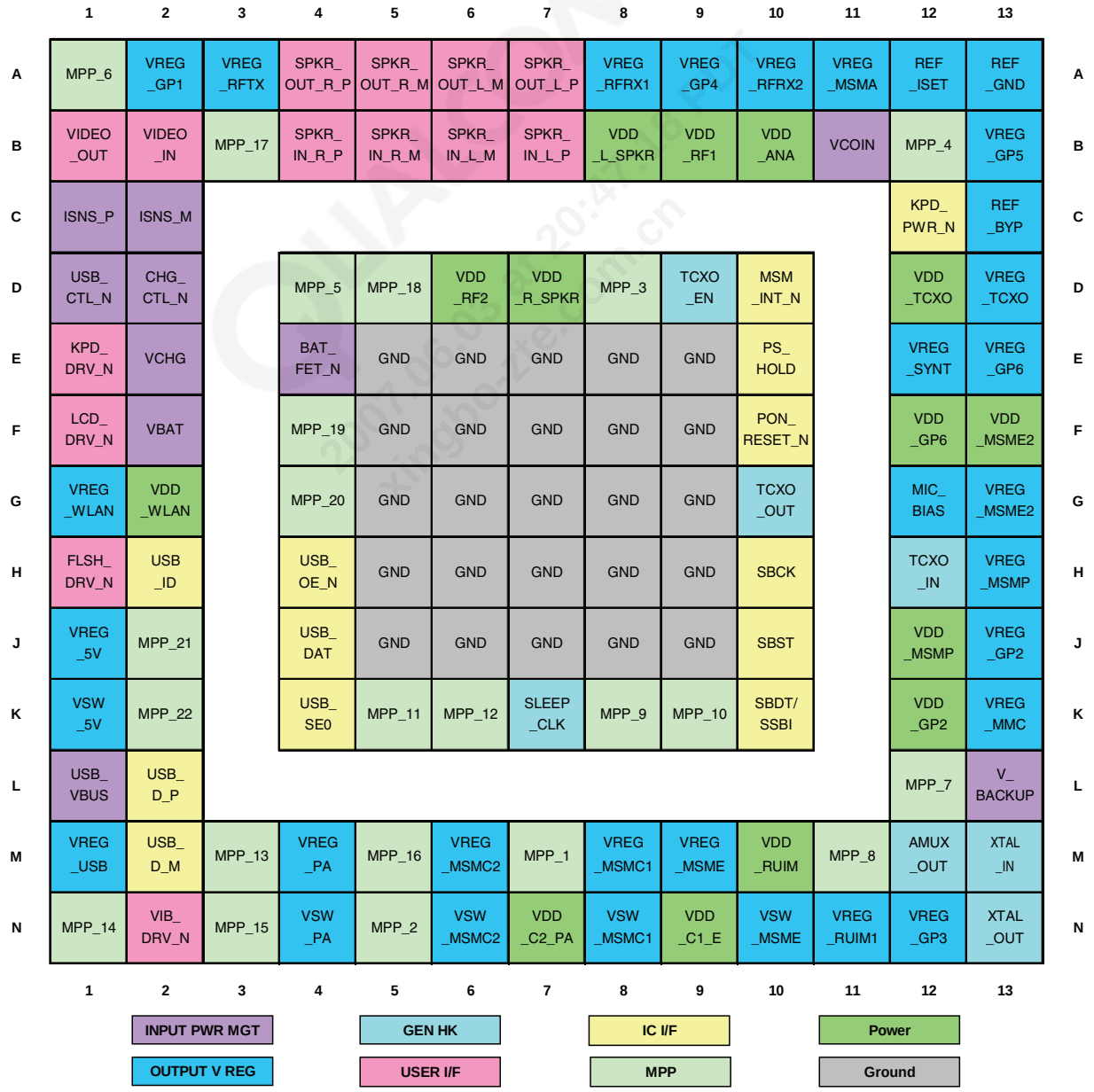

Figure 2-1 PM7540 IC pin assignments (top view)

Table 2-1 PM7540 IC pin descriptions - listed in alpha-numeric order [1]

Pin	Pin name [2]	Fcn [3]	Pin	Pin name	fcn [3]	Pin	Pin name	fcn [3]
A1	MPP_6 (RUIM_RST)	MPP/ICI	D8	MPP_3 (CBL0PWR_N)	MPP/ICI	G12	MIC_BIAS	OVR
A2	VREG_GP1 (CAM)	OVR	D9	TCXO_EN	GH	G13	VREG_MSME2	OVR
A3	VREG_RFTX	OVR	D10	MSM_INT_N	ICI	H1	FLSH_DRV_N	UI
A4	SPKR_OUT_R_P	UI	D12	VDD_TCXO	PWR	H2	USB_ID	ICI
A5	SPKR_OUT_R_M	UI	D13	VREG_TCXO	OVR	H4	USB_OE_N	ICI
A6	SPKR_OUT_L_M	UI	E1	KPD_DRV_N	UI	H5	GND	GND
A7	SPKR_OUT_L_P	UI	E2	VCHG	IPM	H6	GND	GND
A8	VREG_RFRX1	OVR	E4	BAT_FET_N	IPM	H7	GND	GND
A9	VREG_GP4 (AUX1)	OVR	E5	GND	GND	H8	GND	GND
A10	VREG_RFRX2	OVR	E6	GND	GND	H9	GND	GND
A11	VREG_MSMA	OVR	E7	GND	GND	H10	SBCK	ICI
A12	REF_ISET	OVR	E8	GND	GND	H12	TCXO_IN	GH
A13	REF_GND	OVR	E9	GND	GND	H13	VREG_MSMP	OVR
B1	VIDEO_OUT	UI	E10	PS_HOLD	ICI	J1	VREG_5V	OVR
B2	VIDEO_IN	UI	E12	VREG_SYNT	OVR	J2	MPP_21	MPP
B3	MPP_17	MPP	E13	VREG_GP6 (BT)	OVR	J4	USB_DAT	ICI
B4	SPKR_IN_R_P	UI	F1	LCD_DRV_N	UI	J5	GND	GND
B5	SPKR_IN_R_M	UI	F2	VBAT	IPM	J6	GND	GND
B6	SPKR_IN_L_M	UI	F4	MPP_19	MPP	J7	GND	GND
B7	SPKR_IN_L_P	UI	F5	GND	GND	J8	GND	GND
B8	VDD_L_SPKR	PWR	F6	GND	GND	J9	GND	GND
B9	VDD_RF1	PWR	F7	GND	GND	J10	SBST	ICI
B10	VDD_ANA	PWR	F8	GND	GND	J12	VDD_MSMP	PWR
B11	VCOIN	IPM	F9	GND	GND	J13	VREG_GP2 (MDDI)	OVR
B12	MPP_4 (CBL1PWR_N)	MPP/ICI	F10	PON_RESET_N	ICI	K1	VSW_5V	OVR
B13	VREG_GP5 (AUX2)	OVR	F12	VDD_GP6 (BT)	PWR	K2	MPP_22	MPP
C1	ISNS_P	IPM	F13	VDD_MSME2	PWR	K4	USB_SE0	ICI
C2	ISNS_M	IPM	G1	VREG_WLAN	OVR	K5	MPP_11 (RUIM_M_IO)	MPP/ICI
C12	KPD_PWR_N	ICI	G2	VDD_WLAN	PWR	K6	MPP_12 (RUIM_IO)	MPP/ICI
C13	REF_BYP	OVR	G4	MPP_20	MPP	K7	SLEEP_CLK	GH
D1	USB_CTL_N	IPM	G5	GND	GND	K8	MPP_9 (RUIM_M_CLK)	MPP/ICI
D2	CHG_CTL_N	IPM	G6	GND	GND	K9	MPP_10 (RUIM_CLK)	MPP/ICI
D4	MPP_5 (RUIM_M_RST)	MPP/ICI	G7	GND	GND	K10	SBDT/SSBI	ICI
D5	MPP_18	MPP	G8	GND	GND	K12	VDD_GP2 (MDDI)	PWR
D6	VDD_RF2	PWR	G9	GND	GND	K13	VREG_MMC	OVR
D7	VDD_R_SPKR	PWR	G10	TCXO_OUT	GH	L1	USB_VBUS	IPM

Table 2-1 PM7540 IC pin descriptions - listed in alpha-numeric order [1] (continued)

Pin	Pin name [2]	Fcn [3]	Pin	Pin name	fcn [3]	Pin	Pin name	fcn [3]
L2	USB_D_P	ICI	M8	VREG_MSMC1	OVR	N5	MPP_2 (AMUX_IN2)	MPP/GH
L12	MPP_7 (GP1_DRV_N)	MPP/UI	M9	VREG_MSME	OVR	N6	VSW_MSMC2	OVR
L13	V_BACKUP	IPM	M10	VDD_RUIM	PWR	N7	VDD_C2_PA	PWR
M1	VREG_USB	OVR	M11	MPP_8 (REF_OUT)	MPP/GH	N8	VSW_MSMC1	OVR
M2	USB_D_M	ICI	M12	AMUX_OUT	GH	N9	VDD_C1_E	PWR
M3	MPP_13	MPP	M13	XTAL_IN	GH	N10	VSW_MSME	OVR
M4	VREG_PA	OVR	N1	MPP_14	MPP	N11	VREG_RUIM1	OVR
M5	MPP_16	MPP	N2	VIB_DRV_N	UI	N12	VREG_GP3 (RUIM2)	OVR
M6	VREG_MSMC2	OVR	N3	MPP_15	MPP	N13	XTAL_OUT	GH
M7	MPP_1 (AMUX_IN1)	MPP/GH	N4	VSW_PA	OVR			

1 More detailed descriptions of all I/Os are given below, organized according to the functional groups identified in note 3.

2 All MPPs are configurable as explained in Section 3.4; the intended functions of MPP_1 through MPP_12 are included in their pin name column entries.

3 Functional groups are:

GH = general housekeeping GND = ground ICI = IC-level interfaces IPM = input power mgmt
MPP = multipurpose pin OVR = output V regulation PWR = power supply UI = user interface

PM7540 pins are grouped according to their functionality (as defined in Table 2-1) and described below. Each functional grouping is presented in its own table:

Table 2-2 Input power management

Table 2-3 Output voltage regulation

Table 2-4 General housekeeping

Table 2-5 User interfaces

Table 2-6 IC-level interfaces

Table 2-7 Multipurpose pins

Table 2-8 Power supply pins

Table 2-9 Ground pins

Table 2-2 Input power management pin descriptions

Pin #	Pin name	Pin type [1]	Functional description
E2	VCHG	AI	A valid analog voltage at this pin is recognized by the PM7540 IC to be an external supply, and factors into the IC's power management operating mode. Connect an immediate 1.0 µF capacitor to ground and a 10k resistor to ground.
D2	CHG_CTL_N	AO	Control signal for the external pass transistor – a low voltage turns on the pass transistor. This signal is pulled-up internally to V_{CHG} or V_{DD} depending upon the selected PM7540 operating mode.
L1	USB_VBUS	AI, AO	This pin is configured as an analog input or an analog output depending upon the type of peripheral device connected. Connect an immediate 2.2 µF capacitor to ground and a 47k resistor to ground.
D1	USB_CTL_N	AO	Control signal for the external USB pass transistor - a low voltage turns on the pass transistor. This signal is pulled-up internally to the higher of two voltages, USB_VBUS or V_{DD}.
C1	ISNS_P	AI	The positive current sensor input – connect to the pass transistor side of the sense resistor.
C2	ISNS_M	AI	The negative current sensor input – connect to the V_{DD} side of the sense resistor. Also used to monitor and/or regulate the V_{DD} voltage.
E4	BAT_FET_N	AO	Control signal to the external battery MOSFET; connect directly to its gate. The resulting operation depends upon whether an external supply is present - the battery can charge or provide phone power through the MOSFET.
F2	VBAT	AI, AO	Monitors the battery voltage; connect directly to the battery plus (+) terminal. Also used as an analog output that sources trickle charging current for the battery.
B11	VCOIN	AI, AO	Connection to the optional coin cell. If present, provides backup power to the crystal oscillator and real time clock circuits to maintain time and alarm functions if a valid external supply or main battery is not connected. Used as an analog output for coin cell or capacitor charging.
L13	V_BACKUP	AO	Connect this pin to the SRAM supply pin(s). An internal switch determines the SRAM power source as follows: • VREG_MSMP powers SRAM when the PM7540 IC is on (when PON_RESET_N is high). • The coin cell (VCOIN) powers SRAM when the PM7540 IC is in one of its off states.

[1] Pin type is AI = analog input or AO = analog output.

Table 2-3 Output voltage regulation pin descriptions

Pin #	Pin name	Pin type [1]	Functional description
SMPS connections			
K1	VSW_5V	AO	Switching output of the +5 V boost (step-up) SMPS circuit.
J1	VREG_5V	AI	Senses the regulated output of the +5 V boost SMPS; bypass this pin with a 10 µF ceramic capacitor.
N8	VSW_MSMC1	AO	Switching output of the MSM core_1 buck (step-down) SMPS circuit.
M8	VREG_MSMC1	AI	Senses the regulated output of the core_1 buck SMPS; bypass this pin with a 4.7 µF ceramic capacitor.
N6	VSW_MSMC2	AO	Switching output of the MSM core_2 buck (step-down) SMPS circuit.
M6	VREG_MSMC2	AI	Senses the regulated output of the core_2 buck SMPS; bypass this pin with a 4.7 µF ceramic capacitor.
N10	VSW_MSME	AO	Switching output of the EBI_1 buck (step-down) SMPS circuit.
M9	VREG_MSME	AI	Senses the regulated output of the EBI_1 buck SMPS; bypass this pin with a 4.7 µF ceramic capacitor.
N4	VSW_PA	AO	Switching output of the PA buck (step-down) SMPS circuit.
M4	VREG_PA	AI	Senses the regulated output of the PA buck SMPS; bypass this pin with a 4.7 µF ceramic capacitor.
Linear regulator outputs			
A2	VREG_GP1 (CAM)	AO	General-purpose linear regulator output #1 intended to power camera circuits or others. Bypass this pin with a 2.2 µF ceramic capacitor. The VDD_ RF2 voltage powers the GP1 (CAM) regulator circuits.
J13	VREG_GP2 (MDDI)	AO	General-purpose linear regulator output #2 intended to power MDDI circuits or others. Bypass this pin with a 2.2 µF ceramic capacitor. The VDD_GP2 (MDDI) voltage powers the GP2 (MDDI) regulator circuits.
N12	VREG_GP3 (RUIM2)	AO	General-purpose linear regulator output #3 intended to power RUIM_2 circuits or others. Bypass this pin with a 2.2 µF ceramic capacitor. The VDD_RUIM voltage powers the GP3 (RUIM_2) regulator circuits.
A9	VREG_GP4 (AUX1)	AO	General-purpose linear regulator output #4 intended to power AUX_1 circuits or others. Bypass this pin with a 1.0 µF ceramic capacitor. The VDD_ RF1 voltage powers the GP4 (AUX1) regulator circuits.
B13	VREG_GP5 (AUX2)	AO	General-purpose linear regulator output #5 intended to power AUX_2 circuits or others. Bypass this pin with a 2.2 µF ceramic capacitor. The VDD_ TCXO voltage powers the GP5 (AUX2) regulator circuits.
E13	VREG_GP6 (BT)	AO	General-purpose linear regulator output #6 intended to power BT circuits or others. Bypass this pin with a 4.7 µF ceramic capacitor. The VDD_ GP6 (BT) voltage powers the GP6 (BT) regulator circuits.
K13	VREG_MMC	AO	Linear regulator output intended to power MMC circuits or others. Bypass this pin with a 2.2 µF ceramic capacitor. The VDD_GP2 (MDDI) voltage powers the MMC regulator circuits.
A11	VREG_MSMA	AO	Linear regulator output intended to power the MSM device analog functions; not recommended as a general-purpose regulated power source. Bypass this pin with a 4.7 µF ceramic capacitor and connect directly to MSM V_{DDA} pins. The VDD_ANA voltage powers the MSMA regulator circuits.

Table 2-3 Output voltage regulation pin descriptions (continued)

Pin #	Pin name	Pin type [1]	Functional description
G13	VREG_MSME2	AO	Linear regulator output intended to power EBI_2 circuits or others. Bypass this pin with a 2.2 µF ceramic capacitor. The VDD_MSME2 voltage powers the MSME2 regulator circuits.
H13	VREG_MSMP	AO	Linear regulator output intended to power the MSM peripheral functions; not recommended as a general-purpose regulated power source. Bypass this pin with a 4.7 µF ceramic capacitor and connect directly to MSM V_{DDP} pins. The VDD_MSMP voltage powers the MSMP regulator circuits.
A8	VREG_RFRX1	AO	Linear regulator output intended to power primary receiver circuits or others. Bypass this pin with a 2.2 µF ceramic capacitor. The VDD_RF1 voltage powers the RFRX1 regulator circuits.
A10	VREG_RFRX2	AO	Linear regulator output intended to power diversity receiver circuits or others. Bypass this pin with a 2.2 µF ceramic capacitor. The VDD_RF1 voltage powers the RFRX2 regulator circuits.
A3	VREG_RFTX	AO	Linear regulator output intended to power transmitter circuits or others. Bypass this pin with a 2.2 µF ceramic capacitor. The VDD_RF2 voltage powers the RFTX regulator circuits.
N11	VREG_RUIM1	AO	Linear regulator output intended to power RUIM_1 circuits or others. Bypass this pin with a 2.2 µF ceramic capacitor. The VDD_RUIM voltage powers the RUIM_1 regulator circuits.
E12	VREG_SYNT	AO	Linear regulator output intended to power frequency synthesizer circuits or others. Bypass this pin with a 1.0 µF ceramic capacitor. The VDD_TCXO voltage powers the SYNT regulator circuits.
D13	VREG_TCXO	AO	Linear regulator output intended to power VCTCXO circuits (plus others if desired). Bypass this pin with a 1.0 µF ceramic capacitor. The TCXO regulator circuits are powered by the VDD_TCXO voltage and are enabled by the TCXO controller.
M1	VREG_USB	AO	Linear regulator output intended to power the internal USB transceiver; not recommended as a general-purpose regulated power source. Bypass this pin with a 1.0 µF ceramic capacitor. Power to the USB regulator circuits is either VREG_5V or USB_VBUS (software selectable).
G1	VREG_WLAN	AO	Linear regulator output intended to power WLAN circuits or others. Bypass this pin with a 2.2 µF ceramic capacitor. The VDD_WLAN voltage powers the WLAN regulator circuits.
G12	MIC_BIAS	AO	Linear regulator output intended to bias MIC circuits. Bypass this pin with a 1.0 µF ceramic capacitor. An internal PM7540 voltage powers the MIC_BIAS regulator circuits.
Voltage reference			
A12	REF_ISET	AI	Connect this pin to a 121k, ± 1% resistor with its other side connected as directly as possible to pin A13 (REF_GND).
A13	REF_GND	AI	Ground for the internal reference - connect as directly as possible to the handset's reference ground.
C13	REF_BYP	AO	Connect this pin to a 0.1 µF ceramic capacitor with its other side connected as directly as possible to pin A13 (REF_GND). This capacitor is part of a lowpass filter for the internal reference. Do not load this pin with external circuitry.

[1] Pin type is AI = analog input or AO = analog output.

Table 2-4 General housekeeping pin descriptions

Pin #	Pin name	Pin type [1]	Functional description
H12	TCXO_IN	AI	Input from the handset VCTCXO - analog (sinusoidal) or CMOS logic levels. External AC-coupling required.
D9	TCXO_EN	DI	Control signal from MSM device that enables TCXO controller tasks.
G10	TCXO_OUT	DO	Buffered and validated VCTCXO output clock signal - CMOS logic levels compatible with MSM devices.
M13	XTAL_IN	AI	Connect the 32.768 kHz crystal across these pins with capacitors from each pin to ground. Capacitor values depend upon the crystal. An external 32.768 kHz oscillator module may be used.
N13	XTAL_OUT	AO	
K7	SLEEP_CLK	DO	Buffered 32.768 kHz sleep clock signal; connect to MSM device sleep clock input.
M12	AMUX_OUT	AO	Output of the analog multiplexer. Connect directly to one of the MSM HKADC input pins.
M7	MPP_1 (AMUX_IN1)	AI	These are multipurpose pins whose intended functions are the first and second external inputs to the analog multiplexer (battery ID and temperature sensor, respectively). Further descriptions of multipurpose pins are given in the *PM7540 Power Management IC User Guide* (80-VD691-3) and in Table 2-7 of this document.
N5	MPP_2 (AMUX_IN2)	AI	
M11	MPP_8 (REF_OUT)	AO	This is a multipurpose pin whose intended function is a selectable, buffered version of the internal reference voltages (0.5 x VREF, 1 x VREF, or 2 x VREF). Further descriptions of multipurpose pins are given in the *PM7540 Power Management IC User Guide* (80-VD691-3) and in Table 2-7 of this document.

[1] Pin type is AI = analog input; AO = analog output; DI = digital input; or DO = digital output.

Table 2-5 User interface pin descriptions

Pin #	Pin name	Pin type [1]	Functional description
B6	SPKR_IN_L_M	AI	Minus and plus inputs to the left speaker driver circuit. These pins are biased internally and require AC-coupling. Intended for differential inputs, but can be driven single-ended with the unused input AC-coupled to ground.
B7	SPKR_IN_L_P	AI	
A6	SPKR_OUT_L_M	AO	Minus and plus outputs from the left speaker driver circuit. Connect directly to the speaker's (-) and (+) terminals.
A7	SPKR_OUT_L_P	AO	
B4	SPKR_IN_R_P	AI	Plus and minus inputs to the right speaker driver circuit. These pins are biased internally and require AC-coupling. Intended for differential inputs, but can be driven single-ended with the unused input AC-coupled to ground.
B5	SPKR_IN_R_M	AI	
A4	SPKR_OUT_R_P	AO	Plus and minus outputs from the right speaker driver circuit. Connect directly to the speaker's (+) and (-) terminals.
A5	SPKR_OUT_R_M	AO	
B2	VIDEO_IN	AI	Video (TV) amplifier input; driven by the MSM device's TVOUT signal.
B1	VIDEO_OUT	AO	Video (TV) amplifier output; capable of driving shielded cable and a standard 150-Ω TV load.
N2	VIB_DRV_N	AO	Vibration motor driver output - connect to the vibration motor negative terminal. The positive terminal of the motor connects to V_{DD}.
E1	KPD_DRV_N	AO	Programmable current sink intended to support keypad backlights or other functions.
F1	LCD_DRV_N	AO	Programmable current sink intended to support LCD backlights or other functions.
H1	FLSH_DRV_N	AO	Programmable current sink intended to support a camera flash strobe or other functions. This driver has a programmable timer, generates high-current pulses to drive several white LEDs in parallel (each powered off +5 V), and is suitable for a digital camera flash strobe.
L12	MPP_7 (GP1_DRV_N)	AO	This is a multipurpose pin whose intended function is the programmable current sink intended to support general-purpose LED or backlight devices. Further descriptions of multipurpose pins are given in the *PM7540 Power Management IC User Guide* (80-VD691-3) and in Table 2-7 of this document.

[1] Pin type is AI = analog input or AO = analog output.

Table 2-6 IC-level interface pin descriptions

Pin #	Pin name	Pin type [1]	Functional description
Power-on circuit connections			
C12	KPD_PWR_N	AI	Connect to the keypad power button; it is pulled-up internally. Pulling this pin low triggers a power-on sequence.
F10	PON_RESET_N	DO	Connect this pin to the MSM device's RESIN_N pin. During a PMIC power-on sequence, this signal is driven low to initiate an MSM power-on reset. This signal is driven high when an internal counter times out, releasing the MSM power-on reset command.
E10	PS_HOLD	DI	Connect this pin to the MSM device's PS_HOLD output pin. During a PMIC power-on sequence, the MSM device must drive this signal high before an internal counter expires or the PMIC will return the handset to the off state. Once the PMIC is powered on, the MSM device keeps the PMIC on by continuing to drive this signal high. The MSM device requests the PMIC to power-down the handset by driving this signal low.
D8	MPP_3 (CBL0PWR_N)	DI	These two pins are multipurpose pins with the intended function of recognizing a serial cable insertion and initiating the power-on sequence. Both pins are pulled-up internally; both must be pulled to logic low to initiate the power-on sequence. An interrupt is generated for any logic level transition on either pin. Further descriptions of multipurpose pins are given in the *PM7540 Power Management IC User Guide* (80-VD691-3) and in Table 2-7 of this document.
B12	MPP_4 (CBL1PWR_N)	DI	
Serial bus interface and MSM interrupt			
J10	SBST	DI	Configurable SBI: For earlier MSM devices: 3-line serial bus interface (SBI) – data, clock, and strobe signals. The data signal is bidirectional – an open drain driver when configured as an output and a CMOS gate when configured as an input. Strobe and clock are configured as CMOS gate inputs. For later MSM devices: single-wire SBI (SSBI). This configuration communicates over pin K10 only, with pin J10 connected to VREG_MSMP and pin H10 connected to ground.
H10	SBCK	DI	
K10	SBDT/SSBI	DI, DO	
D10	MSM_INT_N	DO	PMIC interrupt status is reported to the MSM device using this signal. Logic low signals that an interrupt event has occurred. The signal stays low until all interrupts are cleared or masked by the MSM device.

Table 2-6 IC-level interface pin descriptions (continued)

Pin #	Pin name	Pin type [1]	Functional description
USB interface			
H2	USB_ID	AI	Analog input used to sense whether a peripheral device is connected, and if connected, to determine the peripheral type.
L2	USB_D_P	DI, DO, AO	Plus (+) line of the differential, bidirectional USB signal to/from the peripheral device. This line complements pin M2 (USB_D_M). Inputs are Schmitt-triggered levels; outputs can be configured as digital logic levels or analog (audio) signals.
M2	USB_D_M	DI, DO, AO	Minus (-) line of the differential, bidirectional USB signal to/from the peripheral device. This line complements pin L2 (USB_D_P). Inputs are Schmitt-triggered levels; outputs can be configured as digital logic levels or analog (audio) signals.
H4	USB_OE_N	DI	USB output enable signal (active LOW); driven by an MSM GPIO pin programmed for the USB_TX_OE_N function.
J4	USB_DAT	DI, DO	Plus (+) line of the digital differential, bidirectional USB signal to/from the MSM device. This line complements pin K4 (USB_SE0). Signal levels are translated between MSM and USB domains within the PMIC.
K4	USB_SE0	DI, DO	Minus (-) line of the digital differential, bidirectional USB signal to/from the MSM device. This line complements pin J4 (USB_DAT). Signal levels are translated between MSM and USB domains within the PMIC.
RUIM/USIM level translators			
K5 K6	MPP_11 (RUIM_M_IO) MPP_12 (RUIM_IO)	DI, DO DI, DO	Any of the six MPP pairs can be configured as a bidirectional level translator. This pair's intended configuration is the bidirectional RUIM I/O level translator, with MPP_11 (pin K5) on the MSM side and MPP_12 (pin K6) on the RUIM side. Both sides are pulled-up internally, with MPP_11 pulled to VREG_MSME or VREG_MSMP (configurable) and MPP_12 pulled to VREG_RUIM. Further descriptions of multipurpose pins are given in the *PM7540 Power Management IC User Guide* (80-VD691-3) and in Table 2-7 of this document.
K8 K9	MPP_9 (RUIM_M_CLK) MPP_10 (RUIM_CLK)	DI DO	Any of the six MPP pairs can be configured as a unidirectional level translator. This pair's intended configuration is the RUIM clock level translator, with MPP_9 (pin K8) the input on the MSM side and MPP_10 (pin K9) the output on the RUIM side. Both sides are pulled-up internally, with MPP_9 pulled to VREG_MSME or VREG_MSMP (configurable) and MPP_10 pulled to VREG_RUIM. Further descriptions of multipurpose pins are given in the *PM7540 Power Management IC User Guide* (80-VD691-3) and in Table 2-7 of this document.
D4 A1	MPP_5 (RUIM_M_RST) MPP_6 (RUIM_RST)	DI DO	Any of the six MPP pairs can be configured as a unidirectional level translator. This pair's intended configuration is the RUIM reset level translator, with MPP_5 (pin D4) the input on the MSM side and MPP_6 (pin A1) the output on the RUIM side. Both sides are pulled-up internally, with MPP_5 pulled to VREG_MSME or VREG_MSMP (configurable) and MPP_6 pulled to VREG_RUIM. Further descriptions of multipurpose pins are given in the *PM7540 Power Management IC User Guide* (80-VD691-3) and in Table 2-7 of this document.

[1] Pin type is AI = analog input, AO = analog output, DI = digital input, or DO = digital output.

Table 2-7 Multipurpose pin descriptions

Pin #	Pin name	Pin type [1]	Functional description
M7	MPP_1 (AMUX_IN1)	CON	These multipurpose pins are software configurable with the following options: • Digital input • Digital output • Digital level translator - uses 1 MPP pair • Analog input (input to analog multiplexer) • Analog output (buffered VREF output) • Current sink The intended functions of the first twelve MPPs are inferred by their pin names and defined elsewhere in this chapter, but can be reconfigured via SBI programming. All 22 MPPs can be programmed to any configuration listed above. See the *PM7540 Power Management IC User Guide* (80-VD691-3) for more details.
N5	MPP_2 (AMUX_IN2)	CON	
D8	MPP_3 (CBL0PWR_N)	CON	
B12	MPP_4 (CBL1PWR_N)	CON	
D4	MPP_5 (RUIM_M_RST)	CON	
A1	MPP_6 (RUIM_RST)	CON	
L12	MPP_7 (GP1_DRV_N)	CON	
M11	MPP_8 (REF_OUT)	CON	
K8	MPP_9 (RUIM_M_CLK)	CON	
K9	MPP_10 (RUIM_CLK)	CON	
K5	MPP_11 (RUIM_M_IO)	CON	
K6	MPP_12 (RUIM_IO)	CON	
M3	MPP_13	CON	
N1	MPP_14	CON	
N3	MPP_15	CON	
M5	MPP_16	CON	
B3	MPP_17	CON	
D5	MPP_18	CON	
F4	MPP_19	CON	
G4	MPP_20	CON	
J2	MPP_21	CON	
K2	MPP_22	CON	

[1] All MPPs are configurable (CON).

Table 2-8 Input power supply pin descriptions [1]

Pin #	Pin name	Functional description
B10	VDD_ANA	Input supply voltage for the MSMA linear regulator circuits.
N9	VDD_C1_E	Input supply voltage for the core_1 and EBI_1 buck converter circuits. Include an individual 4.7 µF bypass capacitor near this pin.
N7	VDD_C2_PA	Input supply voltage for the core_2 and PA buck converter circuits. Include an individual 4.7 µF bypass capacitor near this pin.
K12	VDD_GP2 (MDDI)	Input supply voltage for the MMC and GP2 (MDDI) linear regulator circuits.
F12	VDD_GP6 (BT)	Input supply voltage for the BT linear regulator circuit.
F13	VDD_MSME2	Input supply voltage for the EBI_2 linear regulator circuit.
J12	VDD_MSMP	Input supply voltage for the MSMP linear regulator circuit.
B9	VDD_RF1	Input supply voltage for the RF_RX1, RF_RX2, and AUX_1 linear regulator circuits.
D6	VDD_RF2	Input supply voltage for the RF_TX and GP1 (CAM) linear regulator circuits.
M10	VDD_RUIM	Input supply voltage for the RUIM_1 and RUIM_2 linear regulator circuits.
B8	VDD_L_SPKR	Power supply for the left speaker driver circuit. Include an individual 0.1 µF bypass capacitor near this pin.
D7	VDD_R_SPKR	Power supply for the right speaker driver circuit. Include an individual 0.1 µF bypass capacitor near this pin.
D12	VDD_TCXO	Input supply voltage for the TCXO, SYNT, and AUX_2 linear regulator circuits. Include an individual 0.1 µF bypass capacitor near this pin.
G2	VDD_WLAN	Input supply voltage for the WLAN linear regulator circuit.

[1] All PM7540 VDD pins are driven by the handset supply voltage (VDD or VPH_PWR) that includes a 22 µF (or higher) ceramic bypass capacitor.

Table 2-9 Ground pins

Pin numbers	Pin name	Description
E5, E6, E7, E8, E9, F5, F6, F7, F8, F9, G5, G6, G7, G8, G9, H5, H6, H7, H8, H9, J5, J6, J7, J8, J9	GND	IC ground pins; solder directly to PCB surface ground then connect directly to PCB internal ground plane using many vias.

3 Electrical Specifications

3.1 Absolute maximum ratings

Operating the PM7540 device under conditions beyond its absolute maximum ratings (Table 3-1) may damage the device. Absolute maximum ratings are limiting values to be considered individually when all other parameters are within their specified operating ranges. Functional operation and specification compliance under any absolute maximum condition, or after exposure to any of these conditions, is not guaranteed or implied. Exposure may affect device reliability.

Table 3-1 Absolute maximum ratings

Symbol	Parameter	Min	Max	Unit
	External supply voltages [1]			
V_{CHG}	at VCHG and CHG_CTL_N pins	-0.5	+18	V
V_{USB}	at USB_VBUS, USB_CTL_N, USB_D_P, USB_D_M, USB_ID pins	-0.5	+7.5	V
V_{DD}	Handset DC power supply voltage (at ISNS_M pin)	-0.5	+4.5	V
V_{DD_OV}	V_{DD} supply over-voltage (latch-up)	1.5 x V_{DD}		V
V_{BAT}	Main battery voltage (at VBAT pin)	-0.5	+4.5	V
V_{IN}	Voltage on any non-power supply pin [2]	-0.5	V_{XX} + 0.5	V
V_{DRV_OUT}	Current driver output voltage [1]	-0.5	+7.5	V
I_{TRIG}	I/O latchup trigger current protection	200		mA
t_{SC}	Short circuit duration to GND or V_{DD}	indefinite		sec
T_S	Storage temperature	-55	+125	°C
T_J	Junction temperature		+150	°C
V_{ESD_HBM}	Electrostatic discharge voltage (human body model)	2000		V
V_{ESD_CDM}	Electrostatic discharge voltage (charge device model)	500		V

[1] Most operational pin voltages are limited by the handset power supply voltage (V_{DD}). Exceptions are listed below:

- The VCHG and CHG_CTL_N pins are exposed to the full voltage from the external power supply (such as a wall charger).
- The USB_VBUS, USB_CTL_N, USB_D_P, USB_D_M, and USB_ID pins are exposed to USB voltages.
- The current driver outputs may be tied to the VREG_5V supply.
- The DRV_VIB_N pin is exposed to V_{DD} plus the diode clamping voltage due to inductive kickback from the motor.

[2] V_{XX} is the supply voltage associated with the input or output pin to which the test voltage is applied.

3.2 Recommended operating conditions

Operating conditions include parameters that are under the control of the user: power supply voltage and ambient temperature (Table 3-2). The PM7540 device meets all performance specifications listed in Section 3.3 through Section 3.9 when used within the recommended operating conditions unless otherwise noted in those sections (provided the absolute maximum ratings have never been exceeded).

Table 3-2 Recommended operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
	External supply voltages [1]				
V_{CHG}	at VCHG pin	3.3	4.2	14.5	V
V_{USB}	at USB_VBUS pin [2]	4.4	5.0	5.6	V
	Handset DC power supply voltage [3]				
V_{DD}	at ISNS_M pin	3.0	3.6	4.4	V
V_{BAT}	at VBAT pin	3.0	3.6	4.4	V
V_{COIN}	Coin cell voltage (backup)	1.5	3.0	3.25	V
V_{MSMP}	Digital I/O supply voltage [4]	1.764	2.6	3.0	V
V_{DRV_OUT}	Current driver output voltage [1]	-0.5	V_{DD} or VREG_5V	5.25	V
T_C	Operating temperature (case)	-30	+25	+85	°C

[1] Most operational pin voltages are limited by the handset power supply voltage (V_{DD}). Exceptions are listed below:

The VCHG and CHG_CTL_N pins are exposed to the full voltage from the external power supply (such as a wall charger).

- The USB_VBUS, USB_CTL_N, USB_D_P, USB_D_M, and USB_ID pins are exposed to USB voltages.
- The current driver outputs may be tied to the VREG_5V supply.
- The DRV_VIB_N pin is exposed to V_{DD} plus the diode clamping voltage due to inductive kickback from the motor.

[2] The USB D+ and D- pins cannot tolerate +5.6 V; their maximum voltage is +5.25 V.

[3] Parametric performance is guaranteed for battery and V_{DD} voltages at or above 3.0 V. Under-voltage lockout (UVLO) circuits continue working for battery and V_{DD} voltages as low as the UVLO threshold.

[4] The digital I/O supply voltage (V_{MSMP}) depends upon the MSM device being used.

3.3 Power supply and digital logic characteristics

This section includes physical characteristics, such as I/O capacitance and DC characteristics such as digital I/O levels and power supply currents (Table 3-3). Supply currents are based on PM7540 IC operation at room temperature (+25 °C) using default parameter settings and the nominal supply voltage (V_{DD} = 3.6 V).

Table 3-3 DC characteristics [1] [2] [3]

Parameter		Comments	Min	Typ	Max	Unit
	Battery supply current					
I_{BAT1}	Active mode [4]			2.8	TBD	mA
I_{BAT2}	Sleep mode [5]			130	TBD	µA
I_{BAT3}	Off mode [6]			10	30	µA
	Coin cell supply current					
I_{COIN1}	Off mode, XTAL on [7]			1.45	2.0	µA
I_{COIN2}	Off mode, XTAL off [8]			80	500	nA
I_{CHG}	Ext CHG supply current [9]	Sleep mode		13.5	15	mA
	Ext USB supply current					
I_{USB}	Sleep mode [10]			11.7	15	mA
I_{USB_OFF}	USB charging off [11]			120	150	µA
	Logic input voltage					
V_{IH}	High-level		0.65·V_{DDM}		V_{DDM}+0.3	V
V_{IL}	Low-level		-0.3		0.35·V_{DDM}	V
V_{SHYS}	Schmitt hysteresis voltage		15			mV
I_L	Input leakage current	V_{DDX} = max, V_{IN} = 0 V to V_{DDM}	-200		+200	nA
	Logic output voltage					
V_{OH}	High-level	I_{out} = I_{OH}	V_{DDM}-0.45		V_{DDM}	V
V_{OL}	Low-level	I_{out} = I_{OL}	0		0.45	V
	Logic output current [12]					
I_{OH_TCXO}	High-level, TCXO outputs		6.0			mA
I_{OL_TCXO}	Low-level, TCXO outputs				-6.0	mA
I_{OH_MPP}	High-level, MPP outputs					
	V_{DDX} = 2.85 V		5.0			mA
	V_{DDX} = 1.80 V		3.2			mA
I_{OL_MPP}	Low-level, MPP outputs					
	V_{DDX} = 2.85 V				-5.0	mA
	V_{DDX} = 1.80 V				-3.2	mA
I_{OH}	High-level, all others		3.0			mA
I_{OL}	Low-level, all others				-3.0	mA
C_{IN}	Digital input capacitance [13]		---		5	pF

[1] All specified supply currents are based upon no load conditions at all driver outputs (LEDs, backlights, vibration motor, etc.). Driver leakage currents are specified separately for each driver output.

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[2] Different circuit blocks are powered by different supply voltages. For example, SBI circuits are powered by VREG_MSMP, while TCXO circuits are powered by VREG_TCXO. The specified currents are the sums of currents into all VDD, VBAT, ISNS_P, and ISNS_M pins. **VDD, ISNS_P, and ISNS_M pins must all be kept at the same voltage** - even if the test fixture being used provides separate connections to each of them.

[3] V_{DDM} is the supply voltage for digital I/Os (VREG_MSMP).

[4] I_{BAT1} is the total supply current from the main battery with the PMIC on, the crystal oscillator on, the TCXO buffer on and oscillating at 20 MHz with a 1 Vpp output (no load), TCXO_EN at logic HIGH, and the following regulators on but not loaded: MSMC1 = 1.20 V; MSMC2 = 1.20 V; MSME = 1.80 V; MSME2 = 1.50 V; MSMP = 2.60 V; MSMA = 2.60 V; TCXO = 2.85 V; WLAN = 2.60 V; SYNT = 2.85 V; RFRX1 = 2.85 V; and RFTX = 2.85 V. This value does not include the TCXO buffer current.

[5] I_{BAT2} is the total supply current from the main battery with the PMIC on, the crystal oscillator on, the TCXO buffer off, TCXO_EN at logic LOW, and the following regulators on, not loaded, and set for their low power mode: MSMC1 = 1.20 V; MSMC2 = 1.20 V; MSME = 1.80 V; MSME2 = 1.20 V; MSMP = 2.60 V; and MSMA = 2.60 V.

[6] I_{BAT3} is the total supply current from the main battery with the PMIC off and the crystal oscillator on. This specification applies from -30 to +60 °C only.

[7] I_{COIN1} is the total supply current from a 3.0 V coin cell with the PMIC off and the crystal oscillator on. This spec applies from -30 to +60 °C only.

[8] I_{COIN2} is the total supply current from a 3.0 V coin cell with the PMIC off and the crystal oscillator off. This spec applies from -30 to +60 °C only.

[9] I_{CHG} is the total supply current from an external supply (such as a wall charger) with the PMIC on, the crystal oscillator on, the TCXO buffer off, TCXO_EN at logic LOW, V_{CHG} = 14.0 V, V_{MAXSEL} = 4.2 V, and the following regulators on but not loaded: MSMC1 = 1.20 V; MSMC2 = 1.20 V; MSME = 1.80 V; MSME2 = 1.50 V; and MSMP = 2.60 V.

[10] I_{USB} is the total supply current from an external USB supply with the PMIC on, the crystal oscillator on, the TCXO buffer off, TCXO_EN at logic LOW, V_{USB} = 5.0 V, V_{MAXSEL} = 4.2 V, and the following regulators on but not loaded: MSMC1 = 1.20 V; MSMC2 = 1.20 V; MSME = 1.80 V; MSME2 = 1.50 V; and MSMP = 2.60 V.

[11] I_{USB_OFF} is the USB specification for an unconfigured B-device; this value includes the external 47k pull-down resistor on the USB_VBUS pin.

[12] Output current (I_{OH} and I_{OL}) specifications apply to all digital outputs unless specified otherwise, and are superseded by specifications for specific pins. Specific exceptions include:

- The buffered TCXO output is specified separately as I_{OH_TCXO} and I_{OL_TCXO}
- The MPP outputs (when configured as digital outputs) are specified separately as I_{OH_MPP} and I_{OL_MPP}

[13] Input capacitance is guaranteed by design but is not 100% tested.

3.4 Multipurpose pin specifications

Performance specifications for the 22 multipurpose pins depend upon their programmed configuration, as indicated in Table 3-4.

Table 3-4 Multipurpose pin performance specifications

Parameter	Comments	Min	Typ	Max	Unit
MPP configured as digital input [1]					
Logic high input voltage		$0.65 \cdot V_{DDX}$		V_{DDX} + 0.3	V
Logic low input voltage		-0.3		$0.35 \cdot V_{DDX}$	V
Schmitt hysteresis		15			mV
Logic input leakage current	V_{DDX} = max, V_{in} = 0V to V_{DDX}	-200		+200	nA
Digital input capacitance				5	pF
MPP configured as digital output [2]					
Logic high output voltage	$I_{out} = I_{OH}$	V_{DDY} - 0.45		V_{DDY}	V
Logic low output voltage	$I_{out} = I_{OL}$	0		0.45	V
Logic high output current V_{DDY} = 2.85 V V_{DDY} = 1.80 V		 5.0 3.2			 mA mA

Table 3-4 Multipurpose pin performance specifications (continued)

Parameter	Comments	Min	Typ	Max	Unit
Logic low output current V_{DDY} = 2.85 V V_{DDY} = 1.80 V				 -5.0 -3.2	 mA mA
MPP configured as bidirectional I/O [3]					
Input logic characteristics	see “MPP configured as digital input”				
Output logic characteristics	see “MPP configured as digital output”				
Nominal pull-up resistance	Programmable range [4]	1		30	kΩ
Propagation delay			TBD		ns
Switch on resistance			200		Ω
MPP configured as analog input (analog multiplexer input) [5]					
Input current				100	nA
Input capacitance				10	pF
MPP configured as analog output (buffered VREF output) [6]					
Output voltage error	-100 µA to +100 µA			± 0.7	%
Temperature variation				± 0.35	%
Output current	While meeting error specifications	-100		100	µA
Noise	At output pin		440		μV_{RMS}
Spurious [7]	At output pin		-76		dBm
Load capacitance				TBD	pF
MPP configured as current sink					
Nominal output current	Programmable range [8]	5		40	mA
Output current error	V_{out} = 0.5 to (V_{DD} - 1) V	-37.5		+20	%

1 V_{DDX} is the programmable supply voltage from which digital input thresholds are referenced; options include:
- For MPP_1 through MPP_12: VREG_MSME, VREG_MSMP, VREG_RUIM1, VREG_MMC, and VDD.
- For MPP_13 through MPP_22: VREG_MSME, VREG_MSMP, VREG_GP3 (RUIM2), VREG_MMC, and VDD.

2 V_{DDY} is the programmable supply voltage from which digital output thresholds are referenced; the same options listed under note 1 (above) are available. The input and output supply voltages can be different.

3 MPP pairs are listed in Table 3-5.

4 Pull-up resistance is programmable to values of 1k, 3k, 10k, or 30k; resistor tolerance is ± 20%.

5 MPP inputs can be routed to one of five analog multiplexer inputs (AMUX5 through AMUX9); see Section 3.7.1 for details.

6 MPP outputs can be programmed for any of three voltages: 0.5xVREF (0.625 V), 1xVREF (1.25 V), or 2xVREF (2.5 V).

7 Spurious output is measured with a high-impedance probe and calculated as the spur power into 50 Ω.

8 Output current is programmable in 5 mA steps between 5 and 40 mA (inclusive); the output can also be disabled (tri-state). The actual output current realized depends upon the voltage at the driver’s output pin. Two examples are shown in

Figures 3-1 and 3-2 illustrate the MPP driver's output current dependence upon the available voltage when programmed for 20 mA (Figure 3-1) and 40 mA (Figure 3-2).

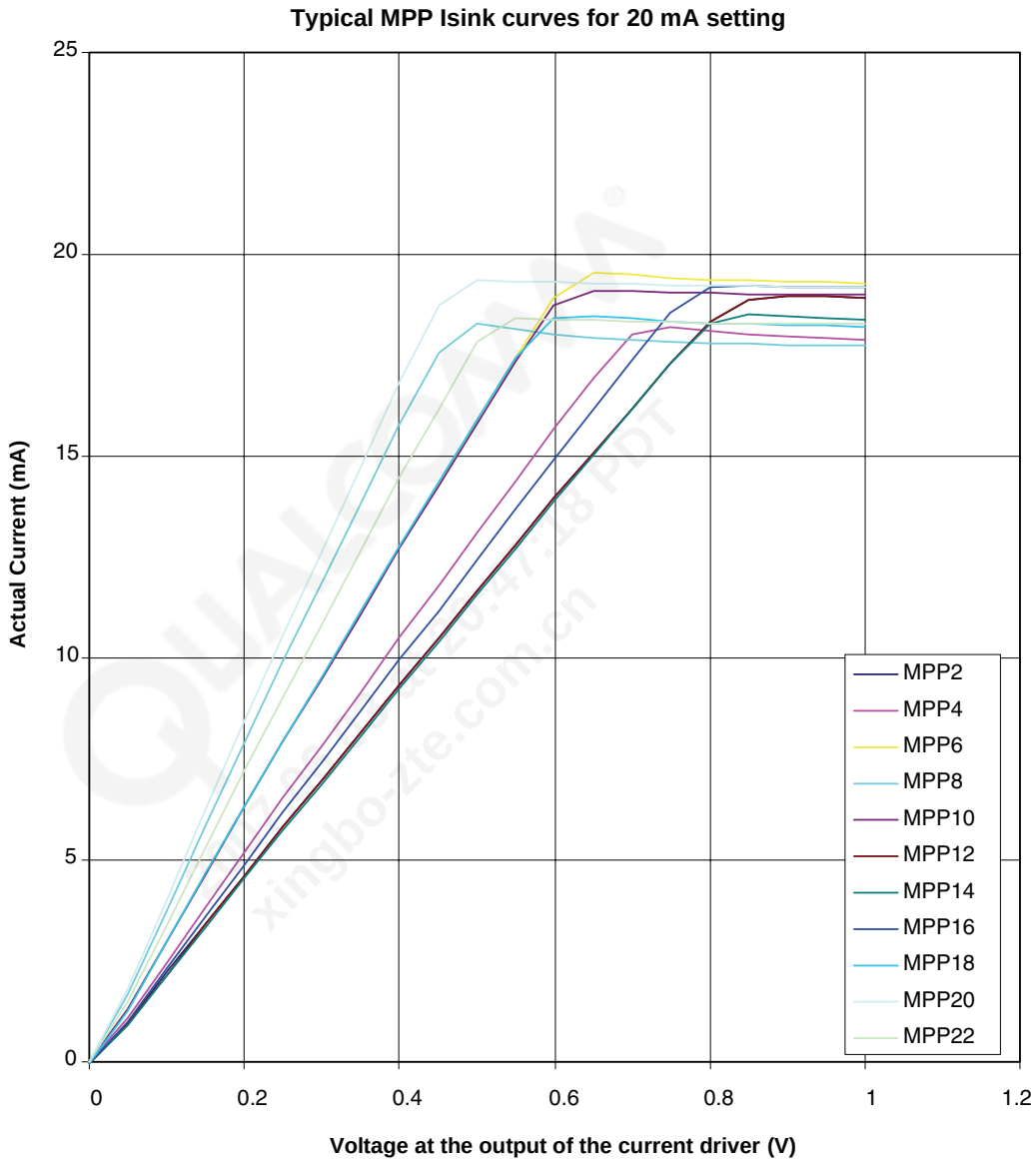

Figure 3-1 Typical MPP current sink performance for 20 mA setting

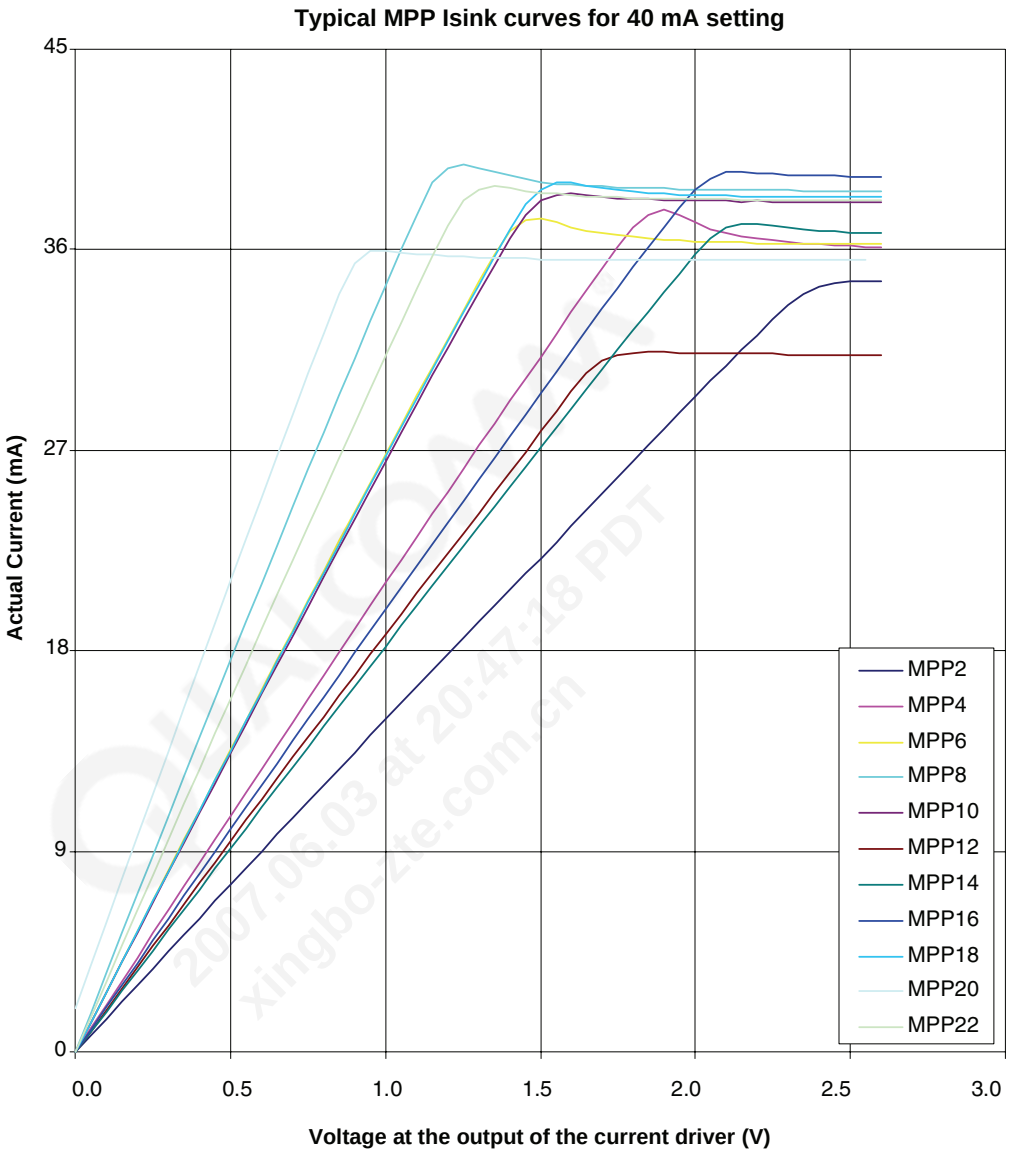

Figure 3-2 Typical MPP current sink performance for 40 mA setting

Table 3-5 MPP pairs

MPP #	Pin #		MPP #	Pin #
1	M7	<=>	2	N5
3	D8	<=>	4	B12
5	D4	<=>	6	A1
7	L12	<=>	8	M11
9	K8	<=>	10	K9
11	K5	<=>	12	K6
13	M3	<=>	14	N1
15	N3	<=>	16	M5
17	B3	<=>	18	D5
19	F4	<=>	20	G4
21	J2	<=>	22	K2

3.5 Input power management specifications

All parameters associated with input power management functions are specified in this section.

3.5.1 External supply detection

The PM7540 IC continually monitors external supply voltages (V_{CHG} and V_{USB}) and the handset supply voltage (V_{DD}). Internal detector circuits measure these voltages to recognize when supplies are connected or removed, and verify they are within their valid ranges when connected. Hysteresis prevents undesired switching near the thresholds, and interrupts notify the MSM device of PM7540 input voltage conditions.

The PMIC detects when the external supply is removed by monitoring the voltage across the external PNP pass transistor. The detection circuitry begins to close the pass transistor when the V_{CHG} (or V_{USB}) voltage drops to about 30 mV higher than V_{DD}. As this differential voltage (V_{CHG} - V_{DD} or V_{USB} - V_{DD}) drops below 30 mV, the detection circuitry cuts the bias to the pass transistor so that the removal can be detected. Without this circuit, when the external supply is suddenly disconnected, the pass transistor can operate in its reverse mode and keep sufficient voltage on VCHG or USB_VBUS so that the phone will not realize that the external supply has been disconnected.

Performance specifications for the supply detection functions are presented in Table 3-6.

Table 3-6 External supply detection performance specifications

Parameter	Comments	Min	Typ	Max	Unit
Supply detection at VCHG					
Min valid supply voltage [1]	Rising, entering valid range	3.183	3.300	3.518	V
Max valid supply voltage [1]	Rising, leaving valid range		16		V
Hysteresis	At min and max thresholds	270	300	330	mV
Supply detection at USB_VBUS					
Min valid supply voltage [2]	Rising, entering valid range	3.183	3.300	3.518	V
Hysteresis	At min and max thresholds	270	300	330	mV
Supply removal detection [3]					
Removal detection offset	V_{CHG} - V_{DD} or V_{USB} - V_{DD}	0	30	60	mV

[1] If the voltage at VCHG meets these conditions, it is deemed within the valid range for an external supply and the ITCHGVAL interrupt is generated. If these conditions are not met, the supply voltage is deemed out of range and the ITCHGINVAL interrupt is generated.

[2] If the voltage at USB_VBUS meets these conditions, it is deemed within the valid range for an external supply and the ITUSBVAL interrupt is generated. If these conditions are not met, the supply voltage is deemed out of range and the ITUSBINVAL interrupt is generated.

[3] Program VMAXSEL to 4.2 V; set VCHG to 4.2 V, ISNS_P to 4.1 V, and ISNS_M to 4.1 V. While measuring the pass transistor's base current, increase the ISNS_P and ISNS_M voltages together until the base current is less than 100 µA. When this occurs, measure the offset voltage V_{CHG} - V_{DD} or V_{USB} - V_{DD}.

3.5.2 USB_VBUS power source

A variety of peripherals can be connected to the phone's USB port. PM7540 circuits not only detect when a peripheral device is connected, but also detect its type. If an OTG type-B device is connected, the PM7540 IC provides a +5 V output power source at the USB_VBUS pin. Performance specifications for this power source are listed in Table 3-7.

Table 3-7 USB_VBUS power source performance specifications

Parameter	Comments	Min	Typ	Max	Unit
For OTG type-B devices					
Output voltage	0 to 100 mA load current	4.4	5.0	5.25	V
Output current		100			mA

3.5.3 Input circuit transistors

Two transistors are required in support of the input power management functions:

- Charger pass transistor – an external PNP bipolar transistor is required. Representative transistor performance specifications are given in Table 3-9.
- Battery transistor – this external P-channel MOSFET is optional. Including this external component provides the highest flexibility—including trickle charging and its advantages, for example —but it is not absolutely required. Representative MOSFET performance specifications are given in Table 3-9.

The specifications for these external components are intended for example purposes only; handset designers are encouraged to use their own choices while understanding that overall performance might be affected by an inappropriate choice.

Table 3-8 Example external PNP charger pass transistor specifications [1]

Parameter	Comments	Min	Typ	Max	Unit
Example specifications based upon the Rohm 2SB1424 device					
Collector-base breakdown voltage	I_C = -50 µA	-20			V
Collector-emitter breakdown voltage	I_C = -1 mA	-20			V
Emitter-base breakdown voltage	I_E = -50 µA	-6			V
C-E saturation voltage	I_C / I_B = -2A / -100mA			-0.5	V
Collector current		-3.0			A
Collector power dissipation				0.6	W
DC current gain (h_{FE})	V_{CE} = -2 V, I_C = -0.1 A	120		390	---
Junction temperature				150	ºC

[1] All specifications are valid at 25 °C unless specified otherwise.

Table 3-9 Example external battery P-channel MOSFET specifications

Parameter	Comments	Min	Typ	Max	Unit
Example specifications based upon International Rectifier model IRF7324					
Drain-source voltage				-20	V
Continuous drain current	V_{GS} = -4.5 V, T_A = +70 ºC			-5.4	A
Pulsed drain current				-40	A
Power dissipation	T_A = +70 ºC			1.3	W
Gate-to-source voltage		-12		+12	V
Junction temperature		-55		+150	ºC
Thermal resistance	Junction-to-ambient			62.5	ºC/W
D-S on resistance	Static, V_{GS} = -2.5 V, I_D = -6.0 A			0.026	Ω
Gate threshold voltage	V_{DS} = V_{GS}, I_D = -6.0 A	-0.45		-1.00	V

3.5.4 Transistor drivers

Control drivers for the charger pass transistor and the battery MOSFET are included within the PM7540 device. The driver outputs are applied to the external devices via the PMIC's CHG_CTL_N, USB_CTL_N, and BAT_FET_N pins. Specifications for both transistor drivers are listed in Table 3-10. Some specifications depend upon suitable external components as identified in the previous section, or they depend upon the control mode as identified in the table.

Table 3-10 External transistor driver specifications

Parameter	Comments	Min	Typ	Max	Unit
Pass transistor drivers (CHG_CTL_N and USB_CTL_N)					
Output current, disabled [1]	V_{DD} is measured at ISNS_M				
CHG_CTL_N	Wall charger disabled	-100			nA
USB_CTL_N	USB charger disabled	-100			nA
Output current, charging [2]	V_{DD} = VMAXSEL - 0.1 V				
CHG_CTL_N	V_{CHG} - V_{DD} = +30 mV	-150		-50	mA
USB_CTL_N	V_{USB} - V_{DD} = +30 mV	-150		-50	mA
Reverse beta [1]	PNP pass transistor			120	---
Battery MOSFET driver (BAT_FET_N) [3]					
High output voltage, V_{OH}	Disables MOSFET; I_{OH} = 100 µA	V_X - 0.1			V
Low output voltage, V_{OL}	Enables MOSFET; I_{OL} = -100 µA			0.25	V
Common to pass transistor and battery MOSFET drivers					
Switchover time [4] invalid charger to battery	10% to 90%, 10 nF load			5	µs

[1] Since the pass transistor control signals do not pull up, they must sink little current while charging is disabled. Output leakage current and pass transistor reverse beta must meet these specifications otherwise the external supply removal detection circuit may not work properly.

[2] If the pass transistor gain is high enough, a series resistor may be inserted to reduce the base current during battery charging.

[3] V_X is the higher of either V_{BAT} or V_{DD}.

[4] The switchover between charger and battery operational modes must be fast enough to avoid phone shutdown (Section 3.5.13 discusses the V_{DD} collapse protection circuit). This switchover time is measured from the time V_{CHG} drops below V_{DD} to when the BAT_FET_N control signal drops to its 10% level (battery FET nearly full-on).

3.5.5 Voltage regulation (VDD or VBAT)

The PM7540 device provides closed-loop control of the pass transistor (via CHG_CTL_N or USB_CTL_N) to regulate either the handset supply voltage (V_{DD}) when not charging, or the main battery final voltage (V_{BAT}) when charging. When fast charging is disabled, the battery MOSFET is opened and the voltage regulation point is the ISNS_M pin (V_{DD}). When fast charging is enabled, the VBAT pin is the voltage regulation point, thereby improving the voltage precision of the fully charged battery (Li-ion battery manufacturers typically specify 1% accuracy).

Table 3-11 lists performance specifications for regulation of the V_{DD} and V_{BAT} voltages.

Table 3-11 Voltage regulation performance specifications (V_{DD} or V_{BAT})

Parameter	Comments	Min	Typ	Max	Unit
Voltage error					
V_{BAT} - low current [1]	4.0 to 4.4 V settings	-0.7		+0.7	%
V_{DD} - high current [2]	0 to 2 A V_{DD} load	-3.0		+3.0	%
PSRR [3]	External supply to V_{DD}				
300 Hz			60		dB
1 kHz			52		dB
3 kHz			47		dB
10 kHz			34		dB
30 kHz			21		dB
100 kHz			29		dB
Load regulation	Current = 0 to 1 A; $V_{CHG} = V_{DD} + 0.5$		0.2		%
Line regulation	V_{CHG} = 4.7 to 14 V; VMAXSEL = 4.2 V		0.005	0.1	%/V
Transient response [4]					
Overshoot				+5	%
Undershoot		-5			%

[1] The voltage at the VBAT pin (V_{BAT}) is measured with fast charging enabled under these conditions:
- The charger voltage (VCHG) is between VMAXSEL + 0.5 V and +14 V, or the USB voltage (V_{USB}) is between (VMAXSEL + 0.5 V and + 5.2 V (whichever is active).
- The charging current is between 30 mA and 100 mA.
- The junction temperature is between -10 and +80 °C (outside this range the temperature coefficient shall be negative); the Zetex ZXTD2M832 device is used as the pass transistor.

[2] The voltage at the ISNS_M pin (V_{DD}) is measured with fast charging enabled.

[3] Power supply rejection ratio is tested with a 100 mA load, and with the external supply voltage (V_{CHG} or V_{USB}) set to V_{DD} + 1 V.

[4] The transient response, overshoot and undershoot, can be due to load steps (such as PA puncturing), changing VMAXSEL settings, or switching charging operations on and off. This includes the effects of the voltage sensing point switching between the VBAT and ISNS_M pins as the charging operations are turned on and off.

3.5.6 Current regulation, monitoring, and over-current protection

An external 0.1-Ω sense resistor is required and must be connected across the ISNS_P and ISNS_M pins to allow the PM7540 IC to continuously monitor the total handset electronics plus charging current. If the programmed current threshold is exceeded, the active pass transistor is forced to a high resistance, disrupting V_{DD} or V_{BAT} regulation but protecting against excess current.

The same circuits are used to regulate the total handset electronics plus charging current during the main battery's constant current charging mode. Either pass transistor (charger or USB) can be active while the current is regulated - only the appropriate control pin (CHG_CTL_N or USB_CTL_N) is active.

Table 3-12 lists the current regulator/monitor performance specifications.

Table 3-12 Current regulator/monitor performance specifications

Parameter	Comments	Min	Typ	Max	Unit
Sense resistor [1]	External, across ISNS_P and ISNS_M		0.100		Ω
Current limit or regulation target [2]	Programmable range				
Charger supply		0.1	1.0	3.0	A
USB supply		0.1	0.5	2.0	A
Current detection gain error [3]	IMAXSEL varied from min to max	-10		+10	%
Current detection offset error [3]	IMAXSEL = 100 mA	-30		+30	mA

[1] The sense resistor detects the total current (handset electronics plus charging), not just the charging current. A 1% tolerance is recommended. The current sensing circuit operates in a voltage mode, sensing the differential voltage across the sense resistor - the detected current scales inversely with the sense resistor.

[2] Either pass transistor (charger or USB) can be active for monitoring and regulating the total current and protecting against over current conditions. Current values are programmable over the stated ranges in 100 mA increments. These values are based upon a 0.1 Ω external sense resistor and need to be scaled if an alternate resistor value is used.

[3] Test conditions: V_{CHG} or V_{USB} = 5.0 V; V_{BAT} = V_{DD} = 3.60 V.

3.5.7 Pass transistor power limiting

The PM7540 device monitors the power dissipated in the pass transistor through voltage and current measurements. If the calculated power exceeds programmable limits, the CHG_CTL_N or USB_CTL_N control signal is driven higher to reduce the pass transistor's through current.

Table 3-13 lists the performance specifications for the pass transistor power limiting functions.

Table 3-13 Pass transistor power limiting performance specifications

Parameter	Comments	Min	Typ	Max	Unit
Power limiting [1] [2]	Programming range				
Charger transistor [3]		0.4		2.0	W
USB transistor [4]		0.4		2.0	W
Power limit gain error [5]	PMAXSEL varied from min to max	-10		+10	%
Power limit offset error [5]	PMAXSEL = 400 mW	-42		+42	mW

1 Separate power dissipation limits are programmable for each transistor (charger and USB).

2 Programmable values are 0.4 W, 0.5 W, 0.6 W, 0.75 W, 1 W, 1.5 W, and 2 W. These values are based upon a 0.1 Ω external sense resistor and need to be scaled if an alternate resistor value is used.

3 The charger pass transistor power dissipation is calculated using voltage measurements at the VCHG and ISNS_P pins, and current measurements based upon the sense resistor voltage across the ISNS_P and ISNS_M pins. Power limiting across V_{CHG} is valid only if V_{CE} > 1.0 V.

4 The USB pass transistor power dissipation is calculated using voltage measurements at the USB_VBUS and ISNS_P pins, and current measurements based upon the sense resistor voltage across the ISNS_P and ISNS_M pins.

5 Test conditions: V_{CHG} or V_{USB} = 5.0 V; V_{BAT} = V_{DD} = 3.60 V.

3.5.8 Main battery charging

The PM7540 device provides support circuitry for charging a lithium-ion battery, cycling through as many as four charging techniques: trickle, constant current, constant voltage, and pulsed. Measured battery voltage, external supply voltage, and total detected current values are available to the MSM device through the PMIC's analog multiplexer. This allows the MSM to monitor charging parameters, make decisions, and control the charging process.

NOTE The sense resistor measures the total current - the sum of battery charging current plus handset electronics operational current. While not ideal, this is a necessary compromise. Inserting the sense resistor in series with the battery would increase the overall series resistance, create an undesired voltage drop, and reduce the run time of the phone.

Charging of a severely depleted battery begins with trickle charging, a mode that limits the current and avoids pulling V_{DD} down. Once a minimum battery voltage is established using trickle charging, constant current charging is enabled via software to charge the battery quickly - this mode is sometimes called fast charging. Once the lithium-ion battery approaches its target voltage (through constant current charging), the charge is completed using either constant voltage or pulse charging. PM7540 circuit performance specifications pertaining to all four charging techniques are presented below.

3.5.8.1 Trickle charging

Trickle charging of the main battery, enabled through software and powered from V_{DD}, is provided by the PM7540 device. This mode is used to raise a severely depleted battery's voltage to a level sufficient to begin fast charging. If fast charging is enabled while the battery is below 2.55 V (the UVLO threshold), the battery pulls V_{DD} down and causes the phone to turn off. Even if the battery voltage is between 2.55 and 3.10 V, fast charging is still not recommended because the regulators can fail. Trickle charging avoids these two potential problems by getting the battery voltage to about 3.1 V or more before attempting fast charging.

The trickle charger is an on-chip programmable current source that supplies current from V_{DD} to the VBAT pin; pertinent performance specifications are given in Table 3-14. Software must terminate trickle charging based upon battery voltage measurements at the MSM device's HKADC (routed through the PM analog multiplexer) and the battery type - there is not a preset termination threshold.

Table 3-14 Trickle charging performance specifications

Parameter	Comments	Min	Typ	Max	Unit
Trickle current range	Programmable [1]	0		80	mA
Trickle current accuracy [2]		-10		+10	%

[1] Valid current settings are: 0, 20, 30, 40, 50, 60, 70, and 80 mA. A value of 0 mA disables trickle charging.
[2] Test conditions: at least 1 V of headroom for accurate current settings ($V_{DD} > V_{BAT} + 1$ V).

3.5.8.2 Constant current charging

The PM7540 device supports constant current charging of the main battery by closing the battery MOSFET (connecting the battery to V_{DD}), and closed-loop controlling the active pass transistor. The closed-loop control regulates the total current (handset electronics plus charging current) to match the programmed value (IMAXSEL). The MSM device monitors the charging process as described earlier, and continues the constant current mode until the battery reaches its target voltage. Lithium-ion batteries require further charging using constant voltage or pulsed techniques.

The PMIC parameters associated with constant current charging are specified in the following subsections:

- External supply voltages Section 3.5.1
- Transistor drivers Section 3.5.4
- VBAT settings Section 3.5.5
- Current regulation Section 3.5.6
- Battery voltage detector Section 3.5.10

Charging current is a function of the external supply voltage (such as VCHG) for a fixed battery voltage (VBAT). The charging current will be reduced significantly if VCHG is not sufficiently larger than VBAT. An example curve showing the charging current versus VCHG is shown in Figure 3-3, with VBAT fixed at 4.1 V.

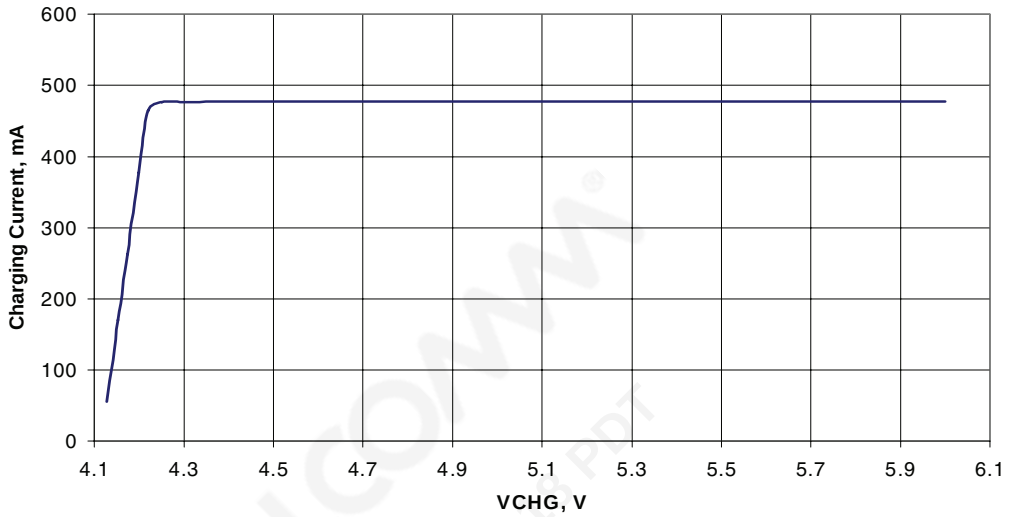

Figure 3-3 Example charging current vs. V_{CHG} when V_{BAT} = 4.1 V

Charging current is also a function of the battery voltage for a fixed external supply voltage. Charging current drops off quickly as V_{BAT} approaches V_{CHG}. An example curve showing the charging current versus V_{BAT} is shown in Figure 3-4, with V_{CHG} fixed at 5 V.

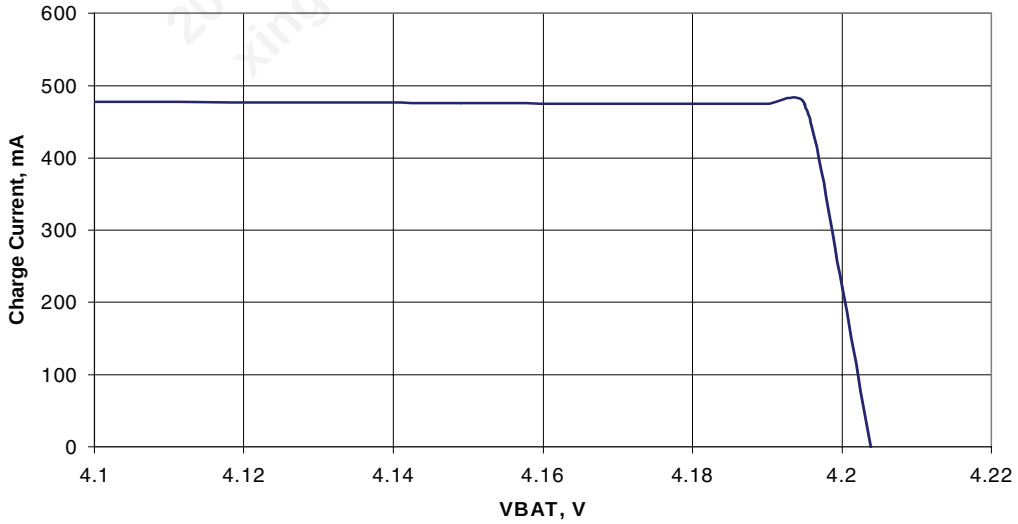

Figure 3-4 Example charging current vs. VBAT when VCHG = 5.0 V

Additional performance specifications for constant current charging are not required.

3.5.8.3 Constant voltage charging

Once constant current charging of a lithium-ion battery is finished, the charging continues using either constant voltage or pulsed techniques. Specifications pertaining to constant voltage charging are addressed in this subsection; pulse charging is covered in the next subsection.

The MSM device and its software determines if and when it is appropriate to begin the constant voltage mode within the charging process. When the battery voltage reaches a target value, a timer is started; when that timer expires, charging is complete.

PM7540 support of constant voltage charging is very similar to its constant current mode: the battery MOSFET is closed and the active pass transistor is closed-loop controlled. But in this case, the closed-loop control regulates the voltage at VBAT to match the programmed value VMAXSEL. This ensures the most accurate final battery voltage - lithium-ion battery manufacturers recommend a voltage accuracy of 1% or better at the end of charge.

The PM7540 parameters associated with constant voltage charging are specified in the following subsections:

- External supply voltages Section 3.5.1
- Transistor drivers Section 3.5.4
- VBAT settings Section 3.5.5
- Battery voltage detector Section 3.5.10

Additional performance specifications are not required.

3.5.8.4 Pulse charging

Once constant current charging of a lithium-ion battery is finished, the charging continues using either constant voltage or pulsed techniques. Specifications pertaining to pulse charging are addressed in this section; constant voltage charging was covered in the previous section.

In addition to this section's specifications, pulsed charging utilizes PM7540 functions that are specified elsewhere in this document:

- Similar to constant current charging, pulsed charging uses the PMIC to set a current limit (IMAXSEL) while the battery is being charged. See Section 3.5.6 for current monitoring, regulation, and protection specifications.
- Charging is terminated after the battery voltage remains above the programmed value VMAXSEL long enough; VMAXSEL is normally set 100 mV higher than the desired final battery voltage. If the voltage is not set high, the current will fall off as the battery voltage approaches VMAXSEL and pulse charging will take longer. See Section 3.5.5 for VMAXSEL threshold characteristics.

Additional pulse charging performance specifications are listed in Table 3-15.

Table 3-15 Pulse charging performance specifications

Parameter	Comments	Min	Typ	Max	Unit
Timing accuracy [1]	T_ON, T_OFF, T_DONE	0		977	µs
Timing variables [2]	Programmable durations				
Nominal T_ON		62.5		500	ms
Nominal T_OFF		62.5		500	ms
Nominal T_DONE		16		128	---

[1] The timing accuracy of pulse charging intervals (T_ON, T_OFF, and T_DONE) is set entirely by the oscillator clocking the counters - either the external 32.768 kHz crystal oscillator or the on-chip RC oscillator. The nominal clock rate at the pulse counter is 1024 Hz.

[2] The timing intervals are defined as follows:

- T_ON is the on time (the current pulse duration) - the battery MOSFET and charger PNP are on, the battery is connected to VDD, and charging current flows to the battery. Valid settings are 62.5, 125, 250, and 500 ms.
- T_OFF is the off time - the battery MOSFET and charger PNP are disconnected from VDD. Valid settings are 62.5, 125, 250, and 500 ms.
- T_DONE is the number of consecutive T_OFF intervals required before the PMIC will end the pulsed charging - the battery is fully charged, so charging is done. The PMIC reports to the MSM device that charging is finished using an interrupt. T_DONE values represent multiples of the programmed T_OFF value; valid settings are 16, 32, 64, and 128.

3.5.9 Coin cell charging

Coin cell charging is enabled through software control and powered from VBAT. The on-chip charger is implemented using a programmable voltage regulator and a programmable series resistor. The MSM device reads the coin cell voltage through the PMIC's analog multiplexer to monitor charging. Coin cell charging performance is specified in Table 3-16.

A backup capacitor can be used instead of a coin cell to maintain just the SMPL feature, if desired. During normal operation, the VCOIN pin voltage will stay above 2.2 V even when the coin cell charger is turned off.

Table 3-16 Coin cell charging performance specifications

Parameter	Comments	Min	Typ	Max	Unit
Target regulator voltage [1]	V_{IN} > 3.3 V, I_{CHG} = 100 µA	3.00	3.10	3.20	V
Target series resistance [2]		800		2100	Ω
Coin cell charger voltage error	I_{CHG} = 0 µA	-5		+5	%
Coin cell charger resistor error		-20		+20	%
Ground current, charger enabled	PMIC = off; VCOIN = open; VBAT = 3.7 V		4.5	8	µA

[1] Valid regulator voltage settings are 3.0, 3.1, and 3.2 V.

[2] Valid series resistor settings are 800, 1200, 1700, and 2100 Ω.

3.5.9.1 Backup voltage and external SRAM

The phone's SRAM is connected to the PM7540 V_BACKUP pin. Performance specifications pertaining to this pin are listed in Table 3-17.

Table 3-17 Backup voltage (V_BACKUP) performance specifications

Parameter	Comments	Min	Typ	Max	Unit
Switch resistance					
VREG_MSMP connected	VREG_MSMP = 2.6 V		4	5	Ω
VCOIN connected	VCOIN = 3.0 V			1000	Ω

3.5.10 Battery voltage alarm

A programmable window detector continuously monitors the battery voltage at VBAT. Both thresholds, upper and lower, are programmable and include voltage hysteresis to ensure stability. To prevent brief voltage transients from interrupting the MSM device unnecessarily, the out-of-range condition must stay triggered for a certain duration before an interrupt is generated. This delay, referred to as time hysteresis, is also programmable. If the battery voltage goes back in-range before the programmed delay, the delay timer is reset and no interrupt is generated.

Performance specifications for the battery voltage alarm circuits are given in Table 3-18.

Table 3-18 Battery voltage alarm performance specifications

Parameter	Comments	Min	Typ	Max	Unit
Threshold voltages [1]	Programmable range	2.800	4.200	4.300	V
Threshold error		-2		+2	%
Threshold voltage hysteresis			50		mV
Time hysteresis [2]	Programmable range	0.122		15.63	ms

[1] The threshold is programmable in 100 mV increments, and can be disabled entirely.

[2] The timing accuracy of the low battery time hysteresis interval is set entirely by the oscillator clocking the counters - either the external 32.768 kHz crystal oscillator or the on-chip RC oscillator. Valid settings are: 0.122, 0.244, 0.488, 0.977, 1.95, 3.91, 7.81, and 15.63 ms.

3.5.11 Under-voltage lockout

The handset supply voltage (V_{DD}) is monitored continuously by an under-voltage lockout (UVLO) circuit that automatically turns off the device at severely low V_{DD} conditions. Of course, the UVLO threshold is lower than the low battery threshold discussed in the previous section.

Software is not involved in UVLO detection. The voltage thresholds, hysteresis, and time delays are not programmable, and UVLO events do not generate interrupts. They are reported to the MSM device via the PON_RESET_N signal, then a register is read that reveals to software that a UVLO condition occurred. UVLO-related voltage and timing specifications are listed in Table 3-19.

Table 3-19 UVLO performance specifications

Parameter	Comments	Min	Typ	Max	Unit
Threshold voltage	Falling, leaving valid range	2.423	2.550	2.678	V
Hysteresis		120	165	210	mV
UVLO detection interval			1.0		µs

3.5.12 Sudden momentary power loss

The PM7540 sudden momentary power loss (SMPL) feature initiates a power-on sequence without MSM intervention if the monitored phone voltage (V_{DD}) drops out of range and then returns in-range within a programmable interval. When enabled by software, SMPL achieves immediate and automatic recovery from momentary power loss (such as a brief battery disconnect when the phone is jarred).

SMPL circuits run off an internal voltage net that runs the crystal oscillator and RTC as well. SMPL performance specifications are given in Table 3-20.

Table 3-20 SMPL performance specifications

Parameter	Comments	Min	Typ	Max	Unit
SMPL interval [1]	Programmable range	0.5		2.0	s
SMPL timing error [2]		-1		+1	ms

[1] The timing accuracy of the SMPL interval is set entirely by the oscillator clocking the counters - either the ext 32.768 kHz crystal oscillator or the on-chip RC oscillator. Valid settings are: 0.5, 1.0, 1.5, and 2.0 seconds.

[2] The SMPL timer is driven by a 1024 Hz clock; the error reflects a single clock cycle error.

3.5.13 VDD collapse protection

Some handset manufacturers may specify a low current charger that cannot handle the peak phone plus charging current. To prevent a sudden load from inadvertently collapsing the V_{DD} voltage when a low current charger is used, the PM7540 device monitors the voltage across the battery MOSFET (through the ISNS_M and VBAT pins) and automatically turns on the MOSFET if V_{DD} drops about 30 mV below VBAT.

Performance specifications related to V_{DD} collapse protection are given in Table 3-21.

Table 3-21 VDD collapse protection performance specifications

Parameter	Comments	Min	Typ	Max	Unit
BAT_FET_N output voltage					
0 V across battery FET [1]	V_{BAT} - V_{DD} = 0 V	V_{DD} - 1	0.5	V_{DD}	V
30 mV across battery FET [2]	V_{BAT} - V_{DD} = -30 mV			V_{DD} - 1 or 1	V
Activation time				5	µs

[1] Battery FET is off.

[2] Battery FET is on. BAT_FET_ON will pull down to (V_{DD} - 1) V or 1 V - whichever is higher; this control signal cannot pull all the way to ground.

3.6 Output voltage regulation specifications

The PM7540 IC includes all the regulated voltages needed for most wireless handset applications (and many other applications). Independent regulated power sources are required for various electronic functions to avoid signal corruption between diverse circuits, to support power management sequencing, and to meet different voltage level requirements. Twenty-four (24) voltage regulators are provided—all programmable, all derived from a common bandgap reference circuit.

Two major types of voltage regulator circuits are on-chip: switched-mode power supplies (SMPS) and linear regulators. There are three types of SMPS supplies: the boost circuit steps up its output voltage relative to the input voltage and is rated for 500 mA; the buck circuits step down their output voltages and are rated for either 300 or 500 mA each. There are four different linear regulator circuits, three categorized by their output current ratings (300, 150, and 50 mA) and the fourth intended for biasing microphones. Each linear regulator and SMPS can provide more than its rated output current, though some performance characteristics might be degraded.

Although the names of the regulators imply an intended function, almost all can be used for any purpose—they support universal applications. Only the following outputs must be used according to their assigned names:

- MSMA – must be used for the MSM analog circuits
- MSMP – must be used for the MSM periphery circuits
- MSMC1 – must be used for the MSM digital core #1
- MSMC2 – must be used for the MSM digital core #2 (if a second core is included within the MSM device)
- MSME – must be used for the EBI #1 bus
- TCXO – must be used for the VCTCXO

A high-level summary of the PM7540 regulators is given in Table 3-22.

Table 3-22 Voltage regulator summary

Type/name [1] [2]	Default conditions [3]	Voltage range	Intended use
SMPS – Boost			
+5V (500 mA)	Off, 5.000 V	3.000 to 6.100 V	USB-OTG host, white LEDs, camera flash
SMPS – Buck			
MSMC1 (500 mA)	On, 1.200 V	0.750 to 3.050 V	MSM core #1; DVS available
MSMC2 (500 mA)	On, 1.200 V	0.750 to 3.050 V	MSM core #2; DVS available
MSME (500 mA)	On, 1.800 V	0.750 to 3.050 V	Devices on EBI #1 bus
PA (300 mA)	Off, 1.800 V	0.750 to 3.050 V	Power amplifier(s); DVS available
Linear – 300 mA			
MSMA [4]	On, 2.600 V	1.500 to 3.050 V	MSM analog circuits
MSMP [6]	On, 2.600 V	1.500 to 3.050 V	MSM pad voltage and other IC digital I/Os
WLAN	Off, 2.850 V	1.500 to 3.050 V	802.11 wireless LAN
GP6 (BT)	Off, 2.850 V	1.500 to 3.050 V	Bluetooth

Table 3-22 Voltage regulator summary

Type/name [1] [2]	Default conditions [3]	Voltage range	Intended use
Linear – 150 mA			
MMC	Off, 2.850 V	1.500 to 3.050 V	Multimedia or SD circuits
MSME2	On, 1.500 V	0.750 to 1.525 V	Devices on EBI #2 bus
RFRX1	Off, 2.850 V	1.500 to 3.050 V	First of two RF receiver circuit supplies
RFRX2	Off, 2.850 V	1.500 to 3.050 V	Second of two RF receiver circuit supplies
RFTX	Off, 2.850 V	1.500 to 3.050 V	RF transmitter circuits
RUIM1	Off, 2.850 V	1.500 to 3.050 V	RUIM module #1
GP1 (CAM)	Off, 2.850 V	1.500 to 3.050 V	Camera circuits
GP2 (MDDI)	Off, 2.850 V	1.500 to 3.050 V	MDDI circuits
GP3 (RUIM2)	Off, 2.850 V	1.500 to 3.050 V	RUIM module #2
GP5 (AUX2)	Off, 2.850 V	1.500 to 3.050 V	Auxiliary #2 analog circuits
Linear – 50 mA			
SYNT	Off, 2.850 V	1.500 to 3.050 V	Tx VCO and PLL circuits
TCXO	On, 2.850 V	1.500 to 3.050 V	VCTCXO and Rx VCO and PLL circuits
USB	Off, 3.300 V	3.000 V to 6.100 V	Internal USB transceiver; not used off-chip
GP4 (AUX1)	Off, 2.850 V	1.500 to 3.050 V	Auxiliary #1 analog circuits
Linear – MIC bias	Off, 2.000 V	1.73, 1.80, 1.93, 2.00 V	Microphone bias

1 All regulator names are based on their intended use, though some may be used to power alternate functions. For example, the WLAN regulator is intended to power an external 802.11 module, but may be used to power other circuits (or not used at all).

2 Each current listed in this table is its regulator's rated value – the current at which the regulator meets all its performance specifications. Higher currents are allowed, but higher input voltages may be required and some performance characteristics may become degraded. See the appropriate regulator sections for details.

3 All regulators have default output voltage settings, even if they default to an off condition.

4 VREG_MSMA and VREG_MSMP power internal circuitry and should be kept on at their default setting.

All regulated output voltages are programmable. All regulators can be set to a low power mode except the VREG_USB circuit. Descriptions of the low power modes and overall performance specifications for all regulator circuits are presented later in this section; but first, the common voltage reference circuit is discussed and specified.

3.6.1 Reference circuit

All PM7540 regulator circuits, as well as other internal circuits, are driven by a common, on-chip voltage reference circuit. An on-chip series resistor supplements an off-chip 0.1 µF bypass capacitor at the REF_BYP pin to create a lowpass function that filters the reference voltage distributed throughout the device.

NOTE Do not load the REF_BYP pin. Use an MPP configured as an analog output if the reference voltage is needed off-chip.

The filtered reference node is scaled, buffered, and provided at any multipurpose pin configured as an analog output. In fact, MPP_8 (REF_OUT) is intended to be used in its analog output configuration, serving an off-chip function such as the power amplifier control reference in GSM applications.

Applicable voltage reference performance specifications (other than those given previously in Section 3.4 for MPP performance) are listed in Table 3-23.

Table 3-23 Voltage reference performance specifications

Parameter	Comments	Min	Typ	Max	Unit
Nominal internal VREF	At REF_BYP pin		1.250		V
Temperature coefficient	All operating conditions	-0.35		+0.35	%
Absolute error		-0.70		+0.70	%

3.6.2 Switched-mode power supplies

Two types of switched-mode power supplies (or DC-to-DC converters) are implemented by the PM7540 IC: boost and buck converters. The boost converter provides output DC voltages larger than its input DC voltage and is also known as a step-up converter. The buck converters provide output voltages smaller than their input voltages and are therefore known as step-down converters.

Performance specifications for the boost and buck converters are given in the following subsections.

3.6.2.1 Boost (step-up) converter

The boost switched-mode power supply (SMPS) is rated for 500 mA output current and is intended for generating +5 V to power circuits such as the USB-OTG host, white LEDs, and a camera flash. Although rated for 500 mA, higher currents are allowed but higher input voltages may be required and some performance characteristics may become degraded as indicated below.

The boost converter offers a low power mode to reduce its quiescent current during the phone's sleep mode. This mode uses pulse burst modulation (PBM). This mode should only be used when the phone is in its sleep mode.

NOTE The boost converter's diode must have a reverse recovery time of less than 9.3 ms to ensure that the transient response peaks at less than 7.5 V.

Boost converter performance specifications are listed in Table 3-24.

Table 3-24 Boost regulator performance specifications [1] [2]

Parameter	Comments	Min	Typ	Max	Unit
Output voltage range [3]	Programmable range	3.000	5.000	6.100	V
Voltage error	0 to 500 mA load	-5	0	+5	%
Temperature coefficient		-100	0	+100	ppm/C
Transient response [4] Settling time Overshoot or undershoot	To within 1% of final value			 100 +3	 µs %
Output ripple	500 mA load, 10 µF X5R cap		33	50	mVpp
Load regulation	$V_{in} > V_{out} + 1$ V; $I_{rated}/100$ to I_{rated}			0.65	%
Line regulation [5]				0.375	%
Spurious [6]	f < 10 MHz		-40		dBm
Efficiency I_{load} = 80 mA I_{load} = 10 to 500 mA	V_{in} = +3.6 V		 85 80		 % %
Ground current No load, PBM mode No load, PWM mode	 PBM – boost low-power mode PWM – boost normal mode		 TBD 225	 TBD 500	 µA µA

1 All specifications apply over the device's recommended operating conditions, load current range, and capacitor ESR range unless noted otherwise.

2 Performance characteristics that may degrade if the rated output current (500 mA) is exceeded:
- Voltage error
- Output ripple
- Efficiency

3 Programmable in 100 mV increments.

4 The stated transient response performance is achieved regardless of the transitory mode – turning the regulator on and off, changing load conditions, changing input voltage, or reprogramming the output voltage setting.

5 Line regulation is the output variation due to a changing input voltage, calculated by dividing the output voltage change by the input voltage change, expressed as a percentage. The valid input range for this test is from V_{out} + 1V (+3 V minimum) to the specified maximum V_{DD} value (+4.4 V).

6 Spurious output is measured with a high impedance probe as the spurious power into 50 Ω. It is specified for loads from zero to I_{rated}.

3.6.2.2 Buck (step-down) converters

There are two buck SMPS implementations:

- Rated for 500 mA: MSMC1, MSMC2, and MSME; intended for powering the MSM device core #1 and core #2 circuits and devices running off the EBI #1 bus
- Rated for 300 mA: PA; intended for powering the power amplifier (PA)

The regulators are capable of sourcing more current than these rated values, but higher input voltages may be required and some performance characteristics may become degraded as indicated later in this section.

The buck converters offer a low power mode to reduce their quiescent current during the phone's sleep mode. This mode uses PFM. This mode should only be used when the phone is in sleep mode.

Buck SMPS performance specifications are listed in Table 3-25.

Table 3-25 Buck regulator performance specifications [1] [2]

Parameter	Comments	Min	Typ	Max	Unit
Output voltage range [3]	Programmable range	0.750		3.050	V
Voltage error		-3	0	+3	%
Temperature coefficient		-100	0	+100	ppm/C
Transient response [4]					
Settling time	To within 1% of final value			100	µs
Overshoot				+3	%
Output voltage dip	5 to 300 mA load change		54	100	mV
Voltage spike	5 to 300 mA load change		75	TBD	mV
Output ripple	300 mA load, 4.7 µF capacitor		10	15	mVpp
Load regulation	$V_{in} > V_{out} + 1$ V; $I_{rated}/100$ to I_{rated}			0.65	%
Line regulation [5]				0.375	%
PSRR	Power supply rejection ratio				
50 Hz to 1000 Hz		40			dB
1 kHz to 100 kHz		20			dB
Spurious [6]	F < 10 MHz		TBD	TBD	dBm
Efficiency [7]	V_{out} = +1.8 V				
I_{load} = 130 mA			90		%
I_{load} = 0.5 to 500 mA			85		%
I_{load} = 600 mA			80		%
Ground current					
No load, PFM mode	PFM - buck low-power mode		20	40	µA
No load, PWM mode	PWM - buck normal mode		425	TBD	µA

1 All specifications apply over the device's recommended operating conditions, load current range, and capacitor ESR range unless noted otherwise.

2 Performance characteristics that may degrade if the rated output current (500 mA) is exceeded:
- Voltage error
- Output ripple
- Efficiency

3 Programmable in 25 mV increments.

4 The stated transient response performance is achieved regardless of the transitory mode – turning the regulator on and off, changing load conditions, changing input voltage, or reprogramming the output voltage setting.

5 Line regulation is the output variation due to a changing input voltage, calculated by dividing the output voltage change by the input voltage change, expressed as a percentage. The valid input range for this test is from V_{out} + 1V (+3 V minimum) to the specified maximum V_{DD} value (+4.4 V).

6 Spurious output is measured with a high impedance probe as the spurious power into 50 Ω. It is specified for loads from zero to I_{rated}.

7 Typical buck converter efficiency versus load current is shown in Figure 3-5 and Figure 3-6.

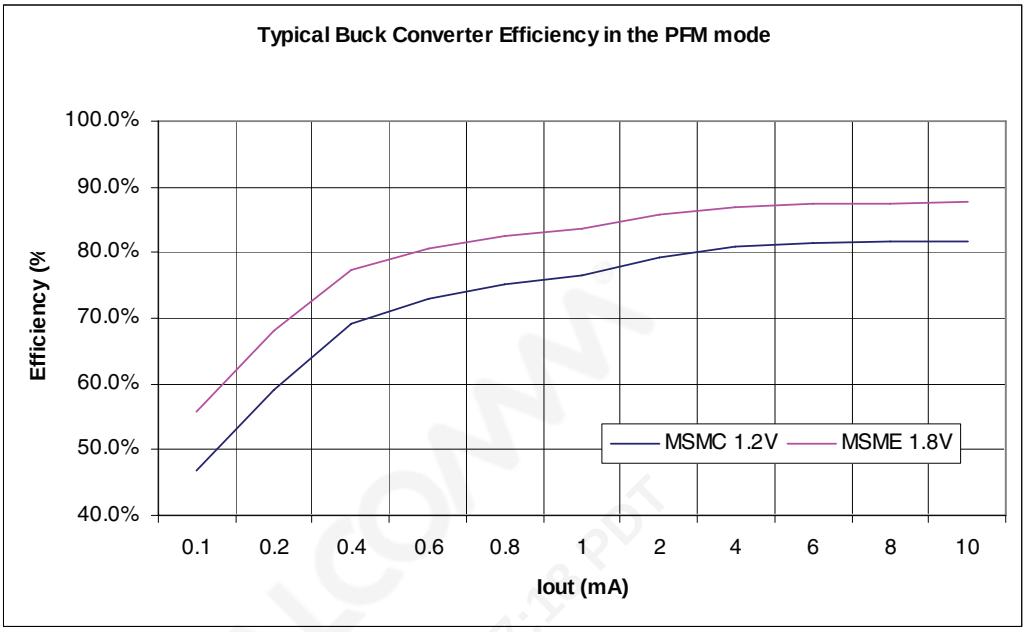

Figure 3-5 Typical buck converter efficiency - PFM mode (low power mode)

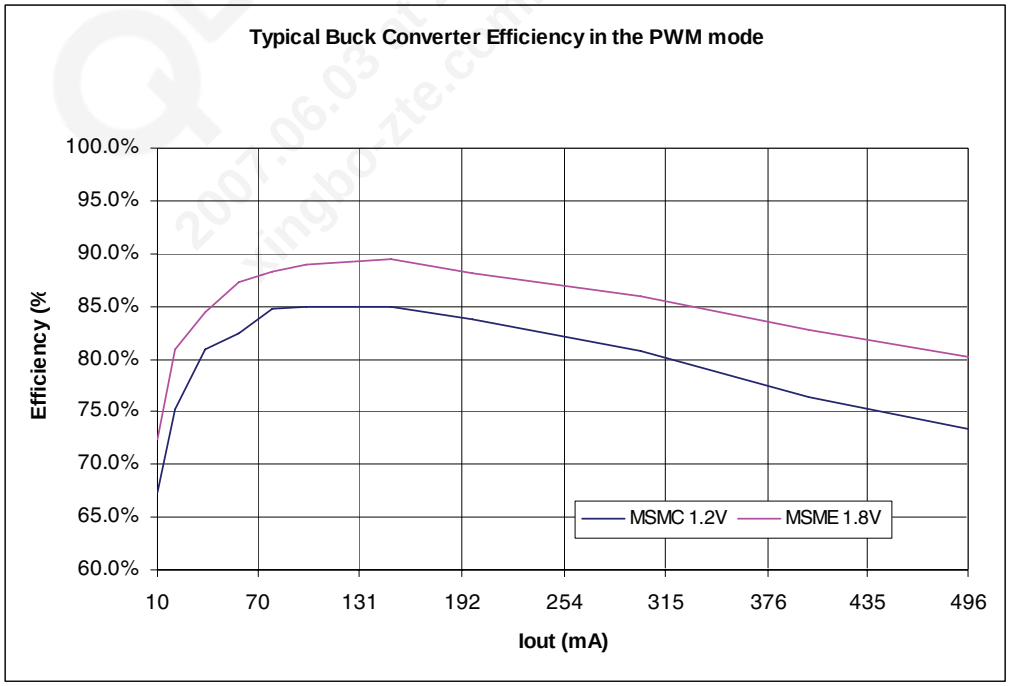

Figure 3-6 Typical buck converter efficiency - PWM mode (normal mode)

3.6.3 Linear regulators

Four low dropout linear regulator designs are implemented within the PM7540 IC:

- Design #1 – Rated for 300 mA, intended for powering MSMA, MSMP, WLAN, and GP6 (BT) circuits. The MSMA and MSMP circuits are on during the phone's sleep mode and therefore have very low ground current.
- Design #2 – Rated for 150 mA, intended for powering MMC, MSME2, RFRX1, RFRX2, RFTX, RUIM1, GP1 (CAM), GP2 (MDDI), GP3 (RUIM2), and GP5 (AUX2) circuits. These sensitive analog and RF circuits require low noise and low spurious levels.
- Design #3 – Rated for 50 mA, intended for powering SYNT, TCXO, USB, and GP4 (AUX1) circuits. These are also sensitive circuits, requiring low noise and low spurious levels.
- Design #4 – Bias voltage for microphones.

Performance specifications for all four designs are presented in the following subsections.

3.6.3.1 300 mA rating

The linear regulators rated for 300 mA output current are intended for powering the MSM device analog (MSMA), MSM periphery (MSMP), wireless LAN, and Bluetooth circuits. Although rated for 300 mA, higher currents are allowed but higher input voltages may be required and some performance characteristics may become degraded as indicated later in this section.

The 300 mA rated linear regulators offer a low power mode to reduce their quiescent current during the phone's sleep mode. This mode uses reduced current in the feedback loop, causing degraded performance (PSRR, output current capability, etc.). In fact, if the load increases beyond 1 mA the output voltage can go out of spec. This mode should only be used when the phone is in its sleep mode.

Performance specifications for the 300 mA rated linear regulators are listed in Table 3-26.

NOTE VREG_MSMA and VREG_MSMP should always be kept on at their default voltage settings. They are used for powering internal circuits - turning them off or changing their voltage settings can cause unpredictable results.

Table 3-26 Linear regulator performance specifications - 300 mA rating [1] [2]

Parameter	Comments	Min	Typ	Max	Units
Output voltage range [3]	Programmable range	1.500		3.050	V
Voltage error		-3	0	+3	%
Temperature coefficient		-100	0	+100	ppm/C
Transient response [4]					
Settling time	To within 1% of final value		20	100	µs
Over or undershoot		-3	0	+3	%

Table 3-26 Linear regulator performance specifications - 300 mA rating [1] [2]

Parameter	Comments	Min	Typ	Max	Units
Dropout voltage [5]					
I_{rated}/3 load				200	mV
I_{rated}/2 load				250	mV
I_{rated} load				350	mV
Load regulation [6]	$V_{in} > V_{out} + 1$ V; I_{rated}/100 to I_{rated}			0.65	%
Line regulation [7]				0.375	%
Output noise density					
100 Hz to 1000 Hz			2		µV/rt-Hz
1 kHz to 10 kHz			1		µV/rt-Hz
10 kHz to 100 kHz			0.5		µV/rt-Hz
> 100 kHz			0.35		µV/rt-Hz
PSRR [8]	Power supply rejection ratio				
50 Hz to 1000 Hz		40			dB
1 kHz to 100 kHz		40			dB
Spurious [9]	F < 10 MHz		TBD	TBD	dBm
Ground current [10]					
No load	Low-power mode		11	21	µA
No load	Normal-power mode		55	TBD	µA
Loaded	Specified as % of load current			0.5	%

1 All specifications apply over the device's recommended operating conditions, load current range, and capacitor ESR range, unless noted otherwise.

2 Performance characteristics that may degrade if the rated output current (300 mA) is exceeded:
- Dropout voltage
- Load regulation

3 Programmable in 50 mV increments.

4 The stated transient response performance is achieved regardless of the transitory mode – turning the regulator on and off, changing load conditions, changing input voltage, or reprogramming the output voltage setting.

5 For a given output current, adjust the input voltage until $V_{in} = V_{out} + 0.5$ V. Assign V_0 to be this regulated output voltage. Decrease the input voltage until the regulated output voltage drops 100 mV (until $V_{out} = V_0 - 0.1$ V). The voltage drop across the regulator under this condition is the dropout voltage ($V_{dropout} = V_{in} - V_{out}$). The minimum allowable input voltage for this test is 3.0 V.

6 A plot of the typical VREG_MSMP load regulation performance is shown Figure 3-7 in as an example.

7 Line regulation is the output variation due to a changing input voltage, calculated by dividing the output voltage change by the input voltage change, expressed as a percentage. The valid input range for this test is from V_{out} + 1V (+3 V minimum) to the specified maximum V_{DD} value (+4.4 V).

8 PSRR is measured with $V_{out} = V_{in} - 1$ V, with $V_{in} > 3$ V.

9 Spurious output is measured with a high impedance probe as the spurious power into 50 Ω. It is specified for loads from zero to I_{rated}.

10 When set to their low power modes, the MSMA and MSMP regulators can operate while the TCXO is off (phone's sleep mode). The ground current is reduced to 20 µA and the following parameters exhibit reduced performance:
- I_{rated} = 1 mA
- Line regulation = ± 5% max
- Load regulation = 100 mV max (10 mV typ)
- PSRR = 40 dB typ at 50 Hz

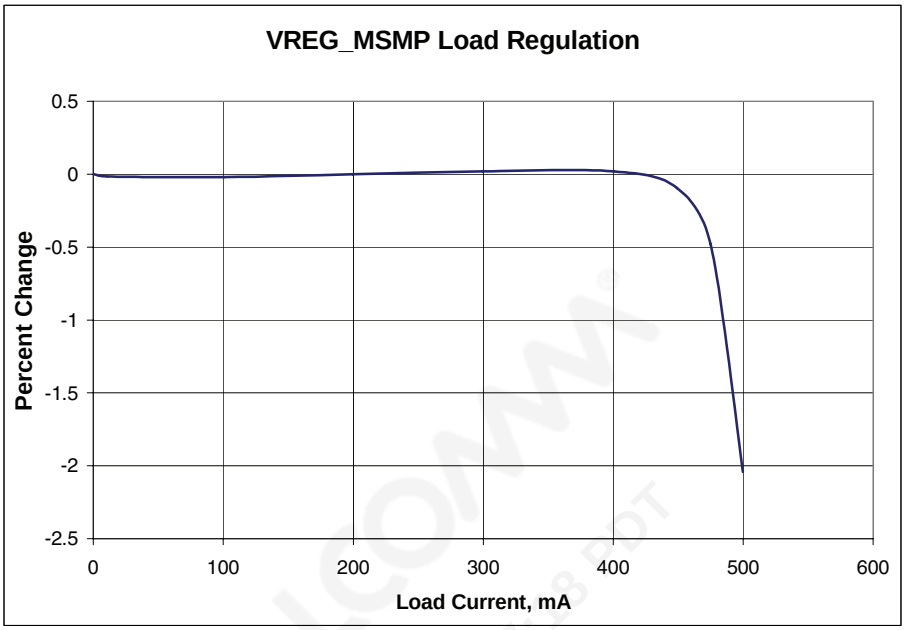

Figure 3-7 Typical VREG_MSMP load regulation

3.6.3.2 150 mA rating

The linear regulators rated for 150 mA output current are intended for powering the MMC, MSME2, RFRX1, RFRX2, RFTX, RUIM2, CAM, MDDI, and AUX2 circuits. Although rated for 150 mA, higher currents are allowed but higher input voltages may be required and some performance characteristics may become degraded as indicated later in this section.

The 150 mA rated linear regulators offer a low power mode to reduce their quiescent current during the phone's sleep mode. This mode uses reduced current in the feedback loop, causing degraded performance (PSRR, output current capability, etc.). In fact, if the load increases beyond 1 mA the output voltage can go out of spec. This mode should only be used when the phone is in its sleep mode.

Performance specifications for the 150 mA rated linear regulators are listed in Table 3-27.

Table 3-27 Linear regulator performance specifications - 150 mA rating [1] [2]

Parameter	Comments	Min	Typ	Max	Unit
Output voltage range [3]	Programmable range				
MSME2 output		0.750	1.500	1.525	V
All other outputs		1.500		3.050	V
Voltage error		-3	0	+3	%
Temperature coefficient		-100	0	+100	ppm/C
Transient response [4]					
Settling time	To within 1% of final value		20	100	µs
Over or undershoot		-3	0	+3	%

Table 3-27 Linear regulator performance specifications - 150 mA rating

Parameter	Comments	Min	Typ	Max	Unit
Dropout voltage [5]					
I_{rated}/3 load				200	mV
I_{rated}/2 load				250	mV
I_{rated} load				350	mV
Load regulation	$V_{in} > V_{out} + 1$ V; I_{rated}/100 to I_{rated}			0.65	%
Line regulation [6]				0.375	%
Output noise density					
100 Hz to 1000 Hz			2		µV/rt-Hz
1 kHz to 10 kHz			1		µV/rt-Hz
10 kHz to 100 kHz			0.5		µV/rt-Hz
> 100 kHz			0.35		µV/rt-Hz
PSRR [7]	Power supply rejection ratio				
MSME2 output					
50 Hz to 1000 Hz		35			dB
1 kHz to 100 kHz		35			dB
All other outputs					
50 Hz to 1000 Hz		50	55		dB
1 kHz to 100 kHz		40	45		dB
Spurious [8]	F < 10 MHz		TBD	TBD	dBm
Discharge time to 0.4 V	RUIM requirement only [9]		0.5	2.0	ms
Ground current					
No load	Low-power mode		11	21	µA
No load	Normal-power mode		55	TBD	µA
Loaded	Specified as % of load current			0.5	%

1 All specifications apply over the device's recommended operating conditions, load current range, and capacitor ESR range, unless noted otherwise.

2 Performance characteristics that may degrade if the rated output current (150 mA) is exceeded:
- Dropout voltage
- Load regulation

3 The MSME2 output is programmable in 25 mV increments; all others in 50 mV increments.

4 The stated transient response performance is achieved regardless of the transitory mode – turning the regulator on and off, changing load conditions, changing input voltage, or reprogramming the output voltage setting.

5 For a given output current, adjust the input voltage until $V_{in} = V_{out} + 0.5$ V. Assign V_0 to be this regulated output voltage. Decrease the input voltage until the regulated output voltage drops 100 mV (until $V_{out} = V_0 - 0.1$ V). The voltage drop across the regulator under this condition is the dropout voltage ($V_{dropout} = V_{in} - V_{out}$). The minimum allowable input voltage for this test is 3.0 V.

6 Line regulation is the output variation due to a changing input voltage, calculated by dividing the output voltage change by the input voltage change, expressed as a percentage. The valid input range for this test is from V_{out} + 1V (+3 V minimum) to the specified maximum V_{DD} value (+4.4 V).

7 PSRR is measured with $V_{out} = V_{in} - 1$ V, with $V_{in} > 3$ V.

8 Spurious output is measured with a high impedance probe as the spurious power into 50 Ω. It is specified for loads from zero to I_{rated}.

9 This specification is driven by RUIM applications that require their supply to be pulled low when disabled. These conditions: nominal load capacitance (2.2 µF) and initial voltage of 3.0 V. Higher capacitance will increase this discharge time.

3.6.3.3 50 mA rating

The linear regulators rated for 50 mA output current are intended for powering the SYNT, TCXO, USB, and AUX1 circuits. Although rated for 50 mA, higher currents are allowed but higher input voltages may be required and some performance characteristics may become degraded as indicated later in this section.

The USB regulator is intended for powering internal USB transceiver circuits only - the VREG_USB output should not be used to power off-chip circuits. Its input voltage is selectable between VREG_5V and USB_VBUS; the desired output voltage of 3.3 V typical requires a higher than usual input voltage.

Performance specifications for the 50 mA rated linear regulators are listed in Table 3-28.

Table 3-28 Linear regulator performance specifications - 150 mA rating [1] [2]

Parameter	Comments	Min	Typ	Max	Unit
Output voltage range [3]	Programmable range				
USB output		3.000	3.300	6.100	V
All other outputs		1.500		3.050	V
Voltage error		-3	0	+3	%
Temperature coefficient		-100	0	+100	ppm/C
Transient response [4]					
Settling time	To within 1% of final value		20	100	µs
Over or undershoot		-3	0	+3	%
Load regulation	$V_{in} > V_{out} + 1$ V; $I_{rated}/100$ to I_{rated}			0.65	%
Line regulation [5]				0.375	%
Output noise density					
100 Hz to 1000 Hz			2		µV/rt-Hz
1 kHz to 10 kHz			1		µV/rt-Hz
10 kHz to 100 kHz			0.5		µV/rt-Hz
> 100 kHz			0.35		µV/rt-Hz
PSRR [6]	Power supply rejection ratio				
50 Hz to 1000 Hz		50	55		dB
1 kHz to 100 kHz		40	50		dB
Spurious [7]	F < 10 MHz		TBD	TBD	dBm
Ground current					
No load	Normal power mode		55	TBD	µA
Loaded	Specified as % of load current			0.5	%

[1] All specifications apply over the device's recommended operating conditions, load current range, and capacitor ESR range, unless noted otherwise.

[2] Performance characteristics that may degrade if the rated output current (50 mA) is exceeded:
- Dropout voltage
- Load regulation

[3] VREG_UBB is programmable in 100 mV increments; all others in 50 mV increments.

[4] The stated transient response performance is achieved regardless of the transitory mode – turning the regulator on and off, changing load conditions, changing input voltage, or reprogramming the output voltage setting.

5 Line regulation is the output variation due to a changing input voltage, calculated by dividing the output voltage change by the input voltage change, expressed as a percentage. The valid input range for this test is from V_{out} + 1V (+3 V minimum) to the specified maximum V_{DD} value (+4.4 V).

6 PSRR is measured with $V_{out} = V_{in}$ - 1 V, with V_{in} > 3 V.

7 Spurious output is measured with a high impedance probe as the spurious power into 50 Ω. It is specified for loads from zero to I_{rated}.

3.6.3.4 MIC bias

The MIC bias circuit supplies a programmable, regulated voltage to the phone's microphone-resistor stack. Pertinent MIC bias performance specifications are listed in Table 3-29.

Table 3-29 Regulator performance specifications - MIC bias

Parameter	Comments	Min	Typ	Max	Units
Output voltage range [1]	Programmable range	1.73	1.80	2.00	V
Voltage error	Max load = 2 mA	-5		+5	%
Start-up time	Max load = 2 mA, 1.0 µF		TBD	TBD	ms
Quiescent current			5		µA
Junction temperature		-55		+150	ºC
Thermal resistance	Junction-to-ambient			62.5	ºC/W
D-S on resistance	Static, V_{GS} = -2.5 V, I_D = -6.0 A			0.026	Ω
Gate threshold voltage	$V_{DS} = V_{GS}$, I_D = -6.0 A	-0.45		-1.00	V

1 Valid settings are 1.73, 1.80, 1.93, and 2.00 V.

3.7 General housekeeping specifications

The PM7540 IC includes many circuits that support handset-level housekeeping functions - tasks that keep the "house," or handset, in order. Integration of these functions reduces the external parts count and the associated size and cost. Housekeeping functions include an analog multiplexer with gain and offset adjustments; system clock circuits; real time clock for time and alarm functions; buffered reference voltage outputs, and over-temperature protection. Associated parameters are specified in the following subsections.

3.7.1 Analog multiplexer with offset and scaling

The PM functions include a 16-to-1 analog multiplexer (Table 3-30) to select a single analog signal for routing to the MSM device's housekeeping analog-to-digital converter.

Table 3-30 Analog multiplexer inputs

Input #	Affiliated PMIC pins	Functional description
0	B11 - VCOIN	Monitors the coin cell voltage; this input path includes a fixed gain of 2/3. Input range = 0 to 3.6 V.
1	F2 - VBAT	Monitors the main battery voltage; this input path includes a fixed gain of 1/2. Input range = 0 to 4.5 V.
2	E2 - VCHG	Monitors the external (charger) supply voltage; this input path includes a fixed gain of 1/8. Input range = 0 to 18 V.
3	C1 - ISNS_P C2 - ISNS_M	Monitors the voltage drop across the external sense resistor; this input path includes a differential amplifier circuit having a gain of 10. Input range = 0 to 0.2 V. The input range is based upon a 0.1 Ω sense resistor and a maximum detected current of 2 A [1].
4	C2 - ISNS_M	Monitors the primary phone power supply voltage (V_{DD}); this input path includes a fixed gain of 1/2. Input range = 0 to 4.5 V.
5 - 9	Multipurpose pins (12) - listed in functional description column	These input paths include two switch matrices and five 2:1 multiplexers that allow up to 10 of the 22 MPPs to be applied as inputs to the analog multiplexer. Input range = 0 to 2.5 V. M7 - MPP_1; N5 - MPP_2; D8 - MPP_3; B12 - MPP_4; D4 - MPP_5; A1 - MPP_6; L12 - MPP_7; M11 - MPP_8; K8 - MPP_9; K9 - MPP_10; K5 - MPP_11; K6 - MPP_12; M3 - MPP_13; N1 - MPP_14; N3 - MPP_15; M5 - MPP_16; B3 - MPP_17; D5 - MPP_18; F4 - MPP_19; G4 - MPP_20; J2 - MPP_21; K2 - MPP_22
10	L1 - USB_VBUS	Monitors the external USB supply voltage; this input path includes a fixed gain of 2/5. Input range = 0 to 5.25 V.
11	None - internal temp sensor	Monitors the on-chip temperature sensor. Input range = -30 °C to +150 °C; output range = 1.216 to 2.116 V.
12	None - internal VREF/2	Monitors the on-chip reference voltage divided by 2 (VREF/2). Input voltage = 0.625 V typical, output voltage = 0.625 V typical.
13	None - internal VREF	Monitors the on-chip reference voltage (VREF). Input voltage = 1.25 V typical, output voltage = 1.25 V typical.
14	None - reserved	This input is reserved for internal test functions.
15	None - multiplexer power off	Disables the multiplexer and disconnects the inputs.

[1] Current detected by the sense resistor includes: charging, the PMIC supply, and the phone's operating currents drawn from V_{DD}.

The output of the analog multiplexer is offset-adjusted, then the new analog voltage is scaled; both the offset and gain are programmable. Performance specifications pertaining to the analog multiplexer and its associated circuits are listed in Table 3-31.

Table 3-31 Offset and scaling performance specifications [1]

Parameter	Comments	Min	Typ	Max	Unit
Minimum output voltage				0.050	V
Maximum output voltage		2.500			V
Fixed prescaler offset errors	Input referred				
Voltage monitors	Channels 0, 1, 2, 4, and 10	TBD		TBD	mV
Current monitor	Channel 3	-30		+30	mA
Fixed prescaler gain errors	Input referred				
Voltage monitors	Channels 0, 1, 2, 4, and 10	TBD		TBD	%
Current monitor	Channel 3	-10		+10	%
AMUX and output adj offset error	Input referred				
With scaling		-30		+30	mV
Bypass mode		-10		+10	mV
AMUX and output adj gain error	Input referred				
With scaling		-1		+1	%
Bypass mode		-0.3		+0.3	%
Integrated non-linearity	INL, input referred			10	mV
Input resistance	Offset = 0, gain = 1	3			MΩ
Input bandwidth	-3 dB corner	1			kHz
Channel-to-channel isolation	f = 1 kHz	50			dB
AMUX output resistance			250	500	Ω
Output settling time [2]			6	15	µs
Reference voltage error [3]	VREF = 1.25 V	-0.35		+0.35	%

[1] Multiplexer offset error, gain error, and INL are measured as illustrated in Figure 3-8. Supporting comments:

- The non-linearity curve is exaggerated for illustrative purposes.
- Input and output voltages must stay within the ranges stated in Table 3-30 and Table 3-31; voltages beyond these ranges result in significant non-linearity and are beyond specification.
- Offset is determined at the minimum output voltage (0.05 V):

$$offset = Vin_{actual}(0.05Volts) - Vin_{ideal}(0.05Volts)$$

- Gain error is calculated from the actual response of the end-point line as the ratio of the two slopes (in percentage):

$$gain\_error = 100\% * \left[\frac{slope\_of\_endpoint\_line}{slope\_of\_ideal\_curve} - 1 \right]$$

- INL is the worst-case deviation from the end-point line. The end-point line removes the gain and offset errors to isolate non-linearity:

$$INL_{\max} = \max\left[Vin_{actual}(x) - Vin_{endpoint\,line}(x)\right]$$
$$INL_{\min} = \min\left[Vin_{actual}(x) - Vin_{endpoint\,line}(x)\right]$$

[2] The output waveform stabilizes within the accuracy specification (no load). This specification does not include the RC settling of the output resistance and the capacitive load on AMUX_OUT.

[3] The reference voltage error is internal, and does not include scaling gain and offset errors.

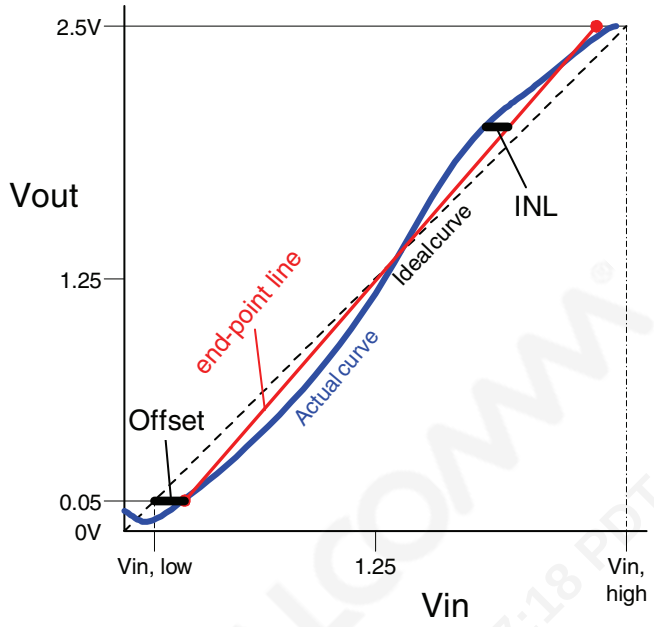

Figure 3-8 Multiplexer offset and gain errors

3.7.2 System clocks

The PM7540 IC includes several clock circuits whose outputs are used for general housekeeping functions and elsewhere within the handset system. These circuits include the TCXO controller and buffers, RC oscillator, 32.768 kHz crystal oscillator, SLEEP clock, and SMPS clocks. These functions are specified in the following subsections.

3.7.2.1 19.2 MHz TCXO controller and buffers

The PM7540 IC optimizes TCXO operation during the slotted mode using a dedicated controller that enables and disables appropriate circuits in the proper sequence. This controller is enabled by the TCXO_EN signal from the MSM device; its polarity is set by software.

The input buffer (at TCXO_IN) accepts sinusoidal or square wave signals at or near 19.2 MHz. This pin's input must be AC-coupled to avoid corrupting internal DC biasing. The input buffer is powered from the TCXO regulator while the output buffer is powered by VREG_MSMP. TCXO_IN and TCXO_OUT meet the digital I/O specifications given that the input amplitude is scaled to VREG_TCXO and the output amplitude is scaled to VREG_MSMP.

TCXO-related circuits are specified in Table 3-32.

Table 3-32 TCXO controller and buffer circuits performance specifications

Parameter	Comments	Min	Typ	Max	Unit
Operating frequency			19.2		MHz
Input amplitude [1]	At TCXO_IN	0.5		V_{TCXO}	Vpp
Input impedance Parallel resistance Parallel capacitance	At TCXO_IN	 50		 2.0	 kΩ pF
Start-up time [2]	From circuit power-on	0.275		62.68	ms
Output logic level Logic high (V_{OH}) Logic low (V_{OL})	$V_X = V_{MSMP}$ I_{OH} = 5 mA I_{OL} = 5 mA	 V_X - 0.45		 0.45	 V V
Output duty cycle [1]	Sinusoid at TCXO_IN	43.5	50	56.5	%
Transition times [3] Rise Fall	10%/90% thresholds; C_{LOAD} < 25 pF	 2 2	 5 5	 10 10	 ns ns
Overshoot voltage [3]				0.3	V
Output clock period [3]			52.08		ns
Output level durations [3] High Low		 20.8 20.8			 ns ns
Current consumption Off Active	 No load on TCXO_OUT			 200 1.2	 nA mA

[1] Sinusoidal or square wave inputs are accepted; an external AC-coupling capacitor is required. Duty cycle testing requires a sinusoidal input. The input buffer is powered by VREG_TCXO (V_{TCXO}), so the input levels are referenced to VREG_TCXO.

[2] Start-up time is programmable; stated values reflect nominal delays based upon clock pulses counted by an on-chip timer. The actual delay is the programmed number of sleep clock periods (accounting for their timing accuracy) plus logic delays. The logic delays fall within the range of (2 sleep clock periods + 2.5 TCXO clock periods) to (3 sleep clock periods + 3.5 TCXO clock periods).

[3] These parameters are specified in support of Bluetooth applications.

3.7.2.2 32.768 kHz crystal oscillator

There are two options for implementing the 32.768 kHz oscillator:

1. Normally: an external crystal that is supplemented by a PMIC inverter and buffer to create an oscillator. The ***external crystal ESR must not exceed 100 kΩ***; if this value is exceeded the circuit may never start oscillating.
2. An external oscillator module could be used rather than a crystal by connecting the module output directly into XTAL_IN and using proper software control. When using an external oscillator module, the XTAL_OUT pin should be unconnected.

Whichever method is used, this oscillator signal is the primary sleep clock source. In both cases, neither the XTAL_IN nor XTAL_OUT pins are capable of driving a load—the oscillator will be significantly disrupted if either pin is loaded.

The PM7540 IC includes a circuit that continually monitors this oscillation. If the circuit stops oscillating, the device automatically switches to the internal RC oscillator and generates an interrupt.

Performance specifications pertaining to the 32.768 kHz oscillator are listed in Table 3-33.

Table 3-33 32.768 kHz oscillator performance specifications

Parameter	Comments	Min	Typ	Max	Units
Oscillation frequency	Set by external components		32.768		kHz
Duty cycle		15	50	85	%
Start-up time [1]				3	s
Halt detection time	Oscillation stopped	30.5		TBD	ns
Jitter					
Cycle-to-cycle				150	ns
Long-term				150	ns
Pulse width at switchover [2]		6.25			µs
External crystal ESR [3]				100	kΩ
Operating voltage		1.5			V

[1] Start-up time is specified with a crystal having an ESR of 60k.

[2] When switching over from RC to crystal (or vice-versa), the SLEEP_CLK pulses will be at least this wide; more narrow pulses could lock-up the MSM device.

[3] The oscillator may fail to start up if the crystal ESR exceeds 100k.

3.7.2.3 RC oscillator

As mentioned in the last section, the PM7540 IC includes a circuit that continually monitors the 32.768 kHz oscillator signal. If this source stops oscillating, the PMIC automatically switches to the on-chip RC oscillator and sends an MSM interrupt. SMPL timers are driven by the RC oscillator; since the oscillator runs off supply voltages as low as 1.5 V a capacitor can be used in place of the coin cell and the SMPL features will still be supported.

RC oscillator performance specifications are listed in Table 3-34.

Table 3-34 RC oscillator performance specifications

Parameter	Comments	Min	Typ	Max	Units
Oscillation frequency		2.4	3.2	4.8	MHz
Divider in SLEEP_CLK path			100		---
Operating voltage		1.5			V

3.7.2.4 Sleep clock

The SLEEP_CLK output is derived from one of two sources:

- RC oscillator - An on-chip circuit with coarse frequency accuracy; not used in a normal mode. This path includes a divide-by-100 circuit that reduces the 3.2 MHz RC oscillator output to a 32 kHz clock (nominal values).
- Crystal oscillator - Usually implemented using an internal inverter and buffer plus an external 32.768 kHz crystal and two capacitors. This low power source can have high accuracy and stability, depending upon the external crystal.

The SLEEP_CLK output toggles only when the PM7540 IC is on; it stays low when the IC is off even though the oscillator continues to run. Additional performance specifications for the SLEEP_CLK output are listed in Table 3-35.

Table 3-35 SLEEP_CLK output performance specifications

Parameter	Comments	Min	Typ	Max	Unit
Output frequency					
Crystal oscillator or module source	Set by external crystal		32.768		kHz
RC oscillator source	RC frequency divided by 100	24	32	48	kHz
Output logic level	$V_X = V_{MSMP}$				
Logic high (V_{OH})	I_{OH} = 2 mA	V_X - 0.45			V
Logic low (V_{OL})	I_{OL} = 2 mA			0.45	V
Duty cycle		15	50	85	%

3.7.3 Real-time clock

The real time clock (RTC) functions are implemented by a 32-bit real time counter and one 32-bit alarm, both configurable in one-second increments. The primary input to the RTC circuits is the 32.768 kHz clock from the crystal oscillator. When the phone is off, the crystal oscillator and RTC continue to run off the main battery. If the main battery is not present, these circuits run off the coin cell attached to VCOIN.

The RTC reset interrupt is generated if the coin cell voltage drops too low (and the main battery is not present). If this interrupt occurs, the RTC might be corrupted. A different interrupt is generated if the crystal oscillator stops—this signifies that handset timing is no longer accurate. Again, the RTC is corrupted.

The RTC is an entirely embedded function, without the external I/Os needing to be specified. All its controls and output data are accessed internally, and its accuracy depends entirely on the oscillator source being used—both are defined elsewhere. Therefore, no RTC performance parameters need to be defined here.

3.7.4 Buffered VREF outputs

All 22 MPPs can be configured as a selectable, buffered VREF output voltage (see Section 3.4 for specification details). One MPP is intended to be used as an analog output voltage: pin M11, MPP_8 (REF_OUT). Selectable voltages are VREF/2, VREF, or 2xVREF.

3.7.5 Over-temperature protection (smart thermal control)

The PM7540 IC provides over-temperature protection in stages, depending upon the level of urgency as die temperature rises:

- Stage 0 – normal operating conditions (less than 105 °C).
- Stage 1 – 105 °C to 125 °C; an interrupt is sent to the MSM device without shutting down any PMIC circuits.
- Stage 2 – 125 °C to 145 °C; an interrupt is sent to the MSM device and high current drivers (LED drivers, speaker drivers, etc.) are shut down.
- Stage 3 – greater than 145 °C; an interrupt is sent to the MSM device and the PMIC is completely shut down.

Temperature hysteresis is incorporated such that the die temperature must cool significantly before the device can be powered on again. If any start signals are present (KPDPWR_N pulled low, charger present, etc.) while the PMIC is at Stage 3, they are ignored until Stage 0 is reached. When the device cools enough to reach Stage 0 and a start signal is present, the PMIC will power up immediately. If no start signal is present at that time, the PMIC stays off but continues to monitor trigger-events for the next start signal.

3.8 User interface specifications

In addition to housekeeping functions, the PM7540 IC also supports common handset-level user interfaces. Three dedicated current sinks are intended for driving the keypad backlight, the LCD backlight, and a camera flash. In addition, one multipurpose pin (MPP) is expected to be used a a general-purpose LED driver, though more of the 22 MPPs could be allocated as LED drivers as well. All drivers provide programmable brightness (current) control.

Alerting the handset user of incoming calls is supported with vibration and audio driver circuits. A vibration motor driver, compatible with 1.3 to 3.0 V devices (programmable), supports silent alarms. A two-channel speaker driver is available for audible alarms; it supports higher audio power applications such as speakerphone or melody ringer as well. The speaker driver has programmable gain, turn-on time, and muting, and operates as two differential devices, each delivering a volume-controlled 500 mW output to its external 8-Ω speaker.

And finally, a video amplifier is included that is capable of driving a standard 150-Ω TV port, allowing the handset to be used as a camcorder or for slide presentations.

All indicator and driver circuits are specified in this section.

3.8.1 Current drivers

The four backlight or LED drivers are independently programmable, ground-referenced current sinks with low voltage compliance, making them suitable for many applications. Three drivers are intended for specific applications and are named accordingly:

- KPD_DRV_N is intended to drive the keypad backlight
- LCD_DRV_N is intended to drive the LCD backlight
- FLSH_DRV_N is intended to drive high-voltage, high-current white or blue LEDs often used as a camera flash

All 22 MPPs can be configured as a current driver (see Section 3.4 for details). One MPP is intended to be used as a current driver: MPP_7 (GP1_DRV_N). MPPs configured as general-purpose drivers are expected to be used to light green or red LEDs. When more than one LED is driven by a single output pin ballast resistors may be required (depending upon the matching between LEDs).

In addition to SBI controls, the flash driver can be enabled and disabled through MPP pins via the internal DBUS. This technique is explained in the *PM7540 Power Management IC User Guide*, 80-VD691-3.

Current driver performance specifications are listed in Table 3-36.

Table 3-36 Current driver performance specifications [1]

Parameter	Comments	Min	Typ	Max	Unit
Keypad backlight driver current	KPD_DRV_N output	0		150	mA
LCD backlight driver current	LCD_DRV_N output	0		150	mA
Flash LED driver current		0		600	mA
General purpose driver current	Any MPP used as a GP current sink	0		40	mA
Driver voltage compliance		0.5			V
LED current error [2]	V_{out} = 0.5 to (V_{DD} - 1) V	-20		+20	%
LED current leakage	Off state; V_{out} = 4.5 V	-200		+200	nA

[1] Driver current settings are programmable as follows:
- Keypad and LCD: from 0 to 150 mA in 10 mA increments
- Flash LED: from 0 to 600 mA in 40 mA increments
- GP: from 5 to 40 mA in 5 mA increments plus a tri-state (disabled) option

[2] The specified current accuracy requires an output voltage within the range of 0.5 to (V_{DD} - 1) V; the drive current can vary if the output voltage is beyond this range.

In addition to SBI controls, the current drivers can be enabled and disabled using MPP pins via the internal DBUS. This technique is explained in the PM7540 IC User Guide (80-VD691-3).

3.8.2 Vibration motor driver

The PM7540 device supports silent incoming-call alarms with its vibration motor driver. The vibration driver is a programmable voltage output that is referenced to V_{DD}; when off, its output voltage is V_{DD}. The motor is connected between V_{DD} and the VIB_DRV_N pin.

In addition to SBI controls, the vibration motor driver can be enabled and disabled using MPP pins via the internal DBUS. This technique is explained in the PM7540 IC User Guide (80-VD691-3).

Performance specifications for the vibration motor driver circuit are listed in Table 3-37.

Table 3-37 Vibration motor driver performance specifications

Parameter	Comments	Min	Typ	Max	Unit
Vibration motor voltage (V_m) [1]	Programmable range, 100 mV steps	1.2		3.1	V
Output voltage (V_m) error	V_{DD} > 3.2 V; I_m = 0 to 175 mA; V_m setting = 1.2 to 3.1 V	-350		+100	mV
Short circuit current	VIB_DRV_N = V_{DD}	225		525	mA
Driver bias current [2]	I_m = 175 mA			TBD	µA
Driver leakage current				100	nA

[1] The vibration motor driver circuit is a low-side driver. The motor is connected directly to V_{DD}, and the voltage across the motor is $V_m = V_{DD} - V_{out}$, where V_{out} is the PMIC voltage at VIB_DRV_N.

[2] Driver bias current is the change in I_{DD} when the motor driver is turned on less the motor current.

3.8.3 Speaker drivers

The PM7540 IC supports audio outputs with its two-channel variable gain audio amplifier and speaker driver. The inputs can be configured for stereo differential, stereo single-ended, or mono differential; outputs can be configured for stereo or mono sound. Each output is designed for direct differential connection to an 8-Ω speaker. Several speaker parameters are SBI-programmable, with independent controls for each channel:

- Gain – can be set from -16 to +12 dB in 4 dB increments.
- On/off – speaker circuits can be enabled or disabled.
- Mute – speaker output can be muted or not.
- Delay – a short (~10 ms) or long (~100 ms) delay is selectable.

Speaker driver performance specifications are listed in Table 3-38.

Table 3-38 Speaker driver performance specifications [1]

Parameter	Comments	Min	Typ	Max	Unit
Input frequency range		0.20		20	kHz
Input resistance	Differential	10	72	86	kΩ
Input drive level				0.5	V_{RMS}

Table 3-38 Speaker driver performance specifications [1] (continued)

Parameter	Comments	Min	Typ	Max	Unit
Output power (P_{rated}) [2]	THD < 0.5%		500		mW
Power efficiency [2]	at P_{rated}	50			%
Amplifier gain	Programmable, 4 dB increments	-16		+12	dB
Amplifier gain error		-1	0	+1	dB
Amplifier gain flatness	20 Hz to 20 kHz	-0.2		+0.2	dB
Output referred noise	V_{in} = 0 V, 20 Hz to 20 kHz, 8 Ω, measured with A-weighting applied				
G = -16 dB			1.90	13.1	μV_{RMS}
G = -12 dB			2.03	13.0	μV_{RMS}
G = -8 dB			2.80	16.6	μV_{RMS}
G = -4 dB			9.60	25.3	μV_{RMS}
G = 0 dB			18.5	25.1	μV_{RMS}
G = +4 dB			24.8	44.2	μV_{RMS}
G = +8 dB			38.2	82.4	μV_{RMS}
G = +12 dB			55.7	82.4	μV_{RMS}
Output bandwidth at P_{rated} [3]	8 Ω load, 12 dB gain		20		kHz
Output offset voltage		-40		+40	mV
THD + noise	20 Hz to 20 kHz, P_{rated}			5	%
Power supply rejection ratio	V_{in} = 0V; V_{DD} = 3.6 V + 0.1 V_{RMS}				
f = 20 Hz to 100 Hz		55			dB
f = 100 Hz to 5 kHz		65			dB
f = 5 kHz to 15 kHz		55			dB
f = 15 kHz to 20 kHz		50			dB
Turn-on time delay	Amplifier enable to output within 1% of its final value				
Short delay			10	12.5	ms
Long delay			100	125	ms
Pop and click levels [4]	Power, enable, gain, or mute transitions			11	mV_{PK}
Mute suppression	V_{in} = 2 V_{RMS}	80			dB
Channel-to-channel isolation	500 mW each, 1 kHz	40			dB
High pass filter accuracy			15		%
High pass filter programmability			15		%
Quiescent current [5]				6.2	mA

1 All specifications are valid when tested with an 8 Ω, differentially connected load resistor, output power levels from 0 to 500 mW, and V_{DD} = 3.6 V (unless stated otherwise).

2 The specified output power (P_{rated}) and efficiency is achieved while meeting the stated total harmonic distortion (THD) performance. Test conditions include: differential output pins connected to an 8 Ω resistor, 1 kHz sinusoidal test signal, amplifier programmed for 12 dB gain, and V_{DD} = 3.6 V. A plot showing typical speaker output power and THD performance versus the supply voltage is shown in Figure 3-9.

3 The output bandwidth specification maintains the specified total harmonic distortion and gain flatness under the given test conditions.

4 Pop-and-click is measured as the peak transient output voltage during power on/off, enable/disable, gain step, or mute/unmute transitions, with an A-weighted filter applied.

5 The quiescent current does not include the output current at the load due to any output offset voltage.

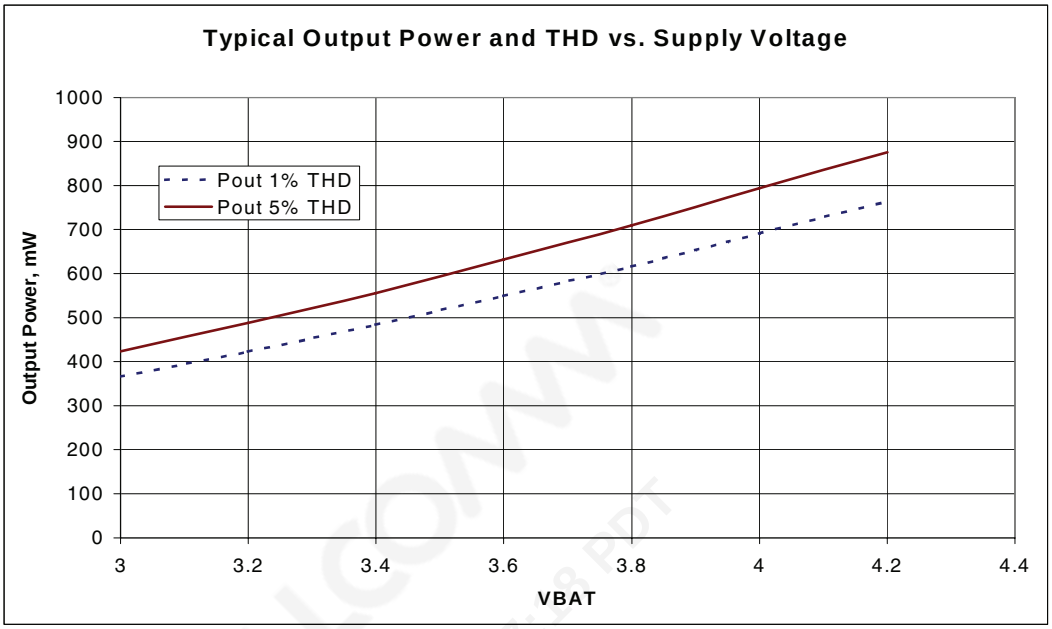

Figure 3-9 Speaker output power and THD vs. supply voltage

3.8.4 Video (TV) amplifier

The PM7540 IC includes a video amplifier that is capable of driving a standard 150-Ω TV port. The PMIC video input (VIDEO_IN) is driven by the MSM device's TV_OUT signal. The PMIC output (VIDEO_OUT) detects when a load is connected and automatically enables the amplifier. The output also detects when the load is disconnected and reports the changed status to the MSM device. This eliminates the need to change user interface settings when the phone is being used as a camcorder for playing videos or making slide presentations.

Video amplifier performance specifications are listed in Table 3-39.

Table 3-39 Video amplifier performance specifications

Parameter	Comments	Min	Typ	Max	Unit
Input voltage		0.05		1.35	V_{PK}
Passband		0		6	MHz
Passband gain		5.6	6.0	6.4	dB
Gain flatness	Over passband; V_{out} = 1.4 V_{PP}	-0.1		+0.1	dB
Input offset voltage				TBD	mV
Input voltage noise	f = 1 MHz			5.8	nV/rt-Hz
Signal-to-noise ratio	f - 6 MHz	50			dB
Spur free dyn range	f = 1 MHz; V_{out} = 1.4 V_{PP}	52			dBc
Slew rate		75			V/µs
Settling time	2 V step			40	µs

Table 3-39 Video amplifier performance specifications (continued)

Parameter	Comments	Min	Typ	Max	Unit
PSRR					
< 100 kHz		75			dB
100 kHz to 1 MHz		50			dB
1 MHz to 6 MHz		35			dB
Output impedance					
< 100 kHz				0.1	Ω
100 kHz to 1 MHz				0.5	Ω
1 MHz to 6 MHz				3.0	Ω
Output drive current		TBD			mA
Supply voltage	Powered from VDD	3.3		4.5	V
Power supply current					
Off			3.4	10	µA
Quiescent			3.9	5	mA
All black screen			TBD	TBD	mA
All white screen			TBD	TBD	mA

3.9 IC-level interface specifications

The PM7540 IC-level interface circuits include power-on circuits, the SBI, the interrupt manager, a USB-OTG transceiver, and RUIM level translators. Performance specifications for all these circuits and functions are presented in the following subsections.

3.9.1 Power-on circuits and the power sequences

Dedicated circuits continuously monitor five events that might trigger a power-on sequence. If any of the five events occur these circuits power-on the PMIC, determine the handset's available power sources, enable the correct source, and take the MSM device out of reset.

The inputs to the power-on circuit {MPP_3 (CBL0PWR_N), MPP_4 (CBL1PWR_N), PS_HOLD, and KPDPWR_N} are basic digital control signals that must meet the input voltage level requirements stated in Table 3-3. The KPDPWR_N input is pulled-up to an internal voltage. When the cable power-on feature is enabled via fuse trim, the CBL0PWR_N and CBL1PWR_N inputs are also pulled-up to an internal voltage.

The only external output is PON_RESET_N; it must meet the output voltage level and current drive requirements stated in Table 3-3. Additional power-on circuit performance specifications are listed in Table 3-40. Complete definitions for time intervals included in the table are defined in the *PM7540 Power Management IC User Guide* (80-VD691-3).

Table 3-40 Power-on circuit performance specifications

Parameter	Comments	Min	Typ	Max	Units
Internal pull-up resistor [1]	At xxxPWR_N pins	200	250	300	kΩ
Sequence time intervals [2]					
t_{reg1}	Power-on event to first regulator enable [3]	0	6	10	ms
t_{reg}	Delay between regulator turn-ons [4]		4		clocks
t_{settle}	Regulator settling time [4]		4		clocks
t_{reset1}	Last regulator on to PON_RESET_N = H	10	20	30	ms
t_{pshold}	PS_HOLD timeout	133	200	300	ms
t_{reset0}	PON_RESET_N = L to first regulator off	6.67	10	15	ms
t_{off}	Delay between regulator turn-offs [5]	1.6	2	2.4	ms
Regulator accuracy	To continue power-on sequence	4	7	9	%
Keypad button delay	De-bounce [6]	0		64	ms

[1] These internal resistors are pulled up to an internal voltage net (dVdd). The KPDPWR_N input is pulled-up directly; the CBLxPWR_N inputs are pulled-up through a diode (to approximately dVdd - 0.7 V).

[2] All time intervals are derived from the selected clock source (32.768 kHz typical); their tolerances are set accordingly. See Figure 3-10 and the *PM7540 Power Management IC User Guide* (80-VD691-3) for further discussion.

[3] The first regulator turn-on time (t_{reg1}) depends upon the bandgap reference decoupling capacitor at REF_BYP. The specified value is based upon 0.1 µF.

[4] There is a delay of four SLEEP_CLK cycles after one regulator settles before the next regulator is enabled. Each regulator will settle to within 9% of its final value within four SLEEP_CLK cycles. The regulators are turned on in the following order (as illustrated in Figure 3-10): 1 = MSMC1, 2 = MSMC2, 3 = MSME, 4 = MSME2, 5 = MSMP, 6 = MSMA, and 7 = TCXO.

[5] The TCXO regulator is turned off when PON_RESET_N goes low. The MSMA regulator is turned off next, after a delay of t_{reset0}. VREG_MSMA is allowed to discharge for t_{off} before the MSMP regulator is turned off, and VREG_MSMP is allowed to discharge for another t_{off} before the MSME2 regulator is turned off. After another t_{off} interval, all other regulators are disabled and the PMIC is powered down.

[6] This delay from when the KPDPWR_N signal transitions to when the KPDPWR interrupt is triggered is SBI-programmable to binary values from 1 to 64 ms (with the value of 0 ms available to disable the de-bounce function).

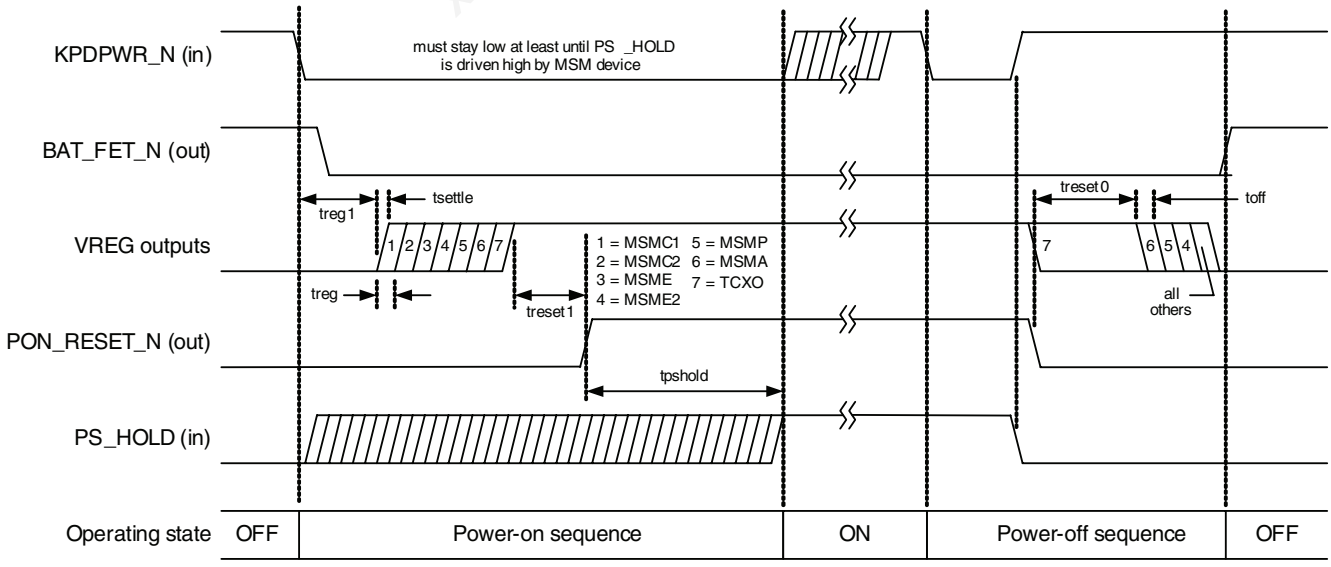

Figure 3-10 High-level power sequences timing diagram

3.9.2 Serial bus interface

The PM7540 IC allows two serial bus interface (SBI) implementations:

- A 3-wire SBI interfaces that support earlier MSM devices
- A single-wire SBI (SSBI) that supports later MSM devices

In both cases, the SBI provides efficient initialization, status, and control communications. Proper connections for both modes are defined in Table 2-6.

Configurable device parameters are set through SBI control registers, while many other registers are available to report parameter settings, device status, and interrupt events. Handset designers use the application programming interface (API) to program the PM7540 IC, indirectly exercising the SBI. The API is documented in DMSS software - please see applicable DMSS software documentation.

The coin cell backs up power to several SBI registers related to the 32.768 kHz crystal oscillator, real-time clock, and SMPL. See Section 3.5.9 for details. Upon PMIC power-up the SBI defaults are all restored except the bits backed up by the coin cell. These backed-up bits are only restored to default values if the coin cell has expired (RTCRST interrupt is active); otherwise the previous values are kept.

Section 3.3 includes SBI logic level requirements; further specification is not required.

3.9.3 Interrupt manager

The PM7540 interrupt manager receives internal reports on numerous functions and conveys real-time and latched status signals to the MSM device, thereby supporting the MSM device's interrupt processing.

The interrupt manager is an embedded function that does not require I/O specifications. All of its controls and output data are accessed via the SBI, and its accuracy depends entirely on circuits implemented elsewhere.

See the *PM7540 Power Management IC User Guide* (80-VD691-3) for a more complete discussion of interrupt functions.

3.9.4 Universal serial bus/on-the-go

The PM7540 IC includes an integrated universal serial bus/on-the-go (USB-OTG) transceiver on-chip. This circuit is compatible with *USB 2.0 Specification*, and the *OTG Supplement*, both of which are available at www.usb.org. The PM7540 IC is also compliant with the *OTG Transceiver Specification* and the *Mini-USB Analog Carkit Interface* (CEA-936-A), both of which are being developed by the Consumer Electronics Association (CEA).

The USB-OTG transceiver provides the following features:

- It supports the USB low-speed (1.5 Mb/s) and full-speed (12 Mb/s) modes.

- Interfaces the handset's MSM device to external USB devices or an RS-232 device. When interfacing with USB devices, the handset could function as a USB A or B type device.
  - When used as an A device, the handset provides power to the peripheral device through the PM7540 USB_VBUS pin.
  - When used as a B device, the handset is powered from the host device.
- UART driver and receiver for USB car kit and RS-232 dongle support.
- Very low power threshold comparators for ID detection and VBUS detection.
- Full complement of interrupts and hardware timers; no polling required.
- USB audio mode for USB car kit support (as specified in the next section).

The PM7540 IC contains the transceiver only; the MSM device provides the USB controller and UART. The MSM side of the transceiver consists of the USB_OE, USB_DAT, and USB_SE0 pins; the external side uses the USB_D_P, USB_D_M, and USB_ID pins.

Performance specifications for the USB-OTG transceiver circuits are given in Table 3-41.

Table 3-41 USB-OTG transceiver performance specifications

Parameter	Comments	Min	Typ	Max	Units
VBUS					
Voltage output to V_{BUS}	I_{VBUS} = 0 to 25 mA	4.40		5.25	V
Current output from V_{BUS}		100			mA
VBUS valid comparator [1] rising threshold falling threshold		 4.554 4.400	 4.600 4.500	 4.646 4.545	 V V
Session valid comparator [2] rising threshold falling threshold		 1.826 1.714	 1.844 1.731	 1.862 1.748	 V V
ID detection					
ID pin pull-up resistance		70	100	130	kΩ
A-device detection threshold			$0.15 \cdot V_{DD}$		V
B-device detection threshold			$0.8 \cdot V_{DD}$		V
Transceiver DC characteristics					
Input sensitivity (differential)	ID+ - D-I, V_{in} = 0.8 to 2.5 V	0.2			V
Common-mode range (diff)	Includes V_{DI}	0.8		2.5	V
Receiver threshold	Single-ended	0.8		2.0	V

Table 3-41 USB-OTG transceiver performance specifications (continued)

Parameter	Comments	Min	Typ	Max	Units
Receiver hysteresis			200		mV
Output voltage	OE = 0				
Logic low	R_L = 1.5k to 3.6 V			0.3	V
Logic high	R_L = 15k to GND, I_O = 1 mA	2.8		3.6	V
High-Z state output impedance	OE = 1; 0 V < V_{DD} < 3.6 V; measured at D+ and D- pins to GND	300			kΩ
Series output resistance	D+, D-	28	36	44	Ω
Internal pull-up resistor	On D+ and D-				
Idle mode		0.900	1.250	1.575	kΩ
Receiving mode		1.425	2.250	3.090	kΩ
Internal pull-down resistor	D+ to GND, D- to GND	14.26	19.53	24.80	kΩ
Transceiver input capacitance	D+ and D- pins to GND			20	pF
Driver characteristics - full and low speed					
Output signal crossover voltage		1.30		2.00	V
Drive disable to tri-state delay				15	ns
High to off				15	ns
Low to off					
Drive tri-state to enable delay				15	ns
Off to high				15	ns
Off to low					
Driver characteristics - full speed					
Transition time					
Rise time (t_R)	C_L = 50 to 125 pF	4		20	ns
Fall time (t_F)	C_L = 50 to 125 pF	4		20	ns
Rise/fall time matching		90		111	%
Output signal crossover voltage	Full to low speed	1.30	1.65	2.00	V
Driver characteristics - low speed					
Transition time					
Rise time (t_R)	C_L = 50 to 600 pF	75		300	ns
Fall time (t_F)	C_L = 50 to 600 pF	75		300	ns
Rise/fall time matching		80		125	%
Power supplies					
Termination voltage	VREG_USB	3.0	3.3	3.6	V

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Table 3-41 USB-OTG transceiver performance specifications (continued)

Parameter	Comments	Min	Typ	Max	Units
System supply voltage	0.1 V regulator headroom	3.1	3.6	4.5	V
System supply current					
Shutdown mode					
from VDD			6	10	µA
from USB_VBUS			3.7	10	µA
Suspend mode					
from VDD			15	50	µA
from USB_VBUS			75	125	µA
Full-speed idle	D+ < 2.8 V, D- < 0.3 V; I_{VBUS} = 0		6	500	µA
Full-speed Tx			TBD	TBD	µA
Low-speed Tx	C_L = 50 pF on D+, D-; I_{VBUS} = 0		TBD	TBD	mA
	C_L = 350 pF on D+, D-; I_{VBUS} = 0				

1 When acting as a USB host, the phone outputs voltage on VBUS. If the voltage on VBUS drops below its Vvbus_vld threshold, the attached peripheral is drawing too much current and cannot be supported.

2 If the voltage on VBUS is greater than its Vsess_vld threshold the phone is allowed to assert D+ and be enumerated as a USB peripheral.

3.9.5 USB pins as an audio interface

The USB pins intended to interface with external circuits, USB_D_P and USB_D_M, can be configured as an audio output capable of driving a car kit; pertinent performance specifications are listed in Table 3-42.

Table 3-42 USB audio mode performance specifications

Parameter	Comments	Min	Typ	Max	Units
Maximum input amplitude	Single-ended, no output clipping	2.2			V_{PP}
Input impedance		28.8	36.0	43.2	kΩ
Output impedance				50	Ω
Bandwidth	-3 dB, 1 kHz reference	20			kHz
Audio path THD + N	1.664 V_{PP} single-ended, 1 Ω input		0.1	0.2	%
USB data to audio isolation [1]		83			dB
Channel-to-channel isolation [2]	Between D+, D- pins and ID pins	60			dB
Power supply rejection ratio	300 mV_{PP} on V_{DD}; 0 to 30 kHz	48	55		dB
Audio output short circuit current	D+ or D- shorted to ground		3	5	mA

Table 3-42 USB audio mode performance specifications

Parameter	Comments	Min	Typ	Max	Units
Bias for car kit in audio mode		1.0		3.0	V
Supply current					
Active			TBD	TBD	µA
Off			TBD	TBD	µA

1 This isolation is measured by disabling the USB audio circuit, turning on the speaker driver, driving the USB outputs with a 3.3 V USB data stream in the audio frequency range, and measuring the USB data leakage level at the speaker driver outputs.

2 Applied signal characteristics: DC bias = 0.4 V, AC amplitude = 600 mV_{PP}, swept in frequency from 20 Hz to 20 kHz.

3.9.6 RUIM level translators

All MPP pairs can be configured as RUIM level translators; three pairs are intended to be used as level translators that interface the handset's MSM device to an external RUIM module: MPP5/6, MPP9/10, and MPP11/12. All MPP pairs, including their pin assignments, are listed in Table 3-5. Performance specifications for MPP circuits configured as RUIM level translators are included in Table 3-4.

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4 Mechanical Specifications

Mechanical specifications for the PM7540 device are presented in this chapter, including physical dimensions, thermal characteristics, moisture sensitivity level, and visible markings. Additional details pertaining to these topics are available in *BGA/CSP Package User Guide* (80-V2560-1).

4.1 Device physical dimensions

The PM7540 device is available in the 137-pin chip-scale package (137 CSP) that includes several ground pins near its center for electrical grounding, mechanical strength, and thermal continuity. The 137 CSP package has a 7 mm by 7 mm body with a maximum height of 1.2 mm. Pin A1 is located by an indicator mark on the top of the package. A complete detailed mechanical drawing is shown in Figure 4-1.

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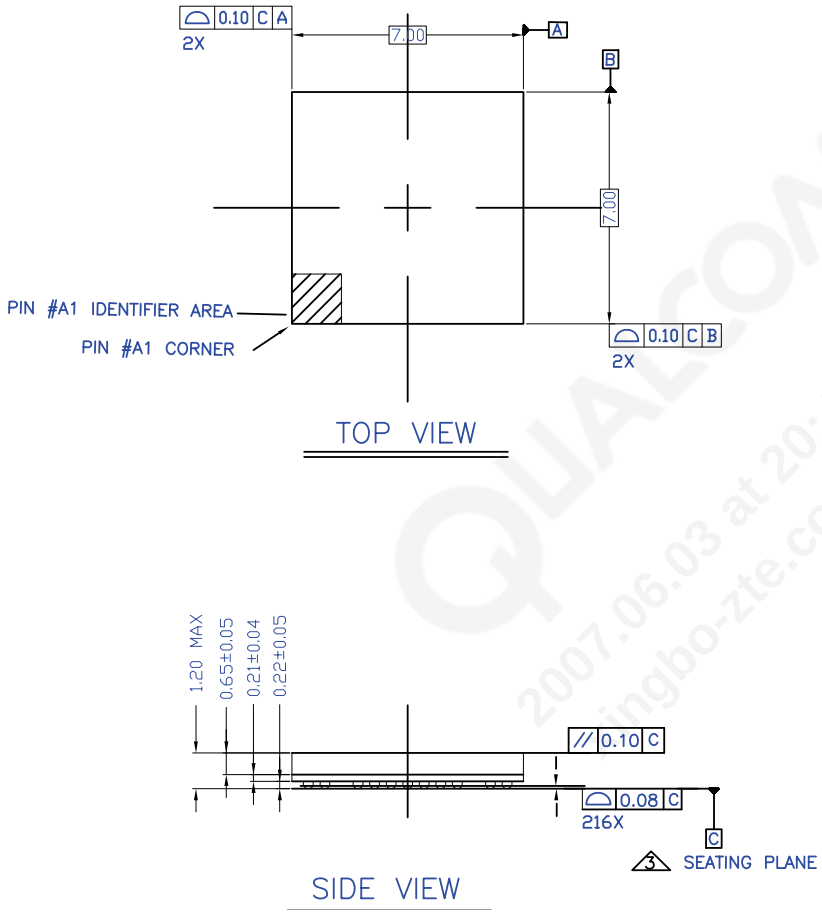

NOTE

1. ALL DIMENSIONS AND TOLERANCE CONFORM TO ASME Y 14.5M–1994.
2. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C .
3. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
4. ALL DIMENSIONS IN MILLIMETERS (MM)

Figure 4-1 PM7540 package outline drawing (137 CSP)

4.2 Device thermal characteristics

The PM7540 device in its 137-CSP package has a typical thermal resistance of TBD °C/W, as shown in Table 4-1.

Table 4-1 Device thermal resistance

Parameter		Comments	Min	Typ	Max	Units
θ_{JA}	Thermal resistance, J-to-A	Junction to ambient (still air) [1] [2]	TBD	TBD	TBD	°C/W
θ_{JC}	Thermal resistance, J-to-C	Junction to case	TBD	TBD	TBD	°C/W

[1] A value of TBD min °C/W was measured during model validation experiments. The conditions and board construction used during the experiment was based on JEDEC standard JESD51-7 with 16 vias, which is an industry baseline used for package-to-package comparison.

[2] The more realistic TBD typ °C/W was obtained from using 70% solder coverage, 16 vias, and 100% epoxy coverage. The following is recommended for optimal thermal conditions: optimize solder coverage during SMT assembly, minimum of 16 filled vias located below the die area (centered), vias to route Cu layer directly below multiple layers (if possible), and optimize board layout.

4.3 Device moisture sensitivity level

Plastic encapsulated surface mount packages are susceptible to damage induced by absorbed moisture and high temperature. During device qualification, QCT follows the latest revision IPC/JEDEC J-STD-020 standards in determining device moisture sensitivity level (MSL). To ensure proper SMT assembly, procedures must abide by the MSL and maximum reflow temperature specified on the ESD shipping bag labels or bar code labels accompanying all QCT devices.

Refer to the shipping bag ESD label or bar code label for the PM7540 device's moisture sensitivity level and reflow temperature.

Refer to Section 5.2 of this document for typical manufacturing solder reflow conditions and component heat exposure limits.

4.4 Device marking

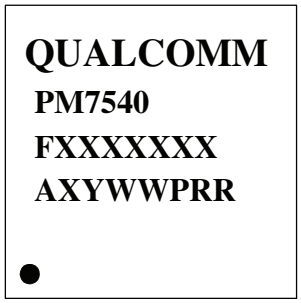

Figure 4-2 PM7540 device marking (top view - not to scale)

Table 4-2 Device marking line descriptions

Line	Marking	Description
1	QUALCOMM	QUALCOMM name or logo
2	PM7540	QUALCOMM product name
3	FXXXXXXX	F = supply source code F = TBD XXXXXXX = traceability number
4	AXYWWPRR	A = assembly site code A = TBD X = traceability number Y = single-digit year code WW = work week (based on calendar year) P = product configuration code P = TBD RR = product version RR = 00 = engineering sample, HW ID = TBD
5 [1]	X...X	X...X = traceability number

[1] Additional lines may appear on some engineering samples - this is manufacturing information that is only relevant to QUALCOMM and its suppliers.

5 PCB Mounting Specifications

Procedures and specifications for mounting the PM7540 device on a printed circuit board (PCB) are presented in this chapter, including land pad and stencil design details, SMT process characterization, surface mount technology (SMT) process verification, and storage recommendations after the devices are removed from their shipping packages. Additional details pertaining to these topics are available in *BGA/CSP Package User Guide* (80-V2560-1).

5.1 Land pad and stencil design

The land pattern and stencil recommendations presented in this section are based upon QUALCOMM internal characterizations for SnPb and lead-free solder pastes on a four-layer test PCB and a 127 microns thick stencil. The PCB land pattern for the 137 CSP package is the same whether SnPb or lead-free solder is used (Figure 5-1).

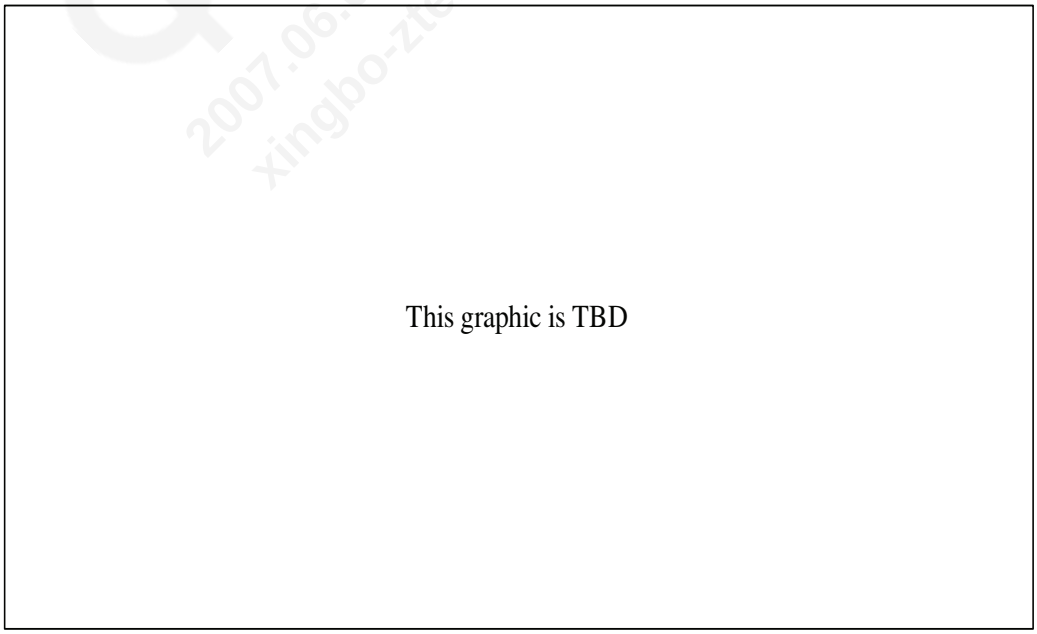

Figure 5-1 Recommended 137 CSP land pattern (TBD)

The 137 CSP solder stencil pattern can use square (Figure 5-2) or circular (Figure 5-3) apertures.

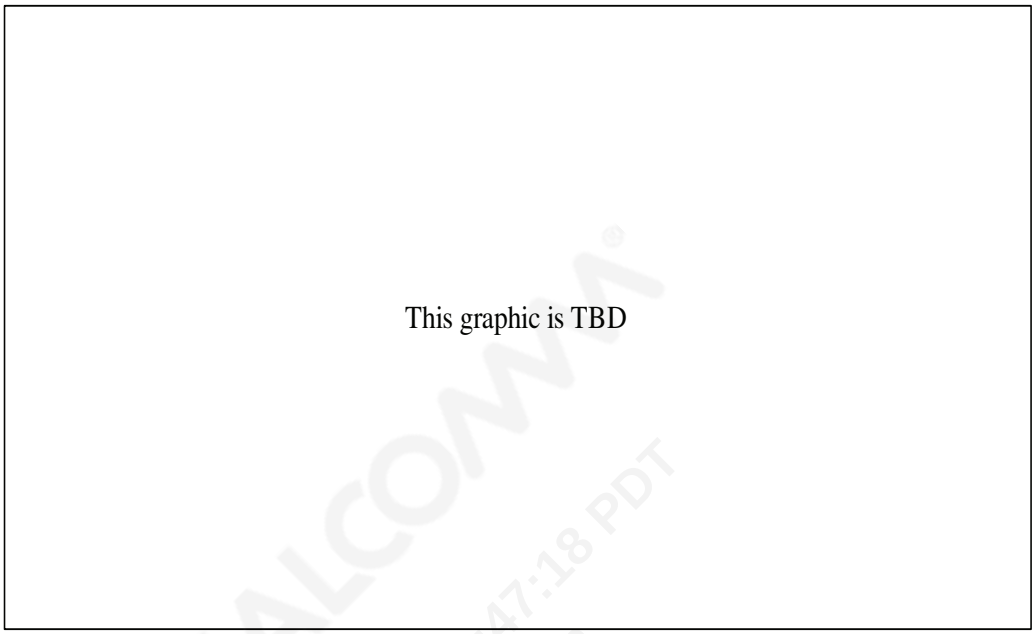

Figure 5-2 Recommended 137 CSP stencil pattern - square apertures (TBD)

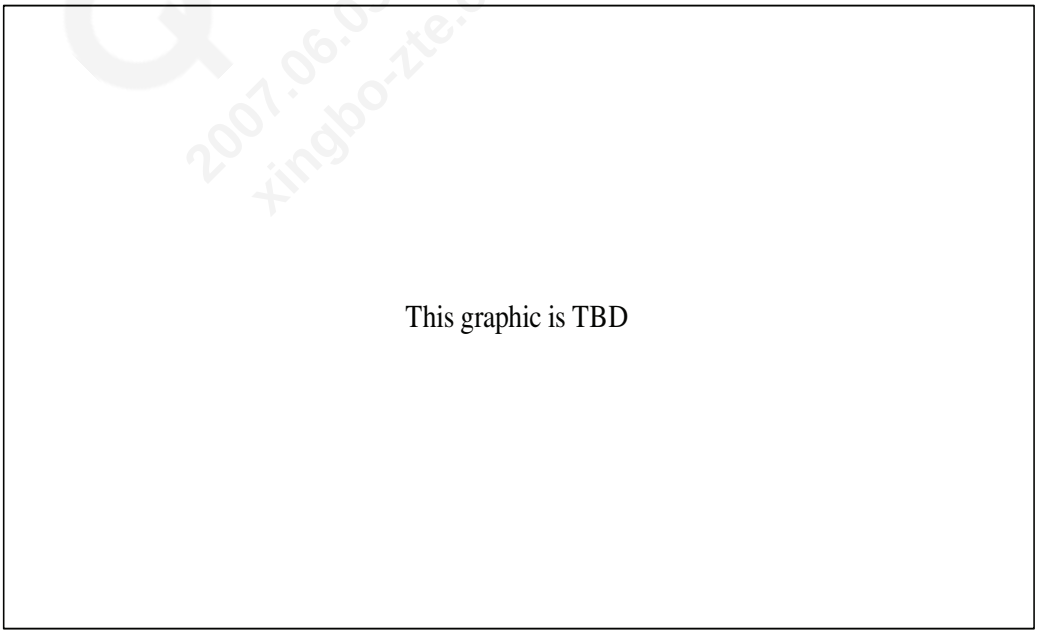

Figure 5-3 Recommended 137 CSP stencil pattern - circular apertures (TBD)

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5.2 Solder reflow

For successful, consistent results during CSP installation, it is important to fully characterize and optimize the SMT process prior to PCB production because circuit assembly can vary depending on application. Characterization should include the land pattern, stencil design, and reflow profile, and must account for the equipment and materials used in manufacturing. This also yields superior board reliability.

The following characterization guidelines are recommended:

- Optimize the solder stencil print for good release – this affects the reflowed solder fillet and is essential to print uniformity.
- Optimize the solder stencil design to minimize voiding.
- Daisy chain packages are suitable for SMT characterization.
- Review the land pattern and stencil pattern design recommendations (Section 5.1) that provide guidelines for characterization.
- *It is important that each handset builder follows their solder paste vendor recommendations for screen printing process parameters and reflow profile conditions.*
- Typical reflow profile conditions for SnPb and lead-free systems are given in Table 5-1.

Table 5-1 Typical reflow profile conditions

Profile stage	Description	SnPb (standard) condition limits	Lead-free (high temp) condition limits
Preheat	Initial ramp	3 °C/sec max	3 °C/sec max
Soak	Dry out and flux activation	135 to 165 °C 60 to 120 sec	135 to 175 °C 60 to 120 sec
Reflow	Time above solder paste melting point	30 to 90 sec	40 to 90 sec
	Peak temperature	230 °C	245 °C
Cool down	Ramp to ambient	6 °C/sec max	6 °C/sec max

In addition, QUALCOMM recommends handset manufacturers perform the following physical tests prior to production:

- Bend to failure
- Bend cycle
- Tensile pull
- Drop shock
- Temperature cycling

5.3 SMT process verification

QUALCOMM recommends verification of the SMT process prior to high-volume PCB fabrication, including:

- Electrical continuity
- X-ray inspection of the package installation for proper alignment, solder voids, solder balls, and solder bridging
- Visual inspection
- Cross-section inspection of solder joints to confirm registration, fillet shape, and print volume (insufficient, acceptable, or excessive)

5.4 Storage conditions, unpacking, and handling

Some high-level instructions for storing, unpacking, and handling PM7540 devices are provided in the following subsections.

5.4.1 Storage conditions

The PM7540 devices, as delivered in tape and reel carriers, must be stored in sealed, moisture barrier, anti-static bags. Shelf life in a proper sealed bag is 12 months; this specification requires an ambient temperature less than 40 °C and relative humidity less than 90 percent.

5.4.2 Out-of-bag duration

After unpacking, the 137 CSP package must be soldered onto the PCB within the time listed on the moisture bag label (see Section 6.3.2 for details). The factory must provide an ambient temperature less than 30 °C and relative humidity less than 60 percent.

5.4.3 Baking

It **is not** necessary to bake the PM7540 devices if the conditions specified in Section 5.4.1 and Section 5.4.2 **have not been** exceeded.

It **is** necessary to bake the PM7540 devices if any condition specified in Section 5.4.1 or Section 5.4.2 **have been** exceeded. The baking conditions are specified on the MSL label attached to each bag (see Section 6.3.2 for details).

CAUTION Components cannot be baked in tape and reel carriers typically supplied by QUALCOMM at the temperature stated on the MSL label.

5.4.4 Electrostatic discharge

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result.

ESD countermeasures and handling methods must be developed and used to control the factory environment at each manufacturing site.

QCT products must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, *Protection of Electrical and Electronic Parts, Assemblies, and Equipment*.

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6 Packing Methods and Materials

Details about the tape and reel carrier, how they should be packed for shipment, and the materials used for packing are discussed in this chapter.

6.1 Tape and reel information

The industry standard EIA-481 dictates basic carrier tape dimensions, but the individual pocket design can vary from vendor to vendor. The pocket protects the part's body and terminals from damaging stresses during shipping and loading onto SMT manufacturing equipment.

The single-feed tape carrier for the PM7540 device is illustrated in Figure 6-1; this figure also shows the proper part orientation. The tape width is TBD mm and the pocket pitch is TBD mm. The reels are TBD mm (TBD inch) diameter with TBD mm (TBD inch) hubs. Each reel contains TBD devices.

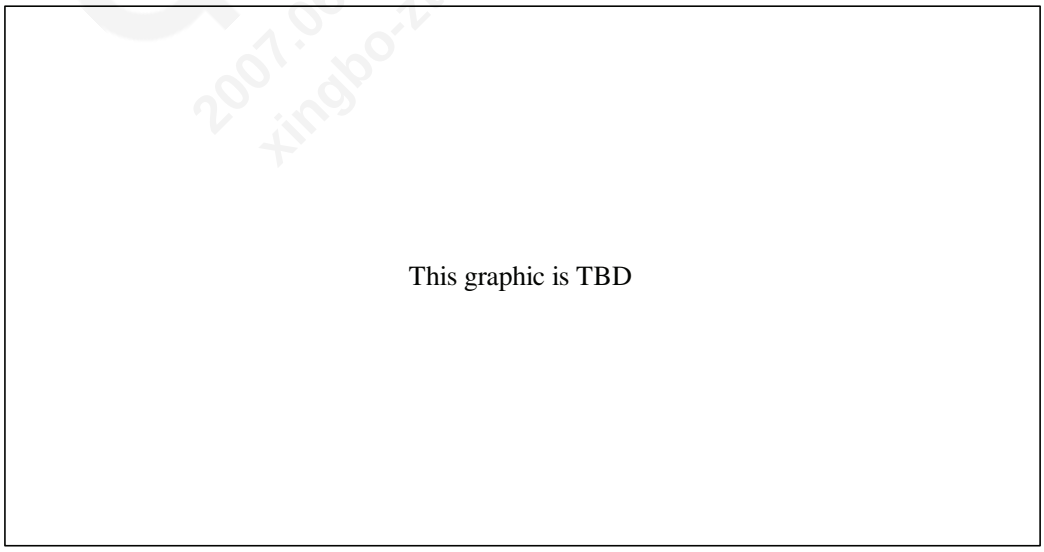


Figure 6-1 Carrier tape drawing with part orientation (TBD)

Information for one potential supplier is given below:

- Supplier: TBD
- Hub part number (2 pieces): TBD
- Carrier tape part number: TBD
- Cover tape part number: TBD

6.2 Packing for shipment

Tape and reel carriers used for shipping PM7540 devices conform to the industry standard EIA-481 and are packed as indicated in the following figures. A moisture-barrier bag (MBB), desiccant, and a humidity indicator card are required for each tape and reel carrier. Details about these packing materials are presented in Section 6.3.

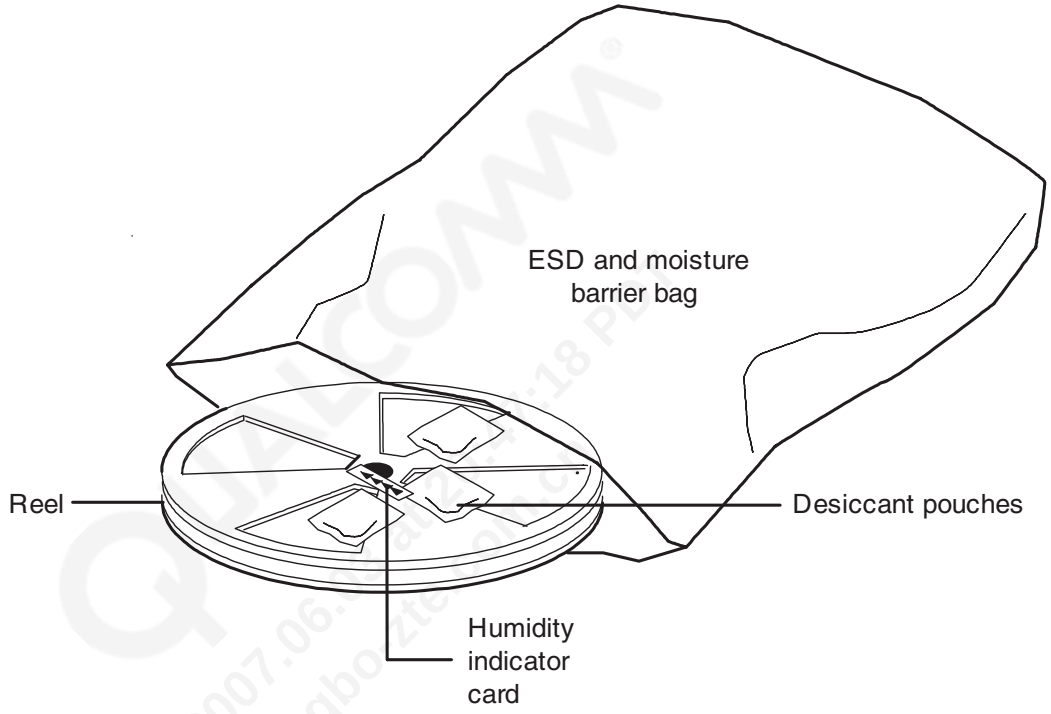


Figure 6-2 Bag packing for tape and reel

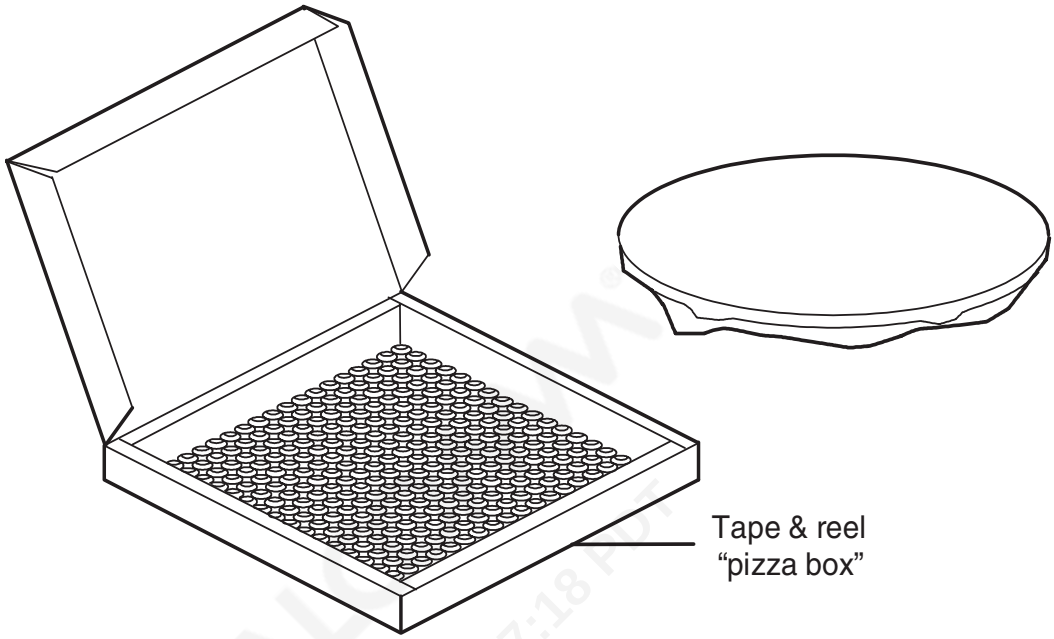


Figure 6-3 Box packing for tape and reel

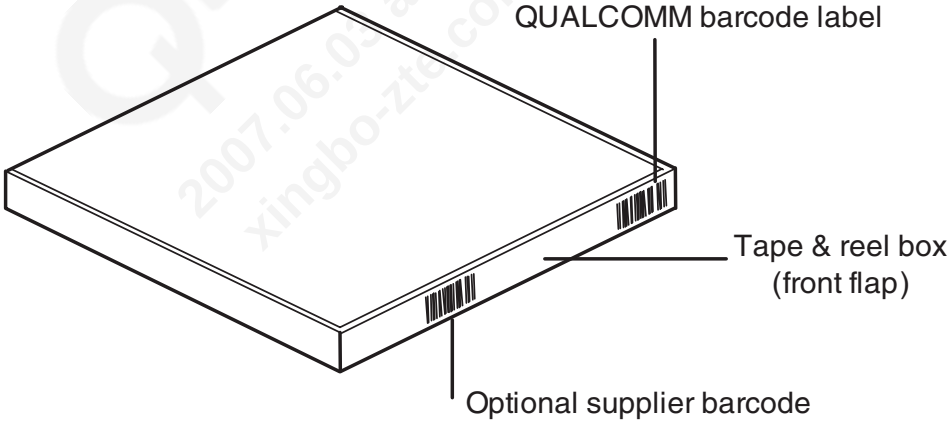


Figure 6-4 Tape and reel box

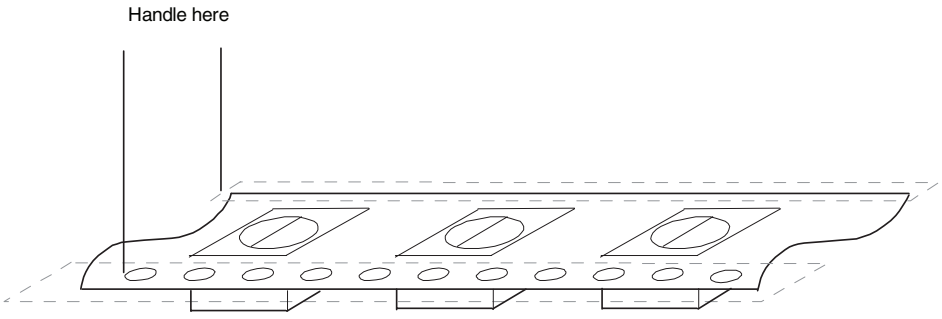


Figure 6-5 Tape handling

6.3 Packing materials

Moisture sensitive SMT components packed on tape and reel carriers are shipped in desiccant packing. Each shipment contains devices that have been baked dry and are enclosed in sealed MBBs with desiccant pouches and humidity indicator cards. The PM7540 devices are considered moisture sensitive products whose shipping technique must include the following added features.

6.3.1 Shipping box barcode label

The barcode label on the shipping box provides the necessary information for incoming inspection or inventory control (see Figure 6-6 for an example). The minimum information includes:

- QUALCOMM item ID number from the SCD
- Lot code or trace code
- Date code
- Description of QUALCOMM product (PM7540)
- Moisture level sensitivity
- Package seal date
- Peak body temperature during SMT soldering
- Countries of die fabrication and device assembly
- Intermediate container quantity

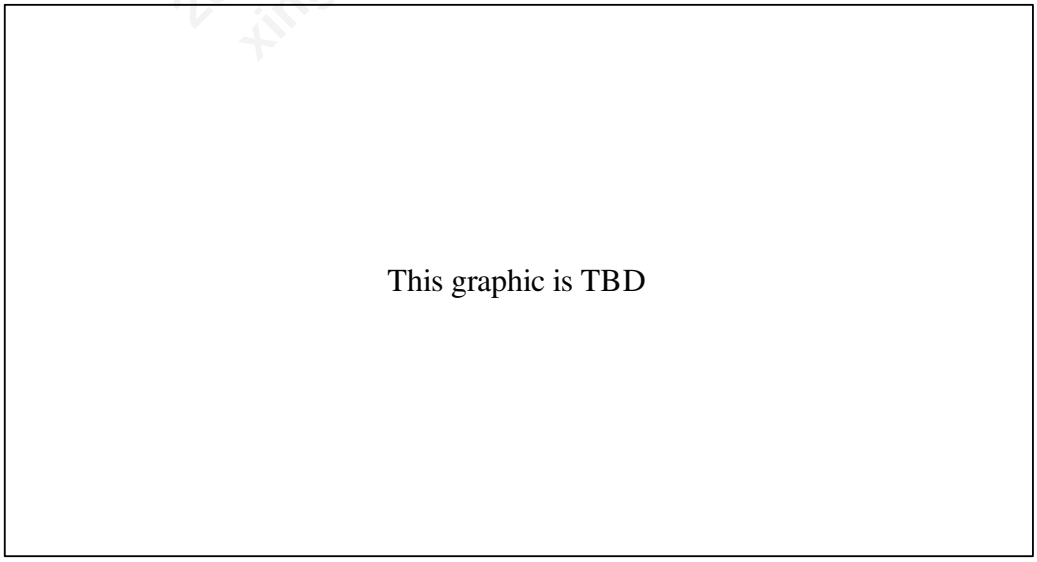


Figure 6-6 Barcode label example (TBD)

6.3.2 Moisture barrier bag

Inside the shipping box is an MBB containing PM7540 devices. The bag is strong, ESD-safe, and allows **minimal** moisture transmission. It is sealed at the factory and should be handled carefully to avoid puncturing or tearing. A caution label (Figure 6-7) on the bag outlines precautions that must be taken with desiccant packed units. This label indicates the MBB seal date (MM/DD/YY), the IPC/JEDEC J-STD-020 moisture sensitivity level, and the maximum shelf life. The remaining shelf life is determined from the seal date and current date. All components are guaranteed to have 12 months of shelf life starting from the seal date on this label.

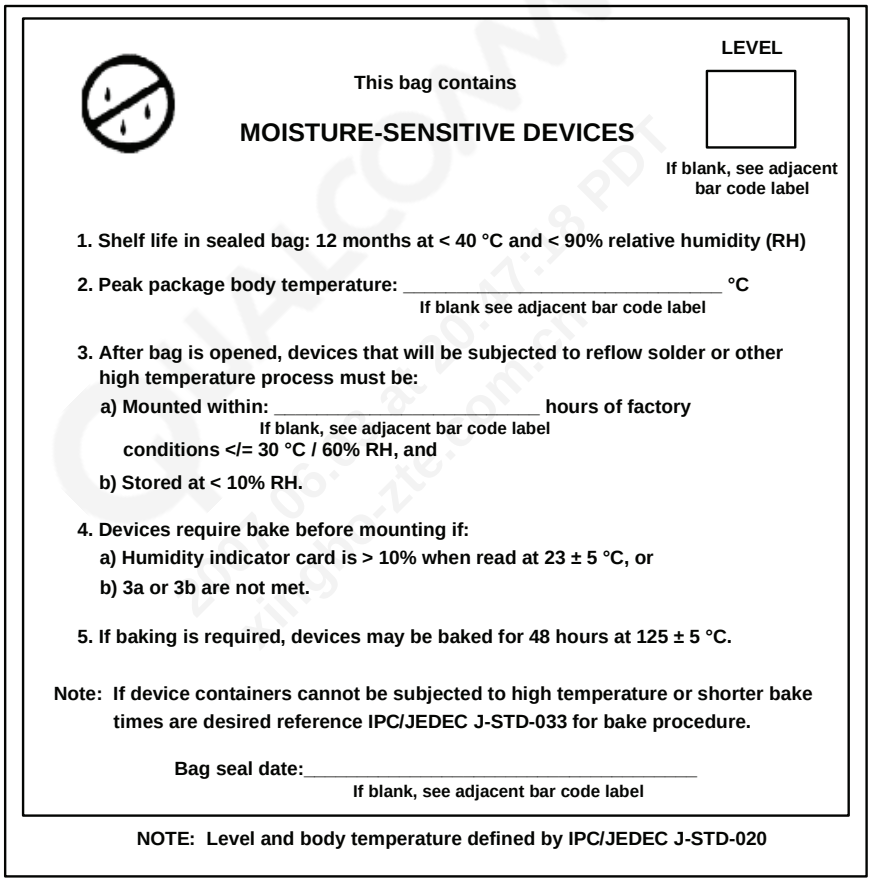


Figure 6-7 Caution label example

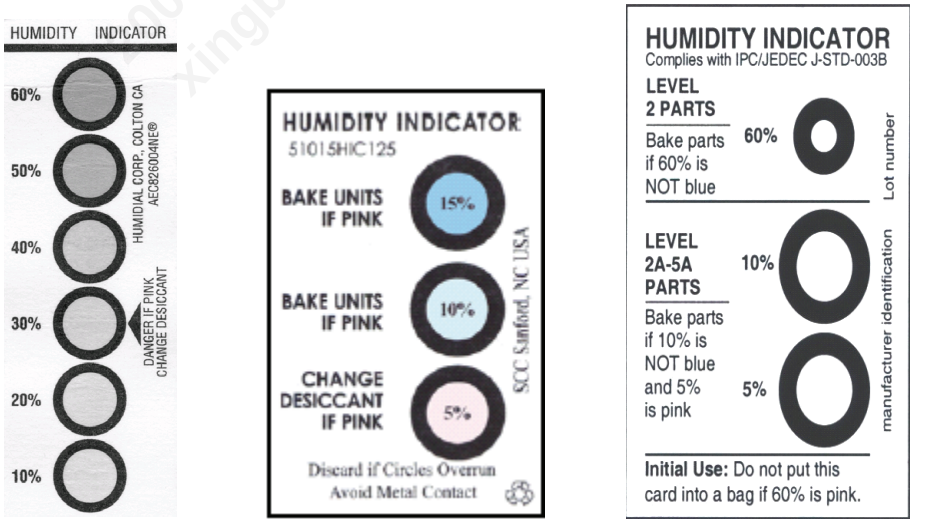
The MBB protects the enclosed devices from moisture exposure and should not be opened until the devices are ready to be board-mounted. The MBB is required for PM7540 devices.

6.3.3 Humidity indicator cards

Along with the desiccant pouches, the MBB contains a humidity indicator card (HIC). This card is a moisture indicator and is included to show the approximate relative humidity level within the bag. Representations of example HICs are shown in Figure 6-8. If the components have been exposed to moisture beyond the recommended limits for use in an SMT process, the units must be rebaked.

A three-button 5-10-60 HIC (right side of Figure 6-8) replaces the three-button 5-10-15 HIC (middle of Figure 6-8) in some packaging to comply with new J-STD-033B specifications. The new 60% RH button on the HIC allows for identification of RH limits on MSL 2 product packaging. The cards should be read as follows:

- Six button HIC (left side of Figure 6-8):
  - For all levels of parts: If the 20% button is *pink* and the 30% button is *not blue* the components have exceeded the limit for moisture exposure and must be rebaked
- Three button 5-10-15 HIC (middle of Figure 6-8):
  - For all levels of parts: If the 5% button is *pink* and the 10% button is *not blue* the components have exceeded the limit for moisture exposure and must be rebaked
- Three button 5-10-60 HIC (right side of Figure 6-8):
  - Level 2 parts: If the 60% button is *not blue* the components have exceeded the limit for moisture exposure and must be rebaked
  - Level 2A - 5A parts: If the 10% button is *not blue* and the 5% button is *pink* the components have exceeded the limit for moisture exposure and must be rebaked



six-button HIC **three-button 5-10-15 HIC** **three-button 5-10-60 HIC**

Figure 6-8 Example humidity indicator cards

The HIC is reversible and can be reused. The HIC is required for all moisture-sensitive devices.

7 Part Reliability

7.1 Reliability qualification summary

Table 7-1 Stress tests

Test condition	Sample size	Results
High temperature operating life (HTOL) JESD22-A108-A At 140 °C, 24 hours Early life failure rate (ELFR) Average failure rate (AFR)	TBD	TBD
Highly accelerated stress test (HAST)	TBD	TBD
High temperature storage life JESD22-A103-B	TBD	TBD
ESD - Human body model JESD22-A114-B	TBD	TBD
ESD - Charge device model JESD22-C101-C	TBD	TBD
Latch-up current test JESD 78	TBD	TBD
Latch-up over-voltage test JESD 78	TBD	TBD
Temp cycle JESD22-A104-B, 1000 cycles Condition B, soak mode 2	TBD	TBD
Moisture sensitivity J-STD-020B, reflow at 255 °C	TBD	TBD

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Table 7-2 Characteristics tests

Test condition	Sample size	Results
Physical dimensions JESD22-B100	TBD	TBD
Internal visual 80-V0691-1	TBD	TBD
X-ray inspection	TBD	TBD
Solderability JESD22-B102, 40 bumps Precondition to level C, test to level A	TBD	TBD
Wire ball sheer JESD22-B116	TBD	TBD
Die shear Mil-Std-883, method 2019	TBD	TBD
Flammability UL-STD-94	TBD	TBD
External visual JESD22-B101	TBD	TBD

7.2 Qualification sample description

Device characteristics:

Device name: PM7540

Package type: 137 CSP

Package body size: 7 mm × 7 mm

Lead count: 137

Lead composition: Sn/Ag/Cu

Processes: TBD

Fab sites: TBD

Assembly sites: TBD

Bump pitch: 0.5 mm