MC74HC4075

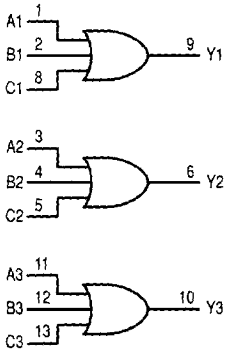
Triple 3-Input OR Gate

High–Performance Silicon–Gate CMOS

The MC74HC4075 is identical in pinout to the MC14075B. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 42 FETs or 10.5 Equivalent Gates

LOGIC DIAGRAM



Y = A + B + C

PIN 14 = V_{CC}
PIN 7 = GND

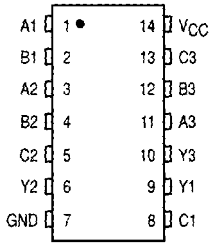
N SUFFIX
PLASTIC PACKAGE
CASE 646–06

D SUFFIX
SOIC PACKAGE
CASE 751A–03

ORDERING INFORMATION

MC74HCXXXXN	Plastic
MC74HCXXXXD	SOIC

PIN ASSIGNMENT



FUNCTION TABLE

Inputs			Output
A	**B**	**C**	**Y**
L	L	L	L
H	X	X	H
X	H	X	H
X	X	H	H

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 1.5 to V_{CC} + 1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air Plastic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1) V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit – 55 to 25°C	≤ 85°C	≤ 125°C	Unit
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\lvert I_{out} \rvert$ ≤ 20 µA	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\lvert I_{out} \rvert$ ≤ 20 µA	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\lvert I_{out} \rvert$ ≤ 20 µA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in} = V_{IH} or V_{IL} $\lvert I_{out} \rvert$ ≤ 4.0 mA $\lvert I_{out} \rvert$ ≤ 5.2 mA	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\lvert I_{out} \rvert$ ≤ 20 µA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} $\lvert I_{out} \rvert$ ≤ 4.0 mA $\lvert I_{out} \rvert$ ≤ 5.2 mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND	6.0	± 0.1	± 1.0	± 1.0	µA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND I_{out} = 0 µA	6.0	2	20	40	µA

NOTE: Information on typical parametric values can be found in Chapter 2.

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A, B, or C to Output Y (*Figures 1 and 2*)	2.0 4.5 6.0	115 23 20	145 29 25	175 35 30	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 2.
2. Information on typical parametric values can be found in Chapter 2.

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Gate)*	26	pF

* *Used to determine the no–load dynamic power consumption:* $P_D = C_{PD} V_{CC}{}^2 f + I_{CC} V_{CC}$. *For load considerations, see Chapter 2.*

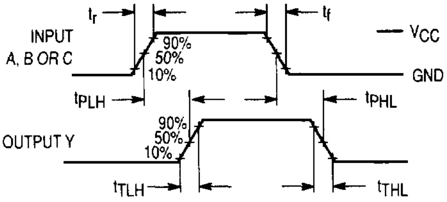
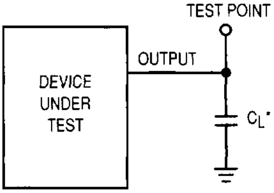


Figure 1. Switching Waveforms



* *Includes all probe and jig capacitance*

Figure 2. Test Circuit

EXPANDED LOGIC DIAGRAM
(1/3 of the Device)