

Applications

- Final Stage Amplifiers for Repeaters
- Mobile Infrastructure

Product Features

- 400 – 2300 MHz
- 18 dB Gain at 900 MHz
- +31.5 dBm P1dB
- +46 dBm Output IP3
- +5 V Single Positive Supply
- Lead-free / green / RoHS-compliant SOIC-8 Package

General Description

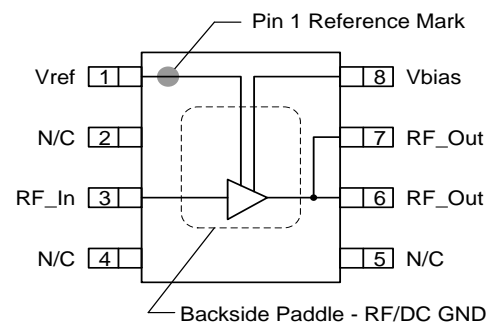
The AH215 is a high dynamic range driver amplifier in a low-cost surface mount package. The InGaP / GaAs HBT is able to achieve superior performance for various narrowband-tuned application circuits with up to +46 dBm OIP3 and +31.5 dBm of compressed 1-dB power. The part is housed in a lead-free/green/RoHS-compliant SOIC-8 package. All devices are 100% RF and DC tested.

The product is targeted for use as driver amplifier for various current and next generation wireless technologies such as CDMA, W-CDMA, and LTE where high linearity and high power is required. The internal active bias allows the AH215 to maintain high linearity over temperature and operate directly off a +5 V supply.



8-Pin SOIC-8 SMT Package

Functional Block Diagram



Pin Configuration

Pin No.	Label
1	V _{REF}
2, 4, 5	N/C
3	RF_In
6, 7	RF_Out / V _{CC}
8	V _{BIAS}
Backside Paddle	RF/DC GND

Ordering Information

Part No.	Description
AH215-S8G	1 Watt, High IP3 InGaP HBT Amp
AH215-S8PCB900	900 MHz Evaluation Board
AH215-S8PCB1960	1960 MHz Evaluation Board
AH215-S8PCB2140	2140 MHz Evaluation Board

Standard T/R size = 1000 pieces on a 7" reel

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-65 to 150 °C
RF Input Power (Continuous)	+26 dBm
Device Voltage	+8 V
Device Current	900 mA
Device Power	+5 W

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V _{CC}	+4.5	+5	+5.25	V
I _{CQ}		450		mA
T _{CASE}	-40		+85	°C
T _j for >10 ⁶ hours MTTF			+200	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

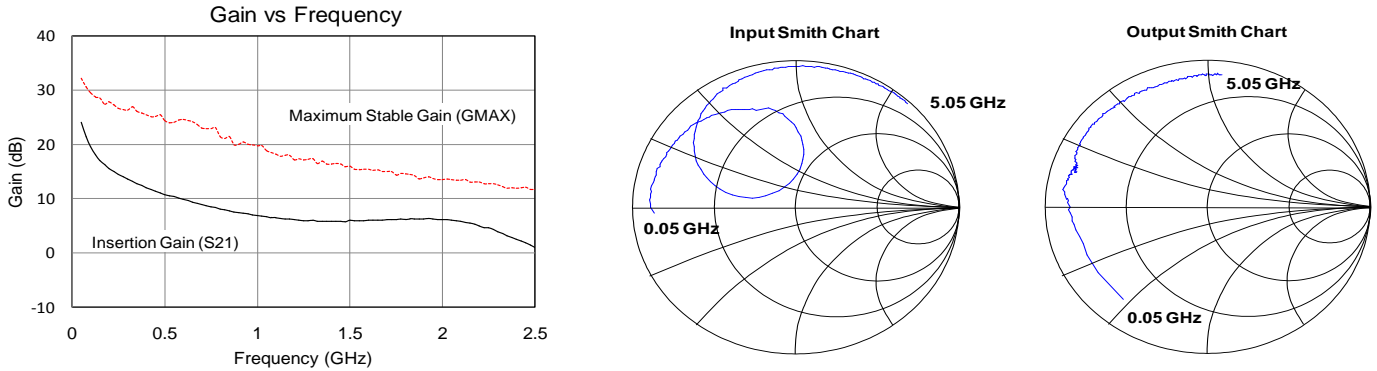
Test conditions unless otherwise noted: V_{CC}=+5 V, I_{CQ}= 300 mA, I_{REF} = 15 mA, Temp= +25 °C, tuned application circuit

Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		400		2300	MHz
Test Frequency			2140		MHz
Gain		10	11		dB
Input Return Loss			18		dB
Output Return Loss			8		dB
Output P1dB		+29	+31.5		dBm
Output IP3	P _{out} = +15 dBm / tone, Δf=1 MHz	+43.8	+45		dBm
WCDMA Channel Power	ACLR= -45 dBc at f=2140 MHz		6.3		dBm
Operating Current Range, I _{CC} ⁽¹⁾			+23		dB
Noise Figure		400	450	500	mA
Thermal Resistance (Junction to case) θ _{jc}				33	°C/W

Notes:

- This corresponds to the quiescent current or operating current under small-signal conditions into pins 6, 7, and 8. It is expected that the current can increase by an additional 90 mA at P1dB. Pin 1 is used as a reference voltage for the internal biasing circuitry. It is expected that Pin 1 will pull 10.8 mA of current when used with a series bias resistor of R1= 51 Ω. (i.e. total device current typically will be 461 mA.)

Device Characterization Data



Notes:

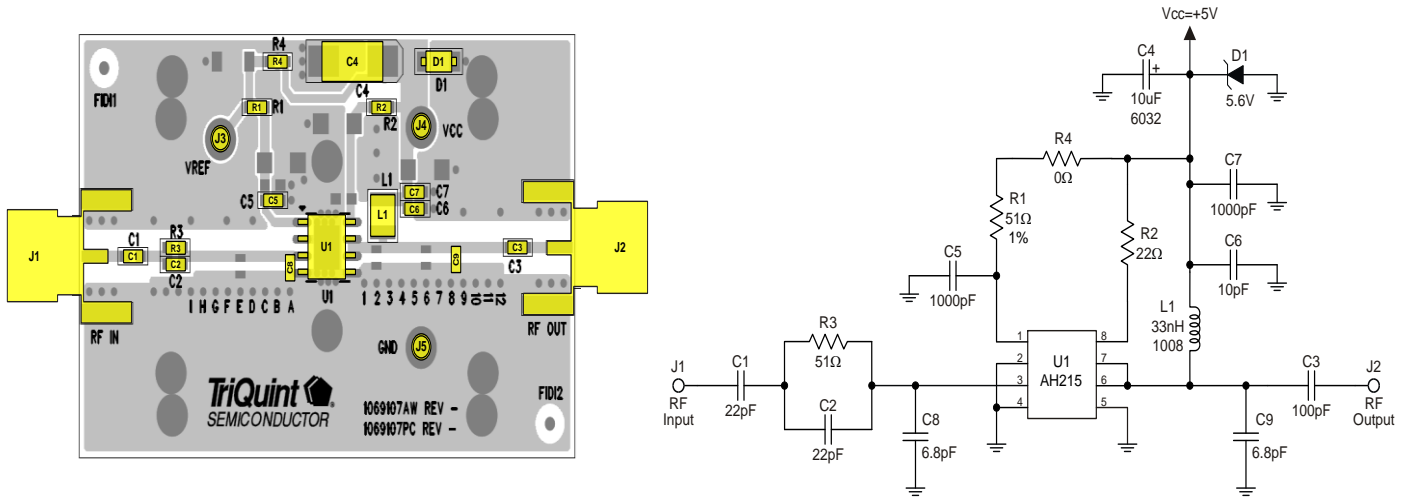
1. Insertion Gain (S21) is for the unmatched device in a 50 ohm system. In a circuit tuned for a particular frequency band, higher gain can be achieved up to the Maximum Stable Gain (GMAX).

S-Parameters

Test Conditions: $V_{CC} = +5\text{ V}$, $I_{CQ} = 450\text{ mA}$, $T = +25\text{ }^\circ\text{C}$, unmatched 50 ohm system, calibrated to device leads

Freq (GHz)	S11 (dB)	S11 (ang)	S21 (dB)	S21 (ang)	S12 (dB)	S12 (ang)	S22 (dB)	S22 (ang)
50	-1.23	-177.95	24.07	122.55	-40.25	17.32	-1.26	-130.4
100	-1.01	178.17	19.55	116.55	-39.49	10.63	-1.33	-155.43
200	-1.01	172.63	15.55	112.97	-40.13	15.98	-1.17	-169.92
400	-1.03	163.72	12.03	98.68	-38.83	10.31	-0.93	179.61
600	-1.21	155.20	9.86	85.80	-39.30	-4.249	-0.66	173.43
800	-1.34	146.17	8.11	73.18	-37.70	-2.398	-0.83	168.67
1000	-1.52	136.69	6.92	61.43	-37.73	-16.27	-0.95	166.34
1200	-2.00	126.65	6.13	49.60	-37.14	-14.34	-1.05	165.13
1400	-2.65	115.04	5.80	37.55	-36.23	-28.50	-1.04	164.55
1600	-3.86	97.52	6.01	21.48	-36.45	-46.08	-1.11	166.24
1800	-6.72	86.05	6.17	1.700	-34.63	-68.99	-1.10	164.44
2000	-14.09	94.99	6.15	-23.83	-35.91	-100.68	-1.00	162.35
2200	-9.98	166.89	4.98	-52.92	-36.75	-147.66	-0.77	158.42
2400	-4.27	157.68	2.52	-80.08	-39.10	171.86	-0.79	154.12
2600	-2.13	142.95	-0.42	-100.8	-37.80	123.26	-0.81	149.03
2800	-1.24	130.88	-3.40	-116.44	-38.58	89.55	-0.84	144.09
3000	-0.82	120.68	-6.09	-128.99	-39.37	67.22	-0.92	138.4

Reference Design: 869 – 960 MHz (AH215-S8PCB900)



Notes:

1. The primary RF microstrip line is 50 Ω.
1. All passive components are 0603 size unless otherwise specified.
2. Observe component value tolerances when specified
3. Zero ohm jumpers may be replaced with metal trace in user applications.
4. Place component C8 at marker 'A' on the PC Board or center of component placed at 0.7 deg at 0.9 GHz away from U1 pin '3'
5. Place component C9 between marker '8' and '9' on the PC Board or center of component placed at 18 deg at 0.9 GHz away from U1 pins '6' and '7'

Bill Of Materials: 869 – 960 MHz (AH215-S8PCB900)

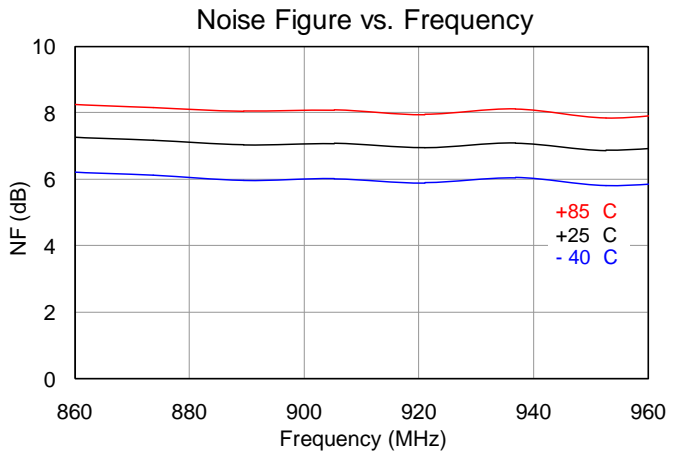
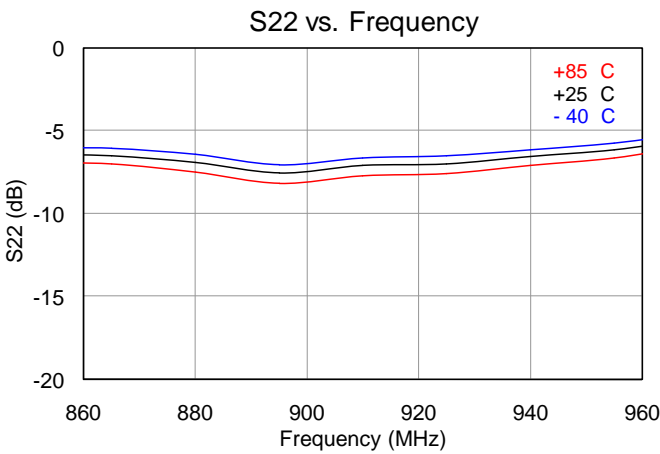
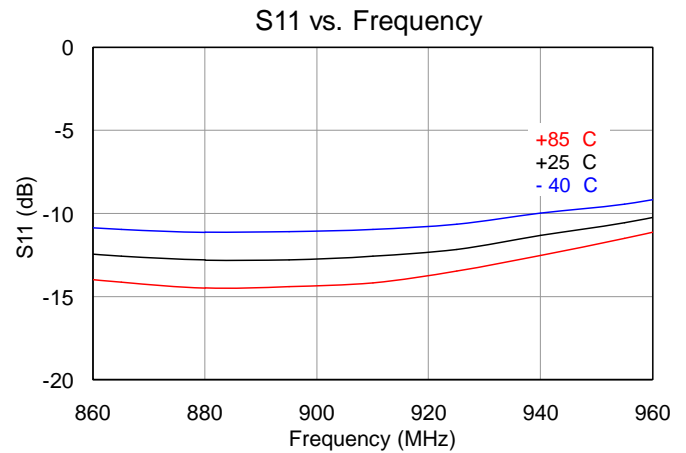
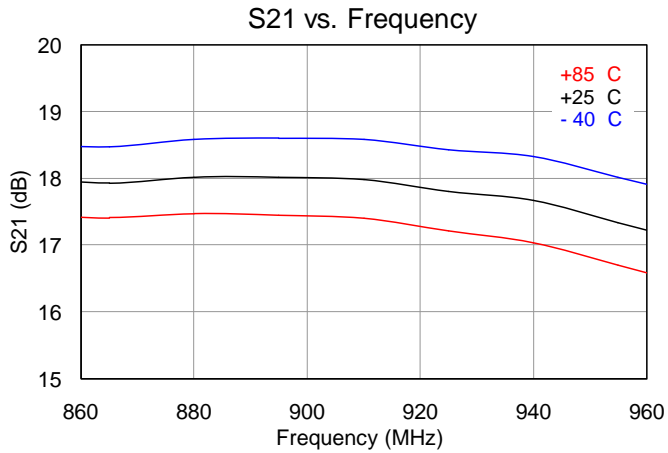
Reference Design	Value	Description	Manufacturer	Part Number
U1		1 Watt High Linearity InGaP Amp	TriQuint	AH215-S8G
C1, C2	22 pF	Cap, Chip, 0603, +50 V, 5%, NPO/COG	various	
C3	100 pF	Cap, Chip, 0603, +50 V, 5%, NPO/COG	various	
C4	10 µF	Cap, Chip, 6032, +25 V, 20%, TANT	various	
C5, C7	1000 pF	Cap, Chip, 0603, +50 V, 5%, X7R	various	
C6	10 pF	Cap, Chip, 0603, +50 V, 5%, NPO/COG	various	
C8, C9	6.8 pF	Cap, Chip, 0603, +50 V, ±0.1 pF, Accu-P	AVX	06035J6R8BBSTR
L1	33 nH	Ind, Coil Wound, 1008, 5%, Ceramic Core	Coilcraft	1008HQ-33NXJLC
R1	51 Ω	Res, Chip, 0603, 1%, 1/16 W	various	
R2	22 Ω	Res, Chip, 0603, 5%, 1/16 W	various	
R3	51 Ω	Res, Chip, 0603, 5%, 1/16 W	various	
R4	0 Ω	Res, Chip, 0603, 5%, 1/16 W	various	
D1		+5.6 V Zener Diode	various	

Typical Performance: 869 – 960 MHz (AH215-S8PCB900)

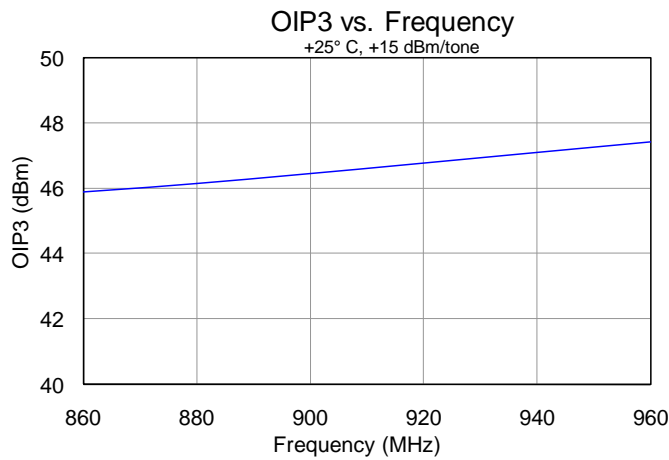
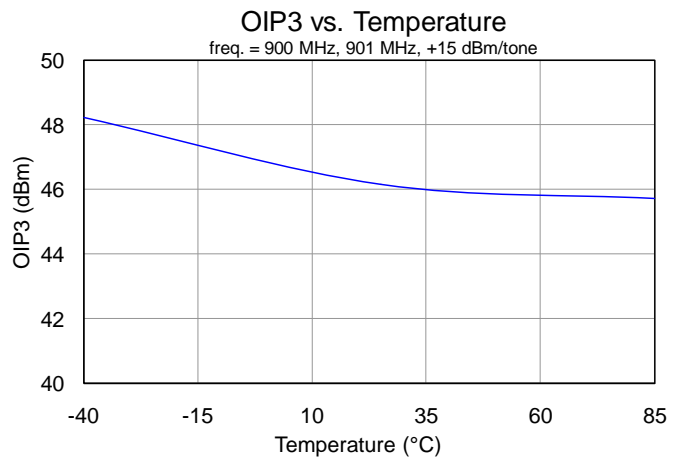
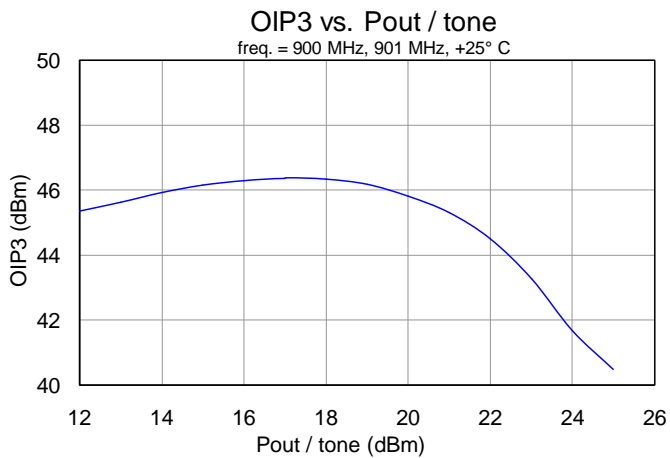
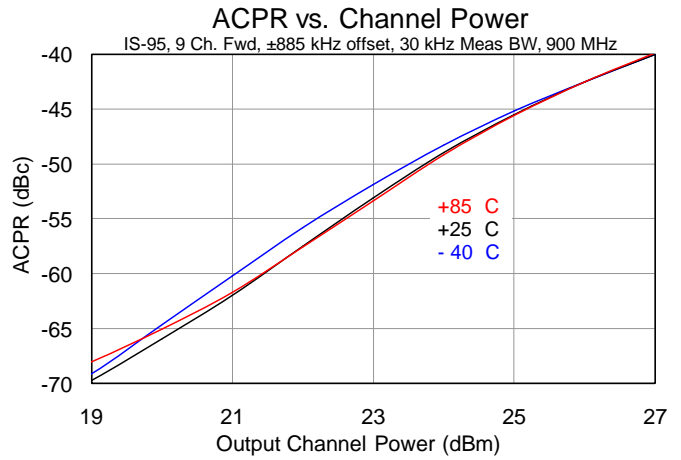
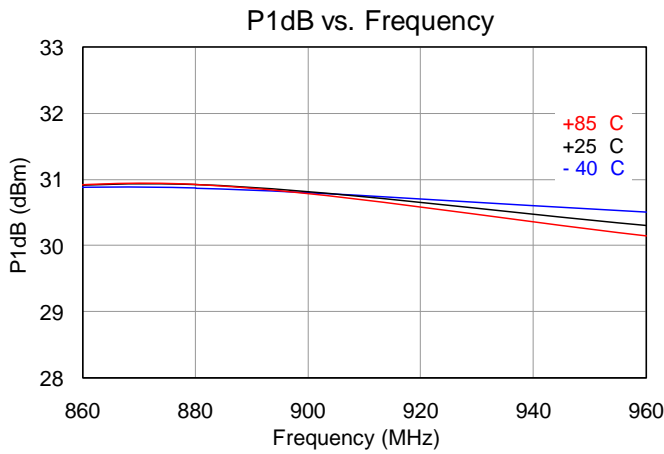
Test conditions unless otherwise noted: $V_{CC} = +5\text{ V}$, $I_{CQ} = 450\text{ mA}$

Parameter	Typical Value			Units
Frequency	869	900	960	MHz
Gain	18	18	17.5	dB
Input Return Loss	13	13	10	dB
Output Return Loss	7	7	6	dB
Output P1dB	+31	+31	+30	dBm
Output IP3 at 22 dBm / tone, $\Delta f = 1\text{ MHz}$	+46	+46	+47	dBm
WCDMA Channel Power ⁽¹⁾ (ACLR= -50 dBc)	+25.5	+25.5	+25.5	dBm
Noise Figure	7.0	7.0	7.0	dB

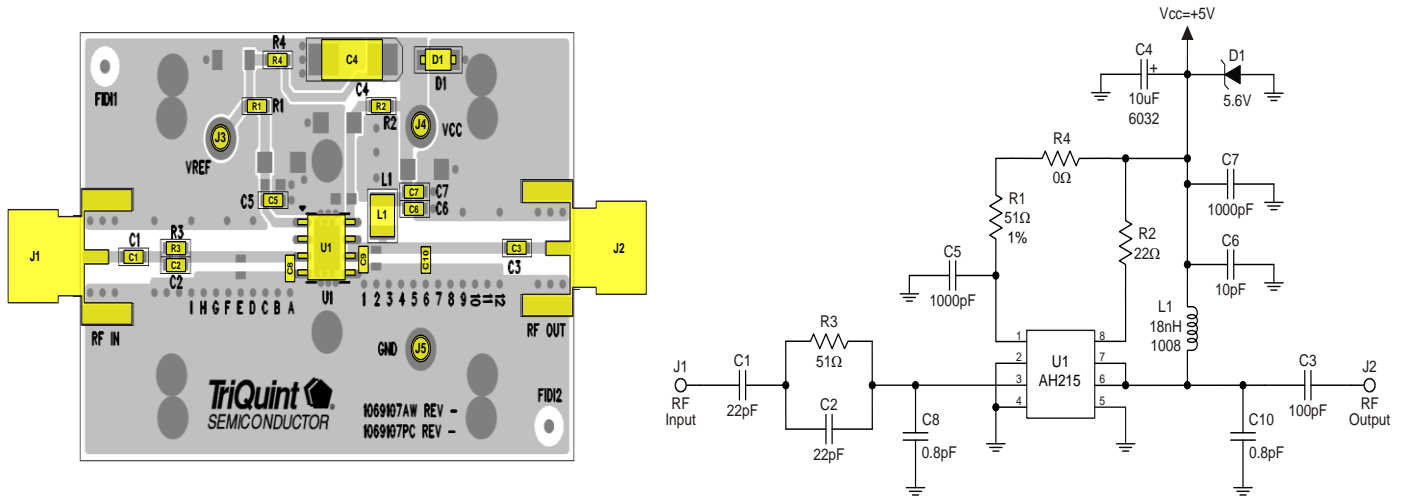
Typical Performance Plots 869 – 960 MHz (AH215-S8PCB900)



Typical Performance Plots 869 – 960 MHz (AH215-S8PCB900)



Application Circuit 1930 – 1990 MHz (AH215-S8PCB1960)



Notes:

1. The primary RF microstrip line is 50 Ω.
2. All passive components are 0603 size unless otherwise specified.
3. Observe component value tolerances when specified.
4. Zero ohm jumpers may be replaced with metal trace in user applications.
5. Place component C8 at marker 'A' on the PC Board or center of component placed at 1.6 deg at 1.9 GHz away from U1 pin '3'.
6. Place component C9 at marker '1' on the PC Board or center of component placed at 1.6 deg at 1.9 GHz away from U1 pins '6'.
7. Place component C10 at marker '6' on the PC Board or center of component placed at 34 deg at 1.9 GHz away from U1 pins '6'.

Bill Of Materials: 1930 – 1990 MHz (AH215-S8PCB1960)

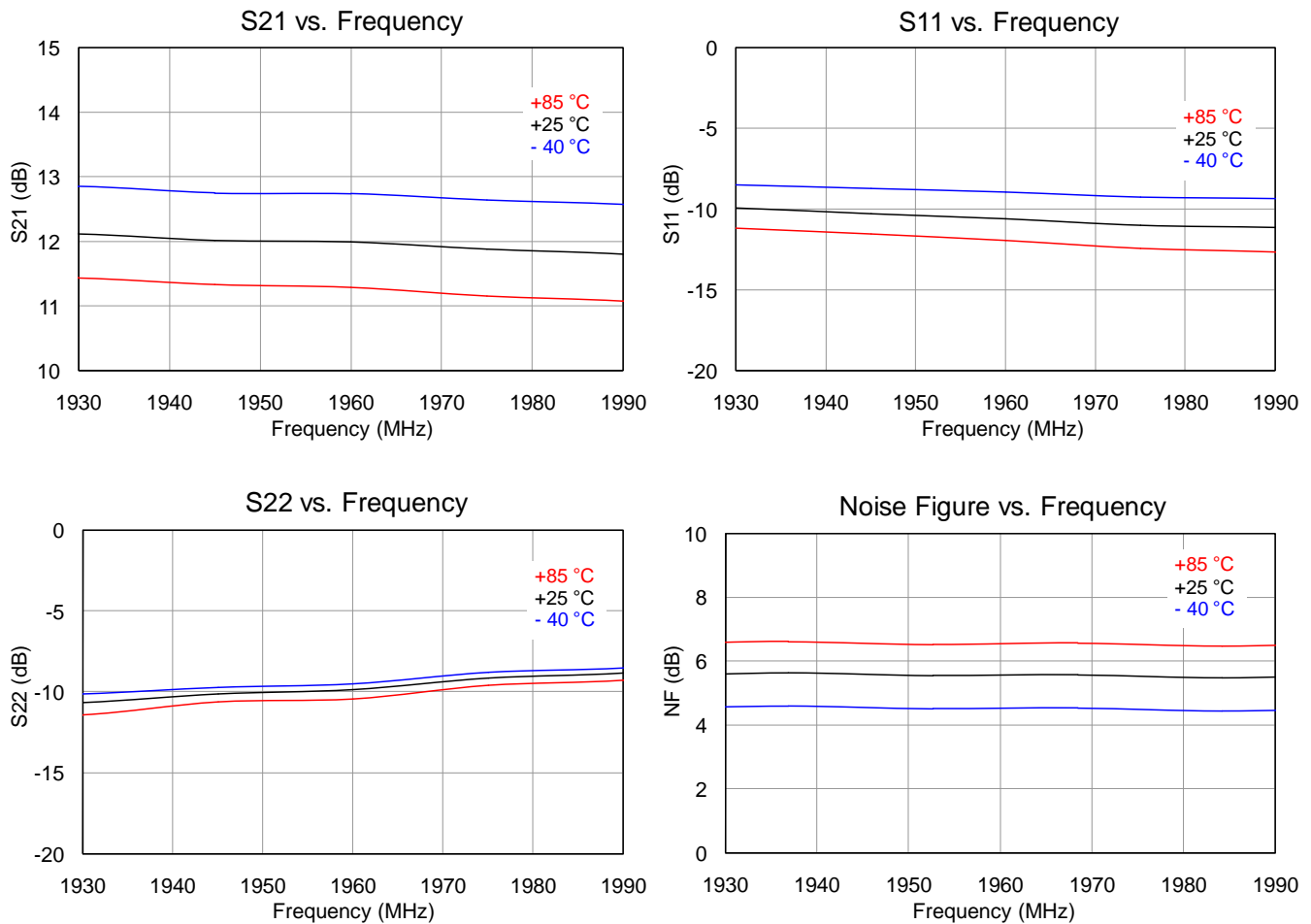
Reference Design	Value	Description	Manufacturer	Part Number
U1		1 Watt High Linearity InGaP Amp	TriQuint	AH215-S8G
C1, C2	22 pF	Cap, Chip, 0603, +50 V, 5%, NPO/COG	various	
C3	100 pF	Cap, Chip, 0603, +50 V, 5%, NPO/COG	various	
C4	10 μF	Cap, Chip, 6032, +25 V, 20%, TANT	various	
C5, C7	1000 pF	Cap, Chip, 0603, +50 V, 5%, X7R	various	
C6	10 pF	Cap, Chip, 0603, +50 V, 5%, NPO/COG	various	
C8, C10	0.8 pF	Cap, Chip, 0603, +50 V, ±0.05 pF, Accu-P	AVX	06035J0R8ABSTR
C9	3.3 pF	Cap, Chip, 0603, +50 V, ±0.05 pF, Accu-P	AVX	06035J3R3ABSTR
L1	18 nH	Ind, Coil Wound, 1008, 5%, Ceramic Core	Coilcraft	1008HQ-18NXJLC
R1	51 Ω	Res, Chip, 0603, 1%, 1/16 W	various	
R2	22 Ω	Res, Chip, 0603, 5%, 1/16 W	various	
R3	51 Ω	Res, Chip, 0603, 5%, 1/16 W	various	
R4	0 Ω	Res, Chip, 0603, 5%, 1/16 W	various	
D1		+5.6 V Zener Diode	various	

Typical Performance 1930 – 1990 MHz (AH215-S8PCB1960)

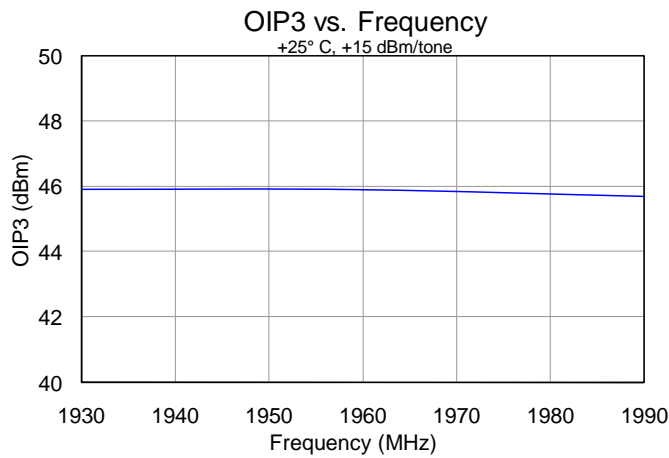
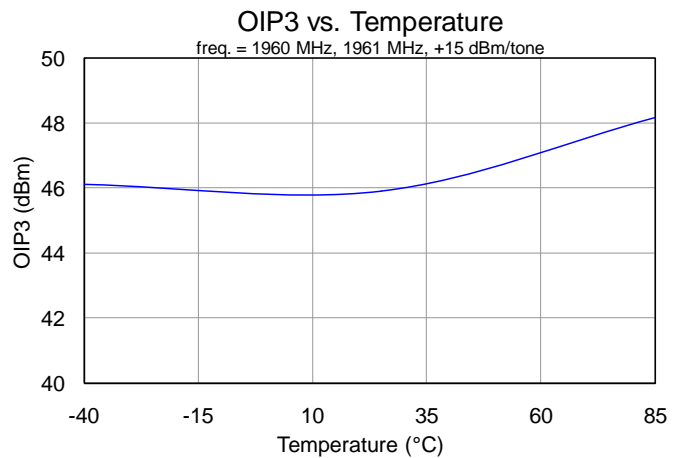
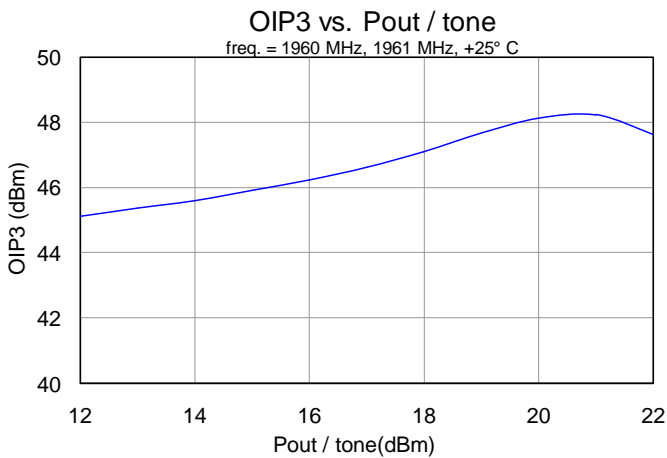
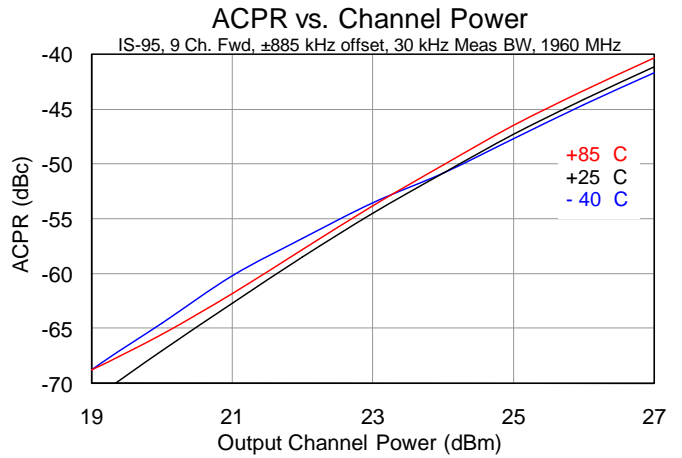
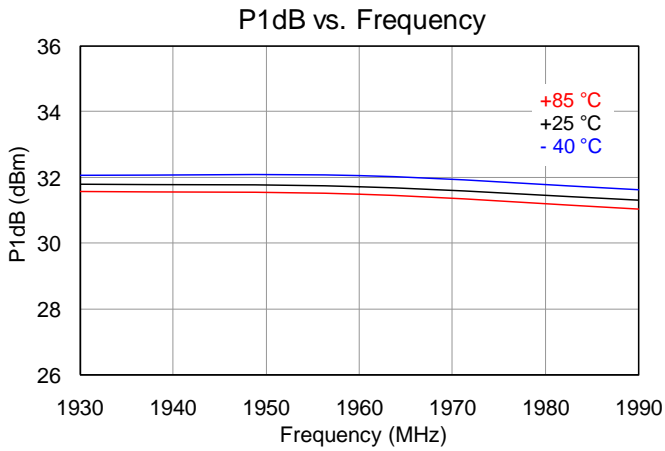
Test conditions unless otherwise noted: $V_{CC} = +5\text{ V}$, $I_{CQ} = 450\text{ mA}$

Parameter	Typical Value			Units
Frequency	1930	1960	1990	MHz
Gain	12.1	12	11.8	dB
Input Return Loss	10	11	11	dB
Output Return Loss	11	10	9	dB
Output P1dB	+32	+32	+31.5	dBm
Output IP3 at +15 dBm / tone, $\Delta f = 1\text{ MHz}$	+46	+46	+46	dBm
WCDMA Channel Power ⁽¹⁾ (ACLR= -45 dBc)	+25.5	+25.5	+25.5	dBm
Noise Figure	5.5	5.5	5.5	dB

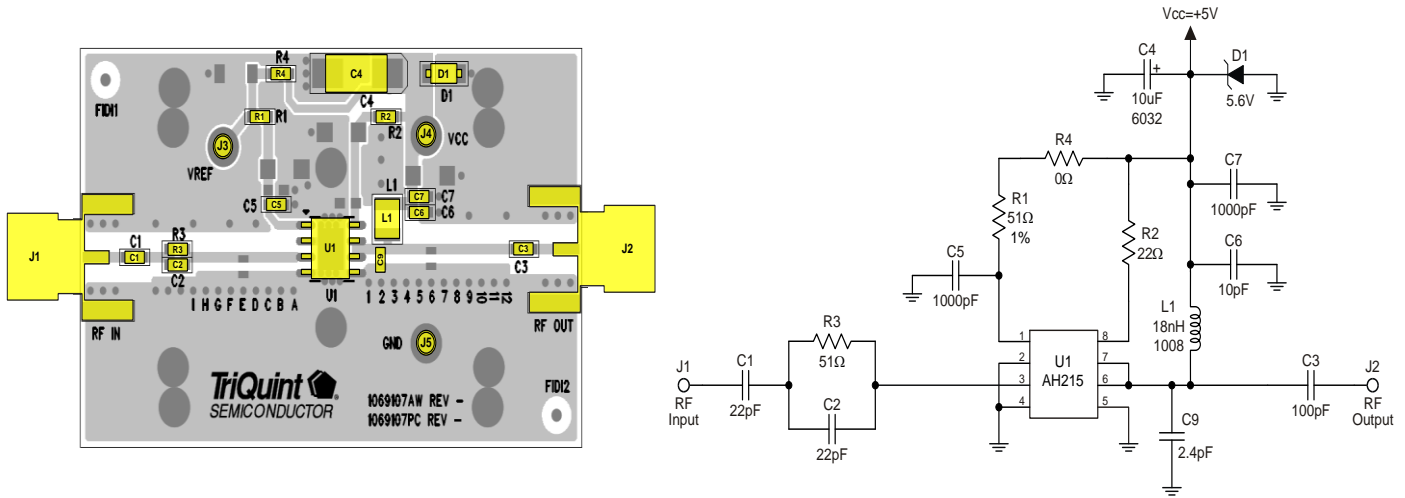
Typical Performance Plots 1930 – 1990 MHz (AH215-S8PCB1960)



Typical Performance Plots 1930 – 1990 MHz (AH215-S8PCB1960)



Reference Design 2110 – 2170 MHz (AH215-S8PCB2140)



Notes:

1. The primary RF microstrip line is 50 Ω.
2. All passive components are 0603 size unless otherwise specified.
3. Observe component value tolerances when specified.
4. Zero ohm jumpers may be replaced with metal trace in user applications.
5. Place component C9 at marker '2' on the PC Board or center of component placed at 7.5 deg at 2.14 GHz away from U1 pins '6' and '7'

Bill Of Materials: 2110 – 2170 MHz (AH215-S8PCB2140)

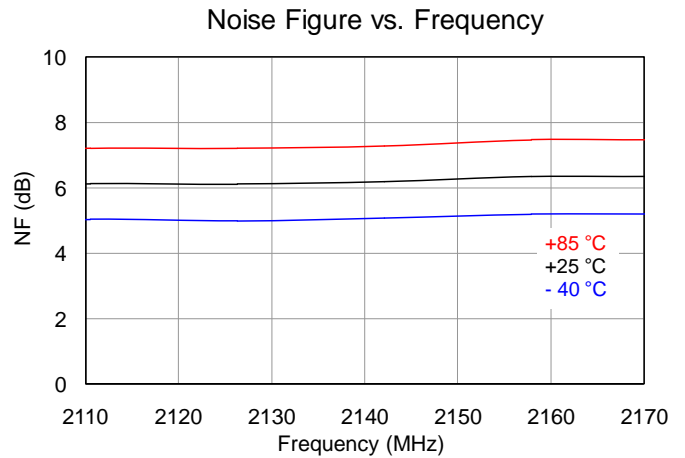
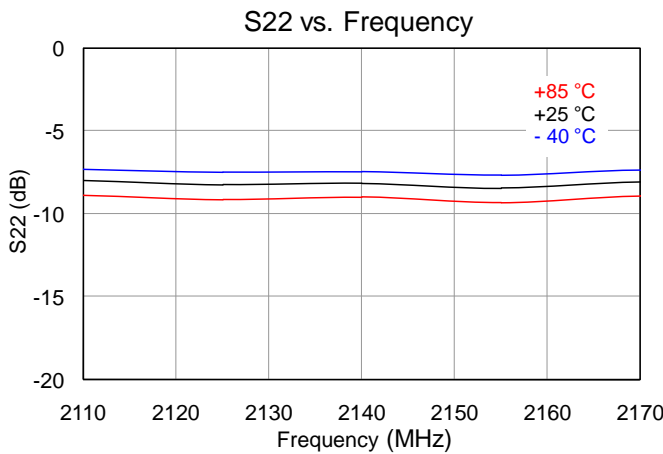
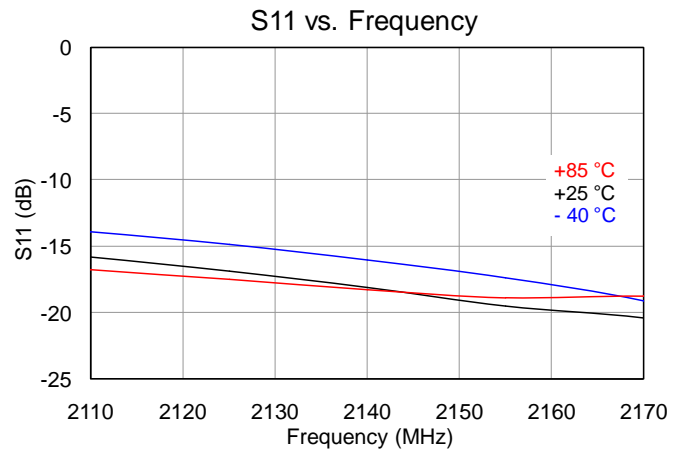
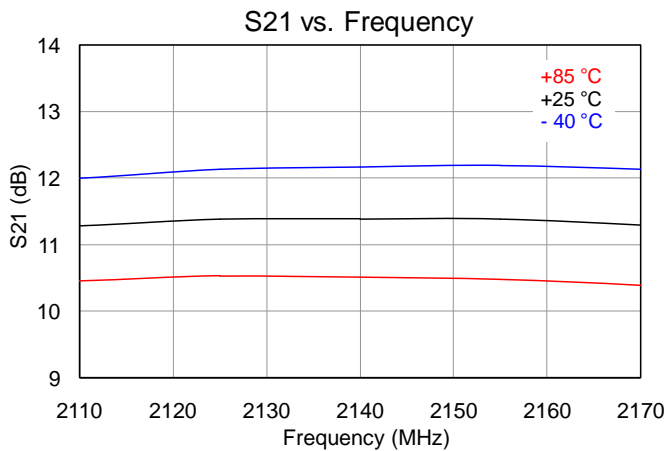
Reference Design	Value	Description	Manufacturer	Part Number
U1		1 Watt High Linearity InGaP Amp	TriQuint	AH215-S8G
C1, C2	22 pF	Cap, Chip, 0603, +50 V, 5%, NPO/COG	various	
C3	100 pF	Cap, Chip, 0603, +50 V, 5%, NPO/COG	various	
C4	10 µF	Cap, Chip, 6032, +25 V, 20%, TANT	various	
C5, C7	1000 pF	Cap, Chip, 0603, +50 V, 5%, X7R	various	
C6	10 pF	Cap, Chip, 0603, +50 V, 5%, NPO/COG	various	
C9	2.4 pF	Cap, Chip, 0603, +50 V, ±0.05 pF, Accu-P	AVX	06035J2R4ABSTR
L1	18 nH	Ind, Coil Wound, 1008, 5%, Ceramic Core	Coilcraft	1008HQ-18NXJLC
R1	51 Ω	Res, Chip, 0603, 1%, 1/16 W	various	
R2	22 Ω	Res, Chip, 0603, 5%, 1/16 W	various	
R3	51 Ω	Res, Chip, 0603, 5%, 1/16 W	various	
R4	0 Ω	Res, Chip, 0603, 5%, 1/16 W	various	
D1		+5.6 V Zener Diode	various	

Typical Performance 2110 – 2170 MHz (AH215-S8PCB2140)

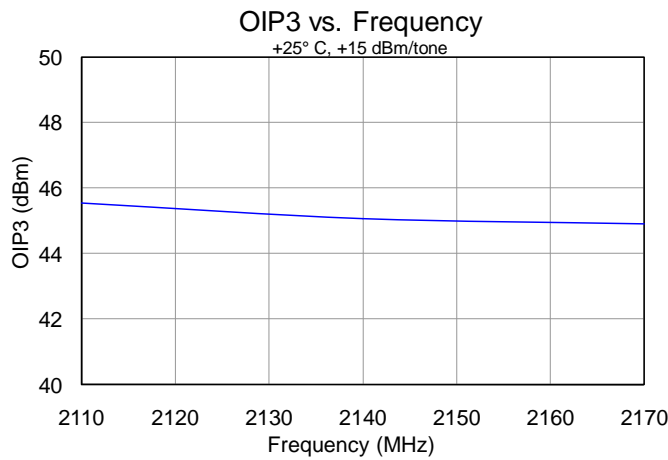
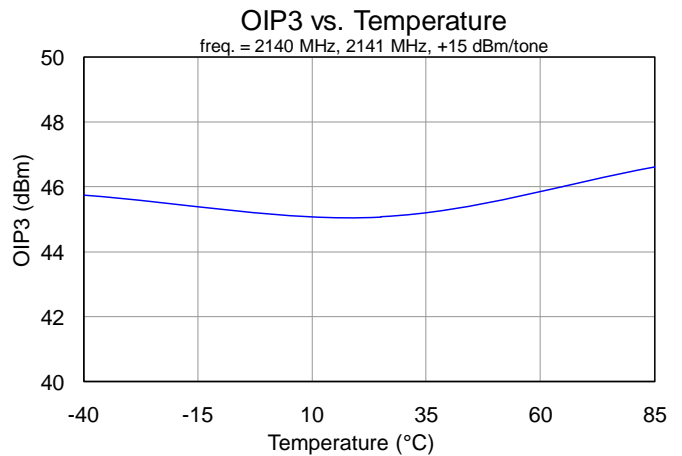
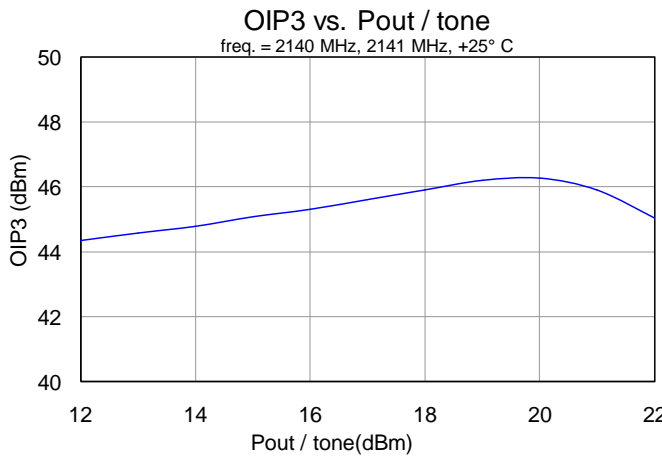
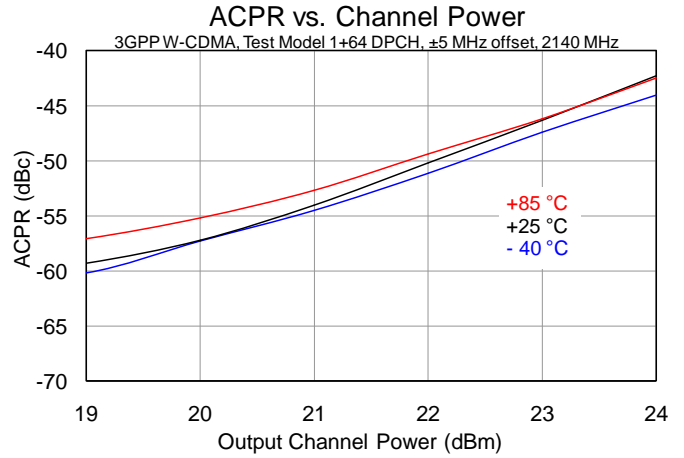
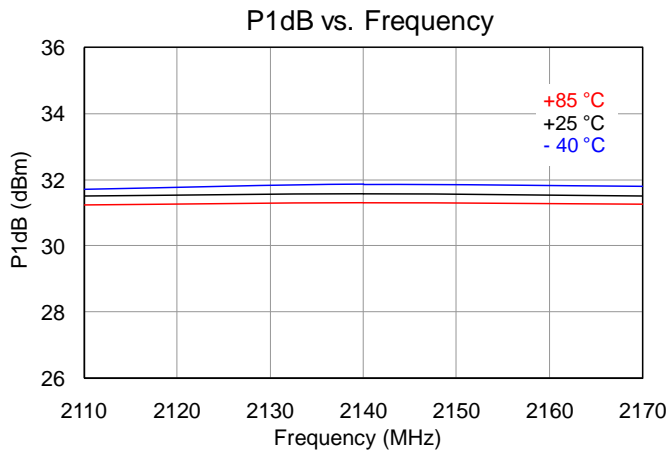
Test conditions unless otherwise noted: $V_{CC} = +5\text{ V}$, $I_{CQ} = 450\text{ mA}$

Parameter	Typical Value			Units
Frequency	2110	2140	2170	MHz
Gain	11.3	11.4	11.3	dB
Input Return Loss	16	18	20	dB
Output Return Loss	8	8	8	dB
Output P1dB	+31.5	+31.5	+31.5	dBm
Output IP3 at 15dBm / tone, $\Delta f = 1\text{ MHz}$	+45.5	+45	+45	dBm
Channel Power (ACLR= -50 dBc, WCDMA, 3GPP) ⁽¹⁾	+23	+23	+23	dBm
Noise Figure	6.1	6.2	6.3	dBm

Typical Performance Plots 2110 – 2170 MHz (AH215-S8PCB2140)



Typical Performance Plots 2110 – 2170 MHz (AH215-S8PCB2140)

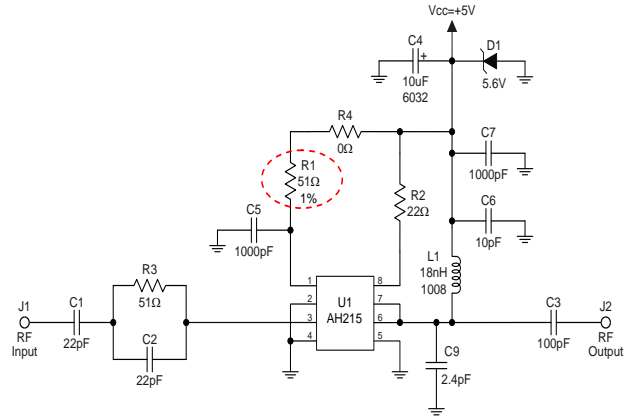


Application Note: Reduced Bias Configuration

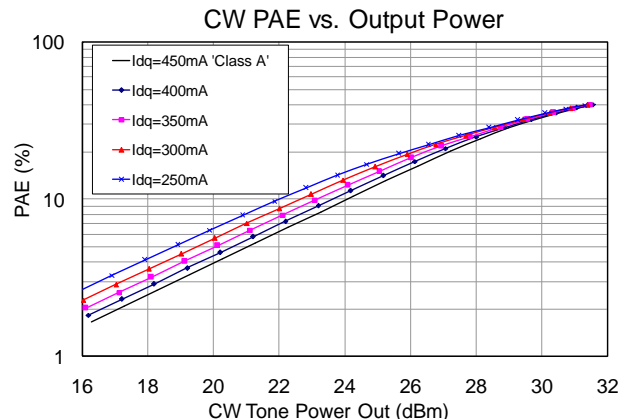
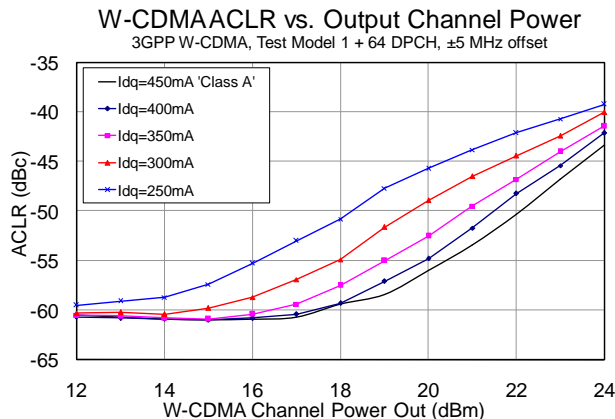
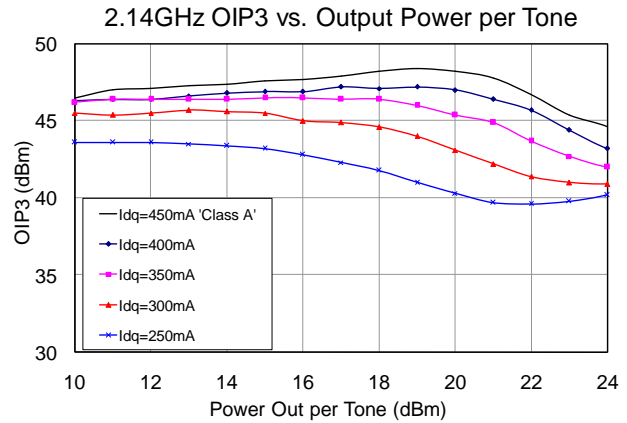
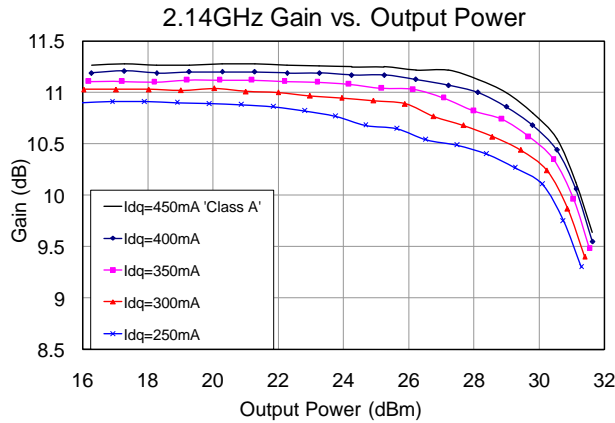
The AH215 can be configured to be operated with lower bias current by varying the bias-adjust resistor R1. The recommended circuit configurations shown previously in this data sheet have the device operating in Class A operation. Lowering the current has little effect on the gain, OIP3, and P1dB performance of the device, but will slightly lower the ACLR/ACPR performance of the device as shown below. An example of the measured data below represents the AH215 measured and configured for 2.14 GHz applications. It is expected that variation of the bias current for other frequency applications will produce similar performance results.

AH215-S8PCB2140 Performance Data

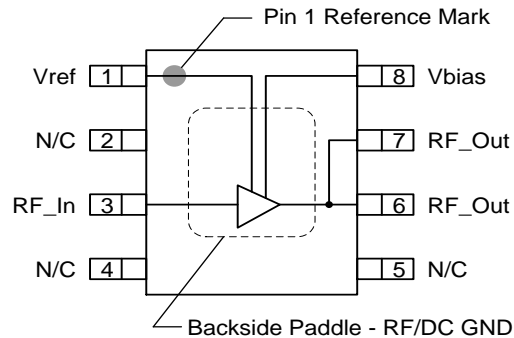
R1 (ohms)	I _{CQ} (mA)	P _{DISS} (W)	P1dB (dBm)	OIP3 (dBm)
51	450	2.25	+31.0	+47.1
68	400	2.00	+30.9	+46.4
100	350	1.75	+30.8	+46.4
130	300	1.50	+30.6	+45.5
180	250	1.25	+30.5	+43.6



Performance Plots: Reduced Bias Configuration



Pin Configuration and Description



Pin No.	Label	Description
1	V _{REF}	Sets reference current
2, 4, 5	N/C	No internal connection. This pin can be grounded or N/C on PCB. Land pads
3	RF Input	RF Input. DC Voltage present, blocking cap required
6, 7	RF Output	RF Output and DC Supply Voltage
8	V _{BIAS}	Voltage supply for active bias for the amp. Connect to same supply voltage as
Backside Paddle	RF / DC GND	Use recommended via pattern shown on page 12 and ensure good solder attach for optimum thermal and electrical performance.

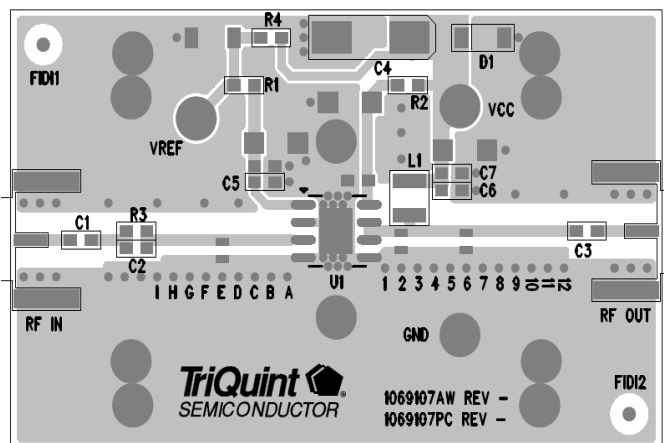
Application Board Information

PC Board Layout

Circuit Board Material: Top RF layer is .014" Getek, 4 total layers (0.062" thick) for mechanical rigidity
1 oz copper, Microstrip line details: width = .026", spacing = .026"

The silk screen markers 'A', 'B', 'C', etc. and '1', '2', '3', etc. are used as place markers for the input and output tuning shunt capacitors – C8 and C9. The markers and vias are spaced in .050" increments.

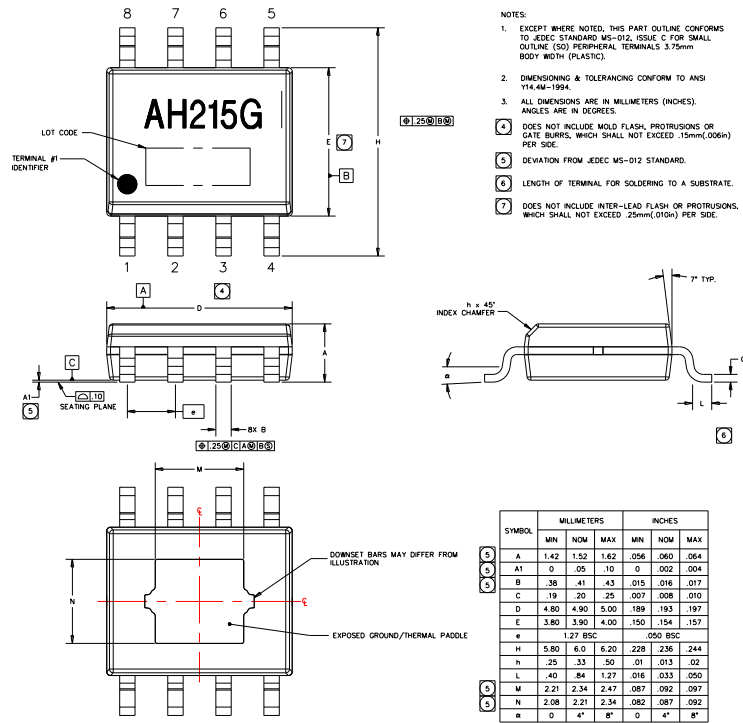
The pad pattern shown has been developed and tested for optimized assembly at TriQuint Semiconductor. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.



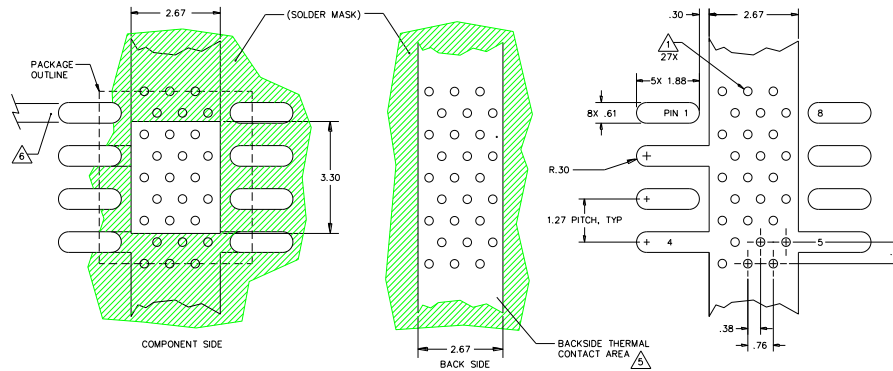
Package Marking and Dimensions

This package is lead-free/green/RoHS-compliant. The plating material on the leads is NiPdAu. It is compatible with both lead-free (maximum 260 °C reflow temperature) and lead (maximum 245 °C reflow temperature) soldering processes.

The component will be marked with an "AH215G" designator with an alphanumeric lot code on the top surface of the package.



PCB Mounting Pattern



Notes:

- A heat sink underneath the area of the PCB for the mounted device is strictly required for proper thermal operation. Damage to the device can occur without the use of one.
- Ground / thermal vias are critical for the proper performance of this device. Vias should use a .35mm (#80 / .0135") diameter drill and have a final plated thru diameter of .25 mm (.010").
- Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.
- Mounting screws can be added near the part to fasten the board to a heat sink. Ensure that the ground / thermal via region contacts the heat sink.
- Do not put solder mask on the backside of the PC board in the region where the board contacts the heat sink.
- RF trace width depends upon the PC board material and construction.
- Use 1 oz. Copper minimum.
- All dimensions are in millimeters (inches). Angles are in degrees.

Product Compliance Information

ESD Sensitivity Ratings



Caution! ESD-Sensitive Device

ESD Rating: Class 1B
Value: ≥ 500 V to < 1000 V
Test: Human Body Model (HBM)
Standard: ESDA/JEDEC Standard JS-001-2012

ESD Rating: Class C3
Value: ≥ 1000 V
Test: Charged Device Model (CDM)
Standard: JEDEC Standard JESD22-C101F

MSL Rating

MSL Rating: Level 2
Test: 260 °C convection reflow
Standard: JEDEC Standard J-STD-020

Solderability

Compatible with both lead-free (260°C max. reflow temperature) and tin/lead (245°C max. reflow temperature) soldering processes.

Package contact plating: NiPdAu

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C₁₅H₁₂Br₄O₂) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

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Email: customer.support@qorvo.com

Tel: 1-844-890-8163

For information about the merger of RFMD and TriQuint as Qorvo:

Web: www.qorvo.com

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