24-Bit Analog-to-Digital Converter (ADC) with Load-cell Power Supply Switch and Battery Voltage Detection for Weigh Scales

DESCRIPTION

Based on Avia Semiconductor's patented technology, HX712 is a precision 24-bit analog-to-digital converter (ADC) with on chip load-cell power supply switch and battery voltage detection. It's designed for weigh scales and industrial control applications to interface directly with a bridge sensor.

The differential inputs connect to the low-noise programmable gain amplifier (PGA) with a gain of 128 or 256, corresponding to a full-scale differential input voltage of ±20mV or ±10mV respectively, when a 5V reference voltage is connected between REFP and REFN pins. Single-ended battery detection input pin BAT can be connected directly to battery output. On chip load-cell power switch can be used to turn off power supply to load-cell to save system power.

Clock input is flexible. It can be from an external clock source, a crystal, or the on-chip oscillator that does not require any external component. On-chip power-on-reset circuitry simplifies digital interface initialization. There is no programming needed for the internal registers. All controls to the HX712 are through the pins.

FEATURES

- **Selectable differential input or battery detection input**
- **On-chip low noise PGA with selectable gain of 128 and 256**
- **On-chip MOS power switch for turning off load-cell power supply in system power save mode**
- **On-chip oscillator requiring no external component with optional external crystal**
- **On-chip power-on-reset**
- **Simple digital control and serial interface: pin-driven controls, no programming needed**
- **Selectable 10SPS or 40SPS output data rate**
- **Simultaneous 50 and 60Hz supply rejection**
- **Current consumption: normal operation < 1.0mA, power down < 1uA**
- **Operation supply voltage range: 2.6 ~ 5.5V**
- **Operation temperature range: -40 ~ +85℃**
- **14 pin SOP-14 package**

APPLICATIONS

- **Weigh Scales**
- **Industrial Process Control**

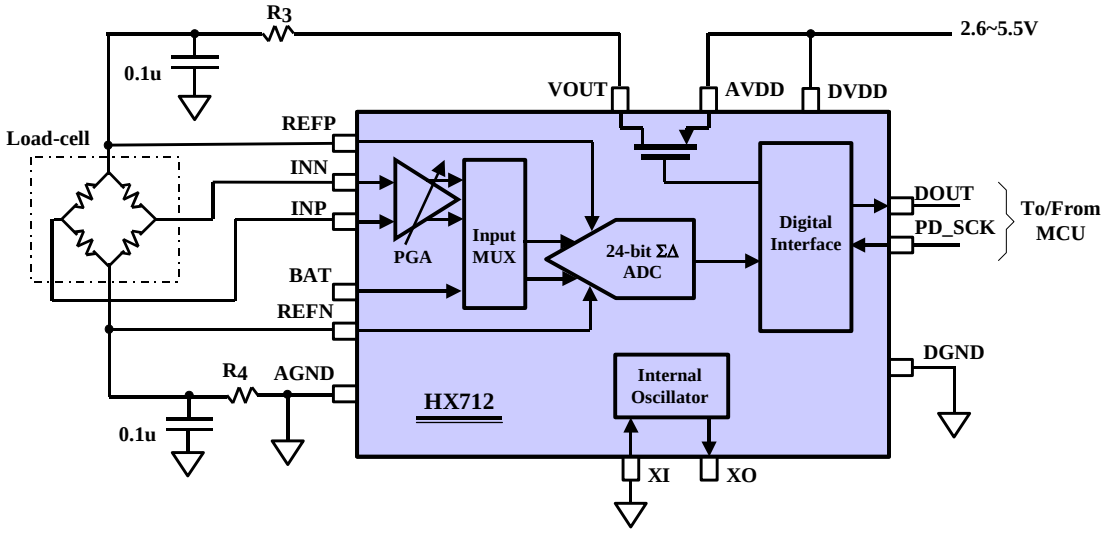
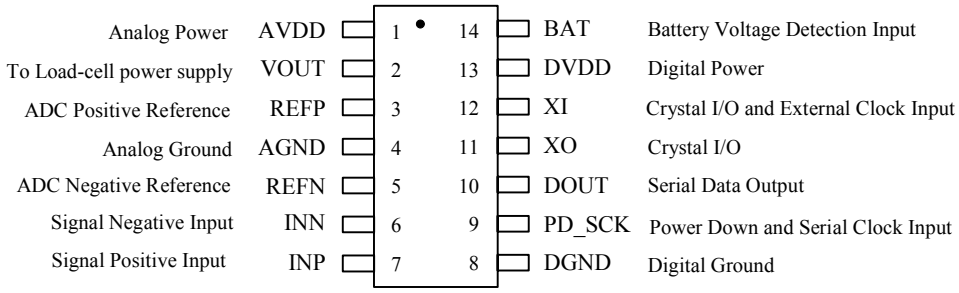


Figure 1 HX712 Block Diagram

Pin Description



SOP-14L Package

Pin #	Name	Function	Description
1	AVDD	Power	Analog supply: 2.6 ~ 5.5V (<= BAT)
2	VOUT	Analog Output	On chip power MOS switch output (NC when not used)
3	REFP	Analog Input	A/D conversion positive reference Input
4	AGND	Ground	Analog ground
5	REFN	Analog Input	A/D conversion negative Reference Input
6	INN	Analog Input	Differential negative input
7	INP	Analog Input	Differential positive input
8	DGND	Ground	Digital ground
9	PD_SCK	Digital Input	Power down control (high active) and serial clock input
10	DOUT	Digital Output	Serial data output
11	XO	Digital I/O	Crystal I/O (NC when not used）
12	XI	Digital Input	Crystal I/O or external clock input, 0: use on-chip oscillator
13	DVDD	Power	Digital supply: 2.6 ~ 5.5V (<= BAT)
14	BAT	Analog Input	Battery voltage detection input（connect to higher of AVDD or DVDD when not used）

Table 1 Pin Description

KEY ELECTRICAL CHARACTERISTICS

Parameter	Notes	MIN	TYP	MAX	UNIT
Full scale differential input range	V(inp)-V(inn)		±0.5(REFP-REFN)/GAIN		V
Effective-Number-of-Bits (ENBs) (1)	Gain=128, Rate=10SPS		19.7		Bits
	Gain=128, Rate=40SPS		18.9		
Noise-Free Bits (NFBs) (2)	Gain=128, Rate=10SPS		17.3		Bits
	Gain=128, Rate=40SPS		16.2		
Integral Nonlinearity （INL）	Differential input, end-point fit		±0.001		%of *FSR*
Input common mode range		AGND+0.8		AVDD-1.3	V
Output data rate	On-chip oscillator		10 or 40		Hz
	External clock or crystal		f_{clk}/1,105,92 or f_{clk}/138,240		
Output data coding	2's complement	800000		7FFFFF	HEX
Power MOS switch on-resistance	AVDD=3.3V		3	5	Ω
Output settling time (3)	Rate=10SPS		400		ms
	Rate=40SPS		100		
Input offset	Gain=128		0.01		mV
Input noise	Gain=128, Rate=10SPS		40		nV (rms)
	Gain=128, Rate=40SPS		80		
Temperature drift （Gain = 128）	Input offset drift		±15		nV/℃
	Gain drift		±7		ppm/℃
Input common mode rejection	Gain=128, Rate=10SPS		100		dB
Power supply rejection	Gain=128, Rate=10SPS		100		dB
Crystal or external clock frequency		1	11.0592	20	MHz
Power supply voltage	DVDD	2.6		5.5	V
	AVDD (< = DVDD)	2.6		5.5	
Analog supply current (AVDD=3.3V)	Normal operation		900		μA
	Power down		0.5		
Digital supply current (DVDD=3.3V)	Normal operation		100		μA
	Power down		0.1		

（1）(2) ENBs = ln(*FSR*/*RMS Noise*)/ln(2), NFBs = ln(*FSR*/*Peak-to-Peak Noise*)/ln(2). *FSR* is full-scale input or output. *RMS Noise* corresponds to input or output RMS noise. *Peak-to-Peak Noise* corresponds to input or output peak-to-peak noise.

（3）Settling time refers to the time from power up, reset, input channel change and gain change to valid stable output data.

Table 2 Key Electrical Characteristics

TYPICAL PERFORMANCE

Test Conditions: Temperature=25℃，AVDD=DVDD=REFP=5V，REFN=AGND，Internal Oscillator

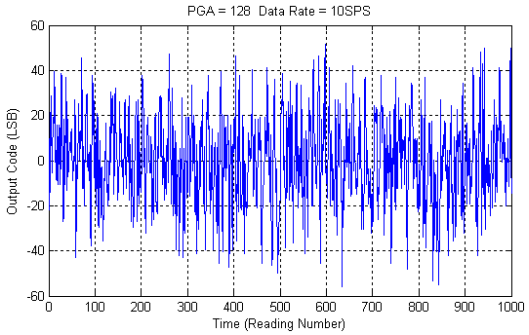


Figure 2 Output Noise（Gain=128，Rate=10Hz）

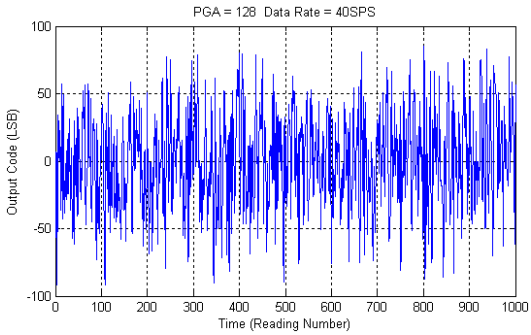


Figure 3 Output Noise（Gain=128，Rate=40Hz）

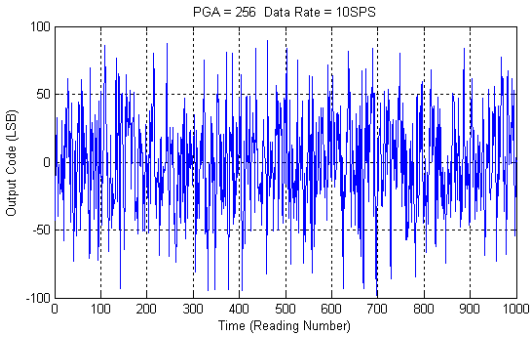


Figure 4 Output Noise（Gain=256，Rate=10Hz）

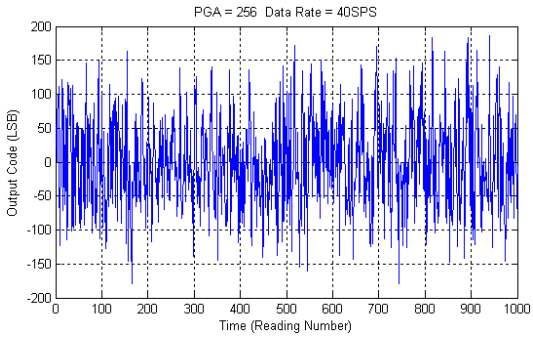


Figure 5 Output Noise（Gain=256，Rate=40Hz）

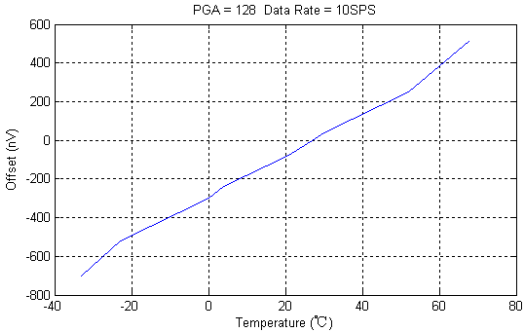


Figure 6 Input Referred Offset Drift (Gain=128, Rate=10Hz)

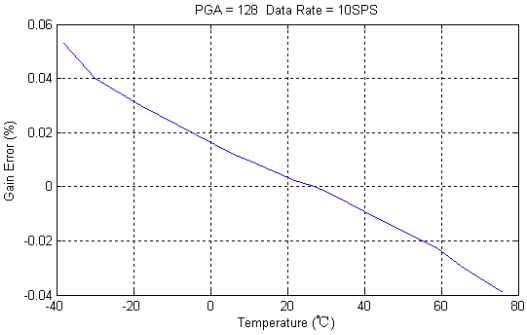


Figure 7 Gain Drift (Gain=128, Rate=10Hz)

Analog Input and Battery Detection

Differential inputs are designed to interface directly with a bridge sensor's differential outputs. It can be programmed with a gain of 128 or 256. When 5V reference is used, these gains correspond to a full-scale differential input voltage of ±20mV or ±10mV respectively.

Single-ended battery input signal (BAT) can be directly connected to a battery output (2.6~5.5V). On-chip 56kΩ and 3.2kΩ resistors divide this input voltage to provide suitable voltage to the ADC, which has a gain of 1. When detecting battery input, AVDD is used as the ADC's data conversion reference voltage. When battery detection circuitry is not in used, a MOS switch is used to turn off the resistor divider path current.

Power Supply Options

DVDD can be connected directly to AVDD power supply. But it should be the same or similar voltage as the MCU power supply to ensure proper communication with the MCU.

A/D conversion reference voltage (REFP, REFN) should be connected to load-cell's supply terminals. It can be connected directly to AVDD, or through a resistor to reduce the power consumption by the load-cell.

Clock Source Options

By connecting pin XI to Ground, the on-chip oscillator is activated. The nominal output data rate when using the internal oscillator is 10 or 40SPS.

If accurate output data rate is needed, crystal or external reference clock can be used. A crystal can be directly connected across XI and XO pins. An external clock can be connected to XI pin, through a 20pF ac coupled capacitor. This external clock is not required to be a square wave. It can come directly from the crystal output pin of the MCU chip, with amplitude as low as 150 mV.

When using a crystal or an external clock, the internal oscillator is automatically powered down.

Output Data Rate and Format

When using the on-chip oscillator, output data rate is typically 10 or 40SPS.

When using external clock or crystal, output data rate is directly proportional to the clock or crystal frequency. Using 11.0592MHz clock or crystal results in an accurate 10 or 40SPS output data rate.

The output 24 bits of data is in 2's complement format. When input differential signal goes out of the 24-bit range, the output data will be saturated at 800000h (MIN) or 7FFFFFh (MAX), until the input signal comes back to the input range.

Serial Interface

Pin PD_SCK and DOUT are used for data retrieval, input selection, gain selection and power down controls.

When output data is not ready for retrieval, digital output pin DOUT is high. Serial clock input PD_SCK should be low. When DOUT goes to low, it indicates data is ready for retrieval. By applying 25~29 positive clock pulses at the PD_SCK pin, data is shifted out from the DOUT output pin. Each PD_SCK pulse shifts out one bit, starting with the MSB bit first, until all 24 bits are shifted out. The 25th pulse at PD_SCK input will pull DOUT pin back to high (Figure 8).

Input and gain selection is controlled by the number of the input PD_SCK pulses (Table 3). PD_SCK clock pulses should not be less than 25 or more than 29 within one conversion period, to avoid causing serial communication error.

PD_SCK pulses	Input	Gain	Rate
25	Differential Signal	128	10Hz
26	BAT		40Hz
27	Differential Signal	128	40Hz
28	Differential Signal	256	10Hz
29	Differential Signal	256	40Hz

Table 3 Inputs, Rate and Gain Selection

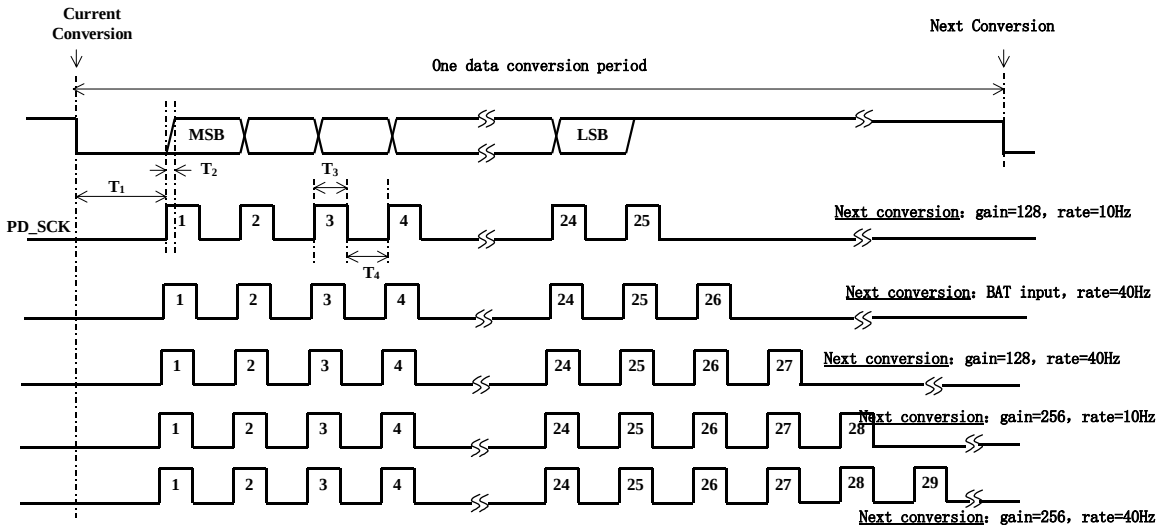


Figure 8 Data output, input and gain selection timing diagram

Symbol	Note	MIN	TYP	MAX	Unit
T_1	DOUT falling edge to PD_SCK rising edge	0.1			μs
T_2	PD_SCK rising edge to DOUT data ready			0.1	μs
T_3	PD_SCK high time	0.2	1	50	μs
T_4	PD_SCK low time	0.2	1		μs

Reset and Power-Down

When chip is powered up, on-chip power on rest circuitry will reset the chip.

Pin PD_SCK input is used to power down the HX712. When PD_SCK input is low, chip is in normal working mode.

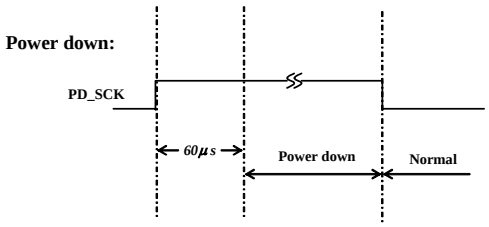


Figure 9 Power down control

When PD_SCK pin changes from low to high and stays at high for longer than 60μs, HX712 enters power down mode (Figure 9). When internal MOS power switch is used for the external load-cell, both HX712 and the load-cell will be powered down. When PD_SCK returns to low, chip will return back to the setup conditions before power down and enter normal operation mode.

If PD_SCK pulse number is changed during the current conversion period, power down should be executed after current conversion period is completed. This is to ensure that the change is saved. When chip returns back to normal operation from power down, it will return to the set up conditions of the last change.

Application Example

Figure 10 is a typical weigh scale application using HX712. It uses on-chip oscillator (XI=0). A single power supply (2.7～5.5V) comes directly from MCU power supply.

Reference PCB Board (Single Layer)

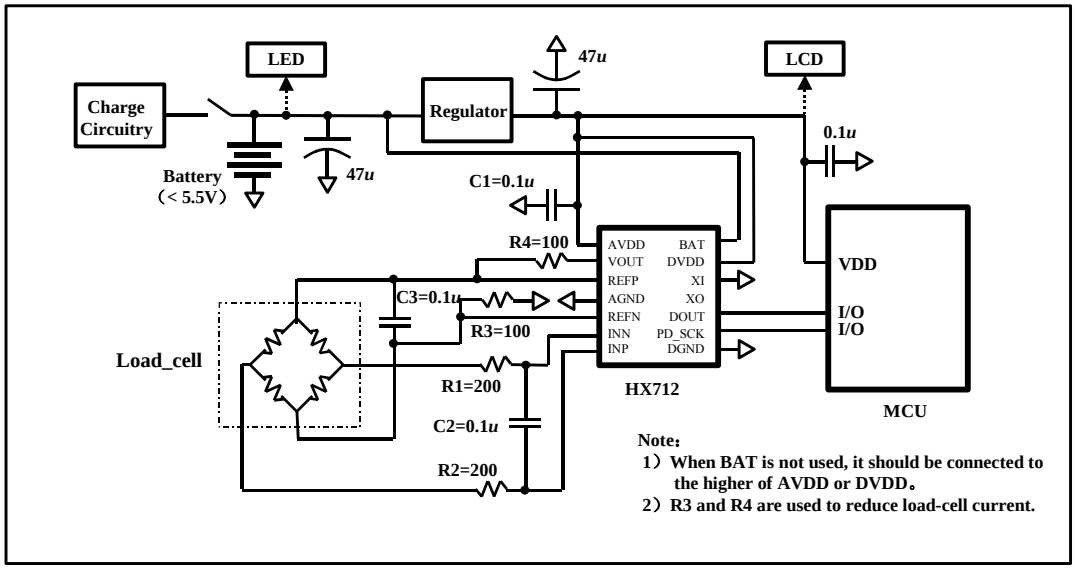


Figure 10 Reference PCB board schematic

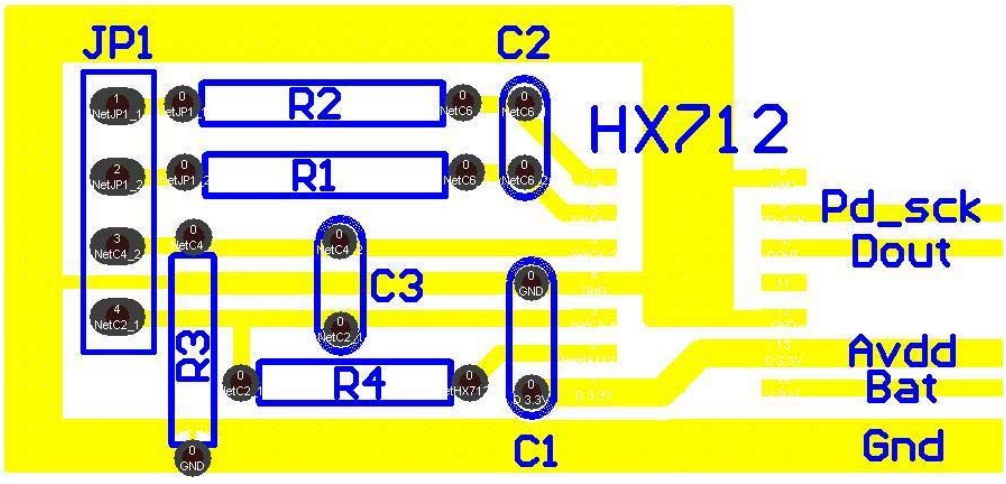


Fig.11 Reference Single Layer PCB board layout

Reference Driver (Assembly)

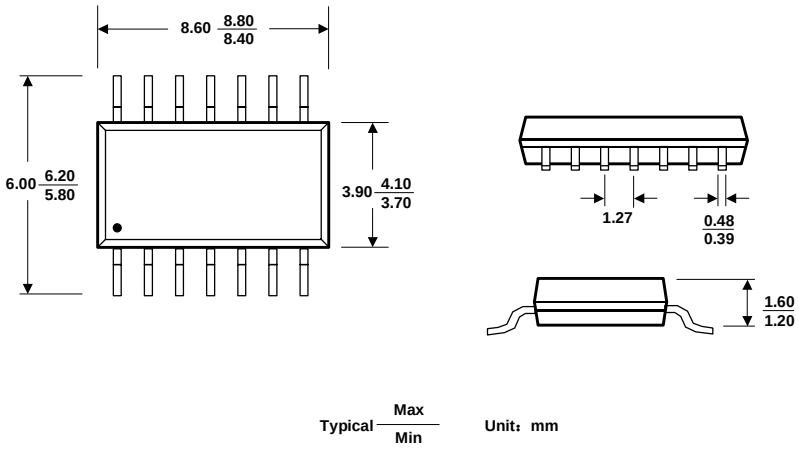
```
/*-----------------------------------------------------------------
Call from ASM:  LCALL   ReaAD
Call from C:    extern unsigned long ReadAD(void);
                  .
                  .
                 unsigned long data;
                 data=ReadAD();
                  .
                  .
-----------------------------------------------------------------*/
PUBLIC        ReadAD
HX712ROM      segment  code
rseg          HX712ROM

sbit           ADDO = P1.5;
sbit           ADSK = P0.0;
/*-------------------------------------------------
 OUT:   R4, R5, R6, R7   R7=>LSB
-------------------------------------------------*/
ReadAD:
    CLR    ADSK              //AD Enable (PD_SCK set low)
    SETB   ADDO              //Enable 51CPU I/O
    JB     ADDO,$            //AD conversion completed?
    MOV    R4,#24
ShiftOut:
    SETB   ADSK              //PD_SCK set high (positive pulse)
    NOP
    CLR    ADSK              //PD_SCK set low
    MOV    C,ADDO            //read on bit
    XCH    A,R7              //move data
    RLC    A
    XCH    A,R7
    XCH    A,R6
    RLC    A
    XCH    A,R6
    XCH    A,R5
    RLC    A
    XCH    A,R5
    DJNZ   R4,ShiftOut        //moved 24BIT?
    SETB   ADSK
    NOP
    CLR    ADSK
    RET
    END
```

Reference Driver（C）

```
//-----------------------------------------------------------------------
sbit   ADDO = P1^5;
sbit   ADSK = P0^0;
unsigned long ReadCount(void){
  unsigned long Count;
  unsigned char i;
  ADDO=1;
  ADSK=0;
  Count=0;
  while(ADDO);
  for (i=0;i<24;i++){
    ADSK=1;
    Count=Count<<1;
    ADSK=0;
    if(ADDO) Count++;
  }
  ADSK=1;
  Count=Count^0x800000;
  ADSK=0;
  return(Count);
}
```

Package Dimensions



SOP-14L Package