



For most current data sheet and other product information, visit [www.burr-brown.com](http://www.burr-brown.com)

## Single-Supply, Rail-to-Rail Output, CMOS INSTRUMENTATION AMPLIFIER

### FEATURES

- RAIL-TO-RAIL OUTPUT SWING: Within 20mV
- LOW OFFSET DRIFT:  $\pm 5\mu\text{V}/^\circ\text{C}$
- INTERNAL FIXED GAIN = 10V/V OR 50V/V
- SPECIFIED TEMPERATURE RANGE:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$
- LOW INPUT BIAS CURRENT: 1pA
- WIDE BANDWIDTH: 550kHz in  $G = 10$
- HIGH SLEW RATE: 6.5V/ $\mu\text{s}$
- LOW COST
- TINY MSOP-8 PACKAGES

### APPLICATIONS

- INDUSTRIAL SENSOR AMPLIFIERS: Bridge, RTD, Thermocouple, Flow, Position
- MEDICAL EQUIPMENT: ECG, EEG, EMG Amplifiers
- DRIVING A/D CONVERTERS
- PCMCIA CARDS
- AUDIO PROCESSING
- COMMUNICATIONS
- TEST EQUIPMENT
- LOW COST AUTOMOTIVE INSTRUMENTATION

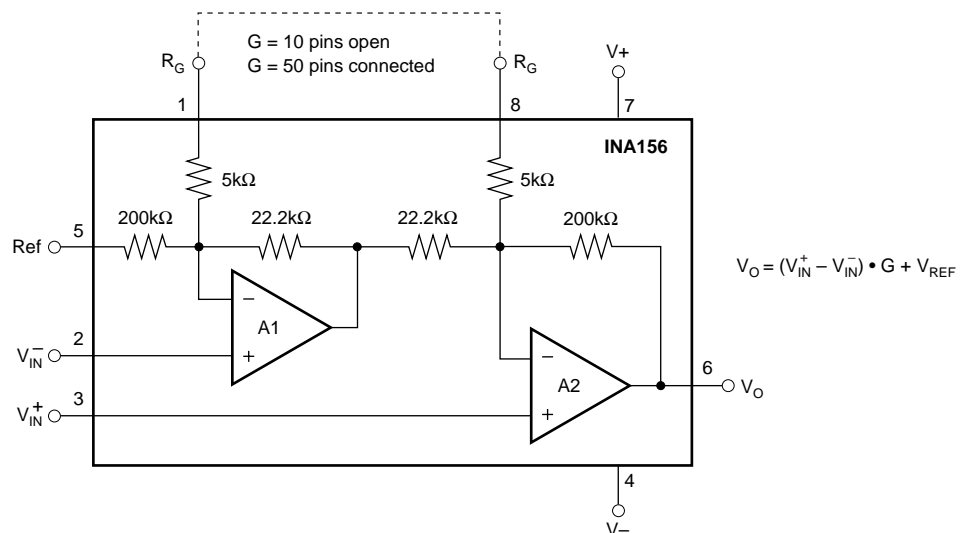
### DESCRIPTION

The INA156 is a low-cost CMOS instrumentation amplifier with rail-to-rail output swing optimized for low-voltage, single-supply operation.

Wide bandwidth (550kHz in  $G = 10$ ) and high slew rate (6.5V/ $\mu\text{s}$ ) make the INA156 suitable for driving sampling A/D converters as well as general purpose and audio applications. Fast settling time allows use with higher speed sensors and transducers, and rapid scanning data acquisition systems.

Gain can be set to 10V/V or 50V/V by pin strapping. Gains between these two values can be obtained with the addition of a single resistor. The INA156 is fully specified over the supply range of +2.7V to +5.5V.

The INA156 is available in an MSOP-8 surface-mount package specified for operation over the temperature range  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ .



# SPECIFICATIONS: $V_S = +2.7V$ to $+5.5V$

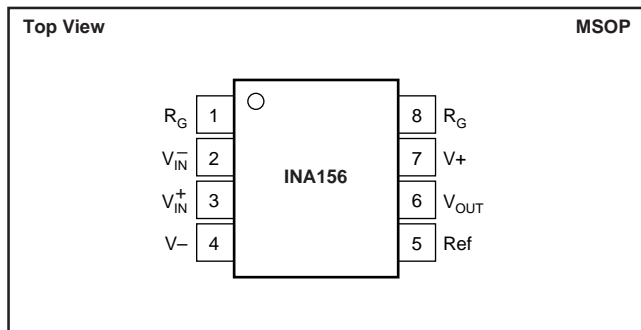
**Boldface** limits apply over the specified temperature range,  $T_A = -55^{\circ}C$  to  $+125^{\circ}C$

At  $T_A = +25^{\circ}C$ ,  $R_L = 10k\Omega$  connected to  $V_S/2$ .  $R_G$  pins open ( $G = 10$ ), and  $Ref = V_S/2$ , unless otherwise noted.

PARAMETER	CONDITION	INA156E, A			UNITS
		MIN	TYP	MAX	
<b>INPUT</b> Offset Voltage, RTI <b>Over Temperature</b> Drift vs Power Supply <b>Over Temperature</b> vs Time	$V_{OS}$  $dV_{OS}/dT$ PSRR  $V_S = +5.0V, V_{CM} = V_S/2$  $V_S = +2.7V$ to $+6V, V_{CM} = 0.2 \cdot V_S$		$\pm 2.5$  $\pm 5$  $\pm 50$  $\pm 0.4$	$\pm 8$  $\pm 9$  $\pm 200$  $\pm 250$	mV mV $\mu V/^{\circ}C$ $\mu V/V$ $\mu V/V$ $\mu V/mo$
<b>INPUT VOLTAGE RANGE</b> Safe Input Voltage Common-Mode Range <sup>(1)</sup>  Common-Mode Rejection Ratio <b>Over Temperature</b>  <b>Over Temperature</b>	$V_{CM}$  CMRR  $V_S = 5.5V, 0.6V < V_{CM} < 3.7V, G = 10$  $V_S = 5.5V, 0.6V < V_{CM} < 3.7V, G = 50$	$(V-) - 0.5$ 0.3 0.2 66 <b>65</b> 74 <b>73</b>		$(V+) + 0.5$ 5.2 <sup>(2)</sup> 2.5 <sup>(2)</sup> 78 87	V V V dB dB dB dB
<b>INPUT IMPEDANCE</b> Differential Common-Mode				$10^{13} \parallel 3$ $10^{13} \parallel 3$	$\Omega \parallel pF$ $\Omega \parallel pF$
<b>INPUT BIAS CURRENT</b> Input Bias Current Offset Current	$I_B$ $I_{OS}$			$\pm 1$ $\pm 1$	pA pA
<b>NOISE, RTI</b> Voltage Noise: $f = 0.1Hz$ to $10Hz$ Voltage Noise Density: $f = 10Hz$ $f = 100Hz$ $f = 1kHz$ Current Noise: $f = 1kHz$	$R_S = 0\Omega, G = 10$ or $50$			4.5 260 99 40 2	$\mu V/Vp-p$ $nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$ $fA/\sqrt{Hz}$
<b>GAIN</b> Gain Equation Gain Error <sup>(3)</sup> <b>vs Temperature</b>  <b>vs Temperature</b> Nonlinearity <b>Over Temperature</b>	$V_S = 5.5V, V_O = 0.02V$ to $5.48V, G = 10$  $V_S = 5.5V, V_O = 0.05V$ to $5.45V, G = 50$  $V_S = 5.5V, G = 10$ or $50$	10	$G = 10 + 400k\Omega/(10k\Omega + R_G)$	50 V/V $\pm 0.08$ $\pm 2$ $\pm 0.1$ $\pm 15$ $\pm 0.005$	V/V % ppm/ $^{\circ}C$ % ppm/ $^{\circ}C$ % of FSR % of FSR
<b>OUTPUT</b> Voltage Output Swing from Rail <b>Over Temperature</b> Short-Circuit Current Capacitance Load (stable operation)	$G = 10, R_L = 10k\Omega, G_{ERR} < 0.4%$  Short-Circuit to Ground			5  $\pm 50$ See Typical Curve	mV mV mA
<b>FREQUENCY RESPONSE</b> Bandwidth, $-3dB$  Slew Rate Settling Time: 0.1%  0.01%  Overload Recovery Total Harmonic Distortion + Noise	BW  SR $t_S$    THD+N	$G = 10$ $G = 50$ $V_S = 5.5V, C_L = 100pF$ $V_S = 5.5V, V_O = 2V$ Step, $C_L = 100pF, G = 10$ $V_S = 5.5V, V_O = 2V$ Step, $C_L = 100pF, G = 50$ $V_S = 5.5V, V_O = 2V$ Step, $C_L = 100pF, G = 10$ $V_S = 5.5V, V_O = 2V$ Step, $C_L = 100pF, G = 50$ 50% Input Overload		550 110 6.5 5 11 8 15 0.2 See Typical Curve	kHz kHz V/ $\mu s$ $\mu s$ $\mu s$ $\mu s$ $\mu s$ $\mu s$
<b>POWER SUPPLY</b> Specified Voltage Range Operating Voltage Range Quiescent Current <b>Over Temperature</b>	$V_{IN} = 0, I_O = 0$ <b><math>V_{IN} = 0, I_O = 0</math></b>	+2.7		+5.5  +2.5 to +6 1.8  <b>3.2</b>	V V mA mA
<b>TEMPERATURE RANGE</b> Specified Range Operating Range Storage Range Thermal Resistance MSOP-8 Surface Mount SO-8 Surface Mount	$\theta_{JA}$	-55 -65 -65		+125 +150 +150  150 150	$^{\circ}C$ $^{\circ}C$ $^{\circ}C$ $^{\circ}C/W$ $^{\circ}C/W$

NOTES: (1) For further information, refer to typical performance curves on common-mode input range. (2) Operation beyond  $(V+) - 1.8V$  (max) results in reduced common-mode rejection. See discussion and Figure 6 in the text of this data sheet. (3) Does not include error and TCR of additional optional gain-setting resistor in series with  $R_G$ , if used.

## PIN CONFIGURATION



## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Supply Voltage, $V^+$ to $V^-$ .....	7.5V
Signal Input Terminals, Voltage <sup>(2)</sup> .....	$(V^-) - 0.5V$ to $(V^+) + 0.5V$
Current <sup>(2)</sup> .....	10mA
Output Short-Circuit <sup>(3)</sup> .....	Continuous
Operating Temperature.....	-65°C to +150°C
Storage Temperature.....	-65°C to +150°C
Junction Temperature.....	+150°C
Lead Temperature (soldering, 10s).....	+300°C

NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied. (2) Input terminals are diode-clamped to the power supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current limited to 10mA or less. (3) Short circuit to ground.

## PACKAGE/ORDERING INFORMATION

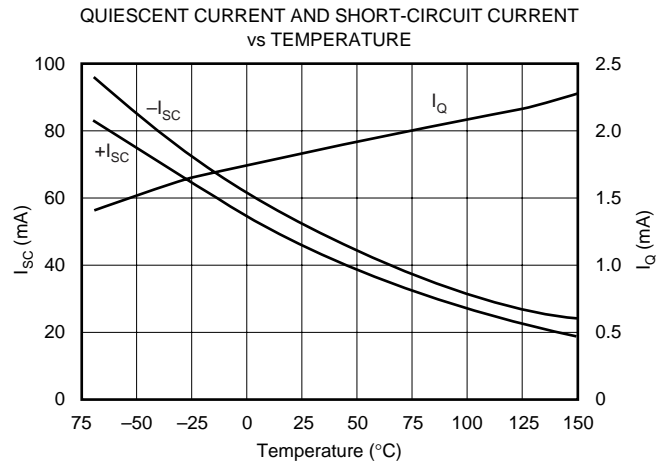
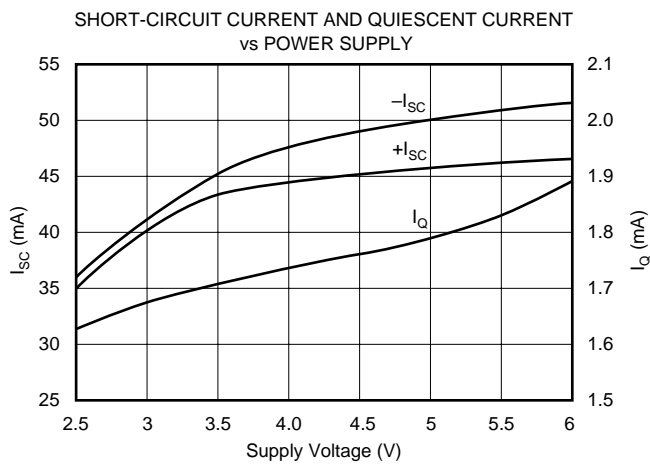
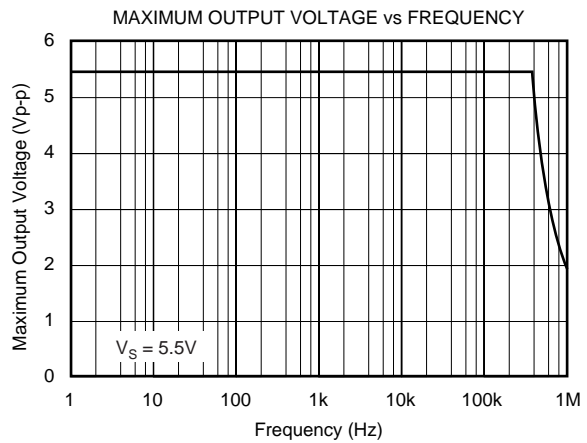
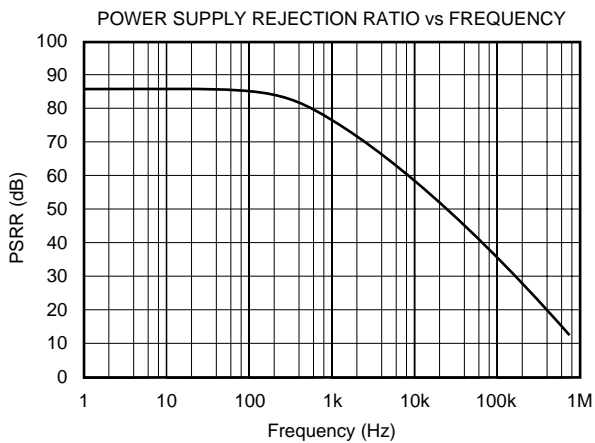
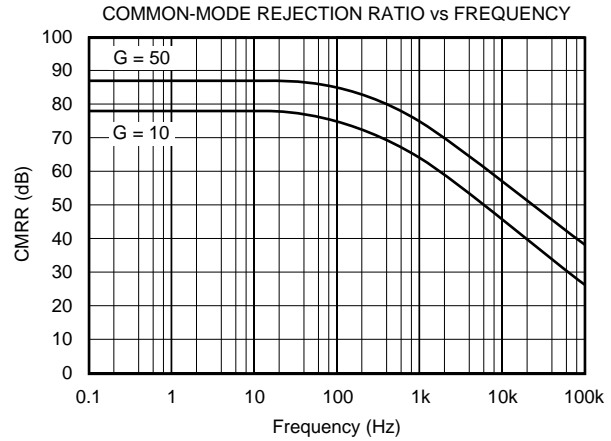
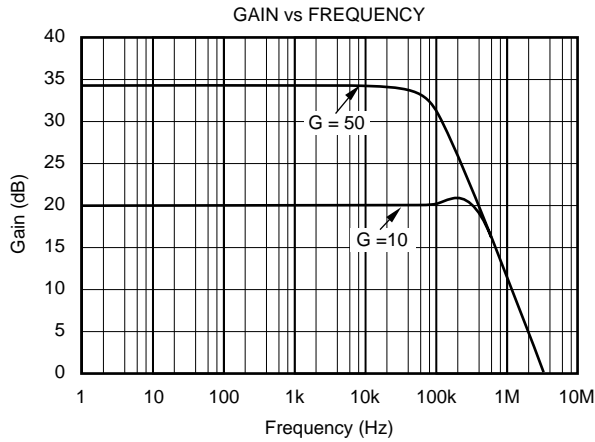
PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER <sup>(1)</sup>	TRANSPORT MEDIA
INA156 EA	MSOP-8	337	-55°C to +125°C	A56	INA156EA/250	Tape and Reel
"	"	"	"	"	INA156EA/2K5	Tape and Reel

NOTE: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K5 indicates 2500 devices per reel). Ordering 2500 pieces of "INA156EA/2K5" will get a single 2500-piece Tape and Reel.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

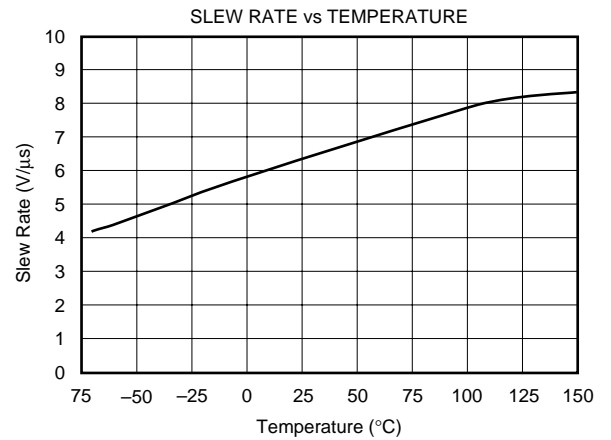
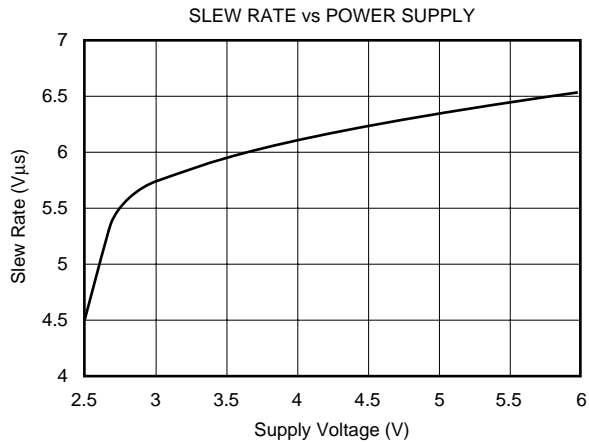
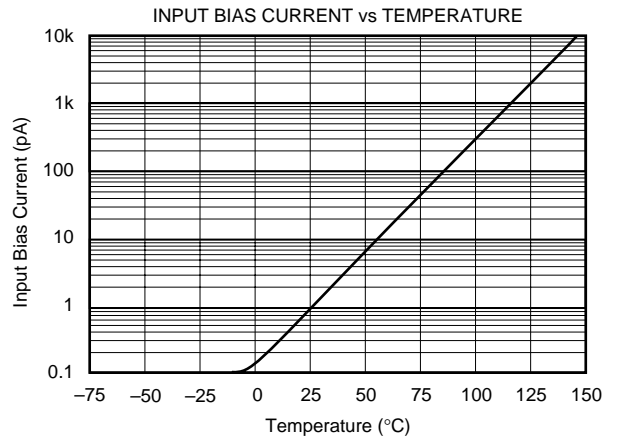
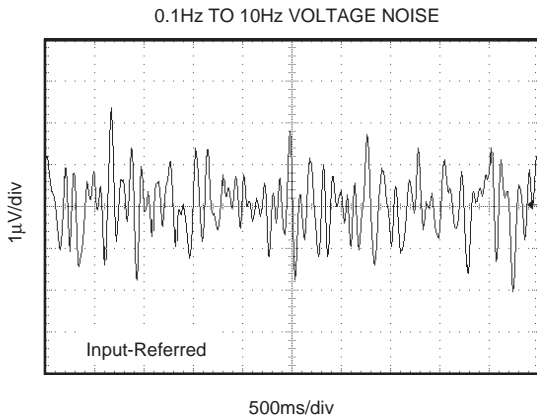
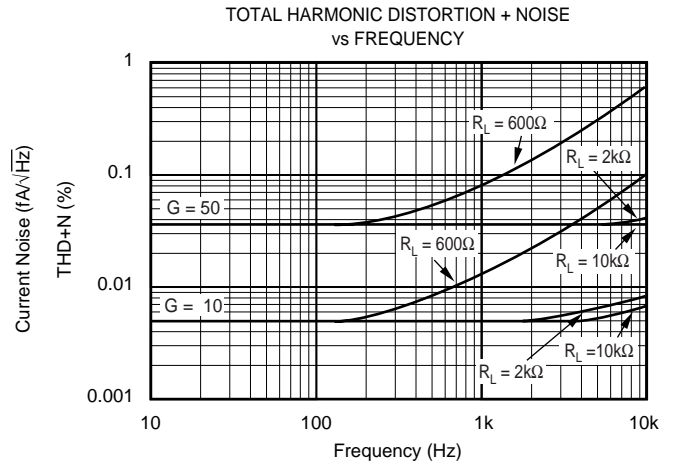
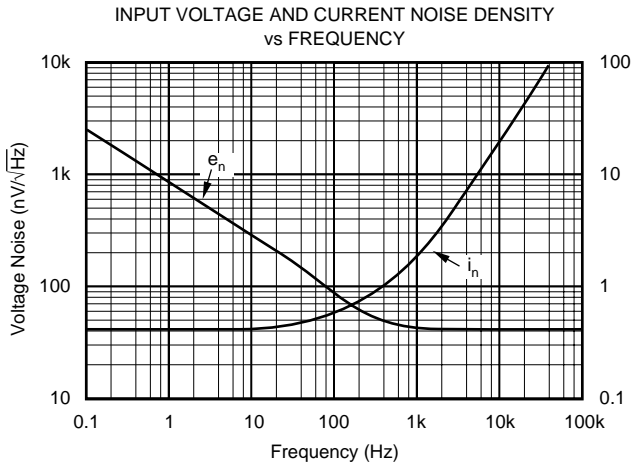
# TYPICAL PERFORMANCE CURVES

At  $T_A = +25^\circ\text{C}$ ,  $V_S = 5.5\text{V}$ ,  $R_L = 10\text{k}\Omega$  connected to  $V_S/2$ .  $R_G$  pins open ( $G = 10$ ), and  $\text{Ref} = V_S/2$ , unless otherwise noted.



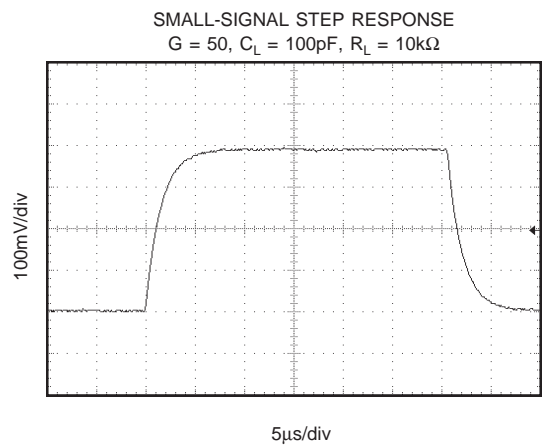
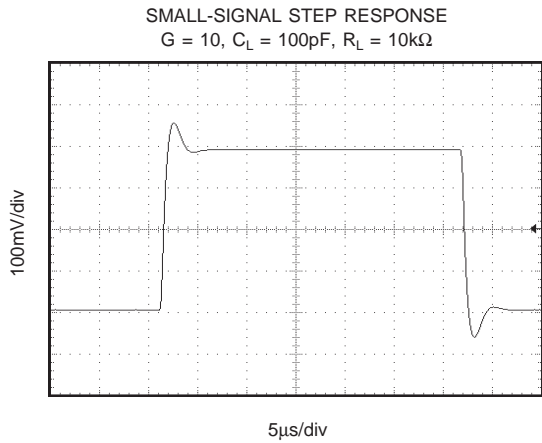
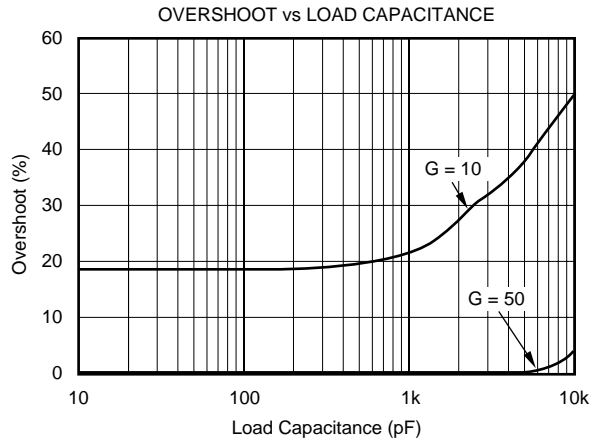
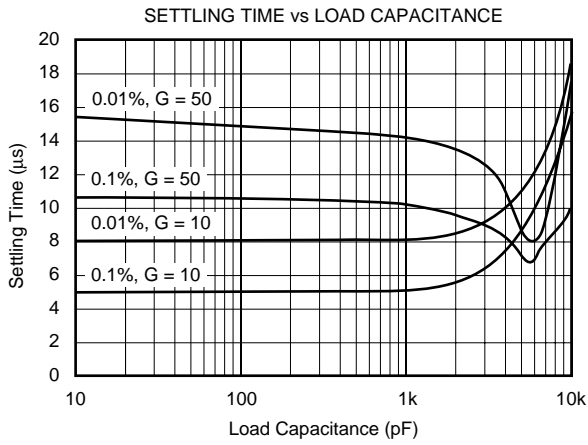
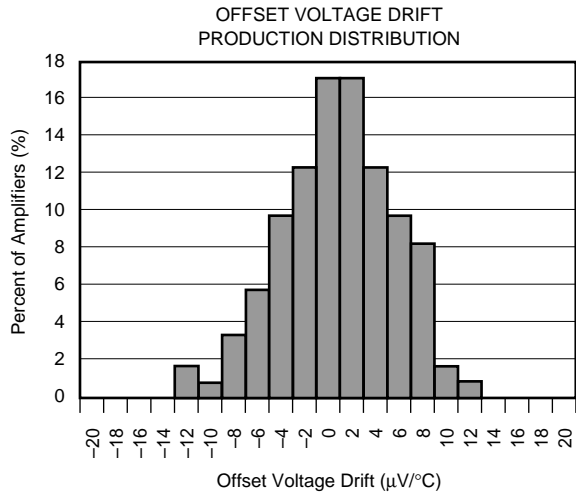
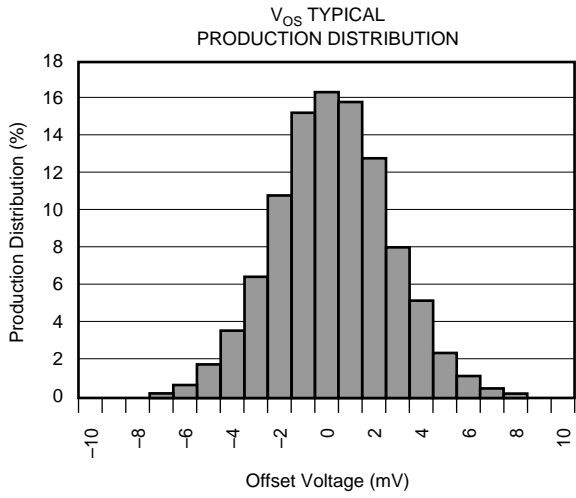
# TYPICAL PERFORMANCE CURVES (Cont.)

At  $T_A = +25^\circ\text{C}$ ,  $V_S = 5.5\text{V}$ ,  $R_L = 10\text{k}\Omega$  connected to  $V_S/2$ .  $R_G$  pins open ( $G = 10$ ), and  $\text{Ref} = V_S/2$ , unless otherwise noted.



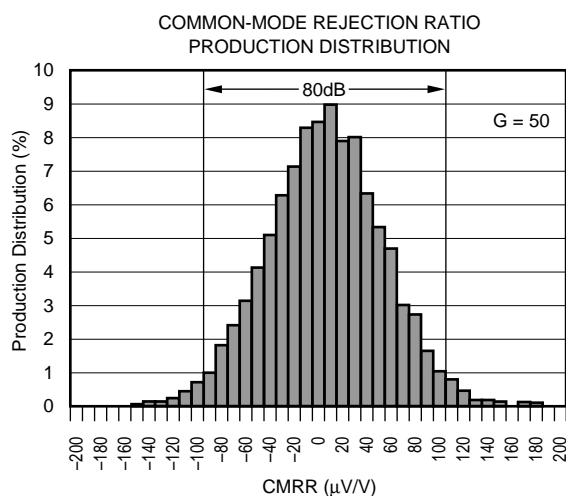
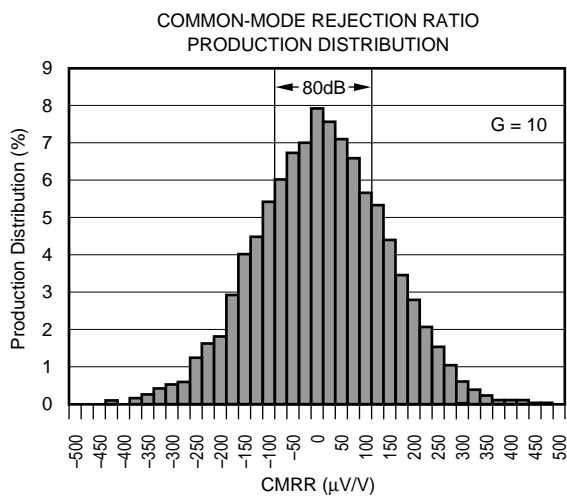
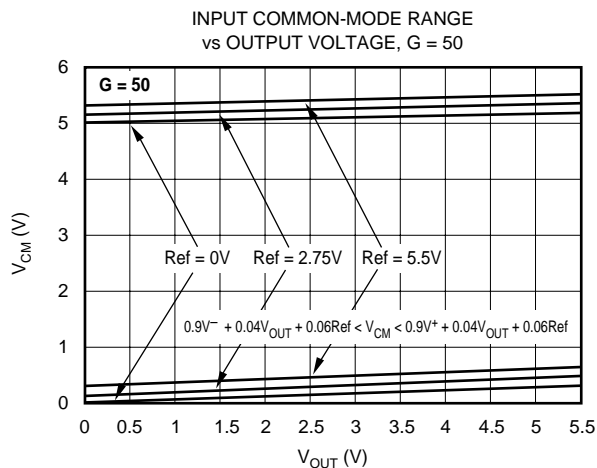
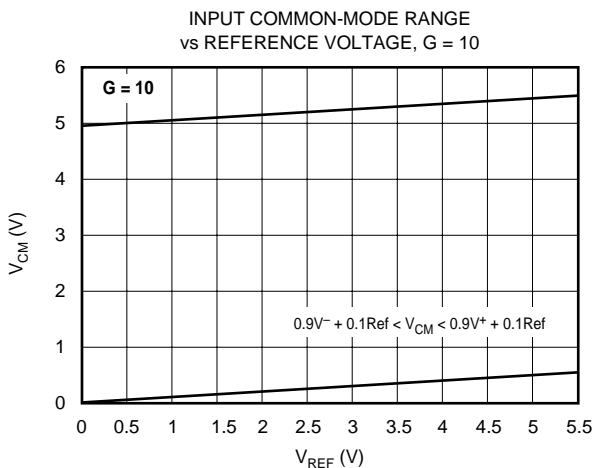
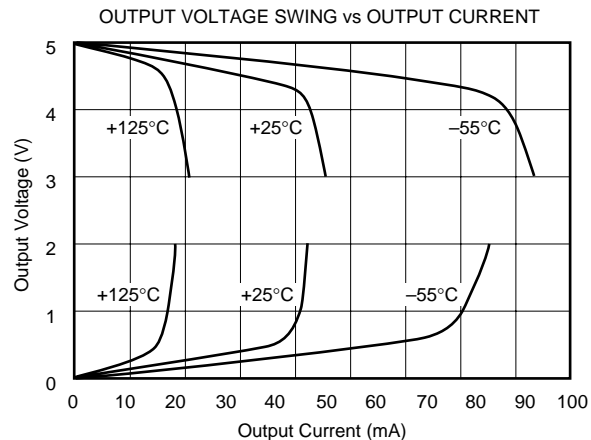
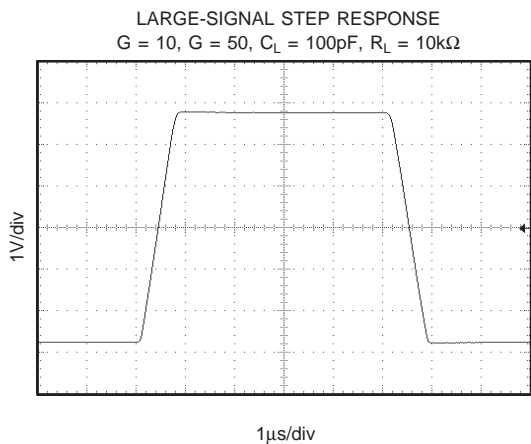
# TYPICAL PERFORMANCE CURVES (Cont.)

At  $T_A = +25^\circ\text{C}$ ,  $V_S = 5.5\text{V}$ ,  $R_L = 10\text{k}\Omega$  connected to  $V_S/2$ .  $R_G$  pins open ( $G = 10$ ), and  $\text{Ref} = V_S/2$ , unless otherwise noted.



# TYPICAL PERFORMANCE CURVES (Cont.)

At  $T_A = +25^\circ\text{C}$ ,  $V_S = 5.5\text{V}$ ,  $R_L = 10\text{k}\Omega$  connected to  $V_S/2$ .  $R_G$  pins open ( $G = 10$ ), and  $\text{Ref} = V_S/2$ , unless otherwise noted.



# APPLICATIONS INFORMATION

Figure 1 shows the basic connections required for operation of the INA156. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins, as shown.

The output is referred to the output reference terminal, Ref, which is normally set to  $V_S/2$ . This must be a low-impedance connection to ensure good common-mode rejection.

In addition, for the  $G = 50$  configuration, the connection between pins 1 and 8 must be low-impedance. A connection impedance of  $20\Omega$  can cause a 0.2% shift in gain error.

# OPERATING VOLTAGE

The INA156 is fully specified and guaranteed over the supply range  $+2.7V$  to  $+5.5V$ , with key parameters guaranteed over the temperature range of  $-55^\circ C$  to  $+125^\circ C$ . Parameters that vary significantly with operating voltages, load conditions or temperature are shown in the Typical Performance Curves.

The INA156 can be operated from either single or dual power supplies. By adjusting the voltage applied to the reference terminal, the input common-mode voltage range and the output range can be adjusted within the bounds shown in the Typical Performance Curves. Figure 2 shows a bridge amplifier circuit operated from a single  $+5V$  power supply. The bridge provides a relatively small differential voltage on top of an input common-mode voltage near  $2.5V$ .

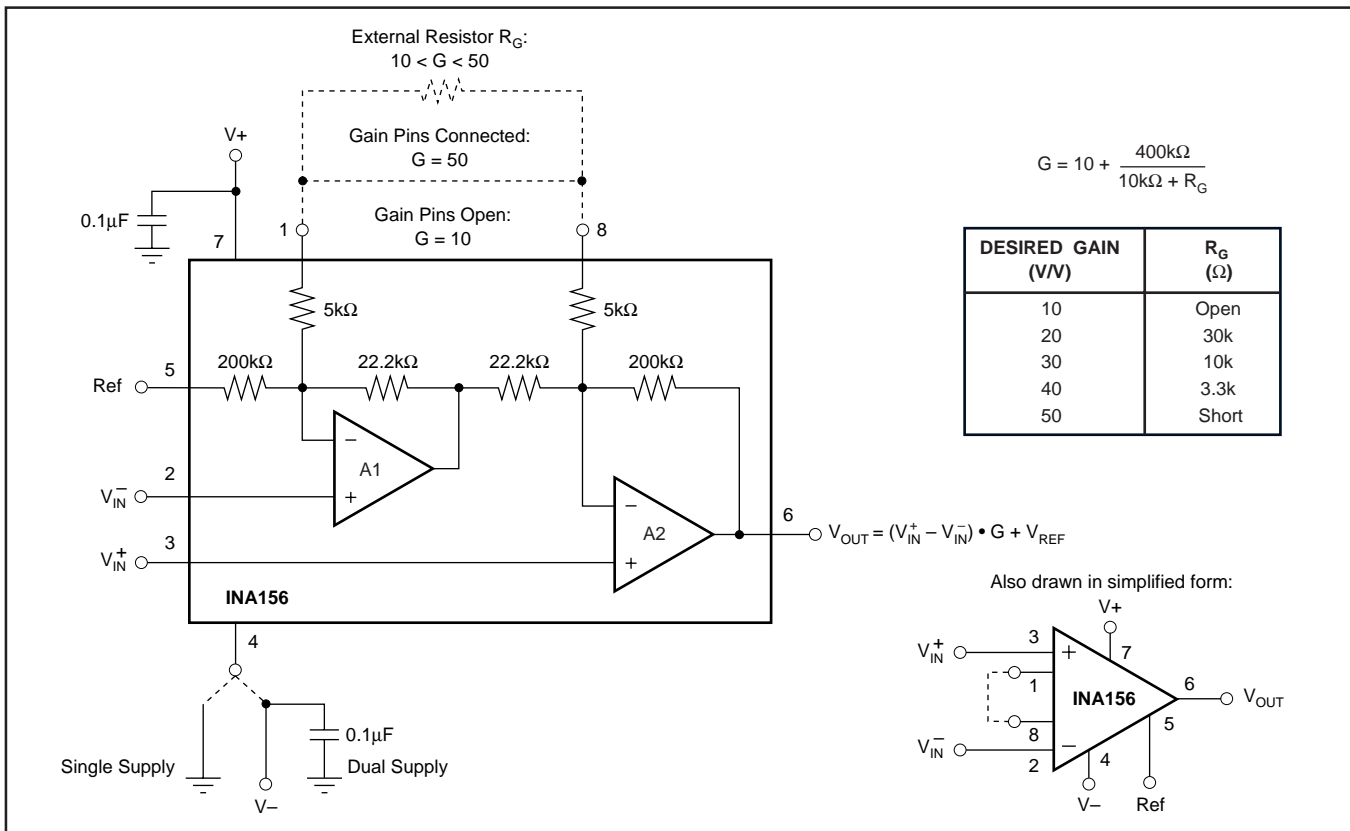


FIGURE 1. Basic Connections.

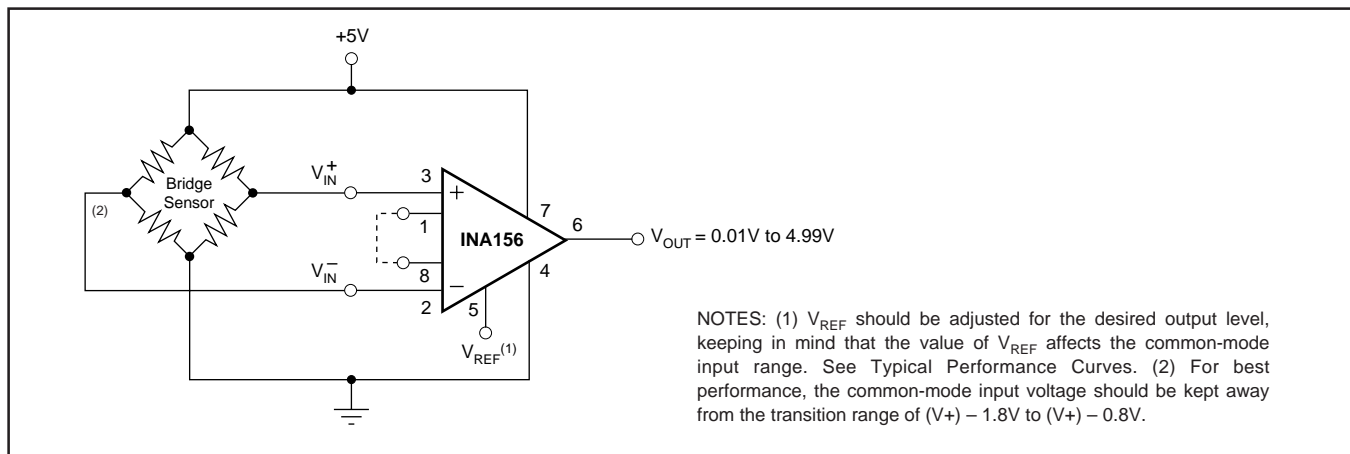


FIGURE 2. Single-Supply Bridge Amplifier.



## SETTING THE GAIN

Gain of 10 is achieved simply by leaving the two gain pins (1 and 8) open. Gain of 50 is achieved by connecting the gain pins together directly. In the  $G = 10$  configuration, the gain error is less than 0.4%. In the  $G = 50$  configuration, the gain error is less than 0.8%.

Gain can be set to any value between 10 and 50 by connecting a resistor  $R_G$  between the gain pins according to the following equation:

$$10 + 400k\Omega / (10k\Omega + R_G) \quad (1)$$

This is demonstrated in Figure 1 and is shown with the commonly used gains and resistor  $R_G$  values. However, because the absolute value of internal resistors is not guaranteed, using the INA156 in this configuration will increase the gain error and gain drift with temperature, as shown in Figure 3.

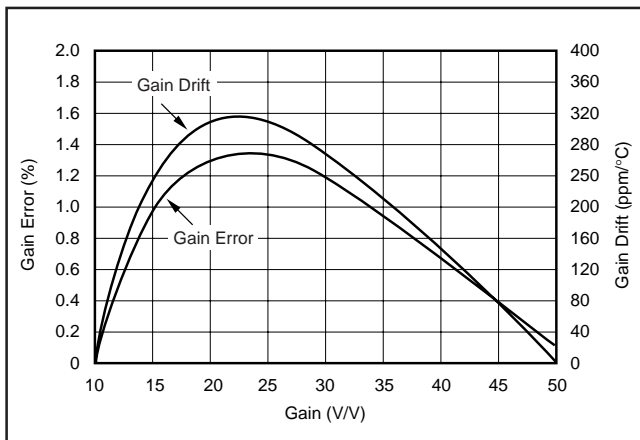


FIGURE 3. Typical Gain Error and Gain Error Drift with External Resistor.

## OFFSET TRIMMING

Offset voltage can be adjusted by applying a correction voltage to the reference terminal. Figure 4 shows an optional circuit for trimming the output offset voltage. The voltage applied to the Ref terminal is added to the output signal. An op amp buffer is used to provide low impedance at the Ref terminal to preserve good common-mode rejection.

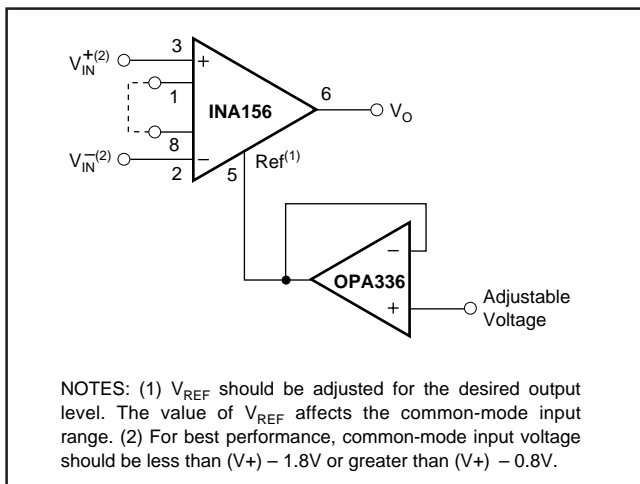


FIGURE 4. Optional Trimming of Output Offset Voltage.

## INPUT BIAS CURRENT RETURN

The input impedance of the INA156 is extremely high—approximately  $10^{13}\Omega$ , making it ideal for use with high-impedance sources. However, a path must be provided for the input bias current of both inputs. This input bias current is less than 10pA and is virtually independent of the input voltage.

Input circuitry must provide a path for this input bias current for proper operation. Figure 5 shows various provisions for an input bias current path. Without a bias current path, the inputs will float to a potential that exceeds the common-mode range and the input amplifier will saturate.

If the differential source resistance is low, the bias current return path can be connected to one input (see the thermocouple in Figure 5). With higher source impedance, using two equal resistors provides a balanced input with advantages of lower input offset voltage due to bias current and better high-frequency common-mode rejection.

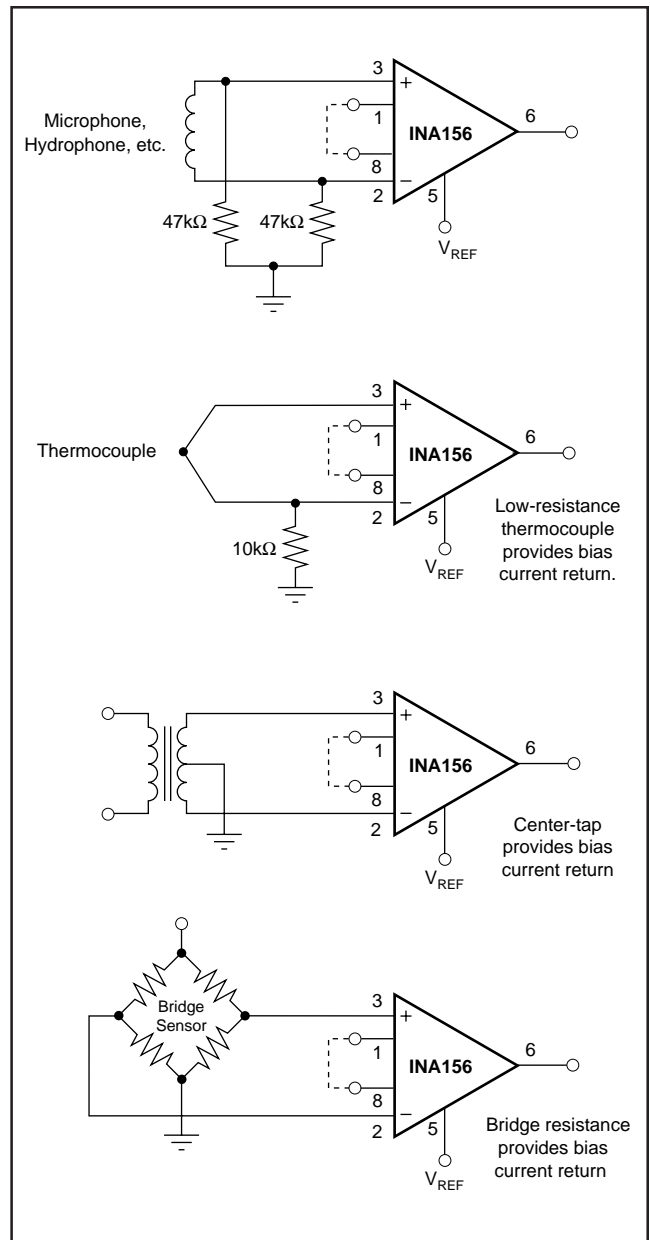


FIGURE 5. Providing an Input Common-Mode Current Path.

## INPUT COMMON-MODE RANGE

The input common-mode range of the INA156 for various operating conditions is shown in the Typical Performance Curves. The common-mode input range is limited by the output voltage swing of A1, an internal circuit node. For the  $G = 10$  configuration, output voltage of A1 can be expressed as:

$$V_{OUTA1} = -1/9 V_{REF} + (1 + 1/9) V_{IN-} \quad (2)$$

The input common-mode voltage range can be calculated using this equation, given that the output of A1 can swing to within 20mV of either rail. When the input common-mode range is exceeded (A1's output is saturated), A2 can still be in linear operation and respond to changes in the non-inverting input voltage. However, the output voltage will be invalid.

The common-mode range for the  $G = 50$  configuration is included in the typical performance curve, "Input Common-Mode Range vs Output Voltage."

## INPUT RANGE FOR BEST ACCURACY

The internal amplifiers have rail-to-rail input stages, achieved by using complementary n-channel and p-channel input pairs. The common-mode input voltage determines whether the p-channel or the n-channel input stage is operating. The transition between the input stages is gradual and occurs between  $(V+) - 1.8V$  to  $(V+) - 1V$ . Due to these characteristics, operating the INA156 with input voltages within the transition region of  $(V+) - 1.8V$  to  $(V+) - 0.8V$  results in a shift in input offset voltage, and reduced common-mode and power supply rejection performance. Typical patterns of the offset voltage change throughout the input common-mode range are illustrated in Figure 6. The INA156 can be operated below or above the transition region with excellent results. Figure 7 demonstrates the use of the INA156 in a single-supply, high-side current monitor. In this application, the INA156 is operated above the transition region.

## RAIL-TO-RAIL OUTPUT

A class AB output stage with common-source transistors is used to achieve rail-to-rail output. For resistive loads greater than  $10k\Omega$ , the output voltage can swing to within a few millivolts of the supply rail while maintaining low gain error. For heavier loads and over temperature, see the typical performance curve "Output Voltage Swing vs Output Current." The INA156's low output impedance at high frequencies makes it suitable for directly driving Capacitive Digital-to-Analog (CDAC) input A/D converters, as shown in Figure 9.

## INPUT PROTECTION

Device inputs are protected by ESD diodes that will conduct if the input voltages exceed the power supplies by more than 500mV. Momentary voltages greater than 500mV beyond the power supply can be tolerated if the current on the input pins is limited to 10mA. This is easily accomplished with input resistors  $R_{LIM}$ , as shown in Figure 8. Many input signals are inherently current-limited to less than 10mA. Therefore, a limiting resistor is not required.

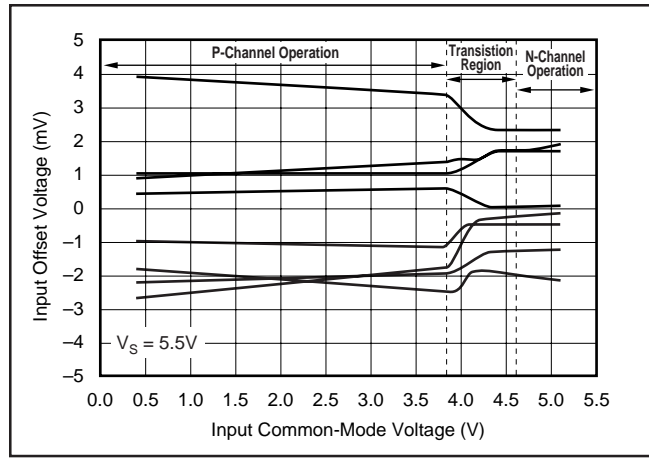


FIGURE 6. Input Offset Voltage Changes with Common-Mode Voltage.

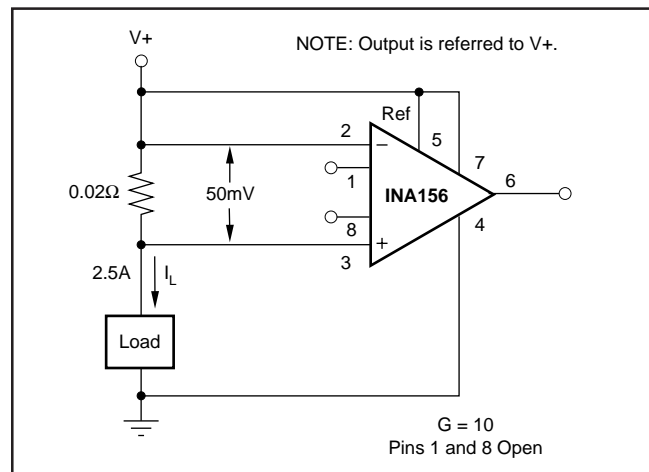


FIGURE 7. Single-Supply, High-Side Current Monitor.

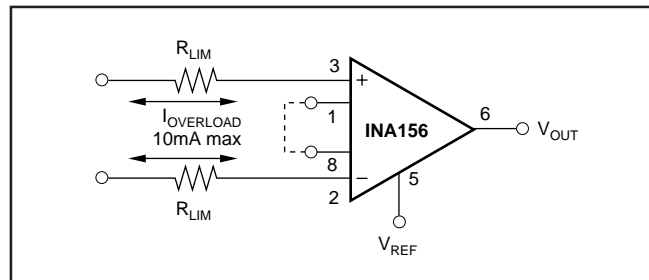


FIGURE 8. Input Current Protection for Voltages Exceeding the Supply Voltage.

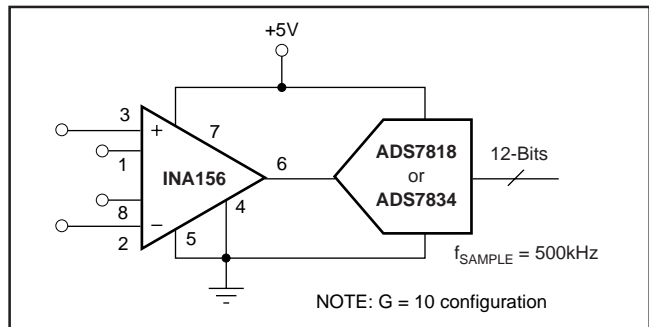


FIGURE 9. Driving Capacitive-Input A/D Converter.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA156EA/250	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	A56	<a href="#">Samples</a>
INA156EA/250G4	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	A56	<a href="#">Samples</a>
INA156EA/2K5	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR		A56	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA156EA/250	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA156EA/2K5	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA156EA/250	VSSOP	DGK	8	250	210.0	185.0	35.0
INA156EA/2K5	VSSOP	DGK	8	2500	367.0	367.0	35.0

## IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.