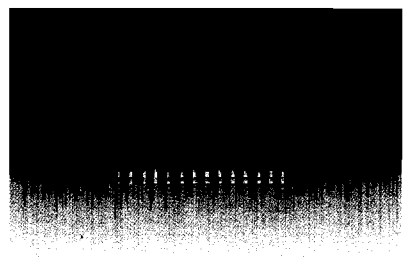
## AK5340/A/B

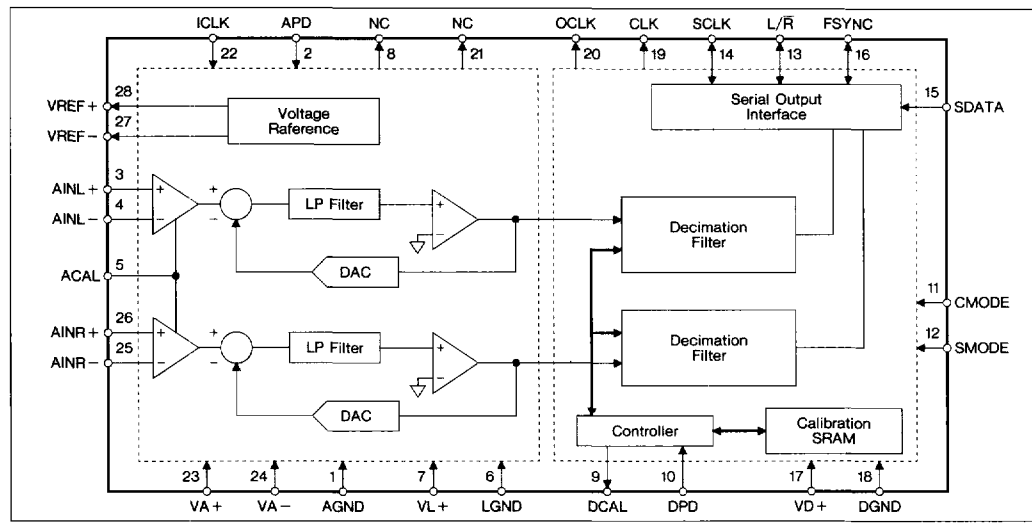
### 18bit ADC



28pin SOP (7.5×18.7×2.2mm)

① +5V Single Supply 18 bit 2ch A/D Converter
② 5th Order Delta-Sigma A/D Converter
③ On-chip Digital Anti-Alias Filter
④ On-chip S/H circuitry and Voltage Reference
⑤ 64 X over sampling
⑥ 2ch Simultaneous Sampling
⑦ Single End Inputs available
⑧ Sampling Rate: max. 50kHz (AK5340/B)
max. 98kHz (AK5340A)
⑨ S/N: 96dB (AK5340/A)
100dB (AK5340B)
⑩ Linear Phase Digital Filter
- Passband: 0 to 22kHz
- Passband ripple: 0.01dB
- Stopband attenuation: 88dB

⑪ Low Power Dissipation: 125mW (AK5340/B)
210mW (AK5340A)
⑫ Package: 28 pin SOP




AK5340/A/B BLOCK DIAGRAM

## AKD5340

### AK5340/A/B Evaluation Board

The AKD5340 is an evaluation board for the AK5340/A/B digital audio 16/18bit A/D converters. The AKD5340 includes the input buffer circuit and also has a digital interface transmitter. Further, the AKD5340 can evaluate direct interface with AKD4328, AKD4303, AKD4310, AKD4311, AKD4320 and AKD4319.
The AKD5340 has an SOP socket (Matsushita Electric Works, AXS628319) for AK5340/A/B which enables easier to change device.

① On-board differential input buffer circuit
② On-board clock generator
③ Compatible with 2 types of interface
- Direct interface with AKD4328, AKD4303, AKD4310, AKD4311, AKD4320 and AKD4319.
- On-board CS8402 as DIT which transmits optical output.

④ BNC connector for an external clock input.

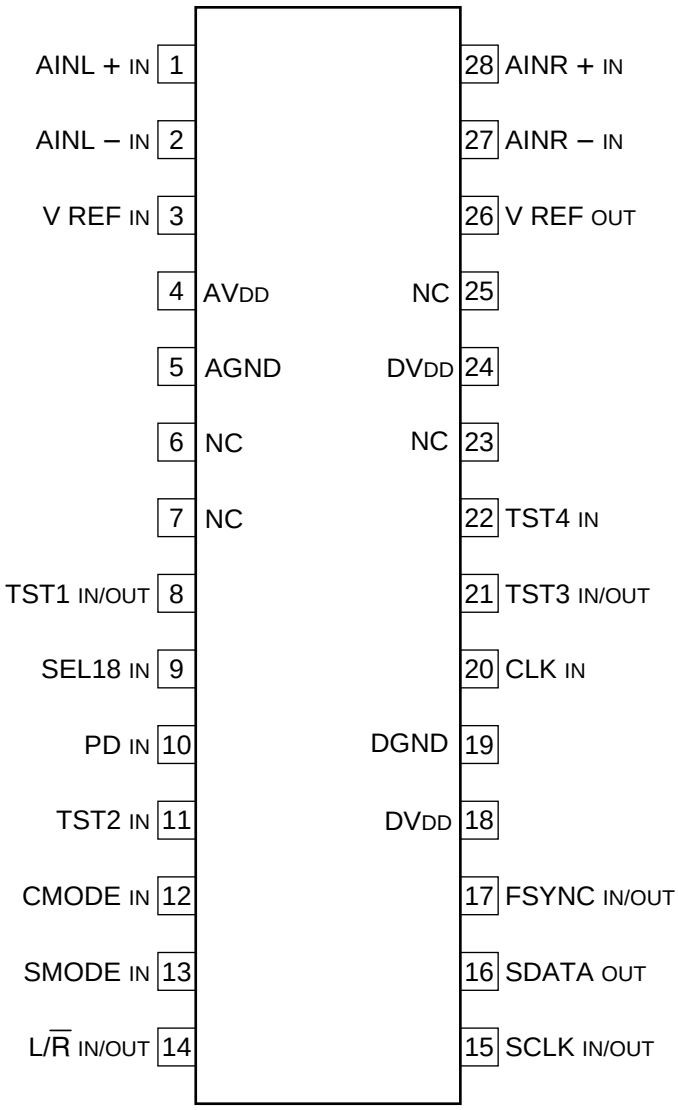
## AK5343

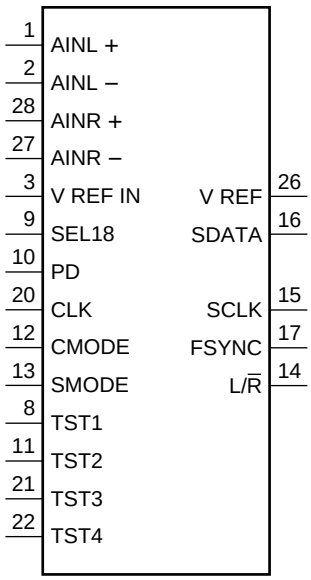
### 16bit ADC

① +3.3V single supply 16 bit 2ch A/D Converter
② 4th Order Delta-Sigma A/D Converter
③ On-chip Digital Anti-Alias Filter
④ On-chip S/H circuitry and Voltage Reference
⑤ 64 X over sampling
⑥ 2ch Simultaneous Sampling
⑦ S/N: 91dB
⑧ Serial Interface
⑨ Low Power Dissipation: 100mW
⑩ Low Voltage Operation: +3.0V to +3.6V
⑪ Compatible with AK5344 & AK5345
⑫ Package: 28 pin SOP (7.5×18.7×2.2mm)

# C-MOS 18-BIT 2 CHANNEL A/D CONVERTER

—TOP VIEW—




AVDD, AGND : FOR ANALOG BLOCK
DVDD, DGND : FOR DIGITAL BLOCK

**INPUT**

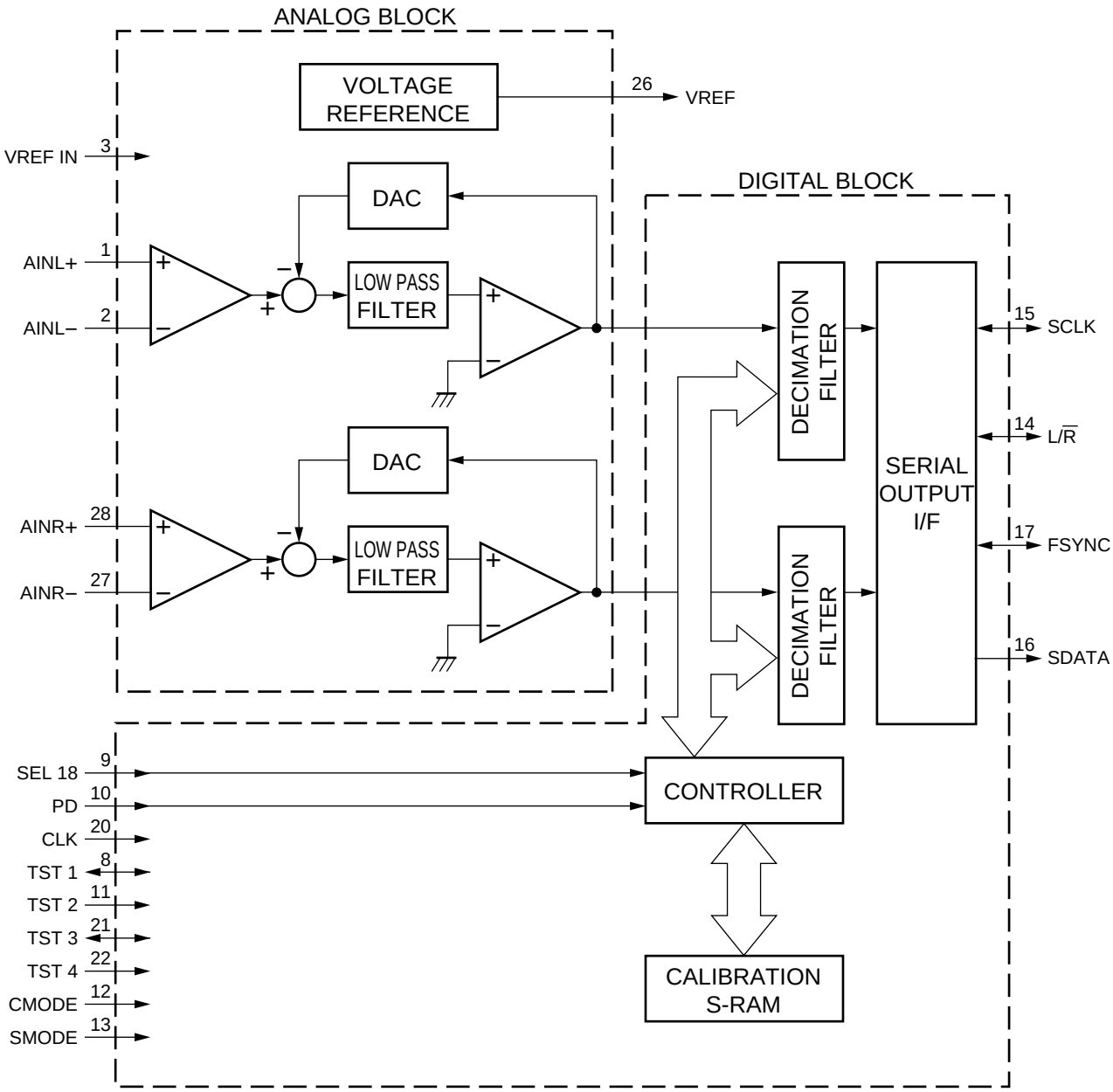
| | | |
|---|---|---|
| AINL + | ; | L-CH ANALOG POSITIVE INPUT |
| AINL – | ; | L-CH ANALOG NEGATIVE INPUT |
| AINR + | ; | R-CH ANALOG POSITIVE INPUT |
| AINR – | ; | R-CH ANALOG NEGATIVE INPUT |
| CLK | ; | MASTER CLOCK<br>(CMODE = H : 384 fs)<br>(CMODE = L : 256 fs) |
| CMODE | ; | MASTER CLOCK SELECT<br>(L : CLK = 256 fs, 12.288 MHz @fs = 48 kHz)<br>(H : CLK = 384 fs, 18.432 MHz @fs = 48 kHz) |
| PD | ; | POWER DOWN FOR DIGITAL SECTION |
| SEL 18 | ; | 18/16 BIT SELECT (L : 16-BIT, H : 18-BIT) |
| SMODE | ; | INTERFACE CLOCK SELECT<br>(L : SUB MODE)<br>(H : MASTER MODE) |
| TST 2, 4 | ; | TEST |
| V REF IN | ; | REFERENCE VOLTAGE |

**OUTPUT**

| | | |
|---|---|---|
| SDATA | ; | SERIAL DATA |
| V REF | ; | REFERENCE VOLTAGE (–2.5V) |

**INPUT/OUTPUT**

| | | |
|---|---|---|
| FSYNC | ; | FRAME SYNC CLOCK<br>(SUB MODE : FSYNC INPUT)<br>(MASTER MODE : FSYNC OUTPUT) |
| L/$\overline{R}$ | ; | INPUT CHANNEL SELECT<br>(SUB MODE : fs CLK INPUT)<br>(MASTER MODE : fs CLK OUTPUT) |
| SCLK | ; | SERIAL DATA CLOCK<br>(SUB MODE : SCLK INPUT)<br>(MASTER MODE : SCLK OUTPUT) |
| TST 1, 3 | ; | TEST |


ANALOG BLOCK
VOLTAGE REFERENCE
26
VREF
VREF IN
3
DAC
DIGITAL BLOCK
AINL+
1
AINL–
2
LOW PASS FILTER
DECIMATION FILTER
SERIAL OUTPUT I/F
15
SCLK
14
L/R
DAC
AINR+
28
AINR–
27
LOW PASS FILTER
DECIMATION FILTER
17
FSYNC
16
SDATA
SEL 18
9
PD
10
CLK
20
TST 1
8
TST 2
11
TST 3
21
TST 4
22
CMODE
12
SMODE
13
CONTROLLER
CALIBRATION S-RAM