USB 2.0 Video / Audio Class PC Camera Controller SN9C259BFG Datasheet

Released Version: v1.01

Revision	Date	Description	Adult
1.00	2010-04-22	Update standby current and THD+N result	Ocean
0.02	2010-02-04	Add SN9C259BFG pin assignment	Ocean
0.01	2010-01-26	Initial draft	Ocean
Apply to	SN9C259BFG		

Table of Contents

1 General Description

SN9C259BFG is a USB 2.0 compatible PC Camera controller. The built-in extreme low-power transceiver provides the superior compatibility with various USB host and the best quality for image applications. It is fully compliant with USB Video and Audio Class. With the integrated sensor interface and color processing engine, it can support up to QXGA CMOS SOC sensors.

SN9C259BFG integrates 2 voltage regulators for sensor power. One is 3.3V-to-2.8V for sensor's analog parts. The other one is 3.3V-to-1.9V for sensor's core power. These build-in regulators can help saving BOM cost and PCB area.

SN9C259BFG is controlled by the embedded micro-controller. The flexible architecture is consisted of mask ROM, internal RAM and external serial-flash which can store the customized codes and parameters. It's also possible to store all the program code in the external flash memory for customized design purpose. With the highly-integrated firmware architecture and the developing kit provided by SONiX, it's easy for 3rd party to integrate a new type of CMOS sensor and GPIO definition for variant board configuration.

2 Features

2.1 System

- 3.3V single power supply, 1.8V Core (generated by internal regulator)，1.8V and 3.3V I/O power
- Extreme low power consumption, < 49mA when standby and < 400uA when suspend (Power consumption of sensor is not included，audio enable)
- Built-in PLL for internal clock generation with input crystal frequency of 12MHz
- Using external serial flash to store customized code and data
- No external RAM needed
- 1.9V and 2.8V output power pin to supply CMOS sensor power need
- LQFP48 package is available; please see later section for more detail

2.2 USB Controller

- USB 2.0 compatible
- USB Video Class 1.1 compliant
- USB2.0 HS/FS auto sense and switch
- USB FS mode and USB disconnection are programmable
- 5 endpoints: CONTROL pipe, 2 Interrupt IN and 2 Isochronous-IN (Video in and Audio in)
- 6 alternate settings for Video Streaming Interface

2.3 Sensor Interface

- Support VGA、SXGA、UXGA and QXGA CMOS ISP sensor
- Raw Bypass Mode（LQFP48：RAW-10 / RAW-8，），requires SONIX driver
- MJPG Bypass Mode and support MJPEG Header output from ASIC
- Support YUY2 image data format from sensor
- Up to 48Mhz output clock for clock request of CMOS sensor silicon.
- Up to 96Mhz pixel clock is acceptable
- Support industrial standard 2-wire serial interface for sensor control
- Support two sensor modes of PCK synchronization and Buffer synchronization

2.4 Image Processing

- Configurable windowing function after sensor output

2.5 Color processing

- AF edge statistics
- Programmable gamma table for Y channel

- Configurable windowing function after processed image

2.6 Scaling Engine

- 1/2, 1/4 smooth scaling on Y/Cb/Cr
- 3/5 second linear scaling for VGA input

2.7 Video / Still Image

- Output video / still image format:
  - USB Video Class Uncompressed YUY2 payload (16bits/pixel)
- Video streaming up to 30fps@VGA or 3.5fps@QXGA at USB2.0 high-speed mode
- Still Image capturing support UVC still image capture method 0/1/2

2.8 Frame rate

- Frame rate considering USB bandwidth limitation

Normal Resolution @ USB High-Speed								
Output format	QXGA	UXGA	SXGA	SVGA	VGA	CIF	QVGA	QCIF
YUY2	3.5fps	6fps	9fps	25fps	30fps	30fps	60fps	60fps
MJPEG	14fps	30fps	30fps	30fps	120fps	120fps	120fps	120fps

Normal Resolution @ USB Full-Speed								
Output format	QXGA	UXGA	SXGA	SVGA	VGA	CIF	QVGA	QCIF
YUY2	<1fps	<1fps	<1fps	1fps	1.5fps	4.5fps	6.5fps	19.5fps
MJPEG	1fps	2fps	3fps	10fps	15fps	30fps	30fps	30fps

- Frame rate considering sensor characteristic

  The maximum frame rate is limited by how many frame per second that sensor can output under 48MHz pixel clock and is limited on High-Speed USB ISO bandwidth 24MB/s

2.9 Audio

- USB Audio Class 1.0 standard compliant
- Programmable audio sampling frequency: 8, 11.025, 16, 22.05, 24, 44.1 and 48 kHz
- Build-In one channel 16 bits ADC
- 16-bit PCM format output to UAC
- Audio performance
  - gain = 0dB: SNR = 74dB, THD+N = 0.021% (input is -3dB)
  - gain = 52.5dB: SNR = 46dB, THD+N = 0.5% (input is -54dB, about 2mV)
- PGA gain range from -12dB to 33dB at 3dB step
- MIC BOOST gain range from 0~30dB and 4 steps

- Digital volume control / mute: -78dB…0dB

2.10 GPIO

- 3 GPIOs are available, predefined as LED、snapshot button and sensor reset pin

2.11 Micro Controller and USB Device Features

- Built-in 8032 micro controller with 3K bytes data memory, and maximum CPU clock rate is 24MHz
- Total 64K bytes mask ROM and 4K bytes programmable SRAM
- Load extended 18KB F/W from external serial flash.
- Load VID/PID, manufacturer, product and serial number string from external serial flash.
- Load UVC parameter definition from external serial flash.
- F/W is upgradeable from PC
- Force USB at FS mode / Force USB disconnect
- Interrupt at the end of H/W windowing
- CPU watch dog

2.12 Pre-Defined for USB Video Class

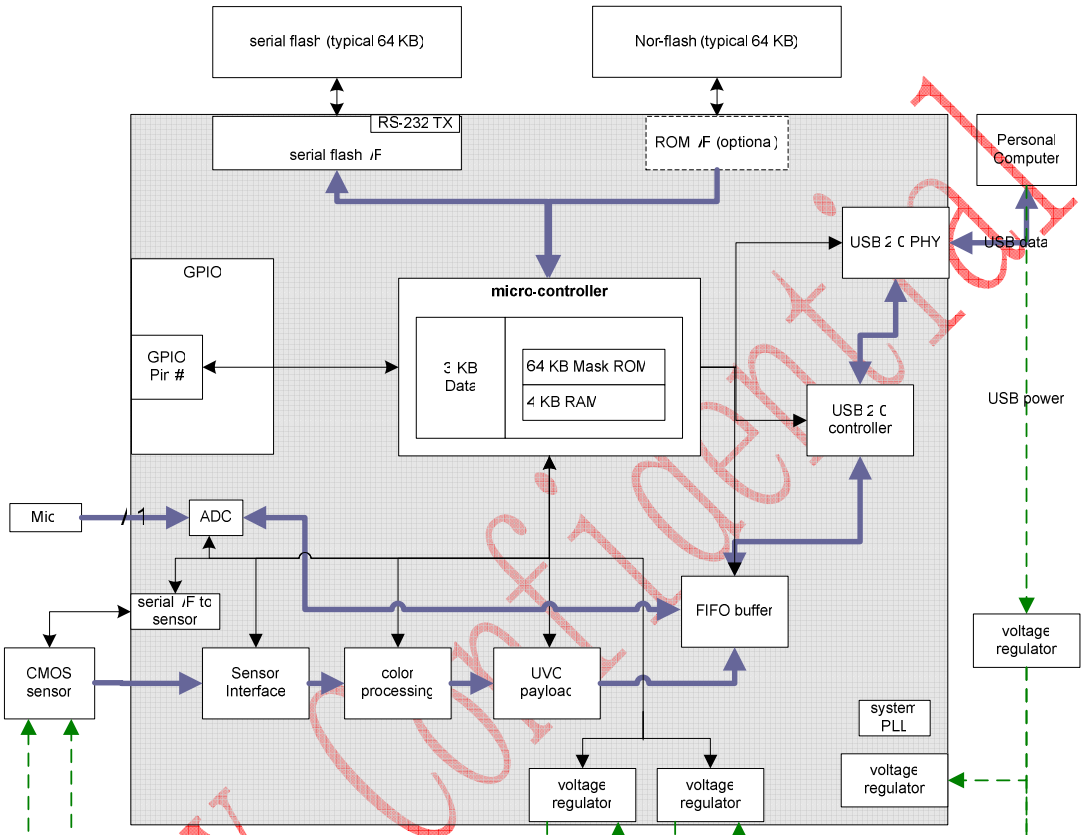
- Brightness control (UVC defined)
- Contrast control (UVC defined)
- Hue control (UVC defined)
- Saturation control (UVC defined)
- Sharpness control (UVC defined)
- Gamma control (UVC defined)
- Privacy control (UVC defined)
- Image auto-flip control triggered by GPIO
- LED indicator on video streaming
- Extension unit support

2.13 Platform Support

- Microsoft Windows XP 32bit SP2, Microsoft Windows XP 64bit, Microsoft Windows Vista 32bit, Microsoft Windows Vista 64bit, Microsoft Windows 7 32bit, Microsoft Windows 7 64bit
- Mac - OS X 10.4.8 or later
- Linux with UVC driver (open source available at http://linux-uvc.berlios.de/)

3 Function Block Diagram

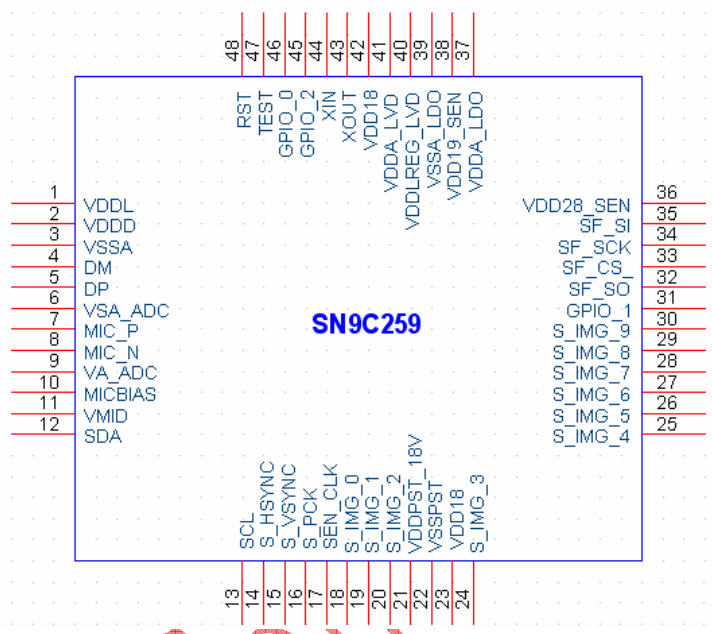
3.1 Block Diagram



4 Pin Assignment

4.1 LQFP48

4.1.1 Pin-out Diagram



4.1.2 Pin Description

Pin No	Mnemonic	DIR			Current	Description
		Power up	Normal	Suspend		
1	VDDL	P	P	P		1.8v digital PWR
2	VDDD	P	P	P		3.3v digital PWR for USB receiver
3	VSSA	P	P	P		Analog GND for PLL/USB receiver
4	DM	A	A	A		D- for USB
5	DP	A	A	A		D+ for USB
6	VSA_ADC	P	P	P		0V analog core ground
7	MIC_P	I	I	I		Microphone differential input, positive
8	MIC_N	I	I	I		Microphone differential input, negative
9	VA_ADC	P	P	P		3.3V analog core power
10	MICBIAS	P	P	P		Microphone bias output
11	VMID	P	P	P		MID reference voltage

12	SDA	I	B	F	4mA	SDA for I2C interface(data)
13	SCL	I	B	F	4mA	SCL for I2C interface(clock)
14	S_HSYNC	I	I	I	4mA	Sensor hsync
15	S_VSYNC	I	I	I	4mA	Sensor vsync
16	S_PCK	I	I	I	4mA	Sensor pixel clock
17	SEN_CLK	OU	O	F	12mA	Sensor clock
18	S_IMG_0	I	I	I	4mA	Sensor image data
19	S_IMG_1	I	I	I	4mA	Sensor image data
20	S_IMG_2	I	I	I	4mA	Sensor image data
21	VDDPST _18V	P	P	P		Sensor interface I/O power. Connect to 3.3V will be 3.3V sensor interface. Connect to 1.8V will be 1.8V sensor interface.
22	VSSPST	P	P	P		Ground
23	VDD18	P	P	P		Digital core power 1.8V
24	S_IMG_3	I	I	I	4mA	Sensor image data
25	S_IMG_4	I	I	I	4mA	Sensor image data
26	S_IMG_5	I	I	I	4mA	Sensor image data
27	S_IMG_6	I	I	I	4mA	Sensor image data
28	S_IMG_7	I	I	I	4mA	Sensor image data
29	S_IMG_8	I	I	I	4mA	Sensor image data
30	S_IMG_9	I	I	I	4mA	Sensor image data
31	GPIO_1	I	B	F	4mA	General purpose I/O
32	SF_SO	OL	O	OL	4mA	Serial flash data out
33	SF_CS_	OH	O	F	8mA	Serial flash chip select
34	SF_SCK	OL	O	OL	4mA	Serial flash clock output
35	SF_SI	I	I	I	4mA	Serial flash data in
36	VDD28_SEN	P	P	P		Sensor power 2.8v output
37	VDDA_LDO	P	P	P		Internal sensor LDO input, 3.3v
38	VDD19_SEN	P	P	P		Sensor power 1.9v output
39	VSSA_LDO	P	P	P		Ground
40	VDDLREG_LVD	P	P	P		USB and digital core power 1.8v, internal LDO output
41	VDDA_LVD	P	P	P		Internal 1.8V LDO input, 3.3V
42	VDD18	P	P	P		Digital core power
43	XOUT	O	O	O		OSC output
44	XIN	I	I	I		OSC input XIN=12/24MHz at XTAL_SEL= 0/1

						Default setting : XTAL_SEL= 0 —> XIN=12MHz
45	GPIO_2	I	B	F	4mA	General purpose I/O
46	GPIO_0	I	B	F	8mA	General purpose I/O
47	TEST	I	I	I	4mA	Test mode
48	RST	I	I	I		Chip reset

Direction denotation:

O	Output	OU	Output unknown	OH	Output high	OL	Output low
I	Input	B	Bi-direction	F	Firmware control		
A	Analog	P	Power				

5 Electrical Characteristics

5.1 DC operating Condition

5.1.1 Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
VDD33	Power Supply	-0.3 ~ 3.6	V
VDD18	Power Supply	-0.18 ~ 1.98	V
Vin	Input Voltage	-0.3 ~ VDD33 + 0.3	V
Vout	Output Voltage	-0.3 ~ VDD33 + 0.3	V

5.1.2 Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
VDD33	Power Supply	3.0	3.3	3.6	V
VDD18	Power Supply	1.62	1.8	1.98	V
Vin	Input voltage	0		VDD33	V
Topr	Operating Temperature	0		70	℃

5.1.3 DC Electrical Characteristics

(Under Recommended Operating Conditions and VDD33=3.0 ~ 3.6V, Tj=0 to +70 ℃)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Vil	Input low voltage	TTL	-0.3		0.8	V
Vih	Input high voltage	TTL	2.0		VDD33+0.3	V
Iil	Input low current	no pull-up or pull-down	-1		1	μA
Iih	Input high current	no pull-up or pull-down	-1		1	μA
Ioz	Tri-state leakage current		-1		1	μA
Vol	Output Low voltage	Iol=4mA / 8mA			0.4	V
Voh	Output high voltage	Ioh=4mA / 8mA	2.4			V
Cin	Input capacitance			10		pF
Cout	Output capacitance			10		pF
Cbid	Bi-directional buffer Capacitance			10		pF
Rpu	Pull-up resistor			70K		Ω
Rpd	Pull-down resistor			70K		Ω

5.1.4 Low Dropout Regulator Electrical Characteristics

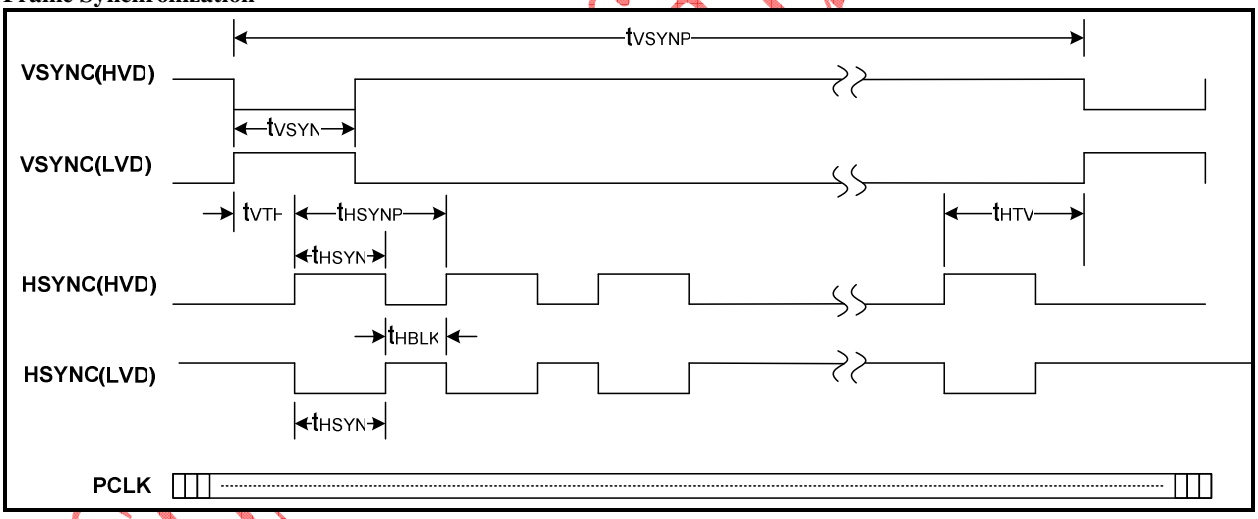
(Under Recommended Operating Conditions and VDD33=3.0 ~ 3.6V, Tj=0 to +70 ℃)

Symbol	Parameter	Min	Typ	Max	Units
VDDA1	Power Supply for 2.80V LDO	3.0		3.6	V
VO280	Voltage output of 2.80V LDO		2.8V±7%		V
IO280	Output current capacity of 2.80V LDO			60	mA
VDD33	Power Supply for 1.90V LDO	3.0		3.6	V
VO190	Voltage output of 1.90V LDO		1.9V±10%		V
IO190	Output current capacity of 1.90V LDO			60	mA
PSRR	52db (Io=60mA / Co=10uF；f=1kHz)				

5.2 AC operating Condition

5.2.1 Sensor Interface

Frame Synchronization



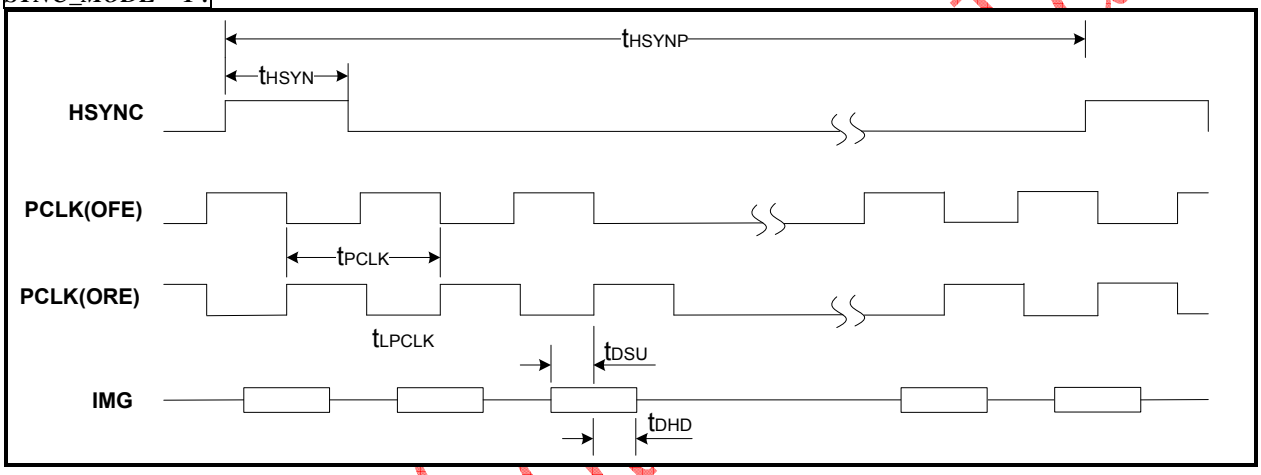
Parameter	Symbol	Min.	Typ.	Max.	Unit
VSYNC pulse width	t_{VSYNC}	t_{PCLK}	-	-	ns
VSYNC to HSYNC	t_{VTH}	t_{PCLK}	-	-	ns
HSYNC pulse width	t_{HSYN}	t_{PCLK}	-	-	ns

Blank time between two HSYNC	t_{HBLK}	t_{PCLK}	-	-	ns
HSYNC to VSYNC	t_{HTV}	t_{HSYNP}			ns

Note:
1. t_{SENCK} is period of internal clock for sensor post processing.
2. t_{HSYNP} is period of Hsync, t_{VSYNP} is period of Vsync.
3. HVD (High Valid), LVD (Low Valid).

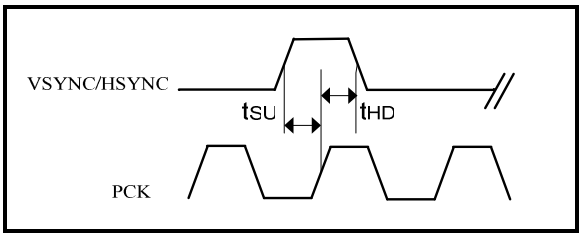
Data Synchronization

SYNC_MODE = 1 :



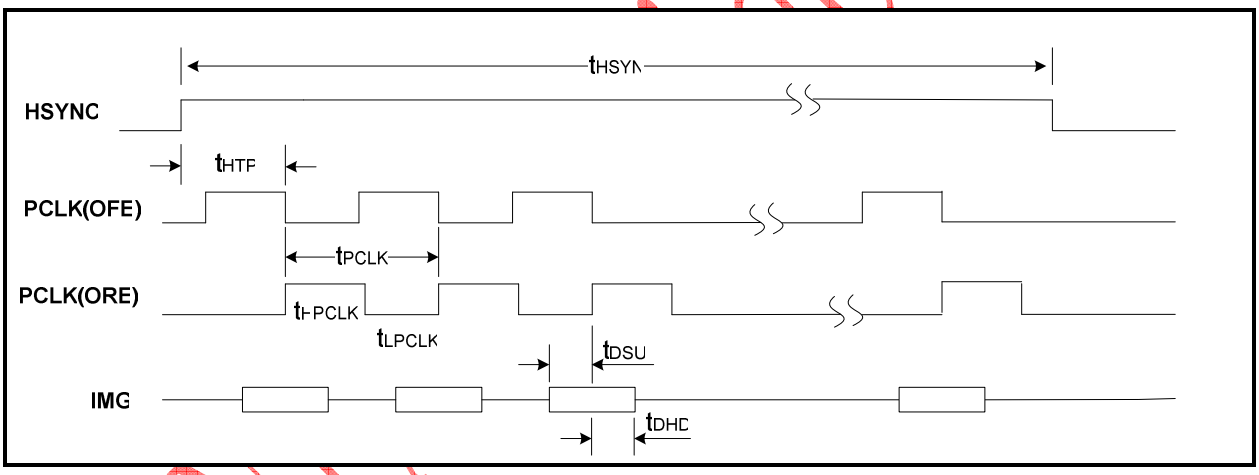
Parameter	Symbol	Min.	Typ.	Max.	Unit
HSYNC pulse width	t_{HSYN}	t_{PCLK}	-	-	ns
PCLK Low Pulse Width	t_{LPCLK}	2	-	-	ns
PCLK High Pulse Width	t_{HPCLK}	2	-	-	ns
Frequency of pixel clock (YUV Mode)	f_{PCLK}	-	-	96	MHz
Image data setup time	t_{DSU}	2	-	-	ns
Image data hold time	t_{DHD}	2	-	-	ns

Note:
1. t_{SENCK} is period of internal clock for sensor post processing
2. ORE (On Rising Edge) means the timing act on rising edge
3. OFE (On Falling Edge) means the timing act on falling edge



Parameter	Symbol	Min.	Typ.	Max.	Unit
VSYNC / HSYNC setup time	t_{SU}	2	-	-	ns
VSYNC / HSYNC hold time	t_{HD}	2	-	-	ns

SYNC_MODE = 0 :

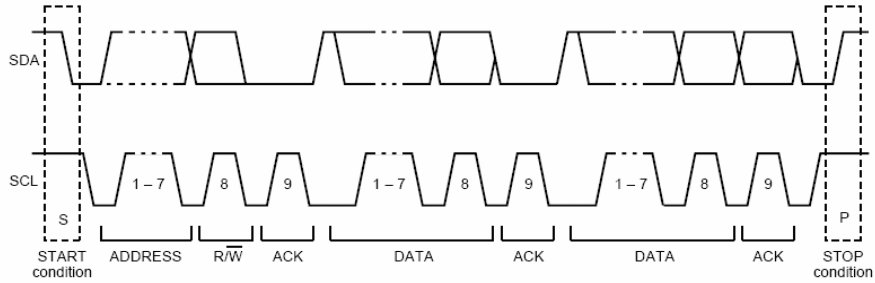


Parameter	Symbol	Min.	Typ.	Max.	Unit
HSYNC pulse width	t_{HSYN}	HSIZE * t_{PCLK}	-	-	ns
HSYNC to PCLK	t_{HTP}	t_{SENCK}	-	-	
PCLK Low Pulse Width	t_{LPCLK}	2	-	-	ns
PCLK High Pulse Width	t_{HPCLK}	2	-	-	ns
Frequency of pixel clock (YUV Mode)	f_{PCLK}	-	-	96	MHz
Image data setup time	t_{DSU}	2	-	-	ns
Image data hold time	t_{DHD}	2	-	-	ns

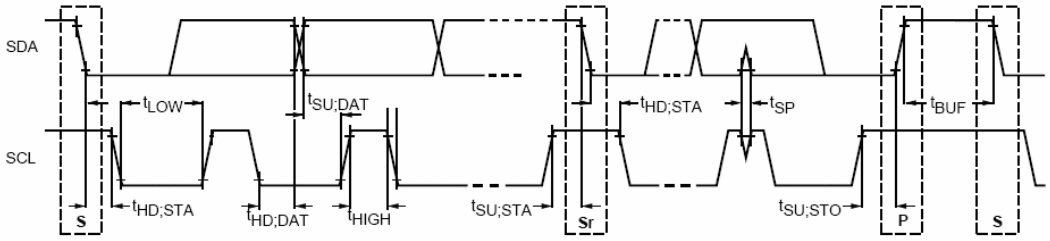
Note:

1. t_{SENCK} is period of internal clock for sensor post processing
2. ORE (On Rising Edge) means the timing act on rising edge
3. OFE (On Falling Edge) means the timing act on falling edge
4. HSIZE represents total valid PCLK number per horizontal line

5.2.2 Sensor Control Interface



A complete data transfer.

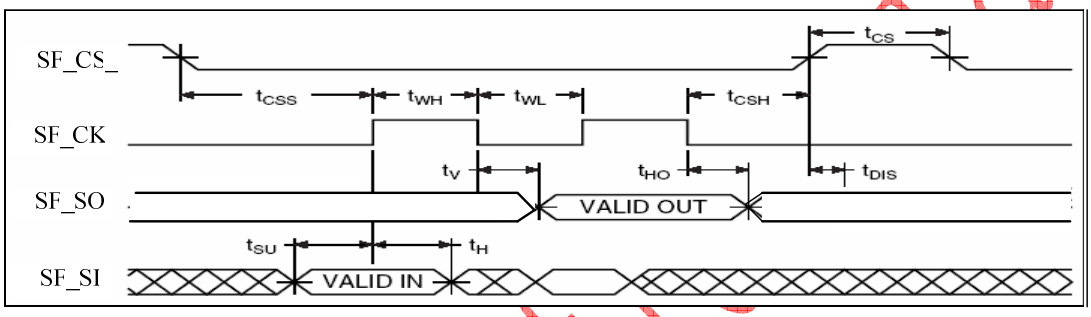


Definition of timing for F/S-mode devices on the I^2C-bus.

Parameter	Symbol	Standard mode			Fast mode			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	-	98.7	-	-	394.7	-	kHz
Hold time START condition	$t_{HD;STA}$	-	5067	-	-	1267	-	ns
LOW period of the SCL clock	t_{LOW}	-	5067	-	-	1267	-	ns
HIGH period of the SCL clock	$t_{HD;STA}$	-	5067	-	-	1267	-	ns
Setup time for a repeated	$t_{SU;STA}$	-	5067	-	-	1267	-	ns

START condition								
Data hold time: Write	$t_{HD:DAT}$	-	2533	-	-	633	-	ns
Data hold time: Read	$t_{HD:DAT}$	10	-	-	10	-	-	ns
Data setup time: Write	$t_{SU:DAT}$	-	2533	-	-	633	-	ns
Data setup time: Read	$t_{SU:DAT}$	10	-	-	10	-	-	ns
Setup time for STOP condition	$t_{SU:STO}$	-	5066	-	-	1267	-	ns
Bus free time between a STOP and START condition	t_{BUF}	4.8	-	-	1.4	-	-	us

5.2.3 Serial Flash Interface



When f_{SCK} = 24 Mhz (SPEED=1)

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCK clock frequency	f_{SCK}	-	24	-	MHz
Chip Select low to SF_CK Edge	t_{CSS}	36		-	ns
SF_CK Edge to Chip Select High	t_{CSH}	36		-	ns
Chip High period	t_{CS}	41.67		-	ns
Clock high period	t_{WH}	20.83	-	-	ns
Clock low period	t_{WL}	20.83	-	-	ns
Input Data setup time	t_{SU}	10	-	-	ns
Input Data hold time	t_H	10	-	-	ns
Output Data Valid time @ CL=20pF	t_V	-	-	5	ns
Output Data Hold time @ CL=20pF	t_{HO}	36	-	-	ns

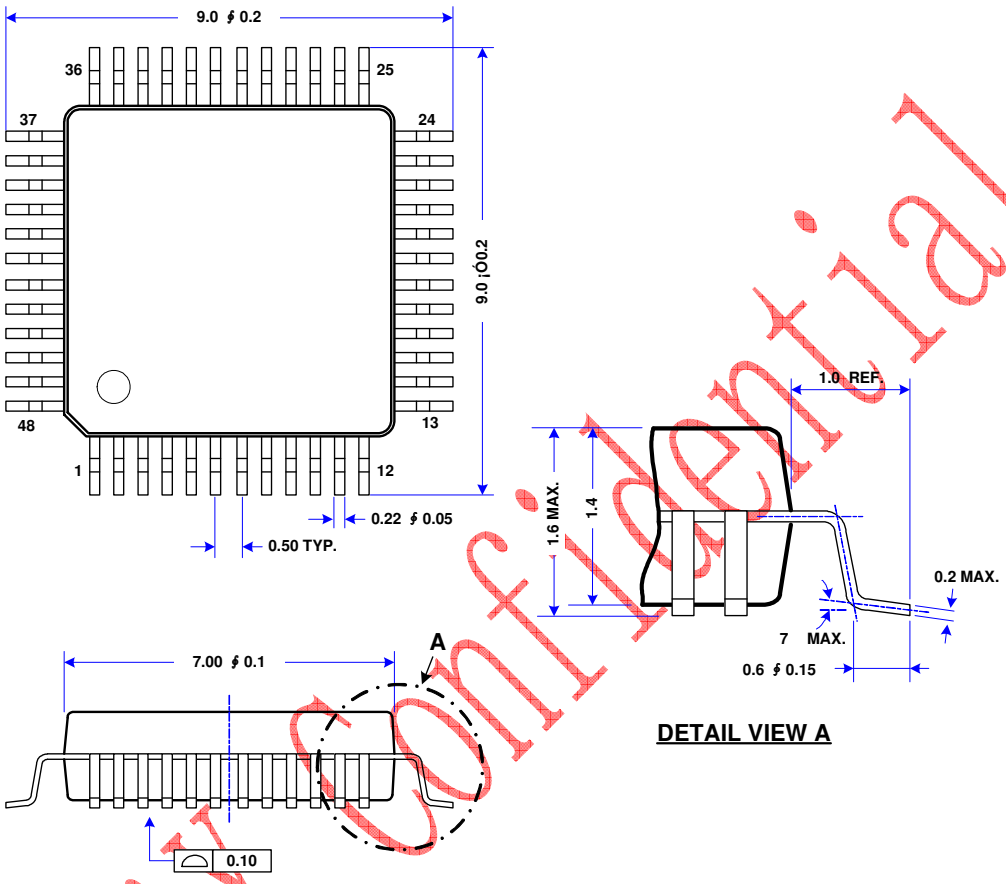
When f_{SCK} = 12 Mhz (SPEED=3)

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCK clock frequency	f_{SCK}	-	12	-	MHz
Chip Select low to SF_CK Edge	t_{CSS}	36	-	-	ns
SF_CK Edge to Chip Select High	t_{CSH}	36	-	-	ns
Chip High period	t_{CS}	41.67	-	-	ns

Clock high period	t_{WH}	41.67	-	-	ns
Clock low period	t_{WL}	41.67	-	-	ns
Input Data setup time	t_{SU}	10	-	-	ns
Input Data hold time	t_{H}	10	-	-	ns
Output Data Valid time @ CL=20pF	t_{V}	-	-	5	ns
Output Data Hold time @ CL=20pF	t_{HO}	78	-	-	ns

6 Package Dimensions

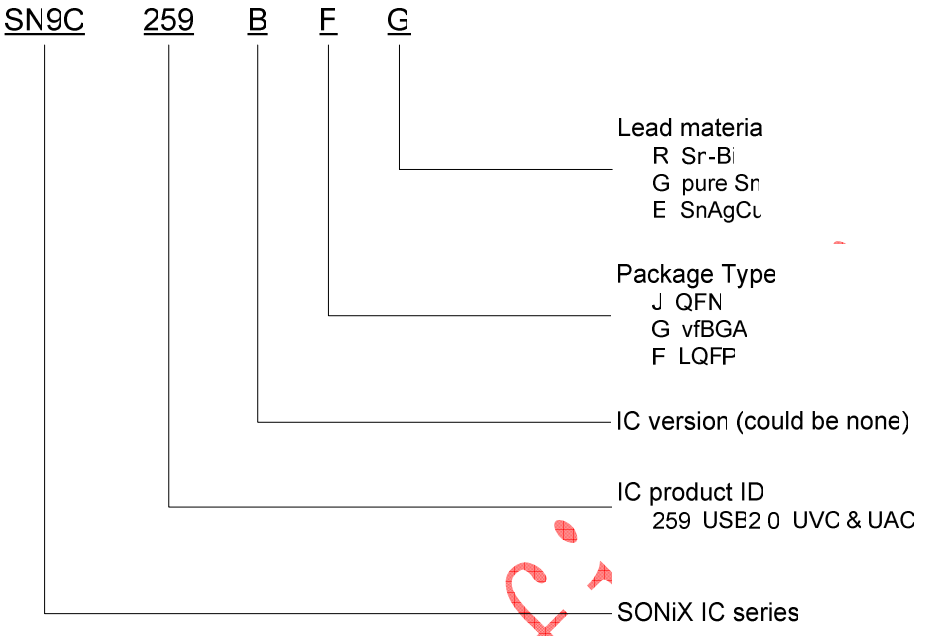
6.1 48 pin LQFP



(All dimensions are in Millimeters)

6.2 Nomenclature

LQFP48:



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