## Features

- **Industry-standard Architecture**
  - **Emulates Many 20-pin PALs®**
  - **Low-cost Easy-to-use Software Tools**
- **High-speed Electrically-erasable Programmable Logic Devices**
  - **10 ns Maximum Pin-to-pin Delay**
- **Several Power Saving Options**

| Device | $I_{CC}$, Standby | $I_{CC}$, Active |
|---|---|---|
| ATF16V8B | 50 mA | 55 mA |
| ATF16V8BQ | 35 mA | 40 mA |
| ATF16V8BQL | 5 mA | 20 mA |

- **CMOS and TTL Compatible Inputs and Outputs**
  - **Input and I/O Pull-up Resistors**
- **Advanced Flash Technology**
  - **Reprogrammable**
  - **100% Tested**
- **High-reliability CMOS Process**
  - **20 Year Data Retention**
  - **100 Erase/Write Cycles**
  - **2,000V ESD Protection**
  - **200 mA Latchup Immunity**
- **Commercial, and Industrial Temperature Ranges**
- **Dual-in-line and Surface Mount Packages in Standard Pinouts**
- **PCI-compliant**
- **Green Package Options (Pb/Halide-free/RoHS Compliant) Available**

# High-performance EE PLD

# ATF16V8B
# ATF16V8BQ
# ATF16V8BQL

## 1. Description

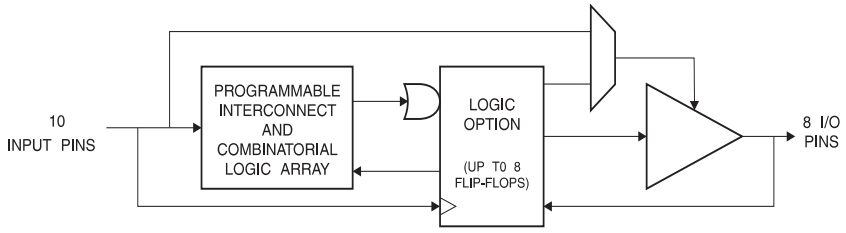
The ATF16V8B is a high-performance CMOS (electricallyerasable) programmable logic device (PLD) that utilizes Atmel's proven electrically-erasable Flash memory technology. All speed ranges are specified over the full 5V ± 10% range for industrial temperature ranges, and 5V ± 5% for commercial temperature ranges.

Several low-power options allow selection of the best solution for various types of power-limited applications. Each of these options significantly reduces total system power and enhances system reliability.

The ATF16V8Bs incorporate a superset of the generic architectures, which allows direct replacement of the 16R8 family and most 20-pin combinatorial PLDs. Eight outputs are each allocated eight product terms. Three different modes of operation, configured automatically with software, allow highly complex logic functions to be realized.

0364J–PLD–7/05

**Figure 1-1.** Block Diagram




## 2. Pin Configurations

**Table 2-1.** Pin Configurations (All Pinouts Top View)

| Pin Name | Function |
|---|---|
| CLK | Clock |
| I | Logic Inputs |
| I/O | Bi-directional Buffers |
| $\overline{OE}$ | Output Enable |
| VCC | +5V Supply |

**Figure 2-1.** TSSOP

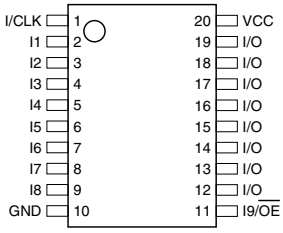



**Figure 2-2.** DIP/SOIC

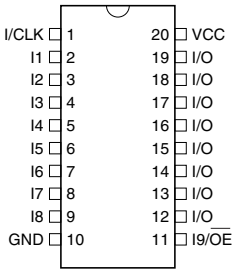
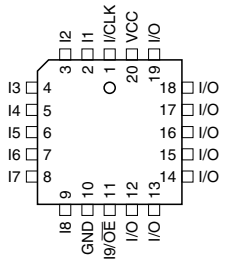



**Figure 2-3.** PLCC



## 3. Absolute Maximum Ratings*

| | |
|---|---|
| Temperature Under Bias | -55°C to +125°C |
| Storage Temperature | -65°C to +150°C |
| Voltage on Any Pin with Respect to Ground | -2.0 V to +7.0 V[1] |
| Voltage on Input Pins with Respect to Ground During Programming | -2.0 V to +14.0 V[1] |
| Programming Voltage with Respect to Ground | -2.0 V to +14.0 V[1] |

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V DC, which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is $V_{CC}$ + 0.75V DC, which may overshoot to 7.0V for pulses of less than 20 ns.

## 4. DC and AC Operating Conditions

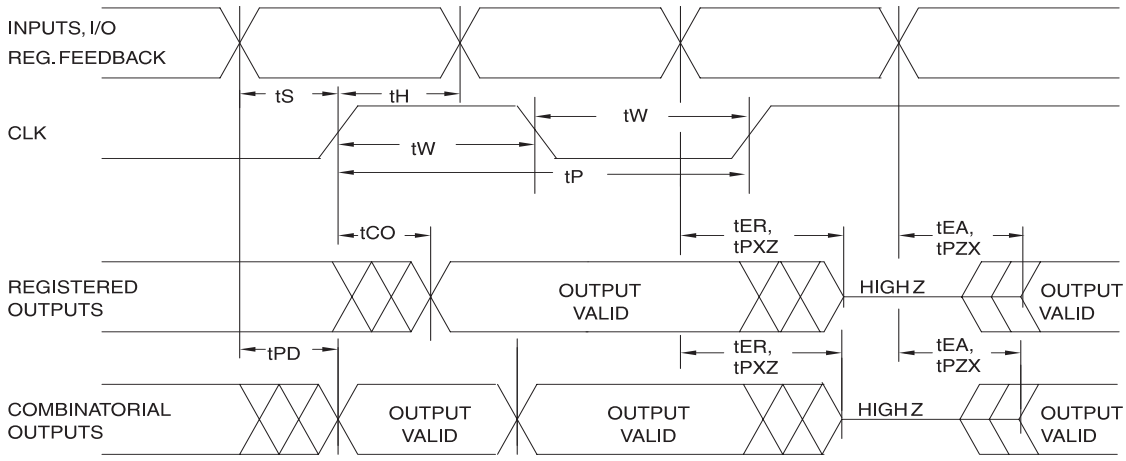
| | Commercial | Industrial |
|---|---|---|
| Operating Temperature (Ambient) | 0°C - 70°C | -40°C - 85°C |
| $V_{CC}$ Power Supply | 5V ± 5% | 5V ± 10% |

## 4.1 DC Characteristics

| Symbol | Parameter | Condition | | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|---|
| $I_{IL}$ | Input or I/O Low Leakage Current | $0 \le V_{IN} \le V_{IL}$(Max) | | | | -35 | -100 | µA |
| $I_{IH}$ | Input or I/O High Leakage Current | $3.5 \le V_{IN} \le V_{CC}$ | | | | | 10 | µA |
| $I_{CC}$ | Power Supply Current, Standby | $V_{CC}$ = Max, $V_{IN}$ = Max, Outputs Open | B-10 | Com. | | 55 | 85 | mA |
| | | | | Ind. | | 55 | 95 | mA |
| | | | B-15 | Com. | | 50 | 75 | mA |
| | | | B-15 | Ind. | | 50 | 80 | mA |
| | | | BQ-10 | Com. | | 35 | 55 | mA |
| | | | BQL-15 | Com. | | 5 | 10 | mA |
| | | | BQL-15 | Ind. | | 5 | 15 | mA |
| $I_{CC2}$ | Clocked Power Supply Current | $V_{CC}$ = Max, Outputs Open, f = 15 MHz | B-10 | Com. | | 60 | 90 | mA |
| | | | | Ind. | | 60 | 100 | mA |
| | | | B-15 | Com. | | 55 | 85 | mA |
| | | | B-15 | Ind. | | 55 | 95 | mA |
| | | | BQ-10 | Com. | | 40 | 55 | mA |
| | | | BQL-15 | Com. | | 20 | 35 | mA |
| | | | BQL-15 | Ind. | | 20 | 40 | mA |
| $I_{OS}$[(1)] | Output Short Circuit Current | $V_{OUT}$ = 0.5 V | | | | | -130 | mA |
| $V_{IL}$ | Input Low Voltage | | | | -0.5 | | 0.8 | V |
| $V_{IH}$ | Input High Voltage | | | | 2.0 | | $V_{CC}$+0.75 | V |
| $V_{OL}$ | Output High Voltage | $V_{IN} = V_{IH}$ or $V_{IL}$, $V_{CC}$ = Min | $I_{OL}$ = -24 mA Com., Ind. | | | | 0.5 | V |
| $V_{OH}$ | Output High Voltage | $V_{IN} = V_{IH}$ or $V_{IL}$, $V_{CC}$ = Min | $I_{OH}$ = -4.0 mA | | 2.4 | | | V |

Note: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.

## 4.2 AC Waveforms[1]




Note: 1. Timing measurement reference is 1.5V. Input AC driving levels are 0.0V 3.0V, unless otherwise specified.

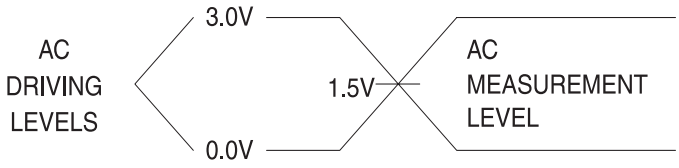
## 4.3 AC Characteristics[1]

| Symbol | Parameter | | -10 Min | -10 Max | -15 Min | -15 Max | Units |
|---|---|---|---|---|---|---|---|
| $t_{PD}$ | Input or Feedback to Non-Registered Output | 8 outputs switching | 3 | 10 | 3 | 15 | ns |
| | | | | | | | |
| $t_{CF}$ | Clock to Feedback | | | 6 | | 8 | ns |
| $t_{CO}$ | Clock to Output | | 2 | 7 | 2 | 10 | ns |
| $t_S$ | Input or Feedback Setup Time | | 7.5 | | 12 | | ns |
| $t_H$ | Hold Time | | 0 | | 0 | | ns |
| $t_P$ | Clock Period | | 12 | | 16 | | ns |
| $t_W$ | Clock Width | | 6 | | 8 | | ns |
| $f_{MAX}$ | External Feedback $1/(t_S + t_{CO})$ | | | 68 | | 45 | MHz |
| | Internal Feedback $1/(t_S + t_{CF})$ | | | 74 | | 50 | MHz |
| | No Feedback $1/(t_P)$ | | | 83 | | 62 | MHz |
| $t_{EA}$ | Input to Output Enable — Product Term | | 3 | 10 | 3 | 15 | ns |
| $t_{ER}$ | Input to Output Disable — Product Term | | 2 | 10 | 2 | 15 | ns |
| $t_{PZX}$ | $\overline{OE}$ pin to Output Enable | | 2 | 10 | 2 | 15 | ns |
| $t_{PXZ}$ | $\overline{OE}$ pin to Output Disable | | 1.5 | 10 | 1.5 | 15 | ns |

Note: 1. See ordering information for valid part numbers and speed grades.

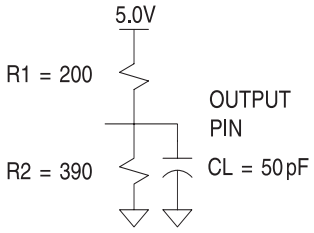
## 4.4 Input Test Waveforms

### 4.4.1 Input Test Waveforms and Measurement Levels




$t_R$, $t_F$ < 5 ns (10% to 90%)

### 4.4.2 Output Test Loads (Commercial)




$C_L$ includes Test fixture and Probe capacitance

## 4.5 Pin Capacitance

**Table 4-1.** Pin Capacitance (f = 1 MHz, T = 25°C[1])

| | Typ | Max | Units | Conditions |
|---|---|---|---|---|
| $C_{IN}$ | 5 | 8 | pF | $V_{IN}$ = 0V |
| $C_{OUT}$ | 6 | 8 | pF | $V_{OUT}$ = 0V |

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

## 4.6 Power-up Reset

The registers in the ATF16V8Bs are designed to reset during power-up. At a point delayed slightly from $V_{CC}$ crossing $V_{RST}$, all registers will be reset to the low state. As a result, the registered output state will always be high on power-up.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how $V_{CC}$ actually rises in the system, the following conditions are required:

1. The $V_{CC}$ rise must be monotonic,
2. After reset occurs, all input and feedback setup times must be met before driving the clock pin high, and
3. The clock must remain stable during $t_{PR}$.

**Figure 4-1.** Power-up Reset Waveforms

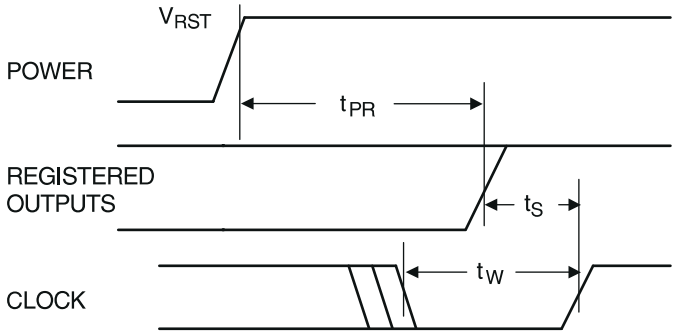



**Table 4-2.** Power-up Reset Parameters

| Parameter | Description | Typ | Max | Units |
|---|---|---|---|---|
| $t_{PR}$ | Power-up Reset Time | 600 | 1,000 | ns |
| $V_{RST}$ | Power-up Reset Voltage | 3.8 | 4.5 | V |

## 4.7 Preload of Registered Outputs

The ATF16V8B's registers are provided with circuitry to allow loading of each register with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A JEDEC file with preload is generated when a source file with vectors is compiled. Once downloaded, the JEDEC file preload sequence will be done automatically by most of the approved programmers after the programming.

# 5. Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the ATF16V8B fuse patterns. Once programmed, fuse verify and preload are inhibited. However, the 64-bit User Signature remains accessible.

The security fuse should be programmed last, as its effect is immediate.

## 6. Electronic Signature Word

There are 64 bits of programmable memory that are always available to the user, even if the device is secured. These bits can be used for user-specific data.

## 7. Programming/Erasing

Programming/erasing is performed using standard PLD programmers. See *CMOS PLD Programming Hardware and Software Support* for information on software/programming.

## 8. Input and I/O Pull-ups

All ATF16V8B family members have internal input and I/O pull-up resistors. Therefore, whenever inputs or I/Os are not being driven externally, they will float to $V_{CC}$. This ensures that all logic array inputs are at known states. These are relatively weak active pull-ups that can easily be overdriven by TTL-compatible drivers (see input and I/O diagrams below).

**Figure 8-1.** Input Diagram

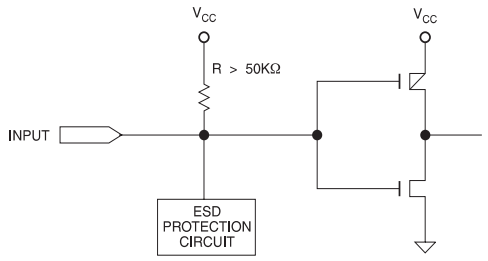
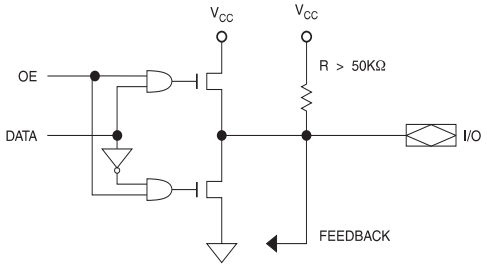



**Figure 8-2.** I/O Diagram




## 9. Functional Logic Diagram Description

The Logic Option and Functional Diagrams describe the ATF16V8B architecture. Eight configurable macrocells can be configured as a registered output, combinatorial I/O, combinatorial output, or dedicated input.

The ATF16V8B can be configured in one of three different modes. Each mode makes the ATF16V8B look like a different device. Most PLD compilers can choose the right mode automatically. The user can also force the selection by supplying the compiler with a mode selection. The determining factors would be the usage of register versus combinatorial outputs and dedicated outputs versus outputs with output enable control.

The ATF16V8B universal architecture can be programmed to emulate many 20-pin PAL devices. These architectural subsets can be found in each of the configuration modes described

in the following pages. The user can download the listed subset device JEDEC programming file to the PLD programmer, and the ATF16V8B can be configured to act like the chosen device. Check with your programmer manufacturer for this capability.

Unused product terms are automatically disabled by the compiler to decrease power consumption. A security fuse, when programmed, protects the content of the ATF16V8B. Eight bytes (64 fuses) of User Signature are accessible to the user for purposes such as storing project name, part number, revision, or date. The User Signature is accessible regardless of the state of the security fuse.

## 10. Software Support

Atmel-WinCUPL is a free tool, available on Atmel's web site and can be used to design in all members of the Atmel ATF16V8B family of SPLDs. Table 10-1 lists popular compilers with the appropriate device mnemonics

**Table 10-1.** Compiler Mode Selection

| | Registered | Complex | Simple | Auto Select |
|---|---|---|---|---|
| **ABEL, Atmel-ABEL** | P16V8R | P16V8C | P16V8AS | P16V8 |
| **CUPL, Atmel-WinCUPL** | G16V8MS | G16V8MA | G16V8AS | G16V8 |
| **LOG/iC** | GAL16V8_R(1) | GAL16V8_C7(1) | GAL16V8_C8(1) | GAL16V8 |
| **OrCAD-PLD** | "Registered" | "Complex" | "Simple" | GAL16V8A |
| **PLDesigner** | P16V8R | P16V8C | P16V8C | P16V8A |
| **Tango-PLD** | G16V8R | G16V8C | G16V8AS | G16V8 |

Note: 1. Only applicable for version 3.4 or lower.

## 11. Macrocell Configuration

Software compilers support the three different OMC modes as different device types. Most compilers have the ability to automatically select the device type, generally based on the register usage and output enable (OE) usage. Register usage on the device forces the software to choose the registered mode. All combinatorial outputs with OE controlled by the product term will force the software to choose the complex mode. The software will choose the simple mode only when all outputs are dedicated combinatorial without OE control. The different device types can be used to override the automatic device selection by the software. For further details, refer to the compiler software manuals.

When using compiler software to configure the device, the user must pay special attention to the following restrictions in each mode.

In **registered mode** pin 1 and pin 11 are permanently configured as clock and output enable, respectively. These pins cannot be configured as dedicated inputs in the registered mode.

In **complex mode** pin 1 and pin 11 become dedicated inputs and use the feedback paths of pin 19 and pin 12 respectively. Because of this feedback path usage, pin 19 and pin 12 do not have the feedback option in this mode.

In **simple mode** all feedback paths of the output pins are routed via the adjacent pins. In doing so, the two inner most pins (pins 15 and 16) will not have the feedback option as these pins are always configured as dedicated combinatorial output.

## 11.1 ATF16V8B Registered Mode

**PAL Device Emulation/PAL Replacement.** The registered mode is used if one or more registers are required. Each macrocell can be configured as either a registered or combinatorial output or I/O, or as an input. For a registered output or I/O, the output is enabled by the $\overline{OE}$ pin, and the register is clocked by the CLK pin. Eight product terms are allocated to the sum term. For a combinatorial output or I/O, the output enable is controlled by a product term, and seven product terms are allocated to the sum term. When the macrocell is configured as an input, the output enable is permanently disabled.

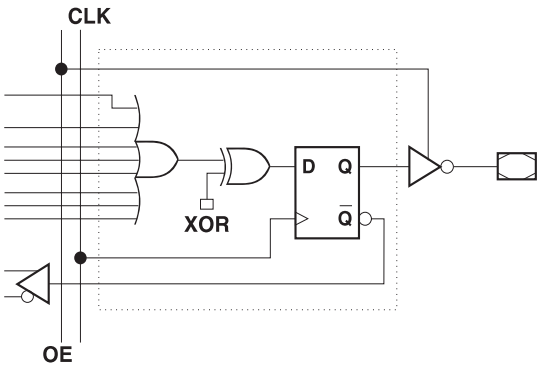
Any register usage will make the compiler select this mode. The following registered devices can be emulated using this mode:

16R8 16RP8

16R6 16RP6

16R4 16RP4

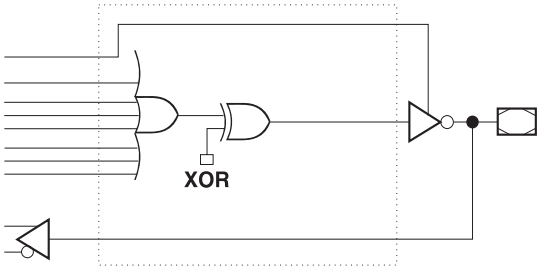
**Figure 11-1.** Registered Configuration for Registered Mode[1][2]




Notes: 1. Pin 1 controls common CLK for the registered outputs. Pin 11 controls common $\overline{OE}$ for the registered outputs. Pin 1 and Pin 11 are permanently configured as CLK and $\overline{OE}$.

2. The development software configures all the architecture control bits and checks for proper pin usage automatically.

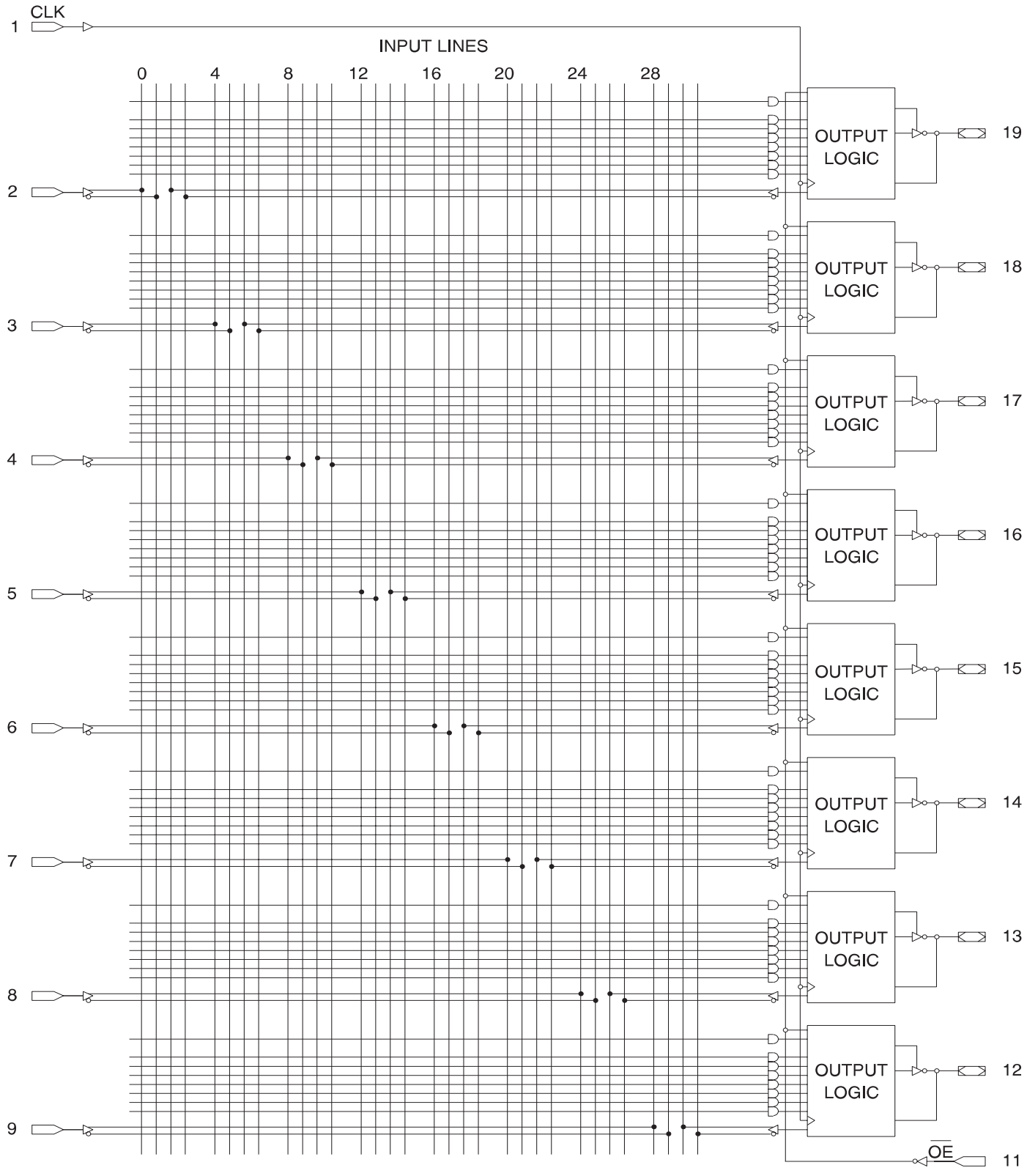
**Figure 11-2.** Combinatorial Configuration for Registered Mode[1][2]




Notes: 1. Pin 1 and Pin 11 are permanently configured as CLK and $\overline{OE}$.

2. The development software configures all the architecture control bits and checks for proper pin usage automatically.

**Figure 11-3.** Registered Mode Logic Diagram



## 11.2 ATF16V8B Complex Mode

**PAL Device Emulation/PAL Replacement.** In the complex mode, combinatorial output and I/O functions are possible. Pins 1 and 11 are regular inputs to the array. Pins 13 through 18 have pin feedback paths back to the AND-array, which makes full I/O capability possible. Pins 12 and 19 (outermost macrocells) are outputs only. They do not have input capability. In this mode, each macrocell has seven product terms going to the sum term and one product term enabling the output.

Combinatorial applications with an OE requirement will make the compiler select this mode. The following devices can be emulated using this mode:

16L8

16H8

16P8

**Figure 11-4.** Complex Mode Option

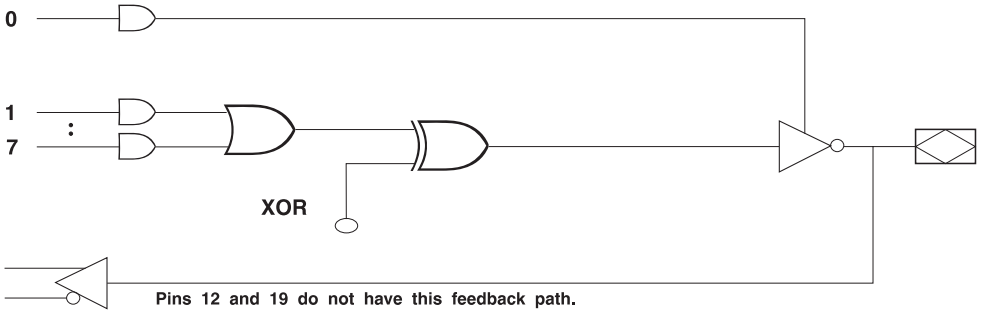
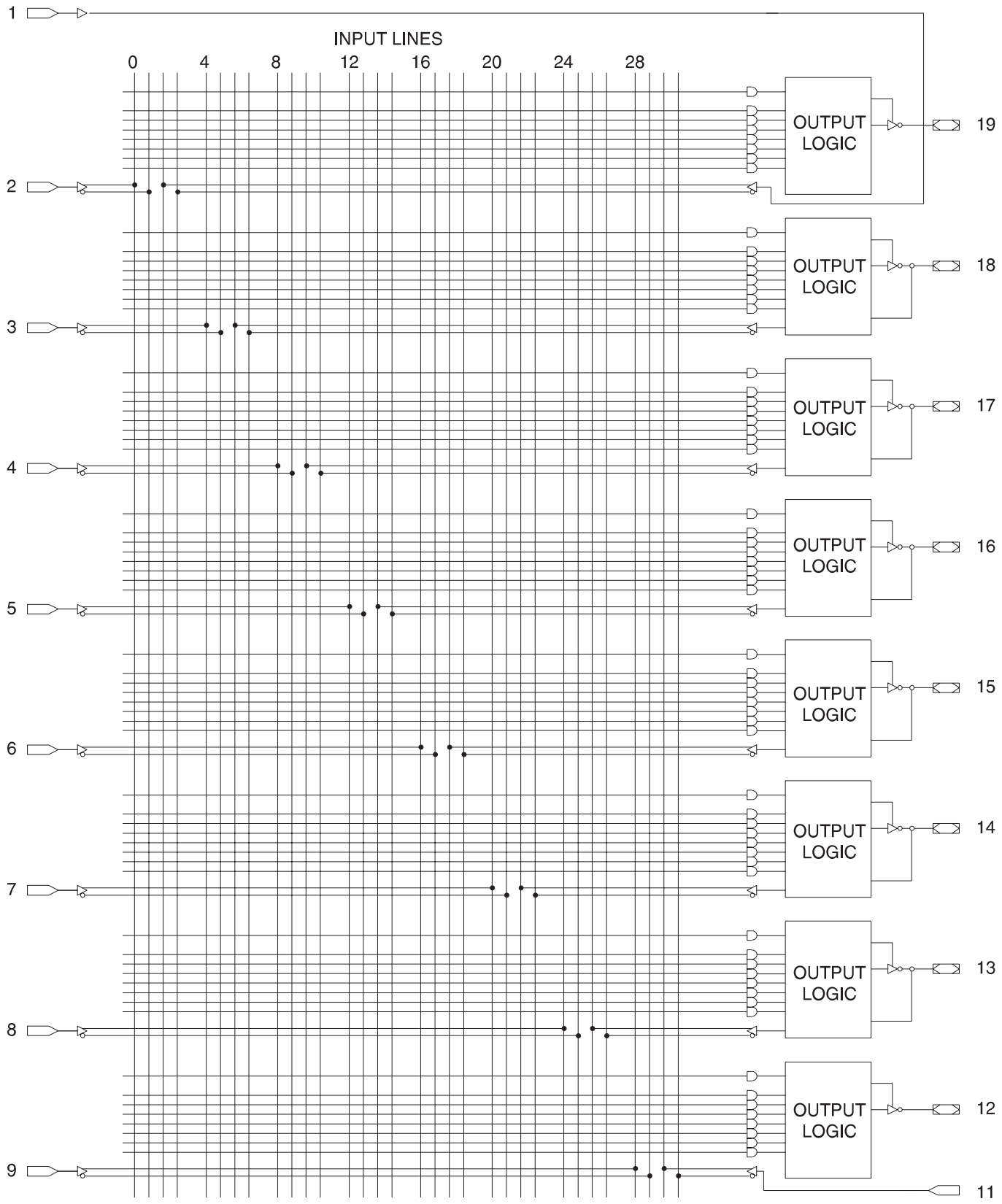


**Figure 11-5.** Complex Mode Logic Diagram



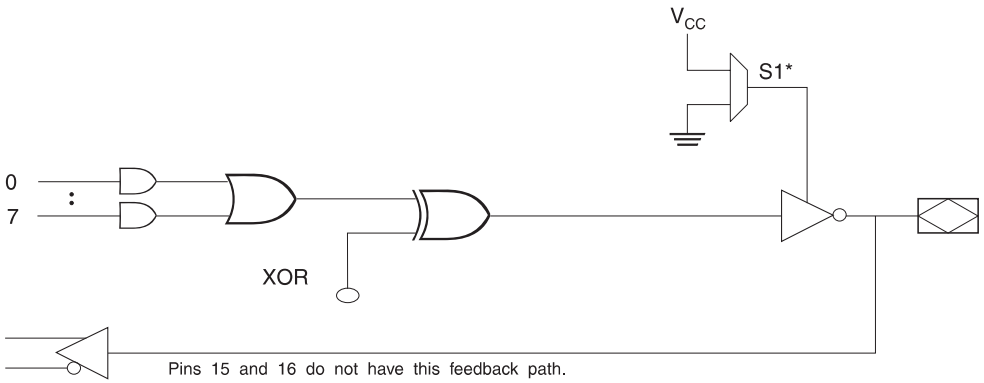
## 11.3 ATF16V8B Simple Mode

**PAL Device Emulation/PAL Replacement.** In the Simple Mode, 8 product terms are allocated to the sum term. Pins 15 and 16 (center macrocells) are permanently configured as combinatorial outputs. Other macrocells can be either inputs or combinatorial outputs with pin feedback to the AND-array. Pins 1 and 11 are regular inputs.

The compiler selects this mode when all outputs are combinatorial without OE control. The following simple PALs can be emulated using this mode:

| | | |
|---|---|---|
| 10L8 | 10H8 | 10P8 |
| 12L6 | 12H6 | 12P6 |
| 14L4 | 14H4 | 14P4 |
| 16L2 | 16H2 | 16P2 |

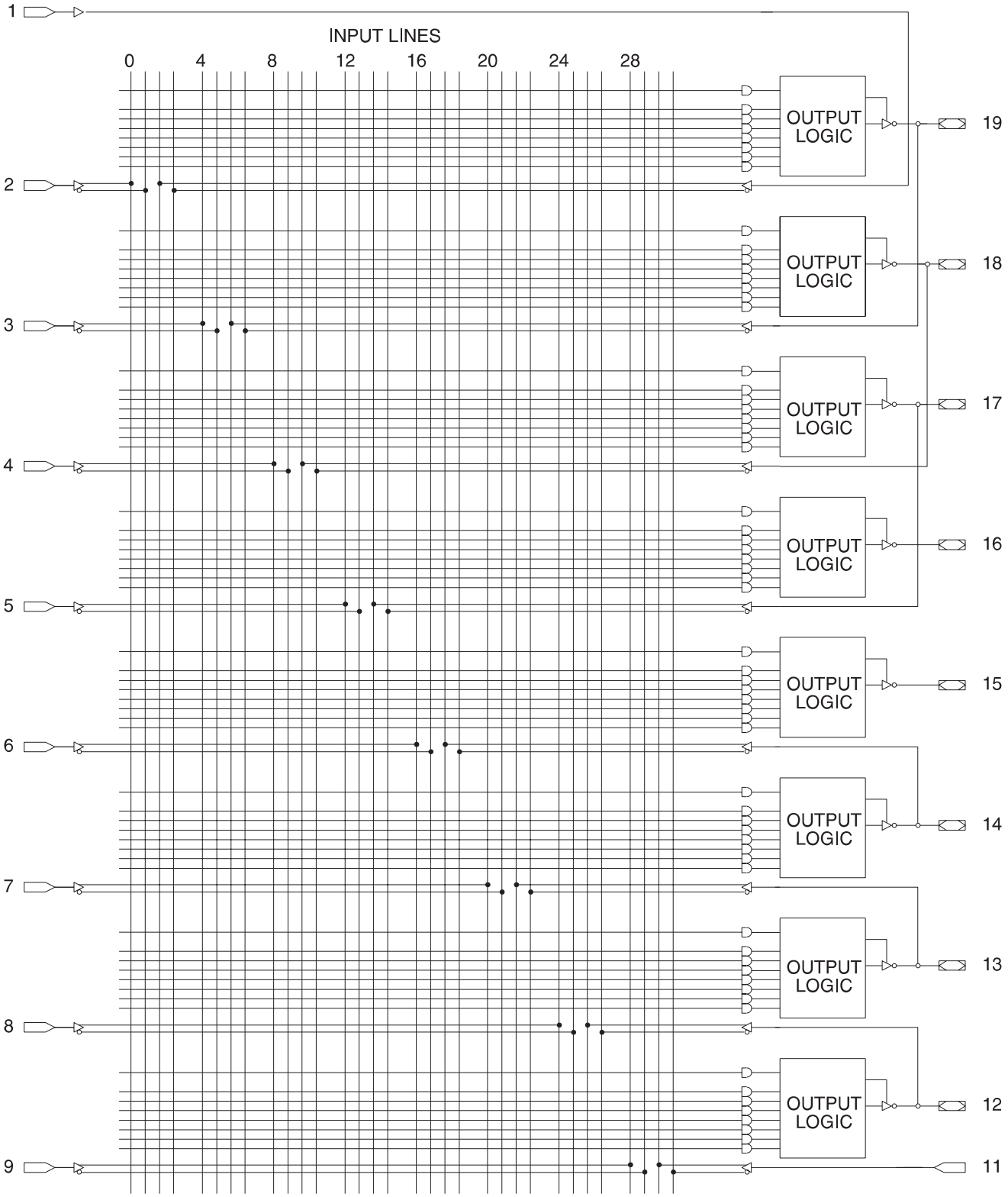
**Figure 11-6.** Simple Mode Option




* - Pins 15 and 16 are always enabled.

Note: * Pins 15 and 16 are always enabled.

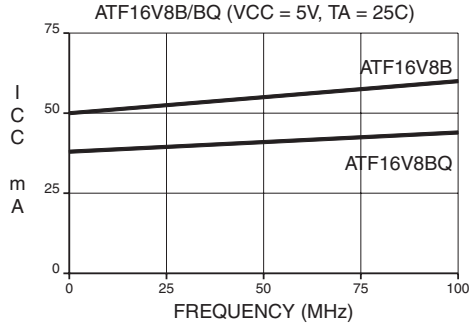
**Figure 11-7.** Simple Mode Logic Diagram



# 12. Test Characterization Data

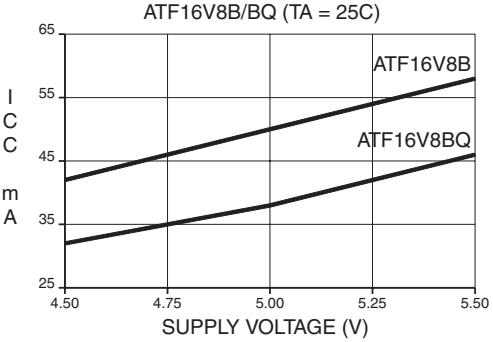
SUPPLY CURRENT vs. INPUT FREQUENCY

ATF16V8B/BQ (VCC = 5V, TA = 25C)



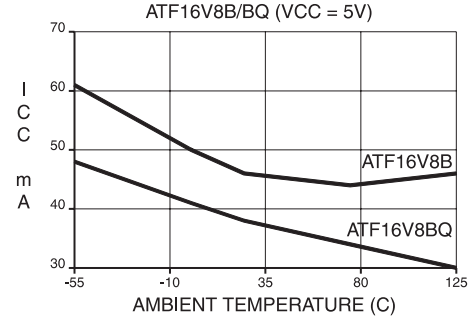

SUPPLY CURRENT vs. SUPPLY VOLTAGE

ATF16V8B/BQ (TA = 25C)



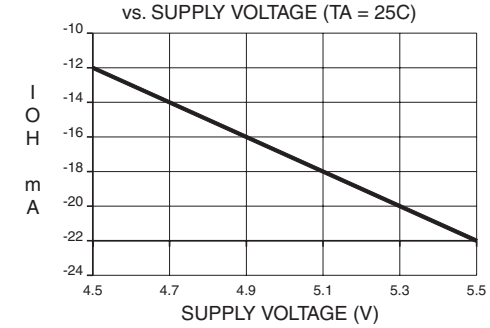

SUPPLY CURRENT vs. AMBIENT TEMPERATURE

ATF16V8B/BQ (VCC = 5V)



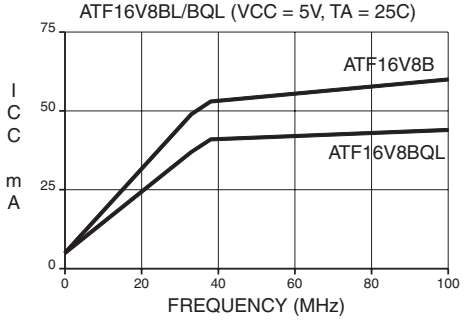

OUTPUT SOURCE CURRENT

vs. SUPPLY VOLTAGE (TA = 25C)



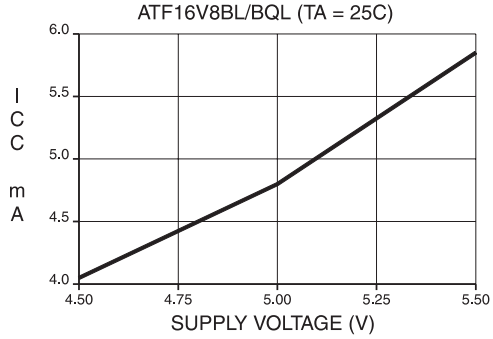

SUPPLY CURRENT vs. INPUT FREQUENCY

ATF16V8BL/BQL (VCC = 5V, TA = 25C)



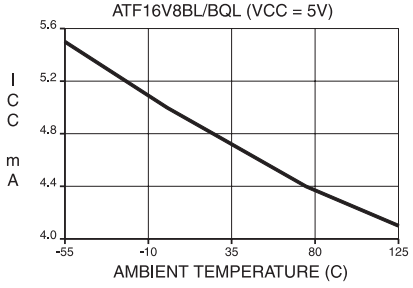

SUPPLY CURRENT vs. SUPPLY VOLTAGE

ATF16V8BL/BQL (TA = 25C)



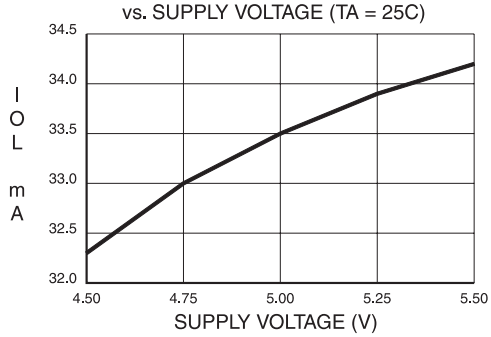

SUPPLY CURRENT vs. AMBIENT TEMPERATURE

ATF16V8BL/BQL (VCC = 5V)

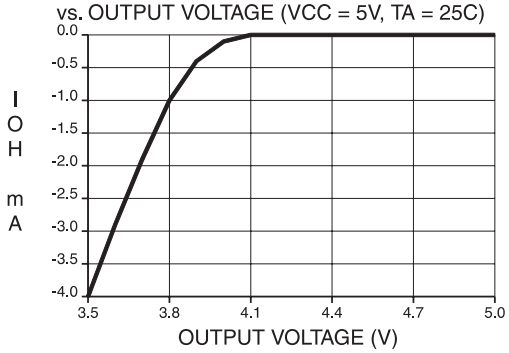



OUTPUT SINK CURRENT

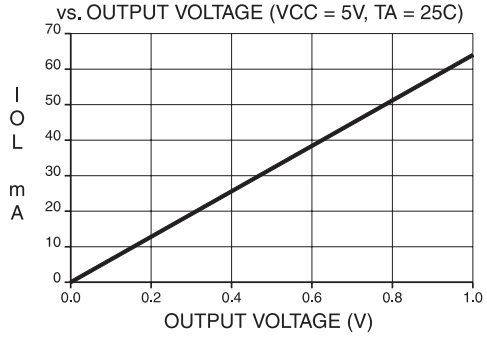
vs. SUPPLY VOLTAGE (TA = 25C)



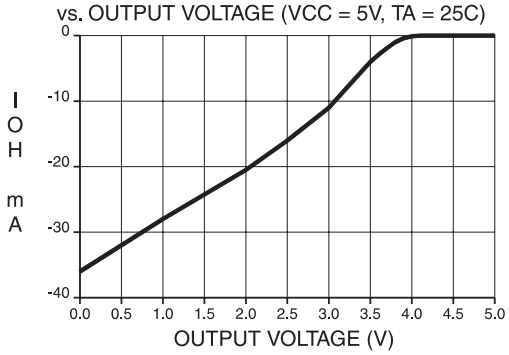
OUTPUT SOURCE CURRENT
vs. OUTPUT VOLTAGE (VCC = 5V, TA = 25C)



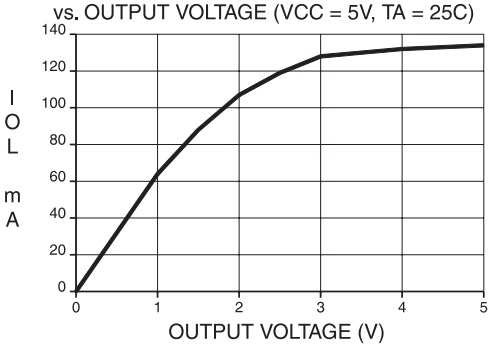

OUTPUT SINK CURRENT
vs. OUTPUT VOLTAGE (VCC = 5V, TA = 25C)



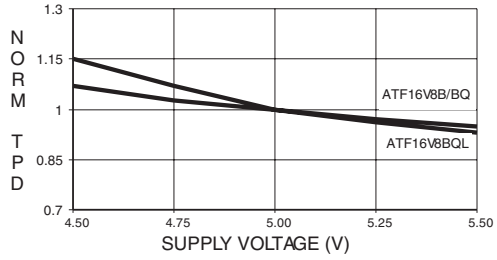

OUTPUT SOURCE CURRENT
vs. OUTPUT VOLTAGE (VCC = 5V, TA = 25C)



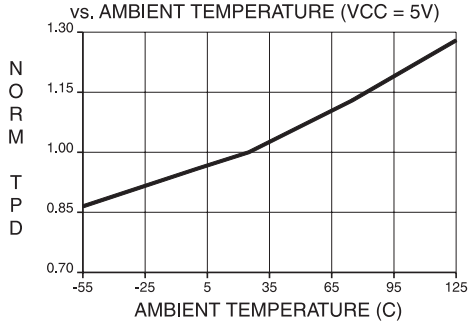

OUTPUT SINK CURRENT
vs. OUTPUT VOLTAGE (VCC = 5V, TA = 25C)



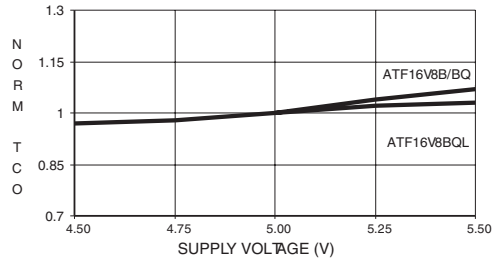

NORMALIZED TPD
vs. SUPPLY VOLTAGE (TA=25°C)



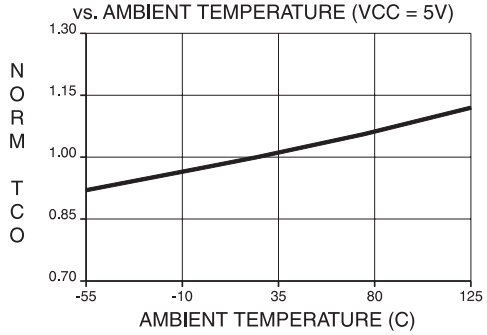

NORMALIZED TPD
vs. AMBIENT TEMPERATURE (VCC = 5V)

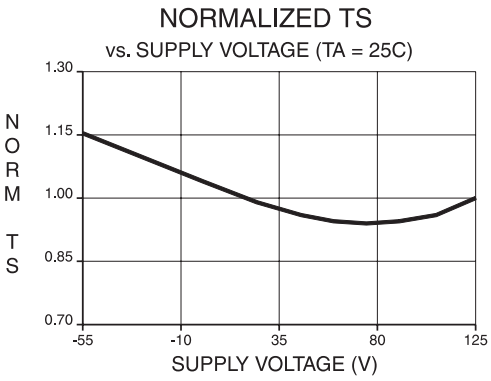


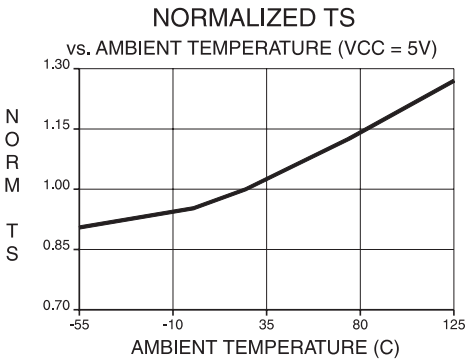

NORMALIZED TCO
vs. SUPPLY VOLTAGE(TA=25°C)

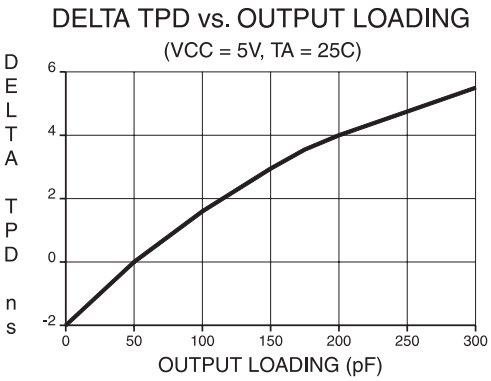


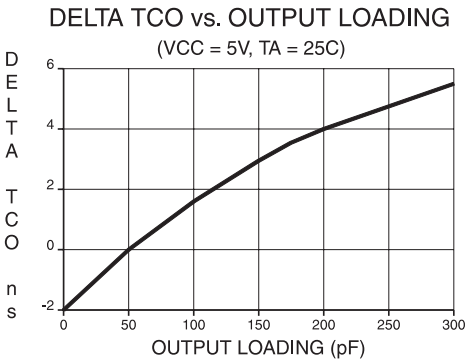

NORMALIZED TCO
vs. AMBIENT TEMPERATURE (VCC = 5V)

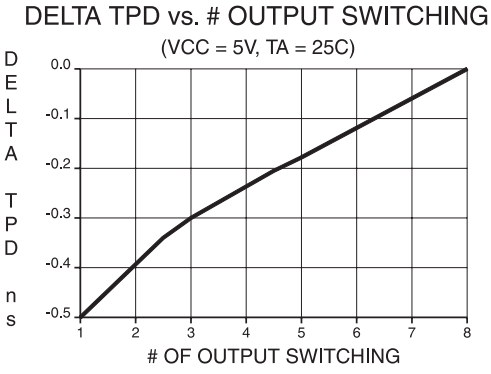


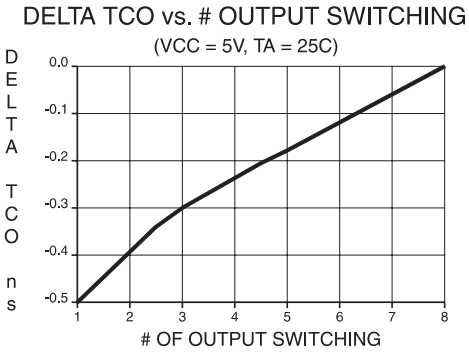

NORMALIZED TS
vs. SUPPLY VOLTAGE (TA = 25C)
NORM TS
1.30
1.15
1.00
0.85
0.70
-55
-10
35
80
125
SUPPLY VOLTAGE (V)

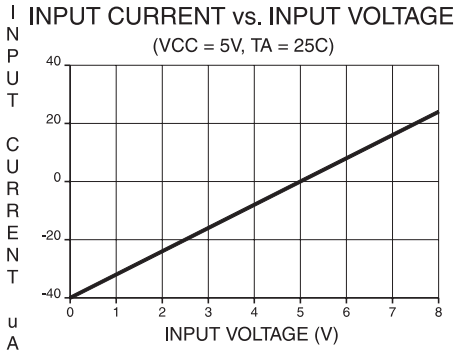

NORMALIZED TS
vs. AMBIENT TEMPERATURE (VCC = 5V)
NORM TS
1.30
1.15
1.00
0.85
0.70
-55
-10
35
80
125
AMBIENT TEMPERATURE (C)

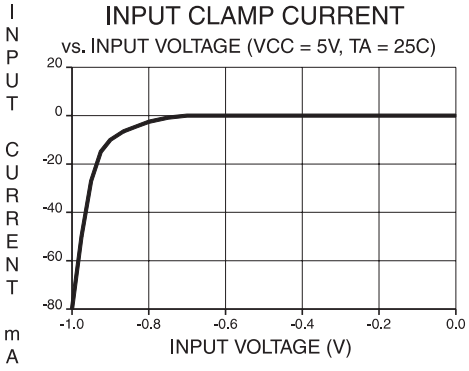

DELTA TPD vs. OUTPUT LOADING
(VCC = 5V, TA = 25C)
DELTA TPD ns
6
4
2
0
-2
0
50
100
150
200
250
300
OUTPUT LOADING (pF)


DELTA TCO vs. OUTPUT LOADING
(VCC = 5V, TA = 25C)
DELTA TCO ns
6
4
2
0
-2
0
50
100
150
200
250
300
OUTPUT LOADING (pF)


DELTA TPD vs. # OUTPUT SWITCHING
(VCC = 5V, TA = 25C)
DELTA TPD ns
0.0
-0.1
-0.2
-0.3
-0.4
-0.5
1
2
3
4
5
6
7
8
# OF OUTPUT SWITCHING


DELTA TCO vs. # OUTPUT SWITCHING
(VCC = 5V, TA = 25C)
DELTA TCO ns
0.0
-0.1
-0.2
-0.3
-0.4
-0.5
1
2
3
4
5
6
7
8
# OF OUTPUT SWITCHING


INPUT CURRENT vs. INPUT VOLTAGE
(VCC = 5V, TA = 25C)
INPUT CURRENT ua
40
20
0
-20
-40
0
1
2
3
4
5
6
7
8
INPUT VOLTAGE (V)


INPUT CLAMP CURRENT
vs. INPUT VOLTAGE (VCC = 5V, TA = 25C)
INPUT CURRENT mA
20
0
-20
-40
-60
-80
-1.0
-0.8
-0.6
-0.4
-0.2
0.0
INPUT VOLTAGE (V)

# 13. ATF16V8B Ordering Information

## 13.1 ATF16V8B Standard Package Options

| $t_{PD}$ (ns) | $t_S$ (ns) | $t_{CO}$ (ns) | Ordering Code | Package | Operation Range |
|---|---|---|---|---|---|
| 10 | 7.5 | 7 | ATF16V8B-10JC<br>ATF16V8B-10PC | 20J<br>20P3<br>20S<br>20X | Commercial<br>(0°C to 70°C) |
| | | | ATF16V8B-10SC<br>ATF16V8B-10XC | | |
| | | | ATF16V8B-10JI<br>ATF16V8B-10PI<br>ATF16V8B-10SI<br>ATF16V8B-10XI | 20J<br>20P3<br>20S<br>20X | Industrial<br>(-40°C to 85°C) |
| 15 | 12 | 10 | ATF16V8B-15JC<br>ATF16V8B-15PC<br>ATF16V8B-15SC | 20J<br>20P3<br>20S<br>20X | Commercial<br>(0°C to 70°C) |
| | | | ATF16V8B-15XC | | |
| | | | ATF16V8B-15JI<br>ATF16V8B-15PI<br>ATF16V8B-15SI | 20J<br>20P3<br>20S<br>20X | Industrial<br>(-40°C to 85°C) |
| | | | ATF16V8B-15XI | | |

Note: The last time buy date is Sept. 30, 2005 for shaded parts.

## 13.2 ATF16V8B Green Package Options (Pb/Halide-free/RoHS Compliant)

| $t_{PD}$ (ns) | $t_S$ (ns) | $t_{CO}$ (ns) | Ordering Code | Package | Operation Range |
|---|---|---|---|---|---|
| 10 | 7.5 | 7 | ATF16V8B-10JU | 20J | Industrial<br>(-40°C to 85°C) |
| 15 | 12 | 10 | ATF16V8B-15JU<br>ATF16V8B-15PU<br>ATF16V8B-15SU<br>ATF16V8B-15XU | 20J<br>20P3<br>20S<br>20X | |

## 13.3 Using “C” Product for Industrial

To use commercial product for Industrial temperature ranges, down-grade one speed grade from the “I” to the “C” device (7 ns “C” = 10 ns “I”) and de-rate power by 30%.

| Package Type | |
|---|---|
| **20J** | 20-lead, Plastic J-leaded Chip Carrier (PLCC) |
| **20P3** | 20-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP) |
| **20S** | 20-lead, 0.300" Wide, Plastic Gull-wing Small Outline (SOIC) |
| **20X** | 20-lead, 4.4 mm Wide, Plastic Thin Shrink Small Outline (TSSOP) |

# 14. ATF16V8BQ/BQL Ordering Information

## 14.1 ATF16V8BQ and ATF16V8BQL Ordering Information

| $t_{PD}$ (ns) | $t_S$ (ns) | $t_{CO}$ (ns) | Ordering Code | Package | Operation Range |
|---|---|---|---|---|---|
| 10 | 7.5 | 7 | ATF16V8BQ-10JC<br>ATF16V8BQ-10PC<br>ATF16V8BQ-10SC<br>ATF16V8BQ-10XC | 20J<br>20P3<br>20S<br>20X | Commercial (0°C to 70°C) |
| 15 | 12 | 10 | ATF16V8BQL-15JC<br>ATF16V8BQL-15PC<br>ATF16V8BQL-15SC<br>ATF16V8BQL-15XC | 20J<br>20P3<br>20S<br>20X | Commercial (0°C to 70°C) |
| | | | ATF16V8BQL-15JI<br>ATF16V8BQL-15PI<br>ATF16V8BQL-15SI<br>ATF16V8BQL-15XI | 20J<br>20P3<br>20S<br>20X | Industrial (-40°C to 85°C) |

Note: The last time buy date is Sept. 30, 2005 for shaded parts.

## 14.2 ATF16V8BQ and ATF16V8BQL Green Package Options (Pb/Halide-free/RoHS Compliant)

| $t_{PD}$ (ns) | $t_S$ (ns) | $t_{CO}$ (ns) | Ordering Code | Package | Operation Range |
|---|---|---|---|---|---|
| 15 | 12 | 10 | ATF16V8BQL-15JU<br>ATF16V8BQL-15PU<br>ATF16V8BQL-15SU<br>ATF16V8BQL-15XU | 20J<br>20P3<br>20S<br>20X | Industrial (-40°C to 85°C) |

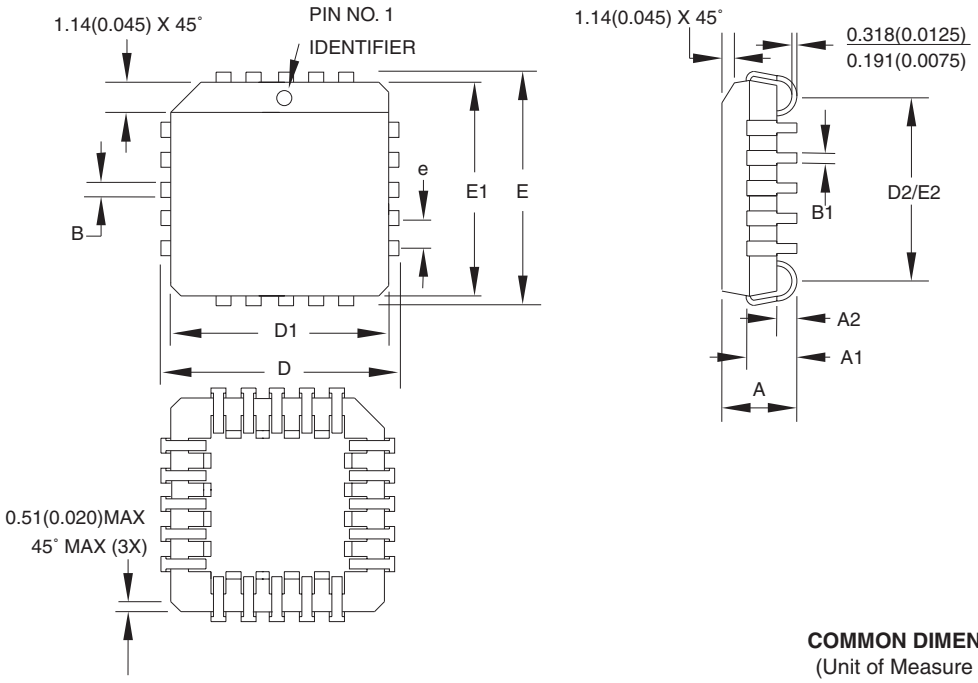
## 14.3 Using “C” Product for Industrial

To use commercial product for Industrial temperature ranges, down-grade one speed grade from the “I” to the “C” device (7 ns “C” = 10 ns “I”) and de-rate power by 30%.

| Package Type | |
|---|---|
| **20J** | 20-lead, Plastic J-leaded Chip Carrier (PLCC) |
| **20P3** | 20-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP) |
| **20S** | 20-lead, 0.300" Wide, Plastic Gull-Wing Small Outline (SOIC) |
| **20X** | 20-lead, 4.4 mm Wide, Plastic Thin Shrink Small Outline (TSSOP) |

# 15. Packaging Information

## 15.1 20J – PLCC




**COMMON DIMENSIONS**
(Unit of Measure = mm)

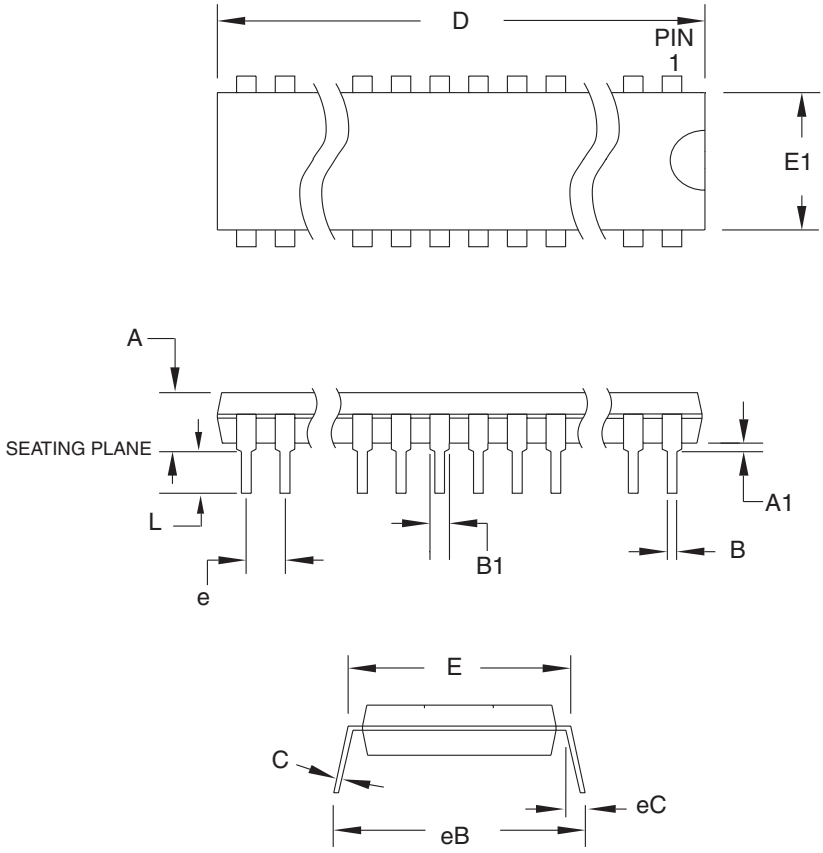
| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | 4.191 | – | 4.572 | |
| A1 | 2.286 | – | 3.048 | |
| A2 | 0.508 | – | – | |
| D | 9.779 | – | 10.033 | |
| D1 | 8.890 | – | 9.042 | Note 2 |
| E | 9.779 | – | 10.033 | |
| E1 | 8.890 | – | 9.042 | Note 2 |
| D2/E2 | 7.366 | – | 8.382 | |
| B | 0.660 | – | 0.813 | |
| B1 | 0.330 | – | 0.533 | |
| e | 1.270 TYP | | | |

Notes:
1. This package conforms to JEDEC reference MS-018, Variation AA.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01

| | TITLE | DRAWING NO. | REV. |
|---|---|---|---|
| 2325 Orchard Parkway<br>San Jose, CA 95131 | **20J**, 20-lead, Plastic J-leaded Chip Carrier (PLCC) | 20J | B |

## 15.2 20P3 – PDIP




**COMMON DIMENSIONS**
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | – | – | 5.334 | |
| A1 | 0.381 | – | – | |
| D | 24.892 | – | 26.924 | Note 2 |
| E | 7.620 | – | 8.255 | |
| E1 | 6.096 | – | 7.112 | Note 2 |
| B | 0.356 | – | 0.559 | |
| B1 | 1.270 | – | 1.551 | |
| L | 2.921 | – | 3.810 | |
| C | 0.203 | – | 0.356 | |
| eB | – | – | 10.922 | |
| eC | 0.000 | – | 1.524 | |
| e | 2.540 TYP | | | |

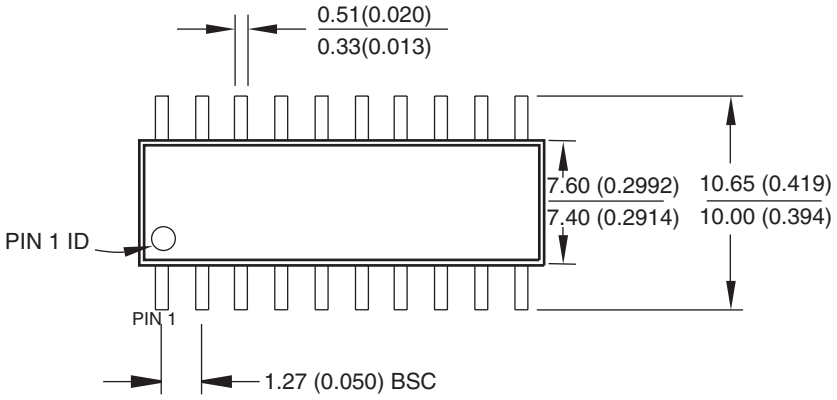
Notes: 1. This package conforms to JEDEC reference MS-001, Variation AD.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

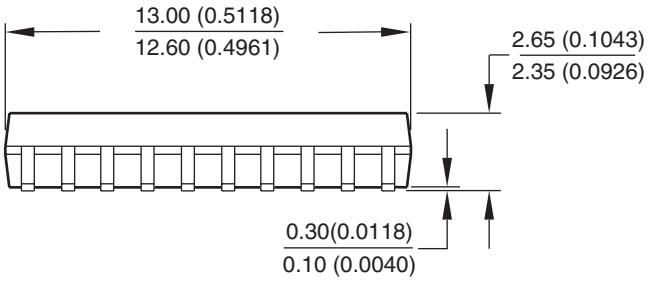
1/23/04

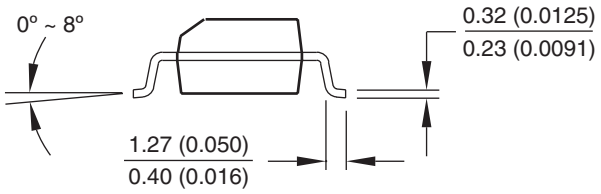
| | TITLE | DRAWING NO. | REV. |
|---|---|---|---|
| 2325 Orchard Parkway<br>San Jose, CA 95131 | **20P3**, 20-lead (0.300"/7.62 mm Wide) Plastic Dual Inline Package (PDIP) | 20P3 | D |

## 15.3 20S – SOIC

Dimensions in Millimeters and (Inches).
Controlling dimension: Inches.
JEDEC Standard MS-013



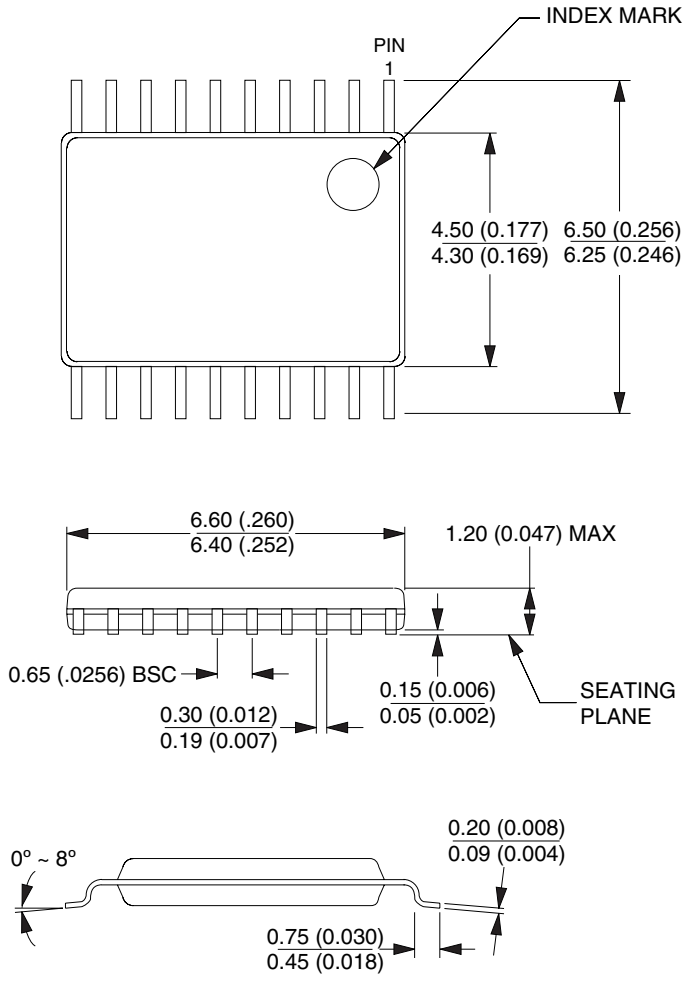




10/23/03

| | TITLE | DRAWING NO. | REV. |
|---|---|---|---|
| 2325 Orchard Parkway<br>San Jose, CA 95131 | **20S**, 20-lead, 0.300" Body, Plastic Gull Wing Small Outline (SOIC) | 20S | B |

## 15.4 20X – TSSOP

Dimensions in Millimeters and (Inches).
Controlling dimension: Millimeters.
JEDEC Standard MO-153 AC




10/23/03

| | TITLE | DRAWING NO. | REV. |
|---|---|---|---|
| 2325 Orchard Parkway<br>San Jose, CA 95131 | **20X**, (Formerly 20T), 20-lead, 4.4 mm Body Width,<br>Plastic Thin Shrink Small Outline Package (TSSOP) | 20X | C |

# 16. Revision History

## 16.1 0364J

1. ATF16V8B-25 JC/PC/SC/XC/JI/PI/SI/XI were obseleted in August 1999
   ATF16V8BQL-25 JC/PC/SC/XC/JI/PI/SI/XI were obseleted in August 1999
   These devices were removed from Section 13. ”ATF16V8B Ordering Information” on page 19 and Section 14. ”ATF16V8BQ/BQL Ordering Information” on page 20.
2. Green Package options added in 2005.

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