Signetics

74LS670
Register File

4 x 4 Register File (3-State)
Product Specification

Logic Products

FEATURES

- **Simultaneous and independent Read and Write operations**
- **Expandable to almost any word size and bit length**
- **3-State outputs**
- **See '170 for open collector version**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74LS670	25ns	30mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±5%; T_A = 0°C to +70°C
Plastic DIP	N74LS670N
Plastic SOL-16	N74LS670D

NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74LS
$D_0 - D_3$, W_A, W_B, R_A, R_B	Inputs	1LSul
$\overline{WE}$	Input	2LSul
$\overline{RE}$	Input	3LSul
$Q_0 - Q_3$	Outputs	10LSul

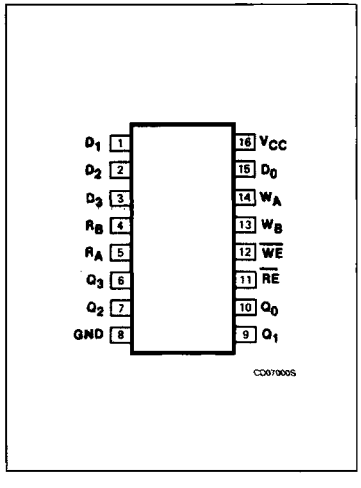
NOTE:
A 74LS unit load (LSul) is 20μA I_{IH} and -0.4mA I_{IL}.

DESCRIPTION

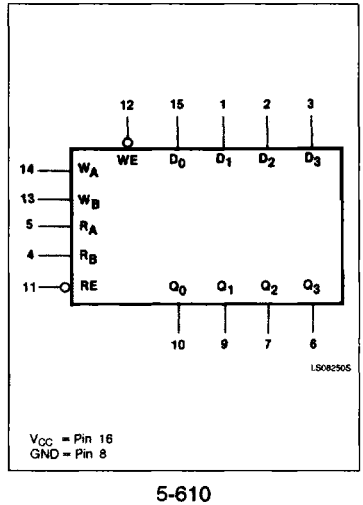
The '670 is a 16-bit 3-State Register File organized as 4 words of 4 bits each. Separate Read and Write Address and Enable inputs are available, permitting simultaneous writing into one word location and reading from another location. The 4-bit word to be stored is presented to four Data inputs. The Write Address inputs (W_A and W_B) determine the location of the stored word. When the Write Enable ($\overline{WE}$) input is LOW, the data is entered into the addressed location. The addressed location remains transparent to the data while the $\overline{WE}$ is LOW. Data supplied at the inputs will be read out in true (non-inverting) form from the 3-State outputs. Data and Write Address inputs are inhibited when $\overline{WE}$ is HIGH.

Direct acquisition of data stored in any of the four registers is made possible by individual Read Address inputs (R_A and R_B). The addressed word appears at the four outputs when the Read Enable ($\overline{RE}$) is LOW. Data outputs are in the HIGH impedance "off" state when the Read Enable input is HIGH. This permits outputs to be tied together to increase the word capacity to very large numbers.

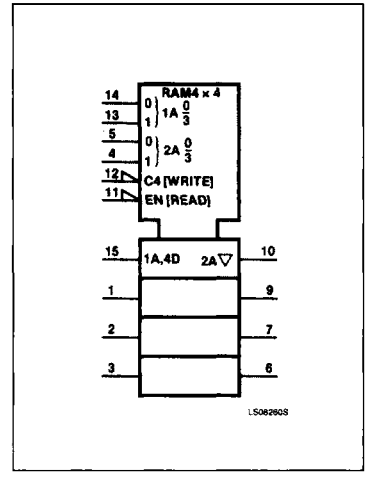
PIN CONFIGURATION



LOGIC SYMBOL



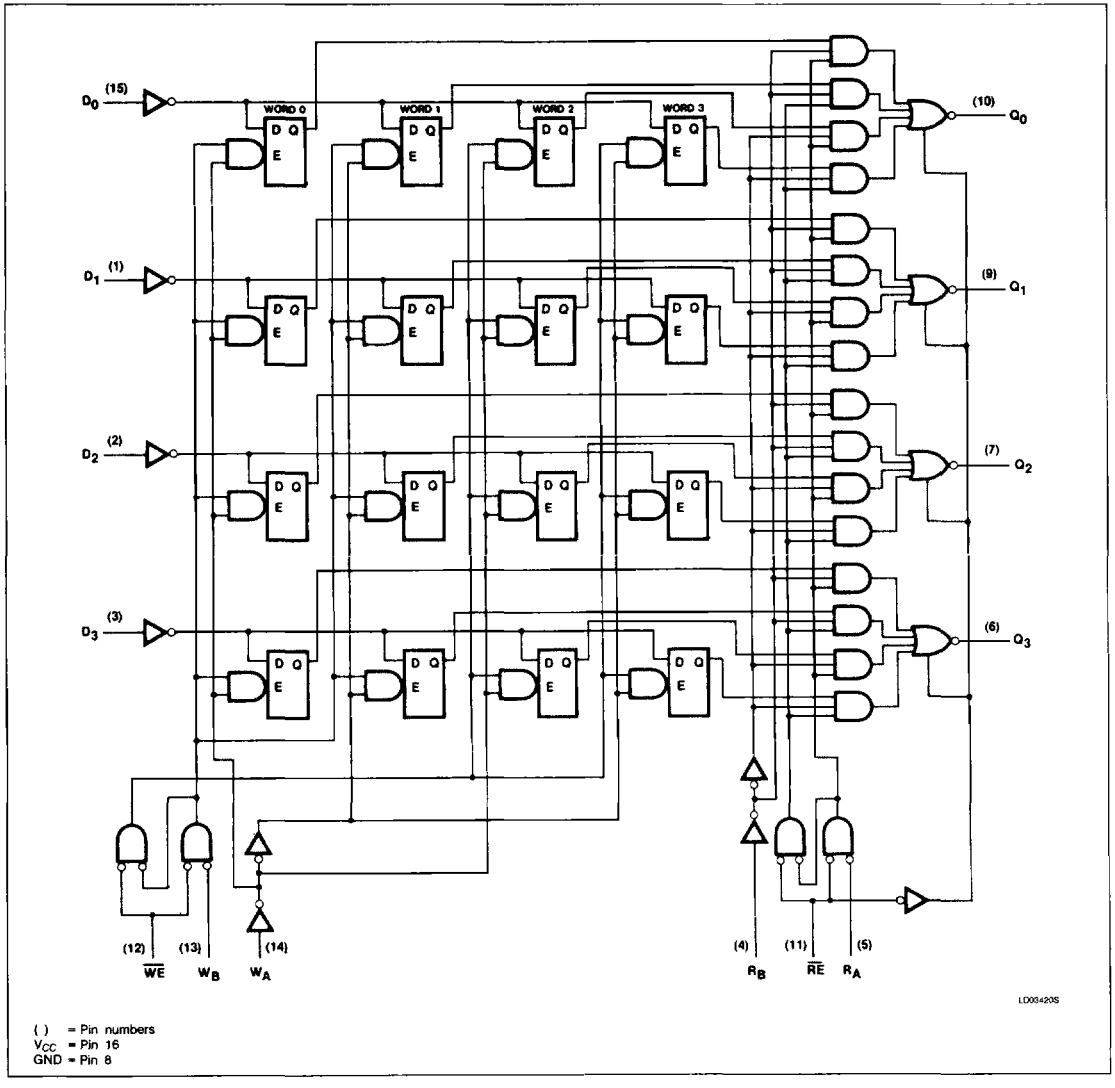
LOGIC SYMBOL (IEEE/IEC)



Register File | 74LS670

Up to 128 devices can be stacked to increase the word size to 512 locations by tying the 3-State outputs together. Since the limiting factor for expansion is the output HIGH current, further stacking is possible by tying pull-up resistors to the outputs to increase the I_{OH} current available. Design of the Read Enable signals for the stacked devices must ensure that there is no overlap in the LOW levels which would cause more than one output to be active at the same time. Parallel expansion to generate n-bit words is accomplished by driving the Enable and Address inputs of each device in parallel.

LOGIC DIAGRAM



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WRITE MODE SELECT TABLE

OPERATING MODE	INPUTS		INTERNAL LATCHES[a]
	$\overline{WE}$	D_n	
Write data	L L	L H	L H
Data latched	H	X	no change

NOTE:

a. The Write Address (W_A and W_B) to the "internal latches" must be stable while $\overline{WE}$ is LOW for conventional operation.

READ MODE SELECT TABLE

OPERATING MODE	INPUTS		OUTPUT Q_n
	$\overline{RE}$	Internal Latches[b]	
Read	L L	L H	L H
Disabled	H	X	(Z)

NOTE:

b. The selection of the "internal latches" by Read Address (R_A and R_B) are not constrained by $\overline{WE}$ or $\overline{RE}$ operation.

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance "off" state.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74LS	UNIT
V_{CC}	Supply voltage	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74LS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			+0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	HIGH-level output current			−2.6	mA
I_{OL}	LOW-level output current			8	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		74LS670			UNIT
				Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		2.4	3.1		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX		0.35	0.5	V
			I_{OL} = 4mA (74LS)		0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				−1.5	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 2.7V				20	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 0.4V				−20	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V	$D_0 - D_3$, W_A, W_B, R_A, R_B inputs			0.1	mA
			$\overline{WE}$ input			0.2	mA
			$\overline{RE}$ input			0.3	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V	$D_0 - D_3$, W_A, W_B, R_A, R_B inputs			20	μA
			$\overline{WE}$ input			40	μA
			$\overline{RE}$ input			60	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V	$D_0 - D_3$, W_A, W_B, R_A, R_B inputs			−0.4	mA
			$\overline{WE}$ input			−0.8	mA
			$\overline{RE}$ input			−1.2	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		−20		−100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX			30	50	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with 4.5V applied to all Data inputs and Read Enable and Write Enable inputs, ground Read Address and Write Address inputs and leave all outputs open. This is a worse-case condition.

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	74LS670 C_L = 15pF, R_L = 2kΩ		UNIT
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay Read address to output	Waveform 2		40 45	ns
t_{PLH} t_{PHL}	Propagation delay Write enable to output	Waveform 1		45 50	ns
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 1		45 40	ns
t_{PZH}	Enable time to HIGH level	Waveform 3		35	ns
t_{PZL}	Enable time to LOW level	Waveform 3		40	ns
t_{PHZ}	Disable time from HIGH level	Waveform 3, C_L = 5pF		50	ns
t_{PLZ}	Disable time from LOW level	Waveform 3, C_L = 5pF		35	ns

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AC SET-UP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

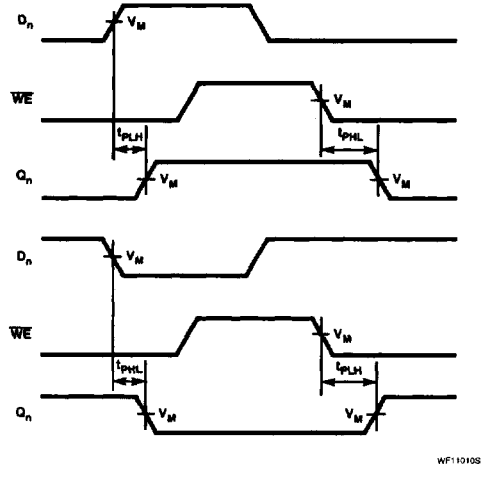
PARAMETER		TEST CONDITIONS	74LS670		UNIT
			Min	Max	
t_W	Read enable pulse width	Waveform 3	25		ns
t_W	Write enable pulse width	Waveform 2, $\overline{RE} = \leqslant 0.8V$	25		ns
t_S	Set-up time, data to positive-going $\overline{WE}$	Waveform 2	10		ns
t_h	Hold time, data to positive-going $\overline{WE}$	Waveform 2	15		ns
t_S	Set-up time, write address to negative-going $\overline{WE}$[c]	Waveform 2	15		ns
t_h	Hold time, write address to positive-going $\overline{WE}$[c]	Waveform 2	5.0		ns
t_{latch}	Latch time for new data[d]	Waveform 2	25		ns

NOTES:

c. Write address set-up time will protect the data written into the previous address. If protection of data in the previous address is not required, t_S (write address to $\overline{WE}$) can be ignored, as any address selection sustained for the final 30ns of the $\overline{WE}$ pulse and during t_h (write address to $\overline{WE}$) will result in data being written into that location. Depending on the duration of the input conditions, one or a number of previous addresses may have been written into.

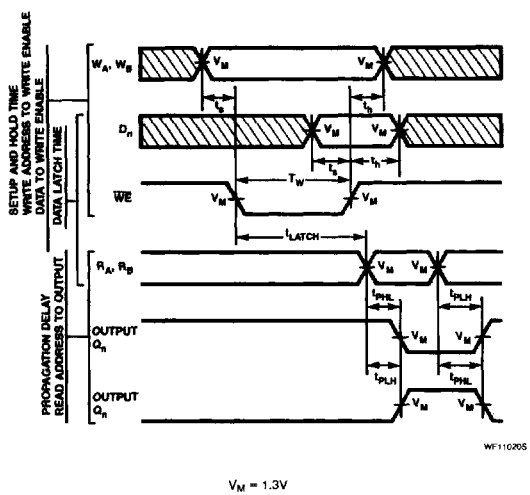
d. Latch time is the time allowed for the internal output of the latch to assume the state of new data. This is important only when attempting to read from a location immediately after that location has received new data. This parameter is measured from the falling edge of $\overline{WE}$ to the rising or falling edge of R_A or R_B. $\overline{RE}$ must be LOW.

AC WAVEFORMS



$V_M = 1.3V$

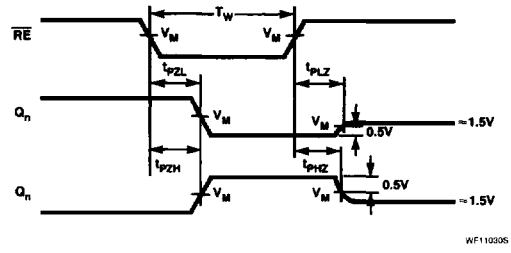
Waveform 1. Propagation Delay, Write Enable And Data To Outputs



$V_M = 1.3V$

Waveform 2. Set-up And Hold Times, Write Address To Write Enable, Data Latch Time, And Propagation Delay Read Address To Output

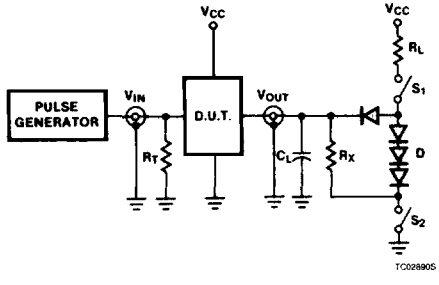
AC WAVEFORMS (Continued)



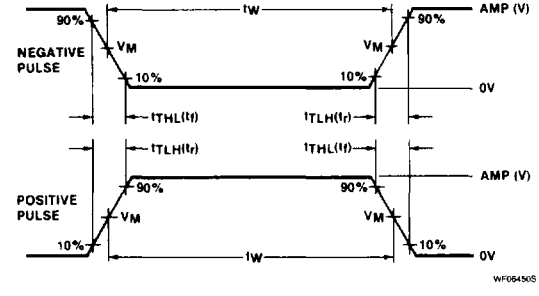
V_M = 1.3V

Waveform 3. 3-State Enable Time To High Or Low Level Disable Time From High Or Low Level

TEST CIRCUITS AND WAVEFORMS



Test Circuit For 3-State Outputs



V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH 1	SWITCH 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

R_X = 1kΩ for 74, 74S, R_X = 5kΩ for 74LS.

t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

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