Data Sheet

For **NT68665/NT68625**

Flat Panel Monitor Controller

Preliminary
V 0.40

2006-01-06

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1. Revision History

NT68665/NT68625 Specification Revision History		
Version	**Content**	**Data**
0.40	Pin out assignment changed	Jan. 2006
0.30	Added BF3 and HDCP	Dec. 2005
0.20	Proposal Ⅱ Spec.	Sep. 2005
0.11	Proposal I Spec.	Aug. 2005
0.10	Original Spec.	Jul. 2005

2. FEATURES

Analog Graphic Input
♦ Integrated triple high speed ADC/PLL
♦ 0.55V to 0.9V Analog input range
♦ Supports both non-interlaced and interlaced input signals
♦ 64 steps of phase adjust for each RGB channel
♦ Sampling rate up to 110MHz for X type, 165MHz for E type
♦ 500 MHz programmable analog bandwidth

Digital Graphic Input
♦ Integrated single link DVI receiver
♦ Direct connect to all DVI compliant TMDS transmitters
♦ Operating up to 165MHz
♦ Supports High-Bandwidth Digital Protection (HDCP)
♦ Supports Encryption HDCP secret key

Digital Video Input
♦ Supports ITU-R BT.656 8-bit Input format
♦ Built-in YUV to RGB color space converter
♦ Spatial de-interlace

Video Processing
♦ Independent horizontal and vertical zoom and shrink
♦ Auto-calibration function for quick video positioning, clock tracking and phase adjust
♦ Programmable H-sync pulse guard window prevents the position detecting errors
♦ Enhancement Back-end brightness, Contrast, Hue, Saturation and Sharpness adjust
♦ Built-in adaptive Noise Reduction function
♦ Built-in Post Pattern generator
♦ Support Bright Frame III function for window media enhancement adjust, that have automatic contrast & brightness adjustment, color correction and color enhancement on regional picture

Sync Processor
♦ Support TTL Sync-On-Green (SOG) (including Sync Slicer)
♦ Polarity detection
♦ Frequency measurement
♦ Fast mode change detection
♦ Interlace or non-interlace input detection
♦ Separate or composite sync auto switching (including Sync Separator)

Internal OSD
♦ Programmable multi-color RAM font as well as a bitmapped graphical OSD are supported
♦ Provide 184 programmable 1 bits/pixel RAM Fonts, 64 programmable 2 bits/pixel RAM Fonts, 8 programmable 4 bits/pixel RAM Fonts
♦ Optional 10x18, 12x18, 10x16, 12x16 dot matrix
♦ Internal SRAM allows up to 2048 characters, with programmable OSD frame size. Width is 64 column, and Height is 32 row
♦ Programmable shadow or border control for each character by each row
♦ Programmable blinking effects for each character
♦ Spacing control to avoid expansion distortion

- ♦ Supports simultaneous display of up to 4 OSD windows
- ♦ Maximum 4 times of global zoom for horizontal and vertical axis
- ♦ Separate row zoom control
- ♦ Support flexible FG or BG optional transparent, translucent, and opaque effects
- ♦ 256 palette with 64K color selectable
- ♦ Top-bottom flip, left-right mirror and 90 degree / 270 degree rotated
- ♦ Flexible Fade-in, Fade-out effect
- ♦ Splitting OSD frame supported

Display Output

- ♦ Supports single pixel or dual pixel output
- ♦ Multi-output interface RSDS/LVDS supported
- ♦ Spread spectrum clock (SSC) output, output signals drive current and slew rate control for low EMI
- ♦ Dithering function supports 24-bit quality for 18-bit panel
- ♦ Optional Frame Sync or Free Run display synchronization modes
- ♦ 10-bit programmable gamma correction
- ♦ 2 channel PWM output for LCD back-light control or volume control
- ♦ Display resolution up to SXGA
- ♦ Supports sRGB input

Built-in Dual Pixel LVDS Transmitter

- ♦ Integrate the Dual Port, 4 Data Channel and Clock-Out Low-Voltage differential LVDS transmitter to supports single or dual pixel 6/8-bit display data transmission
- ♦ Suited for VGA, SVGA, XGA and dual pixel SXGA, UXGA display transmission from controller to display with very low EMI

Built-in Panel Timing Controller

- ♦ Integrate the timing control (TCON) to supports single or dual port column drivers
- ♦ Integrate RSDS transmitter to supports RSDS differential output for RSDS Column Drivers
- ♦ 8 Programmable General Purpose Output provide customized for standard or in-house column drivers and row drivers
- ♦ Flexible flicker detection for 2-line dot inversion

Embedded 8031 On-Chip Microcontroller

- ♦ 8031 8-bit CMOS Micro-Processor (uP) core
- ♦ On-Chip Oscillator ⇨ 12MHz~15MHz operating frequency
- ♦ 64K/128K bytes of on-chip flash memory for program memory, 2K bytes of Mask ROM for ISP control function and 1,280/1792 Bytes On-Chip RAM
- ♦ 4 channels 7-Bit resolution A/D Converter
- ♦ 37 Selectable General Purpose I/O Pins
- ♦ 10 selectable output channels PWM D/A Converter
- ♦ 5-vector interrupt structure with two programmable priority levels for uP F8031
- ♦ Two built-in master/slave I^{2}C bus interfaces support VESA DDC 2Bi/2B+/CI
- ♦ Two DDC2Bi with Selectable 128/256 Bytes EDID-Buffer to internal RAM

MCU Interface

- ♦ High speed serial 2-wire IIC bus

Power

- ♦ 3.3V power supply

♦ Built-in 3.3V to 1.8V LDO regulator

♦ Normal operate less than 1.5 W

♦ Power down less than 50 mW

Package

♦ QFP 128 pin

3. General Description

The NT68665/NT68625 is a highly integrated flat panel display controller that interfaces analog, digital, and video inputs. It combines a triple ADC, a DVI compliant TMDS receiver, a digital YUV receiver, a high quality zoom and shrink engine, a multi-color on screen display (OSD) controller and many other functions in a single chip. It provides the user with a simple, flexible and cost-effective solution for various flat panel display products.

The NT68665/NT68625 operates at frequencies up to 165MHz, suitable for LCD monitor up to SXGA resolution. By using alternate sampling technology, the supported analog input resolution can be extended to UXGA mode.

The NT68665/NT68625 also has a built-in noise reduction function to provide more stable video quality, spread spectrum to provide low EMI solution, sRGB for video color space convert and post pattern for manufacture test.

The display provided multi-interface with timing controller or without timing controller. With timing controller provided single/double pixel clock RSDS interface; without timing controller provide single/double pixel clock LVDS interface.

In addition, NT68665/NT68625 includes an integrated 8-Bit Microcontroller (MCU). It contains an 8-bit 8031 micro-controller, on-chip 64K/128K bytes flash-type program ROM, 1,280-bytes internal data memory, four 7-bit resolution A/D Converter, 10-channel 8-bit resolution PWM DAC, two16-bit timer/counters, and a UART. Except those, it has two-channel hardware DDC solution, and VESA 2Bi/2B+ master/slave I^2C bus interface.
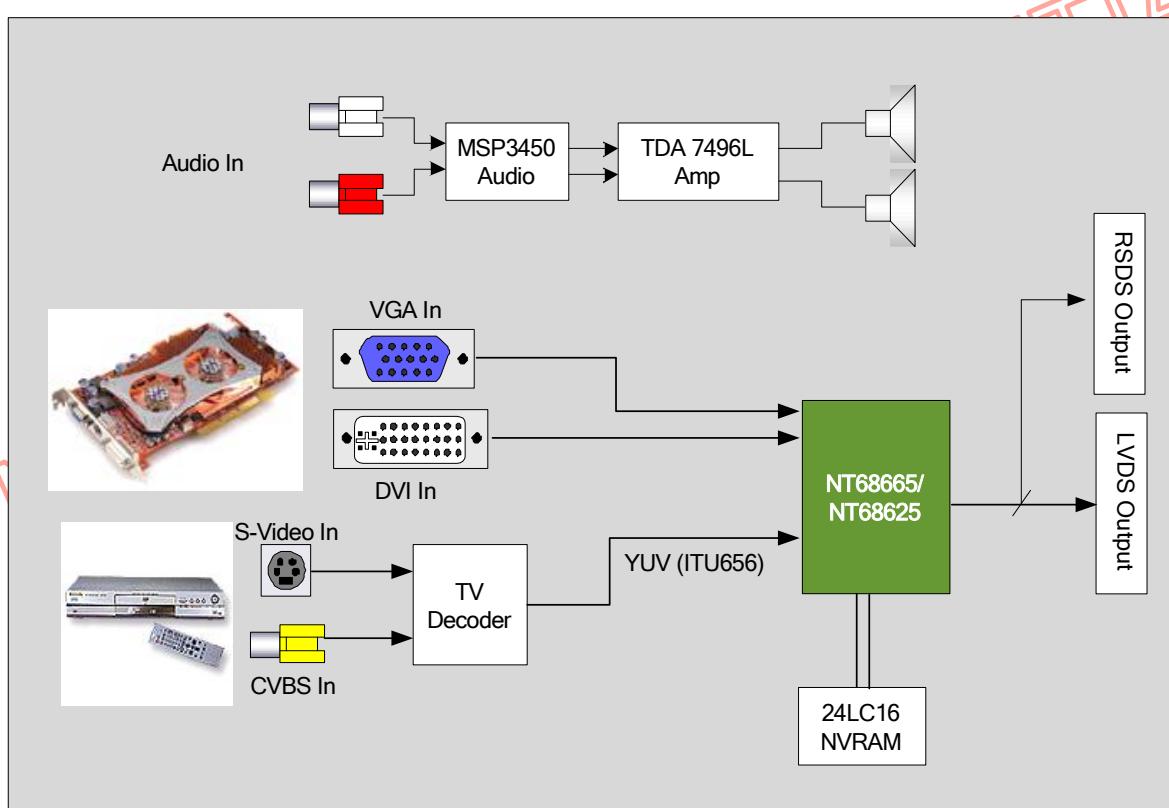
Figure 3-1 NT68665/NT68625 System Design Example

4. Block Diagram
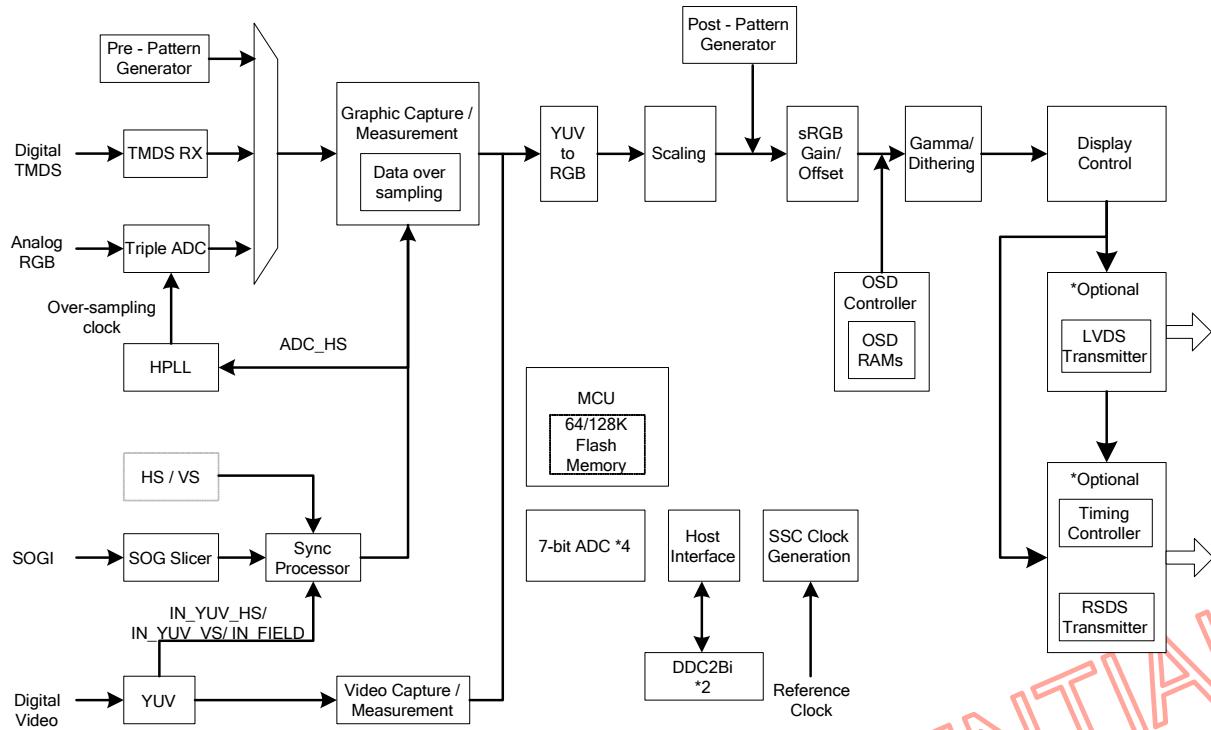
Figure 4-1 Functional Block Diagram

5. Pinout Information

5.1. Pin Diagram
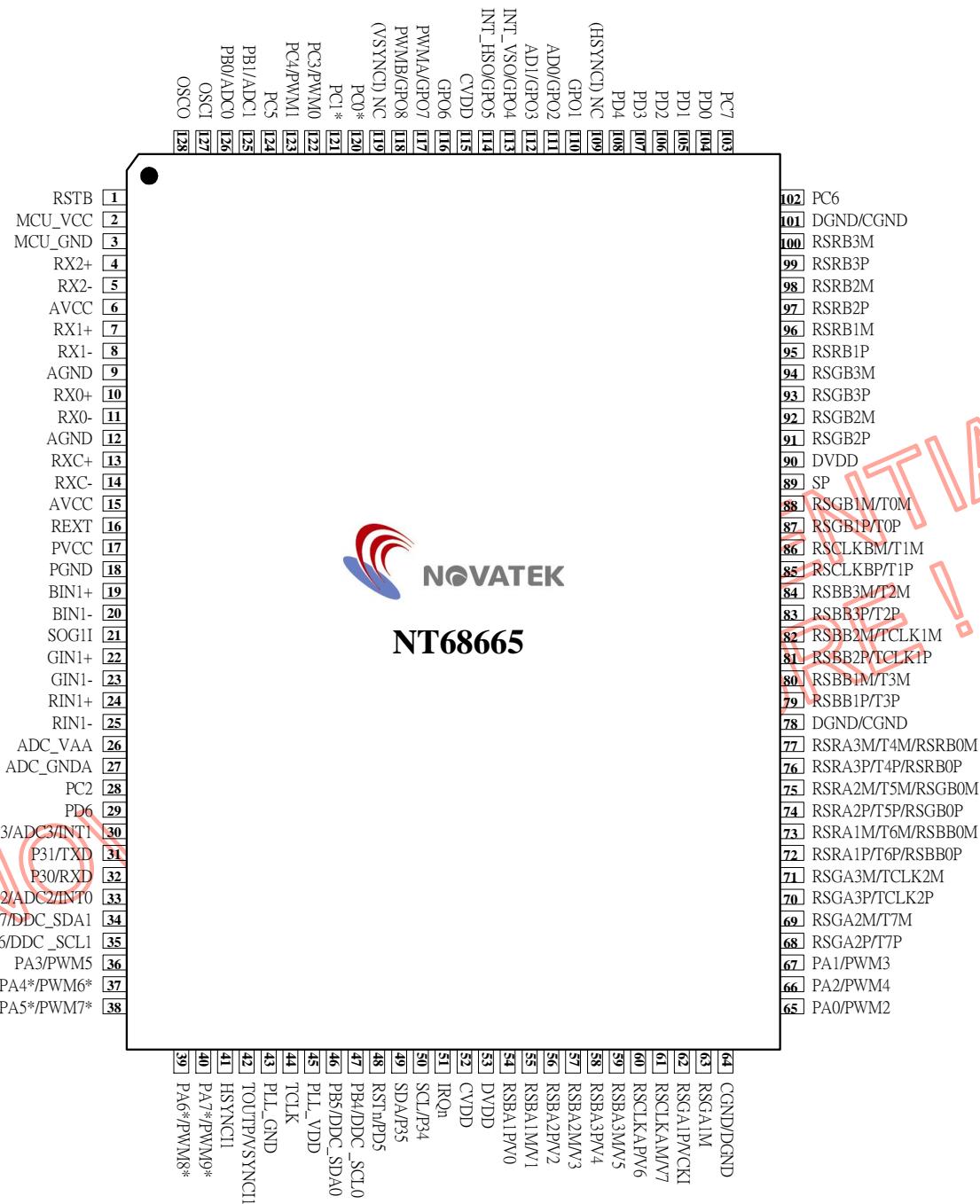
Figure 5.1-1 NT68665/NT68625 Pin Diagram

5.2. Pin Assignment

No.	Pin	Type	Definition
1	RSTB	I	Active-Low Reset Input; with Schmitt Trigger Input
2	MCU_VCC	Power	Micro-controller +3.3V Power Supply Input
3	MCU_GND	Power	Micro-controller Power Ground
4	RX2+	I	TMDS input channel 2+ (For NT68665 only)
5	RX2-	I	TMDS input channel 2- (For NT68665 only)
6	AVCC	Power	TMDS Analog VCC must be set to 3.3V.
7	RX1+	I	TMDS input channel 1+ (For NT68665 only)
8	RX1-	I	TMDS input channel 1- (For NT68665 only)
9	AGND	Power	TMDS Analog GND.
10	RX0+	I	TMDS input channel 0+ (For NT68665 only)
11	RX0-	I	TMDS input channel 0- (For NT68665 only)
12	AGND	Power	TMDS Analog GND.
13	RXC+	I	TMDS input clock pair (For NT68665 only)
14	RXC-	I	TMDS input clock pair (For NT68665 only)
15	AVCC	Power	TMDS Analog VCC must be set to 3.3V.
16	REXT	I	External termination resistor. A 1% 390 Ω resistor must be connected from this pin to AVCC.
17	PVCC	Power	TMDS PLL Analog VCC must be set to 3.3V.
18	PGND	Power	TMDS PLL Analog GND.
19	BIN1+	I	B channel positive analog video input
20	BIN1-	I	B channel negative analog video input
21	SOGI1	I	VGA Port Sync On Green Input with Schmitt trigger
22	GIN1+	I	G channel positive analog video input
23	GIN1-	I	G channel negative analog video input
24	RIN1+	I	R channel positive analog video input
25	RIN1-	I	R channel negative analog video input
26	ADC_VAA	Power	ADC Analog power supply
27	ADC_GNDA	Power	ADC Analog ground
28	PC2	I/O	I/O Pin; Push-Pull Structure with Schmitt Trigger Input
29	PD6	I/O	I/O Pin; Push-Pull Structure with Schmitt Trigger Input
30	PB3	I/O	I/O Pin; Push-Pull Structure with Schmitt Trigger Input
	ADC3	I	A/D Converter Input-3; Hi-Z input
	INTE1	I	External Interrupt input 1; Schmitt Trigger Input
31	P31	I/O	GPIO Port-31 of Micro-Processor F8031
	TXD	O	UART TX Data Output of Micro-Processor F8031
32	P30	I/O	GPIO Port-30 of Micro-Processor F8031
	RXD	I	UART RX Data Input of Micro-Processor F8031
33	PB2	I/O	I/O Pin; Push-Pull Structure with Schmitt Trigger Input
	ADC2	I	A/D Converter Input-2; Hi-Z input
	INTE0	I	External Interrupt input 0, Schmitt Trigger Input

34	PB7*	I/O	I/O Pin; Open-Drain with Schmitt Trigger Input
	DDC_SDA1*	I/O	5V Open-Drain Serial Data I/O Pin for the DDC Port 1 and the slave/master I^{2}C-Bus Port 1
35	PB6*	I/O	5V I/O Pin; Open-Drain with Schmitt Trigger Input
	DDC_SCL1*	I/O	5V Open-Drain Serial Clock I/O Pin for the DDC Port 1 and the slave/master I^{2}C-Bus Port 1
36	PA3	I/O	I/O Pin; Schmitt Trigger Input
	PWM5	O	PWM-Type D/A Converter; 3.3V Push-Pull Structure
37	PA4*	I/O	I/O Pin; Open-Drain Structure with Schmitt Trigger Input
	PWM6*	O	PWM-Type D/A Converter; 5V Open-Drain Structure
38	PA5*	I/O	I/O Pin; Open-Drain Structure with Schmitt Trigger Input
	PWM7*	O	PWM-Type D/A Converter; 5V Open-Drain Structure
39	PA6*	I/O	I/O Pin; Open-Drain Structure with Schmitt Trigger Input
	PWM8*	O	PWM-Type D/A Converter; 5V Open-Drain Structure
40	PA7*	I/O	I/O Pin; Open-Drain Structure with Schmitt Trigger Input
	PWM9*	O	PWM-Type D/A Converter; 5V Open-Drain Structure
41	HSYNCI1	I	VGA Port Channel 1 Horizontal Sync Input with Schmitt trigger. (Schmitt triggered, 5V tolerant)
42	VSYNCI0/TOUTP	O	VGA Port Channel 1 Vertical Sync Input with Schmitt trigger / Testing pin for ADC (Schmitt triggered, 5V tolerant)
43	PLL_ GND	Power	Core Logic Ground pin for PLL.
44	TCLK	I	Reference clock Input
45	PLL_ VDD	Power	Core logic power supply (1.8V) pin for PLL. External capacitor (0.1uF) connected is recommended.
46	PB5*	I/O	5V I/O Pin; Open-Drain with Schmitt Trigger Input
	DDC_SDA0*/ HDCP_SDA	I/O	5V Open-Drain Serial Data I/O Pin for the DDC Port 0 and the slave/master I^{2}C-Bus Port 0/ For DVI HDCP communication interface Serial Data In/Out (5V tolerant)
47	PB4*	I/O	5V I/O Pin; Open-Drain with Schmitt Trigger Input
	DDC_SCL0*/ HDCP_SCL	I/O	5V Open-Drain Serial Clock I/O Pin for the DDC Port 0 and the slave/master I^{2}C-Bus Port 0/ For DVI HDCP communication interface Serial Clock (5V tolerant)
48	RSTn /PD5	I/O	System Reset; I/O Pin; Push-Pull Structure with Schmitt Trigger Input (5V tolerant)
49	SDA/P35	I/O	Host Interface Serial Data In/Out. Incorporate Schmitt trigger buffer & spike filter/ GPIO Port-35 of Micro-Processor F8031 (5V tolerant)
	T1	I	Counter/Timer T1 Input of Micro-Processor F8031
50	SCL	O	Host Interface Serial Clock. Incorporate Schmitt trigger buffer & spike filter (5V tolerant)
	P34	I/O	GPIO Port-34 of Micro-Processor F8031
	T0	I	Counter/Timer T0 Input of Micro-Processor F8031
51	IRQn	O	Interrupt Request
52	CVDD	Power	Core logic power supply (1.8V) pin. External capacitor

			(0.1uF) connected is recommended.
53	DVDD	Power	Display Digital Power Supply
54	RSBA1P/ V0	RSDSO	Port A Blue data RSDS differential data 1 (Positive)/ Video data input
55	RSBA1M/ V1	RSDSO	Port A Blue data RSDS differential data 1 (Negative)/ Video data input
56	RSBA2P/ V2	RSDSO	Port A Blue data RSDS differential data 2 (Positive) / Video data input
57	RSBA2M/ V3	RSDSO	Port A Blue data RSDS differential data 2 (Negative)/ Video data input
58	RSBA3P/ V4	RSDSO	Port A Blue data RSDS differential data 3 (Positive) / Video data input
59	RSBA3M/ V5	RSDSO	Port A Blue data RSDS differential data 3 (Negative)/ Video data input
60	RSCLKAP/ V6	RSDSO	Port A Pixel clock RSDS differential positive/ Video data input
61	RSCLKAM/ V7	RSDSO	Port A Pixel clock RSDS differential Negative /Video data input
62	RSGA1P/ YUV_CLK	RSDSO	Port A Green data RSDS differential data 1 (Positive) /Video Port Clock
63	RSGA1M	RSDSO	Port A Green data RSDS differential data 1 (Negative)
64	DGND/CGND	Power	Digital Ground/ Core Logic Ground
65	PA0	I/O	I/O Pin; Schmitt Trigger Input
	PWM2	O	PWM-Type D/A Converter; 3.3V Push-Pull Structure
66	PA2	I/O	I/O Pin; Schmitt Trigger Input
	PWM4	O	PWM-Type D/A Converter; 3.3V Push-Pull Structure
67	PA1	I/O	I/O Pin; Schmitt Trigger Input
	PWM3	O	PWM-Type D/A Converter; 3.3V Push-Pull Structure
68	RSGA2P/T7P	RSDSO/ LVDSO/	Port A Green data RSDS differential data 2 (Positive)/ Positive LVDS differential data output of channel 7/
69	RSGA2M/T7M	RSDSO/ LVDSO/	Port A Green data RSDS differential data 2 (Negative)/ Negative LVDS differential data output of channel 7
70	RSGA3P/TCLK2P	RSDSO/ LVDSO/	Port A Green data RSDS differential data 3 (Positive)/ Positive LVDS differential clock 2 output
71	RSGA3M/TCLK2M	RSDSO/ LVDSO/	Port A Green data RSDS differential data 3 (Negative)/ Negative LVDS differential clock 2 output
72	RSRA1P/T6P/ RSBB0P	RSDSO/ LVDSO/	Port A Red data RSDS differential data 1 (Positive)/ Positive LVDS differential data output of channel 6
73	RSRA1M/T6M/ RSBB0M	RSDSO/ LVDSO/	Port A Red data RSDS differential data 1 (Negative)/ Negative LVDS differential data output of channel 6
74	RSRA2P/T5P/ RSGB0P	RSDSO/ LVDSO/	Port A Red data RSDS differential data 2 (Positive)/ Positive LVDS differential data output of channel 5
75	RSRA2M/T5M/ RSGB0M	RSDSO/ LVDSO/	Port A Red data RSDS differential data 2 (Negative)/ Negative LVDS differential data output of channel 5
76	RSRA3P/T4P/ RSRB0P	RSDSO/ LVDSO/	Port A Red data RSDS differential data 3 (Positive)/ Positive LVDS differential data output of channel 4
77	RSRA3M/T4M/ RSRB0M	RSDSO/ LVDSO/	Port A Red data RSDS differential data 3 (Negative)/ Negative LVDS differential data output of channel 4
78	DGND/CGND	Power	Digital Ground/ Core Logic Ground

79	RSBB1P/T3P	RSDSO/ LVDSO/	Port B Blue data RSDS differential data 1 (Positive)/ Positive LVDS differential data output of channel 3
80	RSBB1M/T3M	RSDSO/ LVDSO/	Port B Blue data RSDS differential data 1 (Negative)/ Negative LVDS differential data output of channel 3
81	RSBB2P/TCLK1P	RSDSO/ LVDSO/	Port B Blue data RSDS differential data 2 (Positive)/ Positive LVDS differential clock 1 output
82	RSBB2M/TCLK1M	RSDSO/ LVDSO/	Port B Blue data RSDS differential data 2 (Negative)/ Negative LVDS differential clock 1 output
83	RSBB3P/T2P	RSDSO/ LVDSO/	Port B Blue data RSDS differential data 3 (Positive)/ Positive LVDS differential data output of channel 2
84	RSBB3M/T2M	RSDSO/ LVDSO/	Port B Blue data RSDS differential data 3 (Negative)/ Negative LVDS differential data output of channel 2
85	RSCLKBP/T1P	RSDSO/ LVDSO/	Port A Pixel clock RSDS differential positive/ Positive LVDS differential data output of channel 1
86	RSCLKBM/T1M	RSDSO/ LVDSO/	Port A Pixel clock RSDS differential Negative/ Negative LVDS differential data output of channel 1
87	RSGB1P/T0P	RSDSO/ LVDSO/	Port B Green data RSDS differential data 1 (Positive)/ Positive LVDS differential data output of channel 0/ Display Red data 2 output
88	RSGB1M/T0M	RSDSO/ LVDSO/	Port B Green data RSDS differential data 1 (Negative)/ Negative LVDS differential data output of channel 0
89	SP	O	Start pulse for panel source driver
90	DVDD	Power	Display Digital Power Supply
91	RSGB2P	RSDSO	Port B Green data RSDS differential data 2 (Positive
92	RSGB2M	RSDSO	Port B Green data RSDS differential data 2 (Negative
93	RSGB3P	RSDSO	Port B Green data RSDS differential data 3 (Positive
94	RSGB3M	RSDSO	Port B Green data RSDS differential data 3 (Negative
95	RSRB1P	RSDSO	Port B Red data RSDS differential data 1 (Positive)
96	RSRB1M	RSDSO	Port B Red data RSDS differential data 1 (Negative
97	RSRB2P	RSDSO	Port B Red data RSDS differential data 2 (Positive
98	RSRB2M	RSDSO	Port B Red data RSDS differential data 2 (Negative
99	RSRB3P	RSDSO	Port B Red data RSDS differential data 3 (Positive
100	RSRB3M	RSDSO	Port B Red data RSDS differential data 3 (Negative
101	DGND/CGND	Power	Digital Ground/ Core Logic Ground
102	PC6	I/O	I/O Pin; Push-Pull Structure with Schmitt Trigger Input
103	PC7	I/O	I/O Pin; Push-Pull Structure with Schmitt Trigger Input
104	PD0	I/O	I/O Pin; Push-Pull Structure with Schmitt Trigger Input
105	PD1	I/O	I/O Pin; Push-Pull Structure with Schmitt Trigger Input
106	PD2	I/O	I/O Pin; Push-Pull Structure with Schmitt Trigger Input
107	PD3	I/O	I/O Pin; Push-Pull Structure with Schmitt Trigger Input
108	PD4	I/O	I/O Pin; Push-Pull Structure with Schmitt Trigger Input
109	NC	I/O	MCU HSYNCI test pin
110	GPO1	TTL O	General purpose output for panel driver
111	GPO2	TTL O	General purpose output
112	GPO3	TTL O	General purpose output
113	INT_VSO/GPO4	O	Internal Vertical Sync output, this signal is by-pass the Sync-processor/ General purpose output

114	INT_HSO/GPO5	O	Internal Horizontal Sync output, this signal is by-pass the Sync-processor / General purpose output
115	CVDD	Power	Core logic power supply (1.8V) pin. External capacitor (0.1uF) connected is recommended.
116	GPO6	O	General purpose output
117	PWMA/GPO7	O	PWMA/ General purpose output
118	PWMB/GPO8	O	PWMB/ General purpose output
119	NC	I/O	MCU VSYNCI test pin
120	PC0*	I/O	I/O Pin; 5V Open-Drain Structure with Schmitt Trigger Input
121	PC1*	I/O	I/O Pin; 5V Open-Drain Structure with Schmitt Trigger Input
122	PC3	I/O	I/O Pin; Push-Pull Structure with Schmitt Trigger Input
	PWM0	O	PWM-Type D/A Converter; Push-Pull Structure
123	PC4	I/O	I/O Pin; Push-Pull Structure with Schmitt Trigger Input
	PWM1	O	PWM-Type D/A Converter; Push-Pull Structure
124	PC5	I/O	I/O Pin; Push-Pull Structure with Schmitt Trigger Input
125	PB1/ADC1	I/O	I/O Pin; Push-Pull Structure with Schmitt Trigger Input A/D Converter Input-1; Hi-Z input
126	PB0/ADC0	I/O	I/O Pin; Push-Pull Structure with Schmitt Trigger Input A/D Converter Input-0; Hi-Z input
127	OSCO	O	12MHz External Crystal OSC Output
128	OSCI	I	12MHz External Crystal OSC Input

Table 5.2-1 Pin List

5.3. Pin Description

System Interface

Pin	Type	Pin No.	Drive	Definition
TCLK	I	44		Reference clock Input
IRQn	O	51	4 mA	Interrupt Request
RSTn	I (5V tolerant)	48		System Reset
SDA	I (5V tolerant)	49		Host Interface Serial Data In/Out.
SCL	I/O (5V tolerant)	48		Host Interface Serial Clock.

Graphic Analog Interface

Pin	Type	Pin No.	Drive	Definition
ADC_GNDA	Power	27		B channel ADC analog ground
ADC_VAA	Power	26		B channel ADC analog power supply
BIN1+	I	19		B channel positive analog video input
BIN1-	I	20		B channel negative analog video input
SOGI1	I	21		VGA Port 1 Sync On Green Input with Schmitt trigger
GIN1+	I	22		G channel positive analog video input

GIN1-	I	23		G channel negative analog video input
RIN1+	I	24		R channel positive analog video input
RIN1-	I	25		R channel negative analog video input
HSYNCI1	I (5V tolerant)	41		VGA Port Horizontal Sync Input with Schmitt trigger
VSYNCI1	I (5V tolerant)	42		VGA Port Vertical Sync Input with Schmitt trigger

Graphic TMDS Interface (For NT68665 only)

Pin	Type	Pin No.	Drive	Definition
RX2+	I	4		TMDS input channel 2+
RX2-	I	5		TMDS input channel 2-
RX1+	I	7		TMDS input channel 1+
RX1-	I	8		TMDS input channel 1-
RX0+	I	10		TMDS input channel 0+
RX0-	I	11		TMDS input channel 0-
RXC+	I	13		TMDS input clock pair
RXC-	I	14		TMDS input clock pair
REXT	I	16		External termination resistor. A 1% 470 ohm resistor must be connected from this pin to AVCC.
AVCC	Power	6,15		TMDS Analog VCC must be set to 3.3V.
AGND	Power	9,12		TMDS Analog GND.
PVCC	Power	17		TMDS PLL Analog VCC must be set to 3.3V.
PGND	Power	18		TMDS PLL Analog GND.

LVDS Panel Interface

Pin Name	Pin Type	Pin No.	Pin Count	Pin Function
T0M	LVDSO	88	1	Negative LVDS differential data output of channel 0
T0P	LVDSO	87	1	Positive LVDS differential data output of channel 0
T1M	LVDSO	86	1	Negative LVDS differential data output of channel 1
T1P	LVDSO	85	1	Positive LVDS differential data output of channel 1
T2M	LVDSO	84	1	Negative LVDS differential data output of channel 2
T2P	LVDSO	83	1	Positive LVDS differential data output of channel 2
TCLK1M	LVDSO	82	1	Negative LVDS differential clock 1 output
TCLK1P	LVDSO	81	1	Positive LVDS differential clock 1 output
T3M	LVDSO	80	1	Negative LVDS differential data output of channel 3
T3P	LVDSO	79	1	Positive LVDS differential data output of channel 3
T4M	LVDSO	77	1	Negative LVDS differential data output of channel 4
T4P	LVDSO	76	1	Positive LVDS differential data output of channel 4
T5M	LVDSO	75	1	Negative LVDS differential data output of channel 5
T5P	LVDSO	74	1	Positive LVDS differential data output of channel 5
T6M	LVDSO	73	1	Negative LVDS differential data output of channel 6
T6P	LVDSO	72	1	Positive LVDS differential data output of channel 6
TCLK2M	LVDSO	71	1	Negative LVDS differential clock 2 output
TCLK2P	LVDSO	70	1	Positive LVDS differential clock 2 output
T7M	LVDSO	69	1	Negative LVDS differential data output of channel 7
T7P	LVDSO	68	1	Positive LVDS differential data output of channel 7

GPO Interface

Pin	Type	Pin No.	Drive	Definition
GPO1~GPO3	O	110,111,112		General-purpose output signal
GPO4/ VSO / INT_VSO	O	113		General-purpose output signal / Sync-processor Vertical Sync output / Internal Vertical Sync output, this signal is by-pass the Sync-processor
GPO5/ HSO/ INT_HSO	O	114		General-purpose output signal / Sync-processor Horizontal Sync output / Internal Horizontal Sync output, this signal is by-pass the Sync-processor
GPO6	O	116		General-purpose output signal
GPO7/PWMA	O	117		PWMA/General purpose input/output signal
GPO8/PWMB	O	118		PWMB/General purpose input/output signal

Video ITU-R BT656 Interface

Pin	Type	Pin No.	Drive	Definition
V0~V7	O	54~61		Video Port Data[7:0] input
VCLK	O	62		Video Port Clock

TCON PANEL I/F Pin Description – RSDS Mode

Pin Name	Pin Type	Pin No.	Pin Count	Pin Function
SP	TTL O	89	1	Sstart pulse for panel source driver
GPO[1:5]	TTL O	110~114	1	General purpose output for panel driver
GPO[6:8]	TTL O	116~118	1	General purpose output for panel driver
RSCLKAP	RSDSO	62	1	Port A Pixel clock RSDS differential positive
RSCLKAM	RSDSO	61	1	Port A Pixel clock RSDS differential negative
RSRA[1:3]±	RSDSO	72~77	6	Port A Red data RSDS differential pair 1~3
RSGA[1:3]±	RSDSO	62,63,68~71	6	Port A Green data RSDS differential pair 1~3
RSBA[1:3]±	RSDSO	54~59	6	Port A Blue data RSDS differential pair 1~3
RSCLKBP	RSDSO	85	1	Port B Pixel clock RSDS differential positive
RSCLKBM	RSDSO	86	1	Port B Pixel clock RSDS differential negative
RSRB[1:3]±	RSDSO	79~84	6	Port B Red data RSDS differential pair 1~3
RSGB[1:3]±	RSDSO	87,88,91~94	6	Port B Green data RSDS differential pair 1~3
RSBB[1:3]±	RSDSO	95~100	6	Port B Blue data RSDS differential pair 1~3
RSRB[0]±	RSDSO	76,77	2	Port B Red data RSDS differential pair 0
RSGB[0]±	RSDSO	74,75	2	Port B Green data RSDS differential pair 0
RSBB[0]±	RSDSO	72,73	2	Port B Blue data RSDS differential pair 0

Power Pin

Pin	Type	Pin No.	Drive	Definition
CVDD	Power	52, 115		Core logic power supply (1.8V) pin. External capacitor (0.1uF) connected is recommended.
CGND /DVDD	Power	64,78,101		Core Logic Ground /Display Digital Power Supply

PLL_VDD	Power	45		Core logic power supply (1.8V) pin for PLL. External capacitor (0.1uF) connected is recommended.
PLL_GND	Power	43		Core Logic Ground pin for PLL.
AVCC	Power	6,15		TMDS Analog VCC must be set to 3.3V.
AGND	Power	9,12		TMDS Analog GND.
PVCC	Power	17		TMDS PLL Analog VCC must be set to 3.3V.
PGND	Power	18		TMDS PLL Analog GND.
ADC_VAA	Power	26		ADC analog power supply
ADC_GNDA	Power	27		ADC analog ground
MCU_VCC	Power	2		Micro-controller +3.3V Power Supply Input
MCU_GND	Power	3		Micro-controller Power Ground

6. Functional Description

6.1. Power Control

NT68665/NT68625 supports the whole chip power down function. By setting the CHIP_PWDN bit to '1', NT68665/NT68625 will go into power down state except the **I2C** logic and **Sync-processor (include SOG Slicer, and TMDS Sync Detect)** will keep alive.
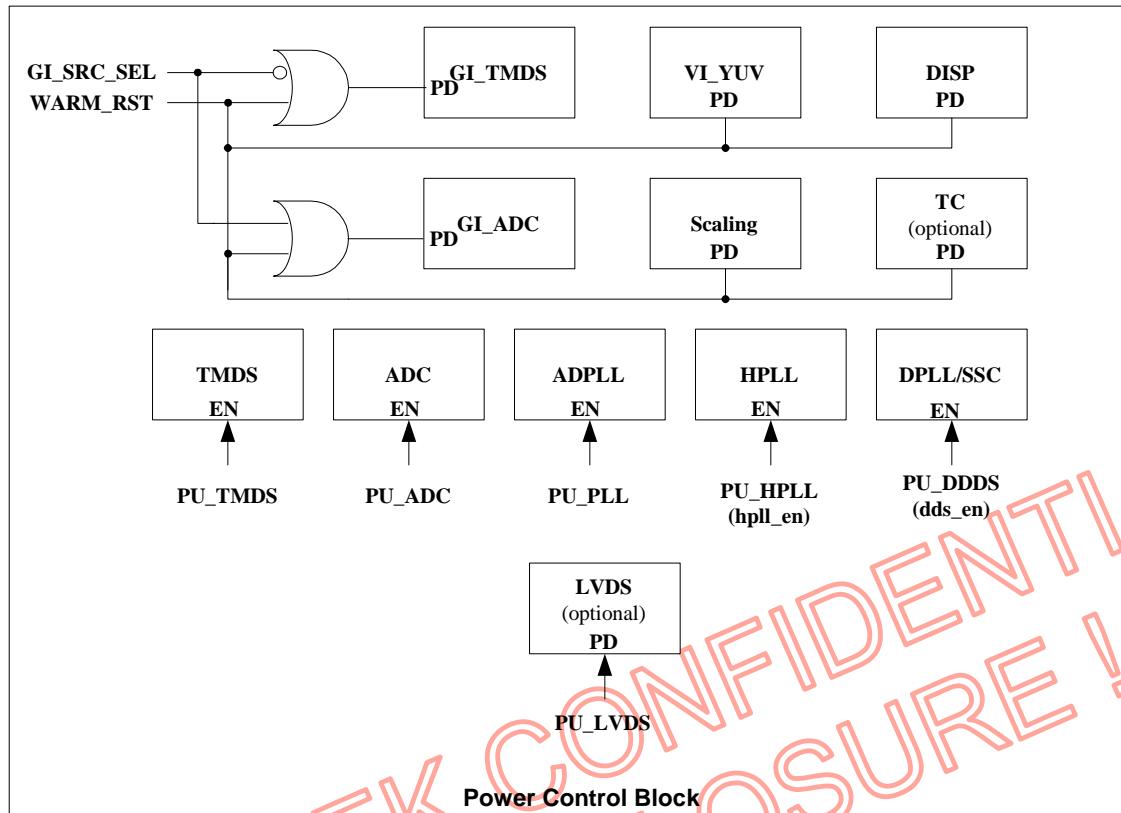
Figure 6.1-1 Power Control Block

6.2. Analog to Digital Converter (ADC)

NT68665/NT68625 provides a clock-recovery circuit and an analog-to-digital converter to effectively save the cost of needing external expensive ADC and PLL. The gain and offset circuit is used to adjust the gain (Contrast) of input video amplitude and shift the DC offset voltage (Brightness). The clock-recovery circuit consisting of a high-speed phase lock loop (PLL) is used to generate the clock to sample analog RGB data. This circuit is locked to the HSYNC of the incoming video signal. The analog-to-digital converter (ADC) transfers the input analog RGB video to digital output data with each color 8-bit resolution.

Gain and Offset Control

RIN/GIN/BIN are high-impedance input pins that accept the RED, GREEN, and BLUE channel graphics signals. They accommodate input signals ranging from 0.55V to 0.9V full scale. Signals should be AC-couple to these pins.

Due to AC coupling, clamping pulse is needed to define the time during which the input signal is clamped to ground, establishing a black reference. Typically the clamping pulse is defined during the back porch period of the graphics signal. NT68665/NT68625 generates the clamping pulse internally

and the position and duration are programmable. The simpler clamp-timing generator clamping pulse-starting position and pulse width is defined in 0x021[7:0] and 0x022[7:0].

NT68665/NT68625 has three independent variable gain amplifiers for each channel with input signal range from 0.55V to 0.9V（p-p）, the full-scale range is set in three 9-bit registers. NT68665/NT68625's offset control shifts the entire input range, resulting in a change in image brightness. The three independent variable 8-bit registers provide independent settings for each channel.

Clamp Pulse generator
This block circuit called **Clamp pulse generator** generates clamp pulse to ADC. There are two input trigger sources of the clamp generator, one is signal **Hin** from separator and another is Row **Hs** from the HSYNCI0 / HSYNCI1. The polarity and the trigger edge of the **clamp** can be selected by using bit CLMP_POL and bit CLMP_EDG respectively. The trigger delay of the **clamp** is waiting **CLMP_BEG [5:0]** x REFCLK time. The pulse width of the **clamp** output may be selected by **CLMP_WID [5:0]**.

➢ *Clamp Pulse Timing*
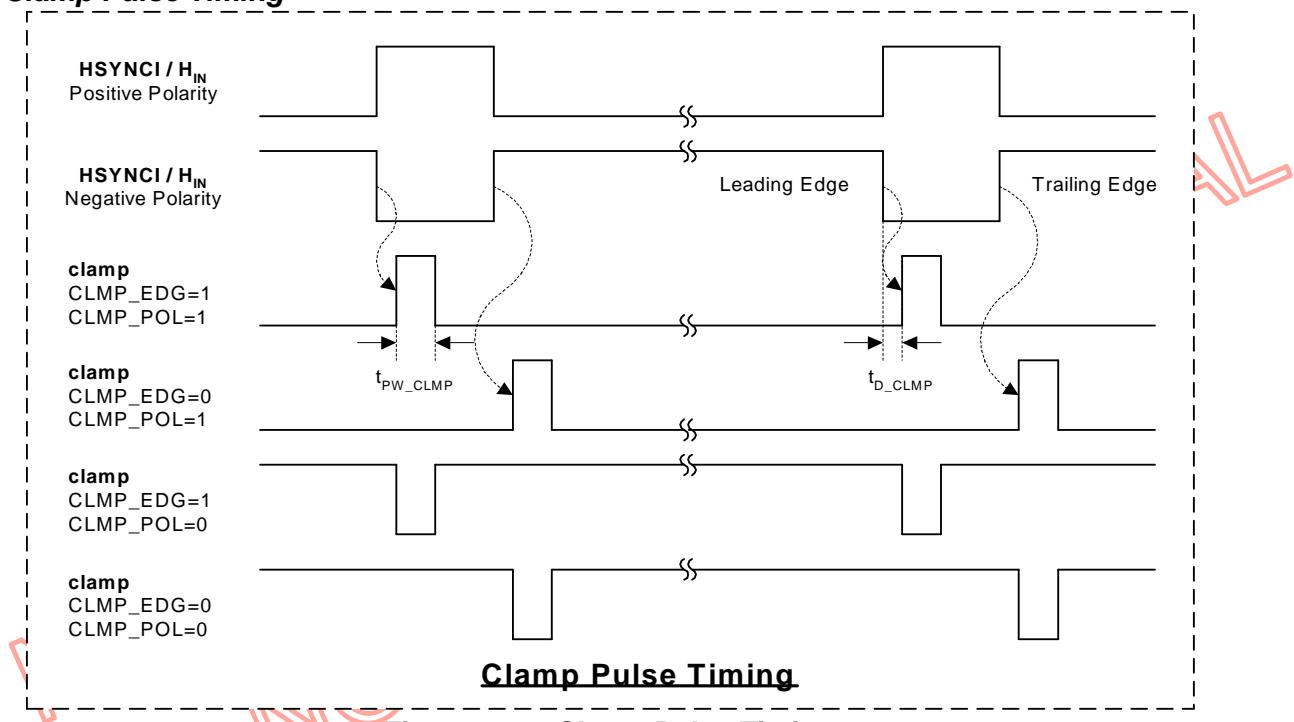
Figure 6.2-1 Clamp Pulse Timing

COAST
This function is used to cause the pixel clock generator to stop synchronizing with Hsync and continues producing a clock at its current frequency and phase. This is useful when processing composite sync that fails to produce horizontal sync pulses when in the vertical interval.

6.3. DVI Receiver

The DVI receiver uses Panel Link Digital technology to support input ranging from VGA to UXGA (25-165 MHz), which is ideal for desktop and specialty applications.

6.4. Graphic Port Capture Interface

The function of Graphic Port Capture Interface is to provide two interfaces between NT68665/NT68625 and external input devices. It can process non-interlaced and interlaced RGB graphic input, and DVI input. User should select the video input source from Graphic Port (VGA or DVI) and the polarity of external control signal, and then program the H/V captures size registers to indicate the display area.

6.5. Video Port Capture Interface

The function of Video Port Capture Interface is to provide Digital YUV interface between NT68665/NT68625 and video decoder. It can process non-interlaced and interlaced digital YUV video ITU BT656 input. It includes color space conversion for YUV to RGB color space conversion.

6.6. Auto Tune

The Auto Tune function consists of Auto Gain, Auto Position, and Auto Phase. With such auto adjustment support it is possible to measure the correct phase, frequency, gain, and offset of ADC. The horizontal and vertical back porches of input image and the horizontal and vertical active regions can also be measured.
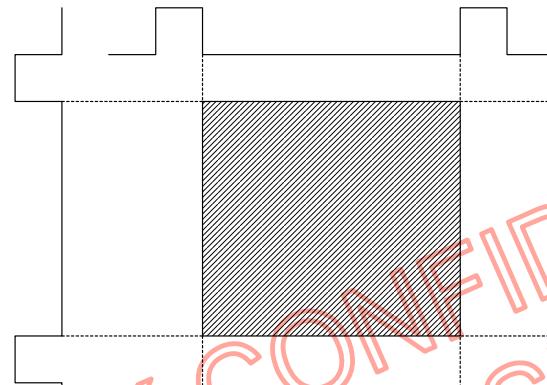
Figure 6.6-1 DISP_AUTO = 0
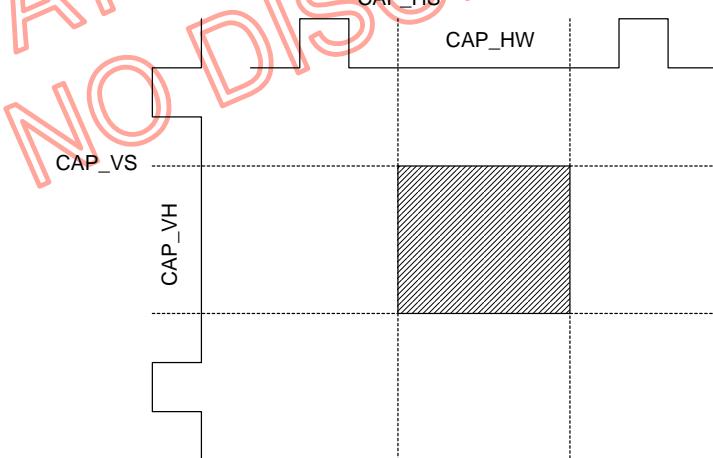
Figure 6.6-2 DISP_AUTO

Auto Gain

Gain value is the Minimum or Maximum pixel value within the specified input image region for each RGB channel. This function is useful for measuring the noise margin of input video or for auto-contrast calibrating by adjusting ADC' s offset and gain.

Programming Steps:

Reference application notice

Auto Position

NT68665/NT68625 provides Horizontal/Vertical back porch and active region information. Users can use these values to set input capture registers to aid in centering the screen automatically, and adjust the ADCPLL's divider value to figure out the correct input pixel frequency.

Programming Steps:

Reference application notice

Auto Clock

Programming Steps:

Reference application notice

Auto Phase

Programming Steps:

Reference application notice

6.7. Video Processor

Video processor consists of Interpolation Control, RGB Gain Control, RGB Offset Control, Hue and Saturation Control, Dithering Control, Gamma Correction Control and sRGB Support.
NT68665/NT68625's enhanced interpolation method makes the zoomed display image look more smooth and comfortable.

User can adjust the RGB Gain (Contrast) and RGB Offset (Brightness) by the registers in the ADCPLL block, or registers in the Video processor block. But for YUV video input, it is suitable to adjust Contrast and Brightness at here. In addition, it supports all YUV color controls including brightness, contrast, hue and saturation.

Dithering function can provide 16.7 million colors space for 6-bit/color panel. It is recommended to open the dithering function while a 6-bit panel is used.

68665 provide independently horizontal and vertical zoom scaler with adjustable zoom factor from 1/4x to 4x. Each of the zoom scaler uses variable sharpness filter to provide high quality scaling of real-time video and still graphic images.

Interpolation
1. Flexible Sharpness Filter
68665 include flexible sharpness filter for horizontal and vertical sharpness adjusting. Users can use them by register programming.
2. Vertical Spatial Interpolation
When interlaced video or images are applied, the 68665 vertical scaling engines will de-interlace the input fields spatially and reposition them to align the display's line map.
3. Advanced Filter
With the aid of two selectable advanced filters when zooming up horizontally, 68665 provides the most undistorted image from the original one.

sRGB Support
sRGB is a standard for color exchange proposed by Microsoft and HP. The sRGB controls can be used to make LCD monitors sRGB compliant.

$$
\begin{bmatrix} R'_{sRGB} \\ G'_{sRGB} \\ B'_{sRGB} \end{bmatrix} = \begin{bmatrix} A0 & B0 & C0 \\ A1 & B1 & C1 \\ A2 & B2 & C2 \end{bmatrix} \begin{bmatrix} R_{sRGB} \\ G_{sRGB} \\ B_{sRGB} \end{bmatrix} + \begin{bmatrix} Offset_R \\ Offset_G \\ Offset_B \end{bmatrix} \text{-------------------------------[1]}
$$

Gamma Correction
♦ Provides 10-bit gamma correction function
♦ Hardware piecewise simulation method
♦ F/W needs to define total 256 end-point value in advance
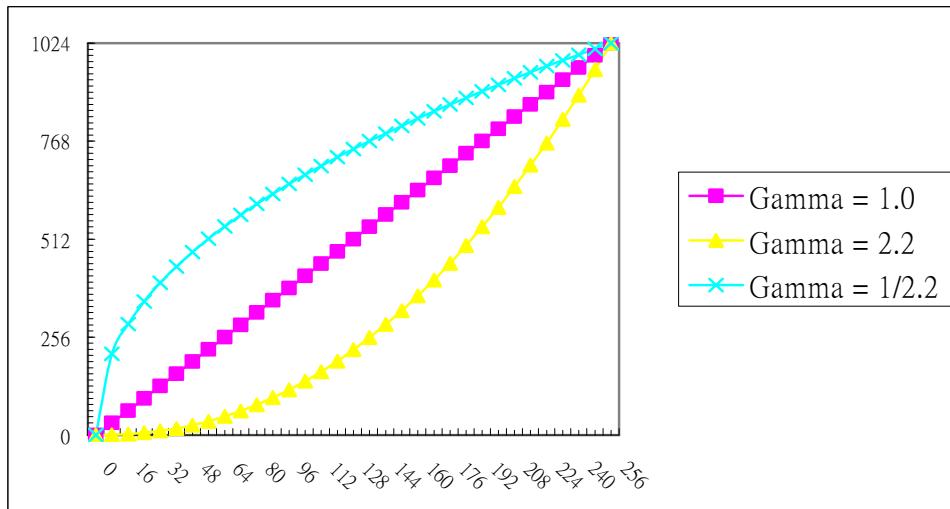
Figure 6.7-1 Gamma Correction Curve

Index Address	Gamma Table	Value
0		LSB0 (2 bits)+MSB0 (8 bits)
1		LSB1+MSB1
2		LSB2+MSB2
….	….	
254		LSB254+MSB254
255		LSB255+MSB255

6.8. Sync Processor

The NT68665/NT68625 has a Sync Processor block providing the capability of measuring the horizontal and vertical timing parameters of the input video source. This information may be used to determine the video format and to detect a change in the input timing. It is also capable of detecting the field type of interlaced formats.

Hsync /Vsync Frequency and Polarity Detection

GI_HCNT, the 13 bits Hsync period counter counts the time of 32xHSYNC period, then loads the result into the GI_HCNT latch. The output value will be $[((REFCLK / 4 \times 32)/HFreq)]$, updated once per VSYNC/CVSYNC period when VSYNC/CVSYNC is present or continuously updated when VSYNC/CVSYNC is non-present.

GI_VCNT, the 13 bits Vsync period counter counts the time between two VSYNC pulses, then loads the result into the GI_VCNT latch. The output value will be $[(REFCLK/(256 \times Vfreq))]$, updated every VSYNC/CVSYNC period. An extra overflow bit indicates the condition of H/V counter overflow. The polarity functions detect the input HSYNC/VSYNC high and low pulse duty cycle. If the high pulse duration is longer than that of the low pulse, the negative polarity is asserted; otherwise, positive polarity is asserted. The INT_HPOL interrupt is set when the GI_HPOL value changes. The INT_VPOL interrupt is set when the GI_VPOL value changes.

H/V Present Check

The Hsync present function checks the input HSYNCI pulse, GI_HPRE flag is set when HSYNCI is over HSYNC Present High Counter Threshold (HPRE_THR_HI) or cleared when HSYNC is under HSYNC Present Low Counter Threshold (HPRE_THR_LO). The Vsync present function checks the input VSYNCI pulse, the GI_VPRE flag is set when VSYNCI is over VSYNC Present High Counter Threshold (VPRE_THR_HI) or cleared when VSYNC is under VSYNC Present Low Counter Threshold (VPRE_THR_LO). The INT_HPRE interrupt is set when the GI_HPRE value changes. The INT_VPRE interrupt is set when the GI_VPRE /GI_CSPRE value change.

Timing Change Detection

The INT_VFREQ/INT_HFREQ interrupt is set when GI_VCNT / GI_HCNT value changes or overflows.

Extract Vsync from Composite/SOG Signal
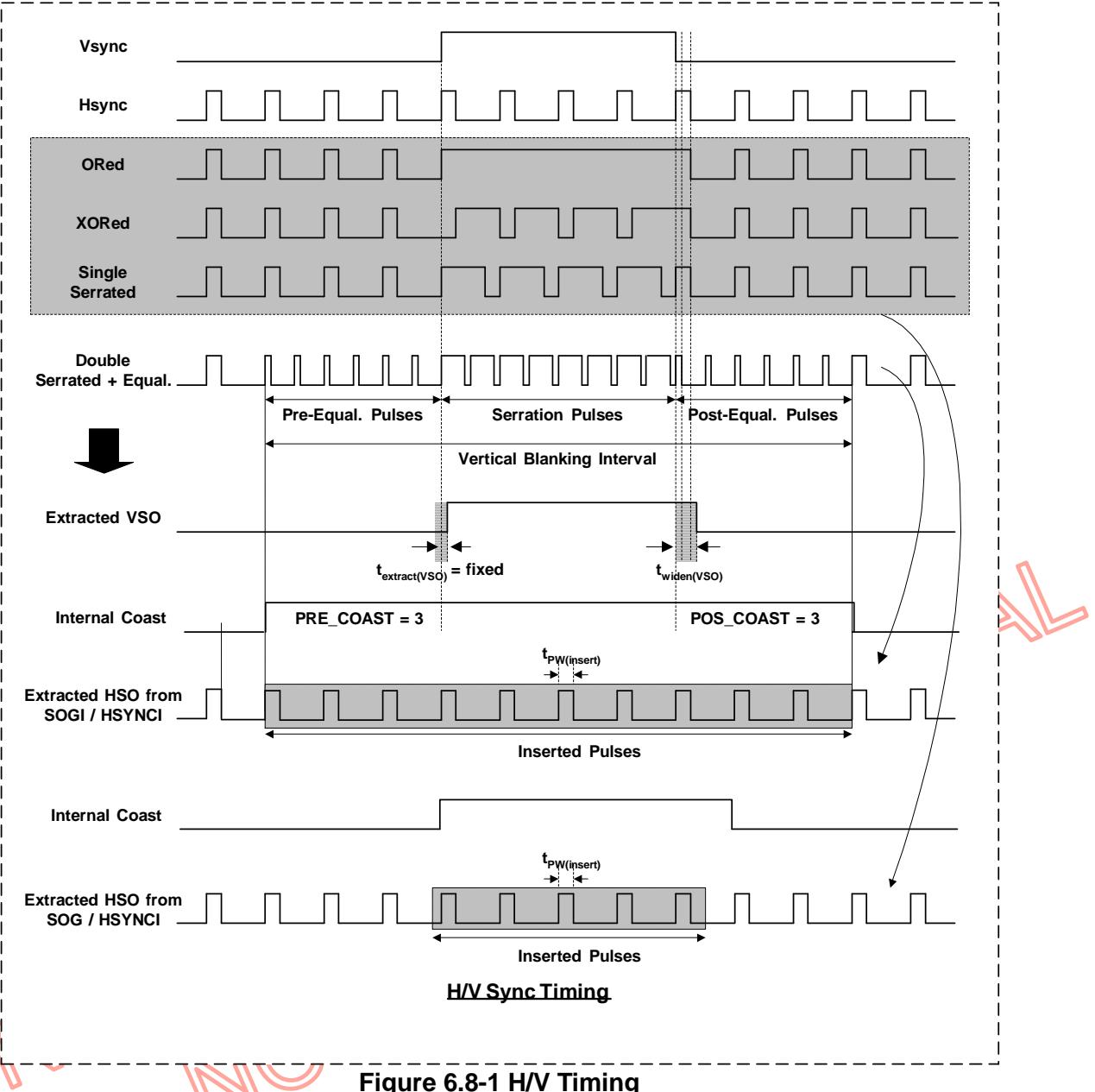
Figure 6.8-1 H/V Timing

Internal Odd/Even Field Detection

Included in the sync detector is circuitry to determine which field is currently being input for interlaced input. To determine the field based on position of VSYNC relative to HSYNC, the GI_FLD_WINBEG (3:0) and GI_FLD_WINEND (3:0) registers are used for Graphic Port and the VI_FLD_WINBEG (3:0) and VI_FLD_WINEND (3:0) registers are used for Video Port. The NT68665/NT68625 divides each horizontal line into 16 equal intervals. The FLD_WINBEG bits are used to specify at which 1/16th of a line to start looking for the leading edge of VSYNC. The FLD_WINEND bits are used to specify at which 1/16th of a line to stop looking. If the leading edge of VSYNC occurs between during or after the 1/16th line specified by FLD_WINBEG, but no later than the 1/16th line specified by FLD_WINEND, the current field is marked as odd. Otherwise, a leading edge transition outside these boundaries will cause the current field to be marked even.
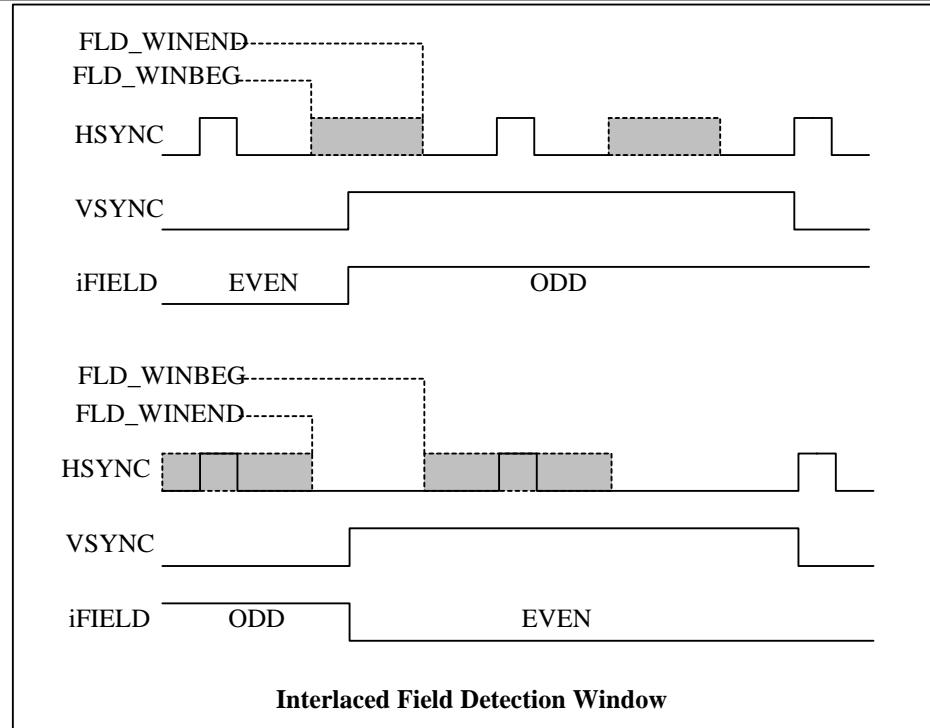
Figure 6.8-2 Interlaced Field Detection Window

Free Run Timing Generator

This Block can generate various free-running outputs to satisfy various application requirements. The pulse width of the H_{FREE} output is fixed **15 x REFCLK** and the V_{FREE} is **3 HFREEs**. User can properly set the content of HSO Free Run divider, HFREE_DIV, to get the need frequency of the HSO, and set the content VSO Free Run divider, VFREE_DIV, to get the frequency of the VSO. Details refer to the descriptions of the free-run registers HFREE_DIV and VFREE_DIV. Refer to the descriptions of the register for details to get user's need frequencies.

Users can disable H/V free run output by clearing GI_HRUN_EN /GI_VRUN_EN.

Sync On Green Slicer

This function is provided to assist with processing signals with embedded sync, typically on the GIN channel. The circuit sliced the signals that with embedded sync, and apply to Sync Separator for extracting Hsync and Vsync.

6.9. OSD Function

NT68665/NT68625 supports internal OSD with following features:

- Programmable Multi-color RAM font OSD
- Totally 184 programmable 1 bits/pixel RAM Fonts, 64 programmable 2 bits/pixel RAM Fonts, and 8 programmable 4 bits/pixel RAM Fonts
- Character attributes for 1, 2, 4 bits/pixel
- Optional 10x18, 12x18 Font Matrix Selection
- Internal SRAM allows up to 2048 characters
- Fully Programmable Character Array of 32 Rows by 64 Columns
- 256 palette up to 64K resolution for each R/G/B colors
- Up to 256-Color Selection from a 64K color palette with Color Intensity Attribute on Each Character
- True 256-Color Selection from a 64K color palette for Windows
- Shadowing on Windows with Programmable Shadow Width/Height/Color
- Row To Row and Column To Column Spacing Control to Avoid Expansion Distortion
- Four Programmable Windows with Overlapping Capability
- Programmable Bordering or Shadowing for each character by each row
- Programmable blinking effects for each character
- Background Translucent, transparent, and opaque effects
- Programmable Vertical and Horizontal Positioning for Display
- Each OSD row can be independently zoomed up to 4 times for horizontal and vertical axis
- Top-bottom flip, left-right mirror and 90 degree / 270 degree rotated
- Maximum Pixel CLK of UXGA resolution
- Fade In / Fade Out effect

OSD Font's Attribute and Code Format, Palette Format Definition:

OSD Palette Format

15:11	10:5	4:0
R	G	B

OSD Code Format

7:0
Font Index

OSD Attribute Format

15:8	7:4	3:2	1	0
PA_Index [7:0]	BG_Index [3:0]	CA_Bit	Mix	Blink

Figure 6.9-1

- Blink : 0 - No blinking
  - 1 - Blinking (All color is blinking except background color)
- Mix : 0 - Normal
  - 1 - Translucent ((1- TP_LEVEL) Display + (TP_LEVEL) OSD_BG)
- CA_Bit [1:0] : Character attribute bits/pixel number
  - 00: one bit/pixel color Font (0-255 font index)
  - 01: one bit/pixel color Font (256-511 font index)
  - 10: two-bits/pixel color Font
  - 11: four bits/pixel color Font
- PA_Index [7:0] / BG_Index [3:0]: Attribute color palette index

Case A: Pixel is outside an active window
One Bit per pixel.
　　Foreground '1' Pixel [7:0] <= PA_Index [7:0] + 1
　　Background '0' Pixel [7:0] <= 0x00 + BG_Index [3:0] (See below Note)

Two Bit per pixel.
　　Foreground '11' Pixel [7:0] <= PA_Index [7:0] + '11'
　　Foreground '10' Pixel [7:0] <= PA_Index [7:0] + '10'
　　Foreground '01' Pixel [7:0] <= PA_Index [7:0] + '01'
　　Background '00' Pixel [7:0] <= 0x00 + BG_Index [3:0] (See below Note)

Four Bit per pixel.
　　Foreground '1111' Pixel [7:0] <= PA_Index [7:0] + '1111'
　　Foreground '1110' Pixel [7:0] <= PA_Index [7:0] + '1110'
　　Foreground '1101' Pixel [7:0] <= PA_Index [7:0] + '1101'
　　Foreground '1100' Pixel [7:0] <= PA_Index [7:0] + '1100'
　　Foreground '1011' Pixel [7:0] <= PA_Index [7:0] + '1011'
　　Foreground '1010' Pixel [7:0] <= PA_Index [7:0] + '1010'
　　Foreground '1001' Pixel [7:0] <= PA_Index [7:0] + '1001'
　　Foreground '1000' Pixel [7:0] <= PA_Index [7:0] + '1000'
　　Foreground '0111' Pixel [7:0] <= PA_Index [7:0] + '0111'
　　Foreground '0110' Pixel [7:0] <= PA_Index [7:0] + '0110'
　　Foreground '0101' Pixel [7:0] <= PA_Index [7:0] + '0101'
　　Foreground '0100' Pixel [7:0] <= PA_Index [7:0] + '0100'
　　Foreground '0011' Pixel [7:0] <= PA_Index [7:0] + '0011'
　　Foreground '0010' Pixel [7:0] <= PA_Index [7:0] + '0010'
　　Foreground '0001' Pixel [7:0] <= PA_Index [7:0] + '0001'
　　Background '0000' Pixel [7:0] <= 0x00 + BG_Index [3:0] (See below Note)

　　Note: If BG_Index [3:0] = "0000", indicates that this background color is transparent
　　　　If BG_Index [3:0] = "0001", Background '0000' Pixel [7:0] <= PA_Index [7:0]

Case B: Pixel is inside an active window

One Bit per pixel.
　　Foreground '1' Pixel [7:0] <= PA_Index [7:0] + '1'
　　Background '0' Pixel [7:0] <= WINx_ATTR [7:0]

Two Bit per pixel.
　　Foreground '11' Pixel [7:0] <= PA_Index [7:0] + '11'
　　Foreground '10' Pixel [7:0] <= PA_Index [7:0] + '10'
　　Foreground '01' Pixel [7:0] <= PA_Index [7:0] + '01'
　　Background '00' Pixel [7:0] <= WINx_ATTR [7:0]

Four Bit per pixel.
　　Foreground '1111' Pixel [7:0] <= PA_Index [7:0] + '1111'
　　Foreground '1110' Pixel [7:0] <= PA_Index [7:0] + '1110'

Foreground '1101' Pixel [7:0] <= PA_Index [7:0] + '1101'
Foreground '1100' Pixel [7:0] <= PA_Index [7:0] + '1100'
Foreground '1011' Pixel [7:0] <= PA_Index [7:0] + '1011'
Foreground '1010' Pixel [7:0] <= PA_Index [7:0] + '1010'
Foreground '1001' Pixel [7:0] <= PA_Index [7:0] + '1001'
Foreground '1000' Pixel [7:0] <= PA_Index [7:0] + '1000'
Foreground '0111' Pixel [7:0] <= PA_Index [7:0] + '0111'
Foreground '0110' Pixel [7:0] <= PA_Index [7:0] + '0110'
Foreground '0101' Pixel [7:0] <= PA_Index [7:0] + '0101'
Foreground '0100' Pixel [7:0] <= PA_Index [7:0] + '0100'
Foreground '0011' Pixel [7:0] <= PA_Index [7:0] + '0011'
Foreground '0010' Pixel [7:0] <= PA_Index [7:0] + '0010'
Foreground '0001' Pixel [7:0] <= PA_Index [7:0] + '0001'
Background '0000' Pixel [7:0] <= WINx_ATTR [7:0]

Palette Address and map
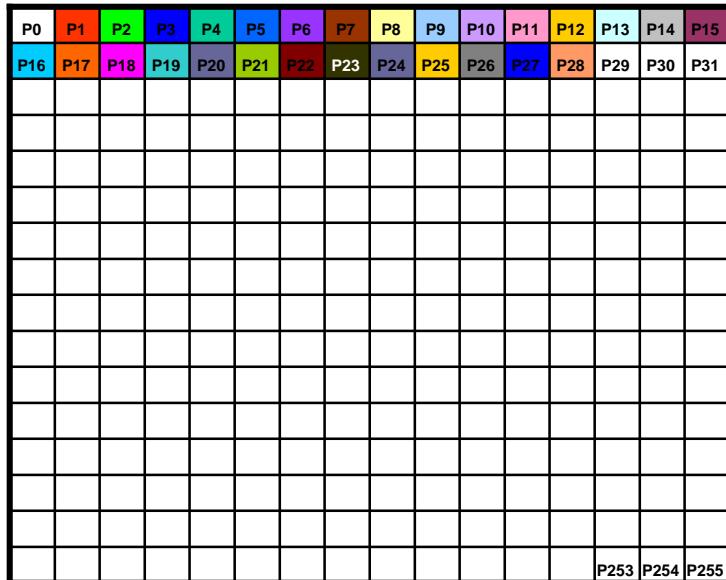
Figure 6.9-2 Palette

Palette N	Palette Address	Bits [15:11]	Bits [10:5]	Bits [4:0]
Palette 0	0 (0x00H)	R0 [4:0]	G0 [5:0]	B0 [4:0]
Palette 1	1 (0x01H)	R1 [4:0]	G1 [5:0]	B1 [4:0]
Palette 2	2 (0x02H)	R2 [4:0]	G2 [5:0]	B2 [4:0]
…	…			
Palette 15	15 (0x0FH)	R15 [4:0]	G15 [5:0]	B15 [4:0]
Palette 16	16 (0x04H)	R16 [4:0]	G16 [5:0]	B16 [4:0]
Palette 17	17 (0x05H)	R17 [4:0]	G17 [5:0]	B17 [4:0]
…	…			
Palette 254	254 (0xFEH)	R254 [4:0]	G254 [5:0]	B254 [4:0]
Palette 255	255 (0xFFH)	R255 [4:0]	G255 [5:0]	B255 [4:0]

Figure 6.9-3 Palette address and map

OSD Character Map
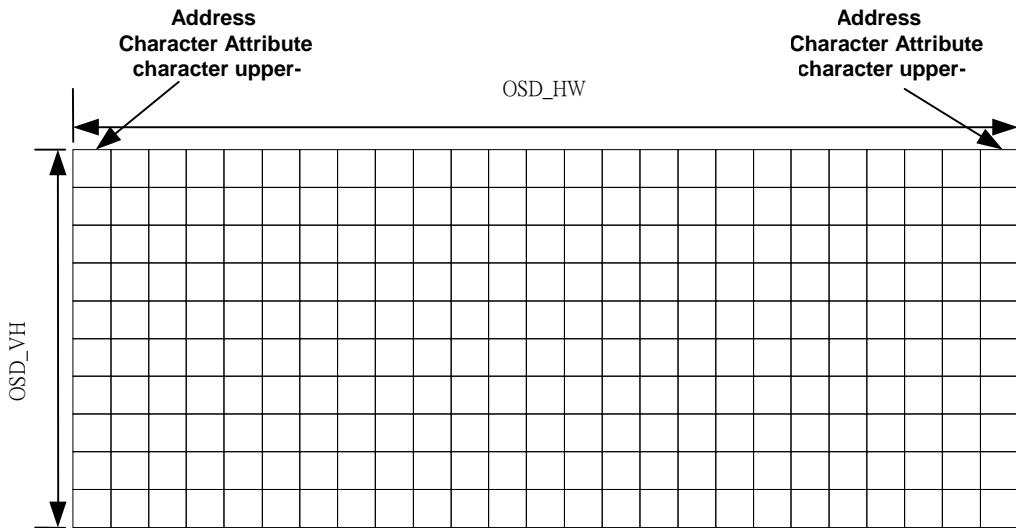
Figure 6.9-4 OSD Character Map

OSD Font Definitions
One Bit per pixel

One bit per pixel font definitions are arranged in Color Character Font SRAM Memory on a 12-bit by 18-address grid. The One bit per pixel OSD programmable font start address is specified in Register 0x089 ~ 0x088. Odd font definitions are stored in SRAM bits [11:0], and even font definitions are stored in SRAM bits [23:12].
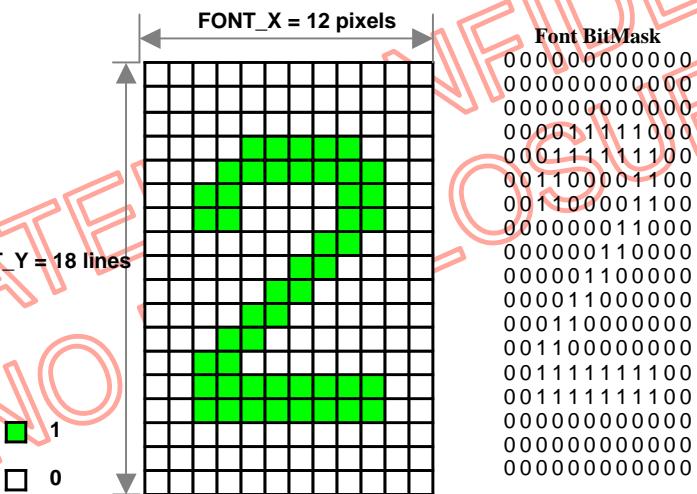
Figure 6.9-5 One Bit Per Pixel Font

Two Bit per pixel

Two bits per pixel font definitions are arranged in Color Character Font SRAM Memory on a 24-bit by 18 addresses. The two bit per pixel OSD programmable font start address is specified in Register 0x08B ~ 0x08A. Font definitions are stored in SRAM bits [23:0].


```
                FONT_X = 12 pixels
                                        Font Bit Mask
                                  000000000000000000000000
                                  000000000000000000000000
                                  000000000010101010000000
                                  000000000101010101100000
                                  000000010101010101011000
                                  000001010000000001011000
                                  000001010000000001011000
                                  000000000000000101100000
                                  000000000000010110000000
                                  000000000001011000000000
FONT_Y = 18 lines                 000000000101100000000000
                                  000000010110000000000000
                                  000001011010101010101010
                                  000001010101010101011000
         ■ 01                     000001010101010101011000
         □ 00                     000000000000000000000000
                                  111111111111111111111111
         ■ 10                     000000000000000000000000
         ■ 11
```

Figure 6.9-6 Two Bit Per Pixel Font

Four Bit per pixel

Four bits per pixel font definitions are arranged in Color Character Font SRAM Memory on a 24-bit by 36 addresses. The four bit per pixel OSD programmable font start address is specified in Register 0x08D ~ 0x08C. Each pixel row of a font contains up 12 pixels, with the font row broken up across two consecutive Color Character Font SRAM Memory addresses.


```
                FONT_X = 12 pixels
                                        Font BitMask
                                  0 1 2 3 4 5 6 7 8 9 a b
                                  c d e f 9 9 9 9 9 9 9 9
                                  0 0 0 0 0 1 1 1 1 0 0 0
                                  0 0 0 0 e e e e e 1 0 0
                                  0 0 0 e e e e e e e 1 0
                                  0 0 e e 0 0 0 0 e e 1 0
                                  0 0 e e 0 0 0 0 e e 1 0
                                  0 0 0 0 0 0 0 0 e e 1 0 0
                                  0 0 0 0 0 0 e e 1 0 0 0
FONT_Y = 18 lines                 0 0 0 0 0 e e 1 0 0 0 0
                                  0 0 0 0 e e 1 0 0 0 0 0
                                  0 0 0 e e 1 0 0 0 0 0 0
                                  0 0 e e 1 1 1 1 1 1 1 0
                                  0 0 e e e e e e e e 1 0
                                  0 0 e e e e e e e e 1 0
                                  0 0 0 0 0 0 0 0 0 0 0 0
                                  5 5 5 5 5 5 5 5 5 5 5 5
                                  0 0 0 0 0 0 0 0 0 0 0 0
```

Color key:
```
□ 0    ■ 8
■ 1    ■ 9
■ 2    ■ a
■ 3    ■ b
■ 4    ■ c
■ 5    ■ d
■ 6    ■ e
■ 7    ■ f
```
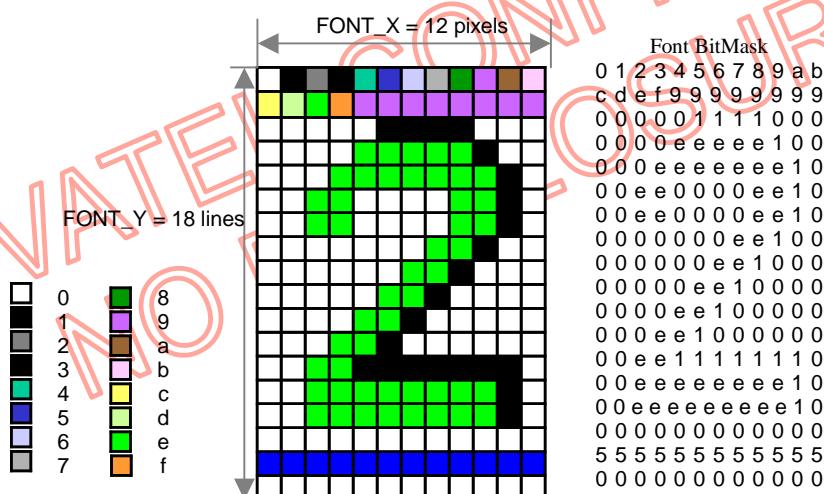
Figure 6.9-7 Four Bit Per Pixel Font

OSD Color Character Font SRAM Memory Arrangement Map:
A single ported SRAM (4096-words × 24-bits) is used for storing character attribute, code index, and programmable fonts. The following example illustrates the contents of SRAM memory for a sample OSD. The OSD is three rows by four columns.

Note: That the OSD Frame SRAM and Font SRAM share the same on Color Character Font SRAM Memory. Thus, the size of the memory map can be traded off against the number of different memory definitions. In particular, the size of the OSD frame and the number of font data must fit in the Color Character Font SRAM Memory. That is, the following inequality must be satisfied.
(OSD_HW+1)×(OSD_VH+1) + 18×CEILING (Number of 1-bit per pixel fonts / 9) × 9 +
2×18×CEILING (Number of 2-bit pixel fonts / 9) × 9 +
4×18×CEILING (Number of 4-bit pixel fonts / 9) × 9 <= 4096

The programmable font start address setting:
    OSD One Bit Font Address (FONT1B_ADDR) = (OSD_HW+1)×(OSD_VH+1)
    OSD Two Bits Font Address (FONT2B_ADDR) = OSD One Bit Font Address (FONT1B_ADDR) +
            (Number of 1-bit per pixel fonts) ×(12×18/24)
    OSD Four Bits Font Address (FONT4B_ADDR) = OSD Two Bit Font Address (FONT2B_ADDR) +
            (Number of 2-bit per pixel fonts) ×(2×12×18/24)
    Note: The following inequality must be satisfied
        MOD (Number of 1-bit pixel fonts / 9) = 0
        MOD (Number of 2-bit pixel fonts / 9) = 0
        MOD (Number of 4-bit pixel fonts / 9) = 0

OSD Frame Definition:
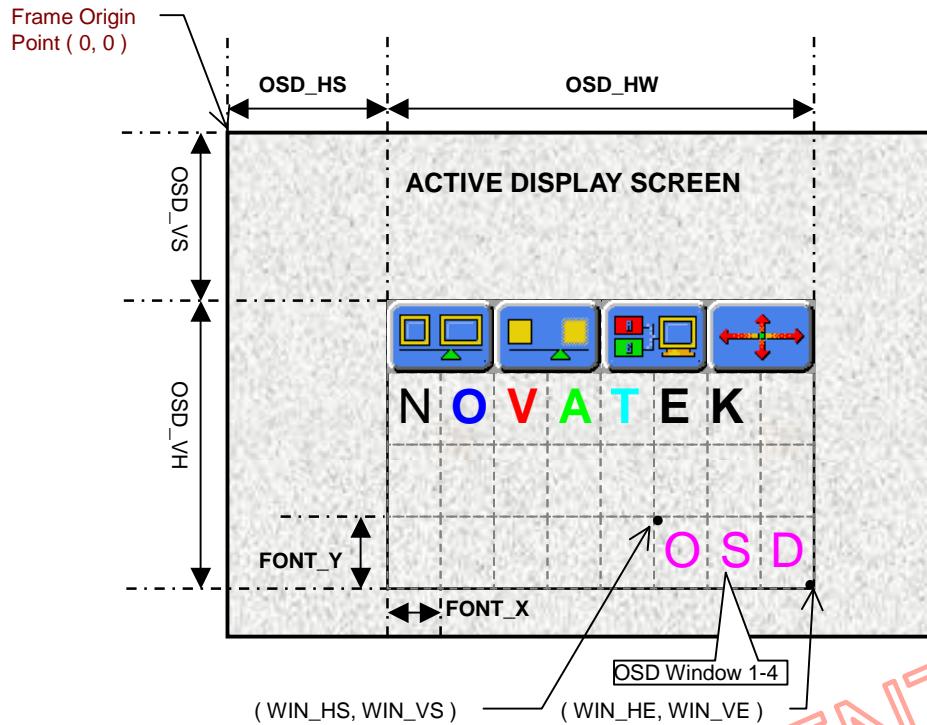
Figure 6.9-8 OSD Active Frame And Windows

OSD_HS : OSD Frame Horizontal Start (0 - 2047 pixels)
OSD_HW : OSD Frame Horizontal Width (1 - 64 chars)
OSD_VS : OSD Frame Vertical Start (0 - 2047 pixels)
OSD_VH : OSD Frame Vertical Height (1 - 32 chars)
WIN_HS : OSD Window Horizontal Start (1 - 64 chars)
WIN_HE : OSD Window Horizontal End (1 - 64 chars)
WIN_VS : OSD Window Vertical Start (1 - 32 chars)
WIN_VE : OSD Window Vertical End (1 - 32 chars)
FONT_X : Font X size (12/10 pixels)
FONT_Y : Font Y size (16/18 lines)

6.10. DPLL Clock Control

NT68665/NT68625 Display PLL (Bandwidth 165MHz) for display timing generator.

Formula:
$F{out}$ = (Reference-Freq × DDDS_RATIO [21:0] / DPLL_FREQ_DIV) / 2^{17}
$F{ref}$ = 12.000 MHz
Note: The value (Reference-Freq × DDDS_RATIO [21:0] / 2^{17}) must be large to 100 MHz

6.11. DISPLAY INTERFACE

NT68665/NT68625 display interface supports single (24-bit) or dual (48-bit) pixel out format, and supports the 6-bit/color or 8-bit/color LCD panel. Built in internal PLL locking to the reference clock generates all of the display timing to various LCD panels.

NT68665/NT68625 also provides the programmable display driving capacity to reduce EMI influence as well as programmable clock delay to compensate clock skew.
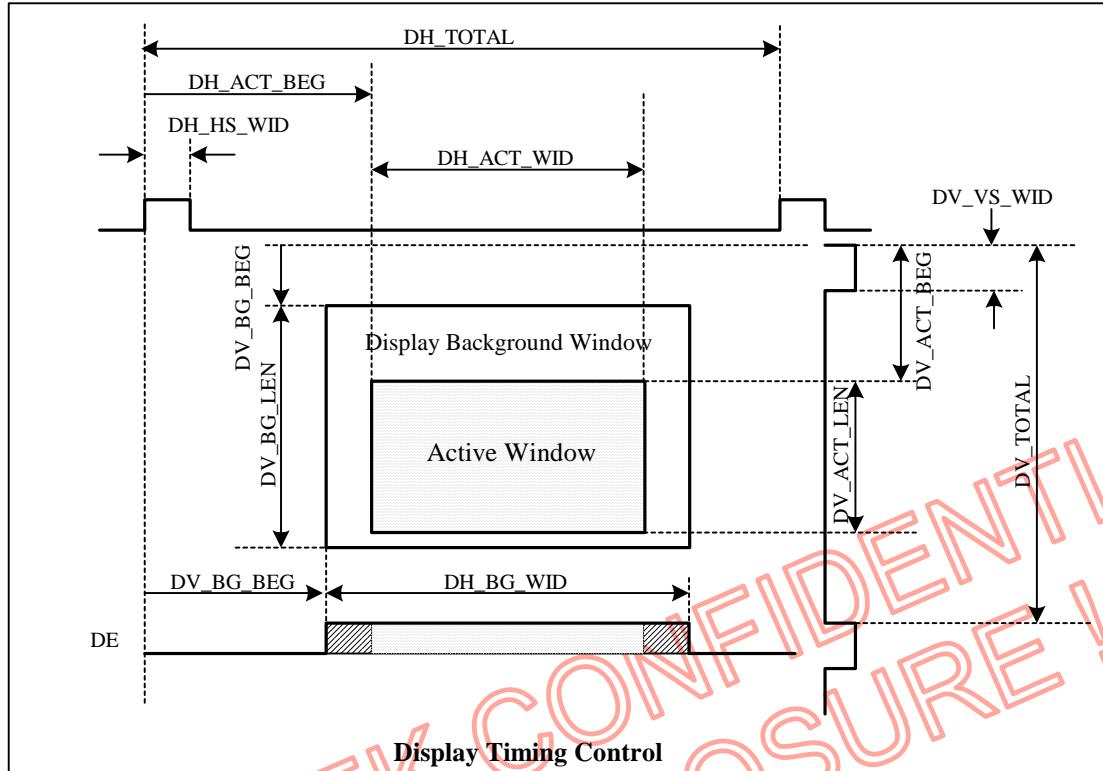
Figure 6.11-1 Display Timing Control

6.11.1. Scaler Display Data
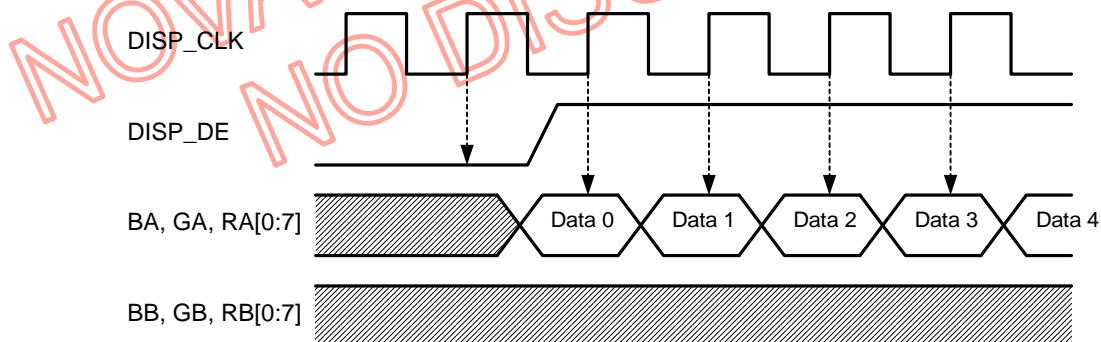
Figure 6.11-2 Single Pixel Width Display Data
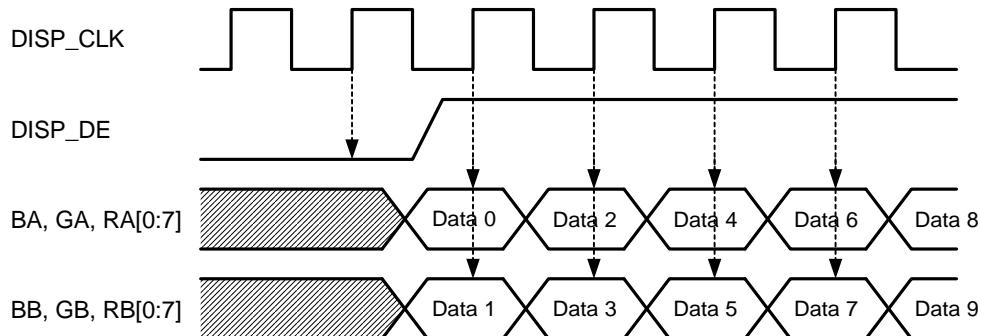
Figure 6.11-3 Double Pixel Width Display Data

6.11.2. Single/Dual pixel LVDS Transmitter

The NT68665/NT68625 transmitter is de-signed to support single or dual pixel data transmission between Scaler and Flat Panel Display up to SXGA resolutions. For dual pixel mode, the transmitter converts 24 bits (single Pixel 24-bit color) of CMOS data into 4 LVDS (Low Voltage Differential Signaling) data streams. For single pixel mode, the transmitter converts 48 bits (Dual Pixel 24-bit color) of CMOS data into 8 LVDS (Low Voltage Differential Signaling) data streams Control signals (VSYNC, HSYNC, DE and two user-defined signals) are sent during blanking intervals at a maximum single pixel rate of 85MHz.

The LVDS transmitter can support the following:

1. Single or double pixel mode
2. 24/48-bit panel mapping to the LVDS channels
3. 18/36-bit panel mapping to the LVDS channels
4. Programmable even/odd LVDS swapping
5. Programmable channel swapping (the clocks are fixed)
6. Support up to UXGA 60Hz output

Supported LVDS 18-bit Panel Data Mappings

Channel 0	R2, R3, R4, R5, R6, R7, G2
Channel 1	G3, G4, G5, G6, G7, B2, B3
Channel 2	B4, B5, B6, B7, HS, VS, DE
Channel 3	Disabled for this mode

Panel Data Mappings

Dual Pixel mode (When DP_BIT_SHF = 0)							
Channel 0 / Channel 4	R0, R1, R2, R3, R4, R5, G0						
Channel 1 / Channel 5	G1, G2, G3, G4, G5, B0, B1						
Channel 2 / Channel 6	B2, B3, B4, B5, HS, VS, DE						
Channel 3 / Channel 7	R6, R7, G6, G7, B6, B7, RSVD						
LVDS channel 0 (T0)	LVDS output	D7	D6	D4	D3	D2	D1	D0
	Data order	GA0	RA5	RA4	RA3	RA2	RA1	RA0
LVDS channel 1 (T1)	LVDS output	D18	D15	D14	D13	D12	D9	D8
	Data order	BA1	BA0	GA5	GA4	GA3	GA2	GA1
LVDS channel 2 (T2)	LVDS output	D26	D25	D24	D22	D21	D20	D19
	Data order	DE	VS	HS	BA5	BA4	BA3	BA2
LVDS channel 3 (T3)	LVDS output	D23	D17	D16	D11	D10	D5	D27

	Data order	RSVD	BA7	BA6	GA7	GA6	RA7	RA6
LVDS channel 4 (T4)	LVDS output	D7	D6	D4	D3	D2	D1	D0
	Data order	GB0	RB5	RB4	RB3	RB2	RB1	RB0
LVDS channel 5 (T5)	LVDS output	D18	D15	D14	D13	D12	D9	D8
	Data order	BB1	BB0	GB5	GB4	GB3	GB2	GB1
LVDS channel 6 (T6)	LVDS output	D26	D25	D24	D22	D21	D20	D19
	Data order	DE	NA	NA	BB5	BB4	BB3	BB2
LVDS channel 7 (T7)	LVDS output	D23	D17	D16	D11	D10	D5	D27
	Data order	NA	BB7	BB6	GB7	GB6	RB7	RB6

Dual Pixel mode (When DP_BIT_SHF = 1)							
Channel 0 / Channel 4	R2, R3, R4, R5, R6, R7, G2						
Channel 1 / Channel 5	G3, G4, G5, G6, G7, B2, B3						
Channel 2 / Channel 6	B4, B5, B6, B7, HS, VS, DE						
Channel 3 / Channel 7	R0, R1, G0, G1, B0, B1, RSVD						
LVDS channel 0 (T0)	LVDS output	D7	D6	D4	D3	D2	D1	D0
	Data order	GA2	RA7	RA6	RA5	RA4	RA3	RA2
LVDS channel 1 (T1)	LVDS output	D18	D15	D14	D13	D12	D9	D8
	Data order	BA3	BA2	GA7	GA6	GA5	GA4	GA3
LVDS channel 2 (T2)	LVDS output	D26	D25	D24	D22	D21	D20	D19
	Data order	DE	VS	HS	BA7	BA6	BA5	BA4
LVDS channel 3 (T3)	LVDS output	D23	D17	D16	D11	D10	D5	D27
	Data order	RSVD	BA1	BA0	GA1	GA0	RA1	RA0
LVDS channel 4 (T4)	LVDS output	D7	D6	D4	D3	D2	D1	D0
	Data order	GB2	RB7	RB6	RB5	RB4	RB3	RB2
LVDS channel 5 (T5)	LVDS output	D18	D15	D14	D13	D12	D9	D8
	Data order	BB3	BB2	GB7	GB6	GB5	GB4	GB3
LVDS channel 6 (T6)	LVDS output	D26	D25	D24	D22	D21	D20	D19
	Data order	DE	NA	NA	BB7	BB6	BB5	BB4
LVDS channel 7 (T7)	LVDS output	D23	D17	D16	D11	D10	D5	D27
	Data order	NA	BB1	BB0	GB1	GB0	RB1	RB0

6.12. Timing Controller control

Features

♦ RSDS (Reduced Swing Differential Signaling) Source Driver bus for low power and reduced EMI
♦ Provide RSDS source driver pixel rate at maximum 135Mb/s
♦ Provide 4 RSDS data pair to support 6 -bit RGB data bus
♦ 12 General Purpose Output allows to suit different production environments
♦ Provide single pixel (18-bit) or dual pixel (36-bit) RSDS output
♦ Support data swap to fit any panel data alignment for PCB layout
♦ Provide bypass timing controller function to output scaler data directly

Block Diagram
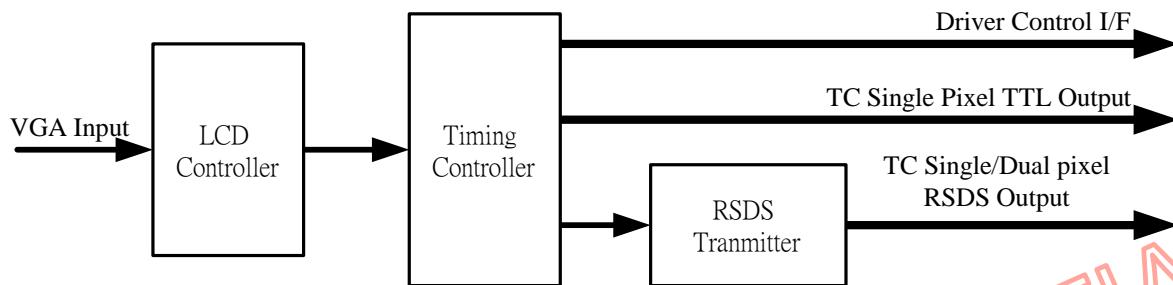
Figure 6.12-1 Timing Control Block Diagram

RSDS Display Data

1. **RSDS output :**
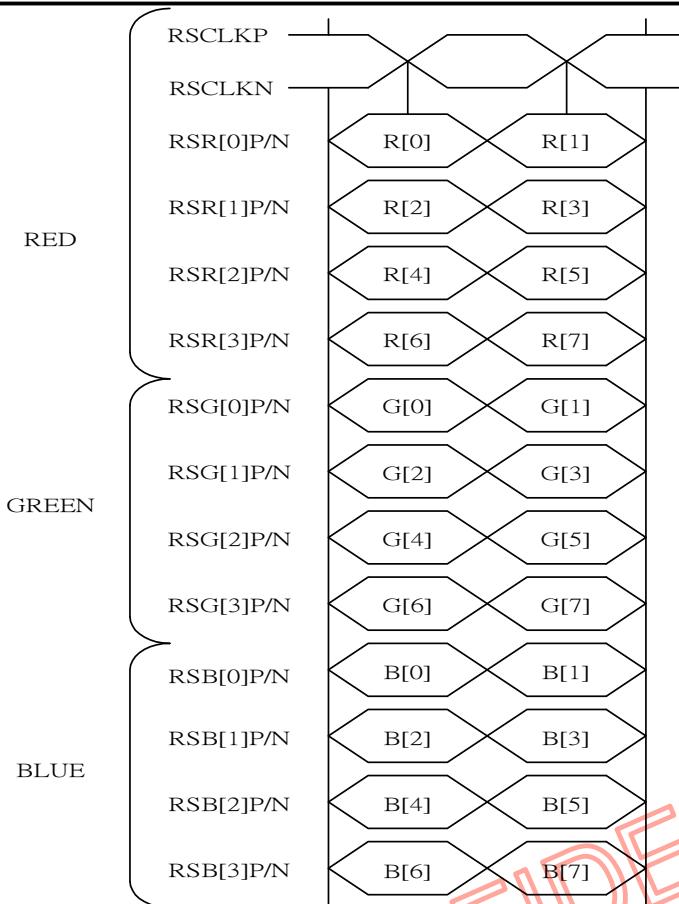
Figure 6.12-2 RSDS Color Bit, Mapping (OCTR_3[7] = "1")

RSDS Single Port Timing:
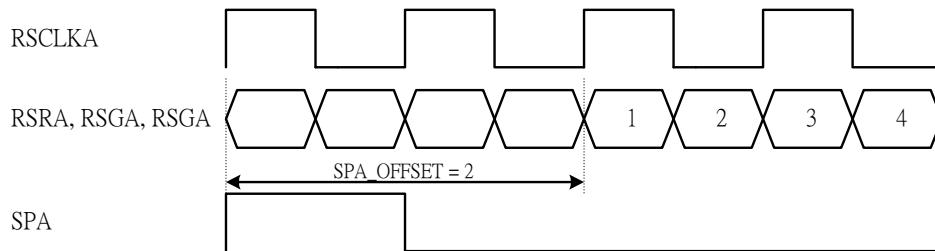
Figure 6.12-3 RSDS Single Port

RSDS Dual Port Timing:

● Line Buffer Size = n
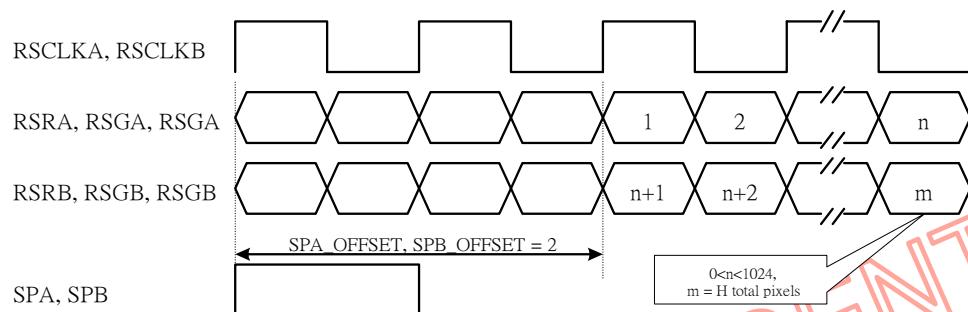
● Line Buffer Size = 1:
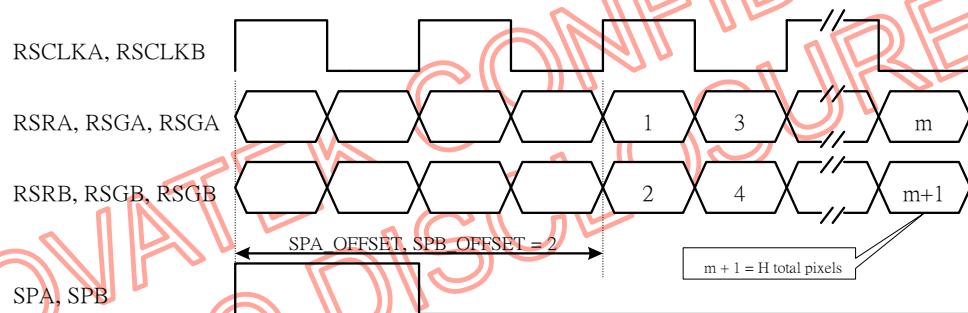
Figure 6.12-4 RSDS Dual Port

● Line Buffer Size = n
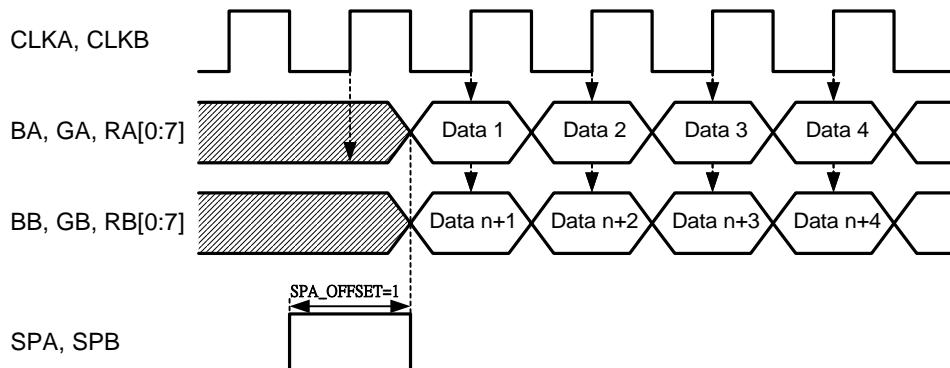
Figure 6.12-5 Dual Port Output, Clock Single pixel

● Line Buffer Size = n
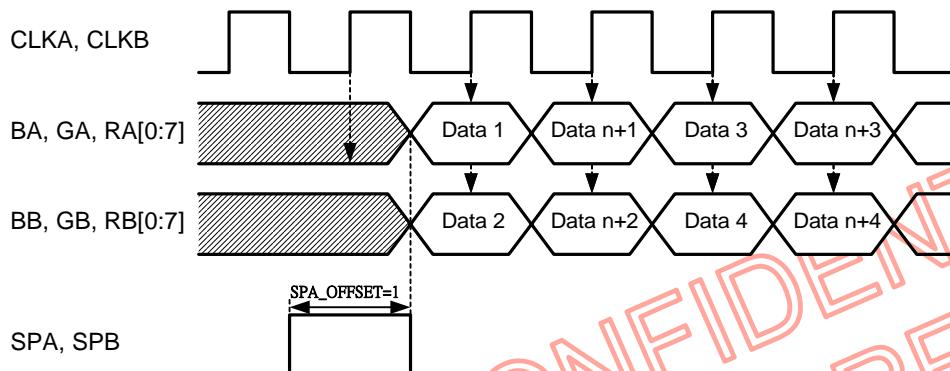
Figure 6.12-6 Dual Port Output, Clock Dual pixel

GPO Control Generation
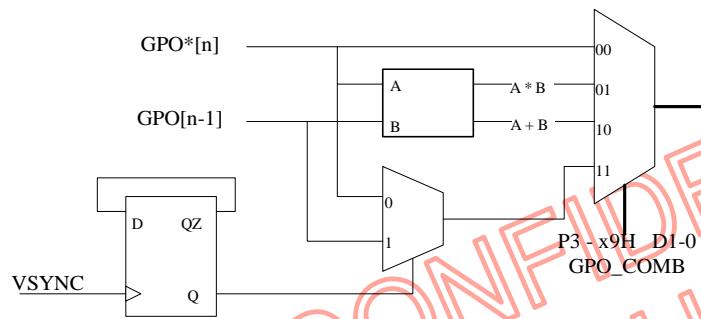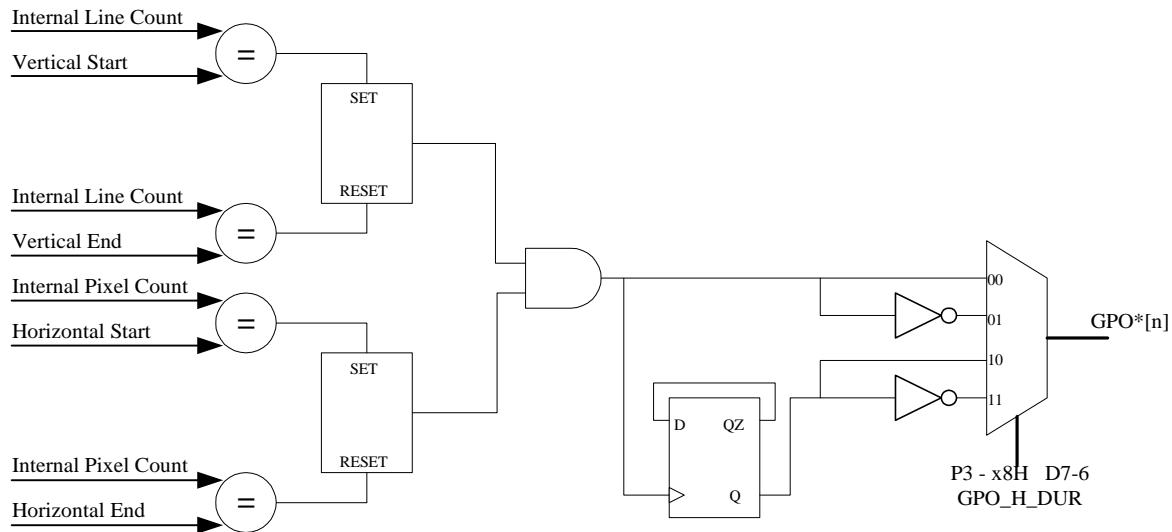
Figure 6.12-7 GPO Control Block Diagram

GPO Count Setting :

- **Non-Early Mode**

Internal Pixel Count For GPO Control Generation
GPO#_CTRL_1[5:4] = "00"

Internal Line Count For GPO Control Generation
GPO#_CTRL_1[3:2] = "00"
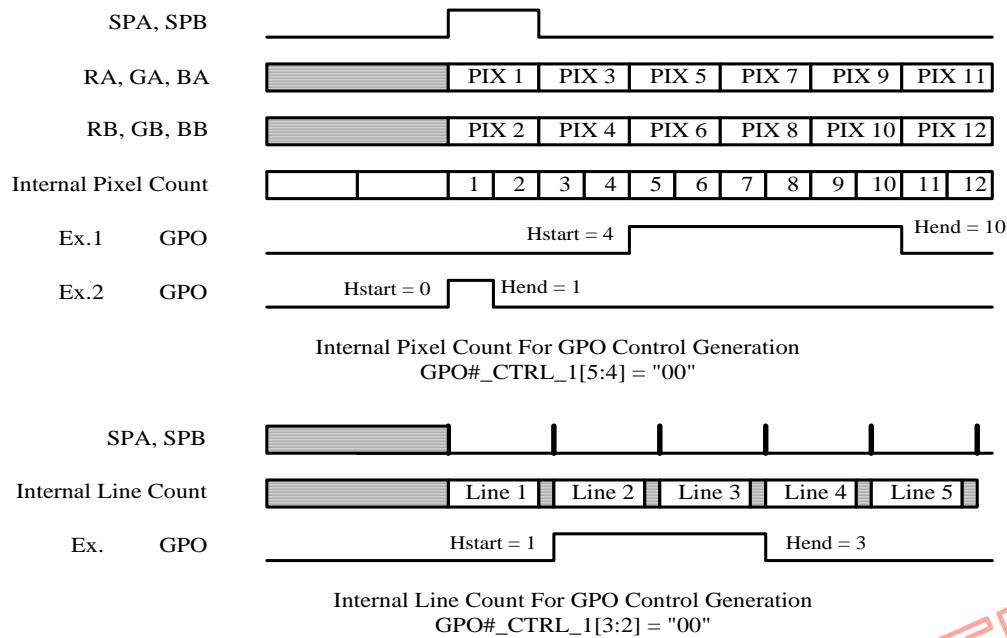
Figure 6.12-8 GPO Non-Early Mode

- **Early Mode :**

Internal Pixel Count For GPO Control Generation
GPO#_CTRL_1[5:4] = "11"

Internal Line Count For GPO Control Generation
GPO#_CTRL_1[3:2] = "11"
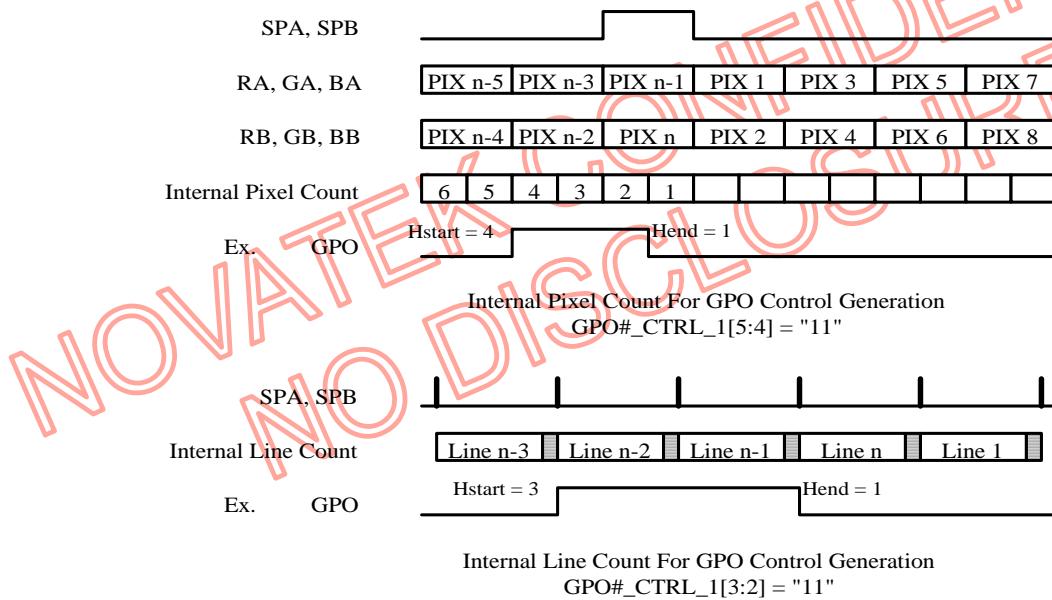
Figure 6.12-9 GPO Early Mode

6.13. Miscellaneous

6.13.1. General-Purpose Input Output (GPIO)

- 11 selectable General Purpose Output Pins
- 2 channels shared with HSYNCO, VSYNCO outputs
- 2 selectable output channels with PWM0, PWM1 outputs

- 2 built-in DDC Port, shared with GPO7, GPO8, GPO4, and GPO5
- GPIO Port Configuration

6.13.2. PWM Output

There are two Pulse Width Modulation signal pins available for controlling the LCD back light or audio volume, PWMA and PWMB. The duty cycle and Frequency of these signals is programmable.
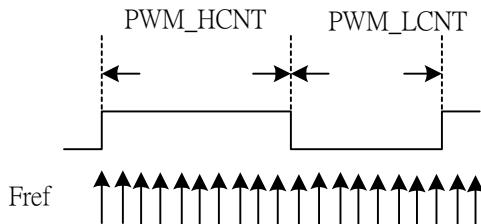
Figure 6.13-1 Pulse Width Modulation Signal (PWM)

When clock source select from reference clock

$$F_{PWM\_CLK} = F_{REFCLK}/(PWM\_DIV\ 1 \times PWM\_DIV\ 2\ )$$

When clock source select from Display Hsync

$$F_{PWM\_CLK} = F_{DISP\_HS}/(PWM\_DIV\ 1 \times PWM\_DIV\ 2\ )$$

$$F_{PWM} = \frac{F_{PWM\_CLK}}{(PWM\_HCNT\ +\ PWM\_LCNT)}$$

$$Duty = \frac{PWM\_HCNT}{(PWM\_HCNT\ +\ PWM\_LCNT\ )}$$

$$PWM\_HCNT = \frac{Duty \times F_{PWM\_CLK}}{F_{PWM}}$$

$$PWM\_LCNT = \frac{(1-Duty) \times F_{PWM\_CLK}}{F_{PWM}}$$

PWM_HCNT	PWM_LCNT	PWM Output
0	0~255	DC '0'
1~255	0	DC '1'
1~255	1~255	PWM pulse

6.14. MCU Interface

NT68665/NT68625 supports two wires of I2C bus and one IRQ output to communicate with MCU. I2C data rate is up to 400K bits/s.

6.14.1. I2C Protocol

General Register R/W

Byte Write
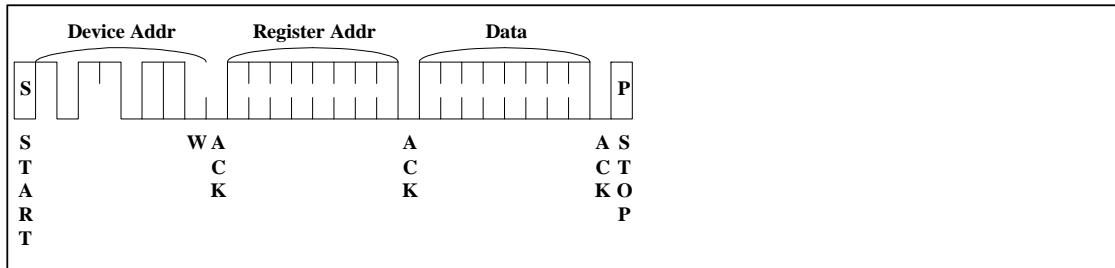
Sequential Write
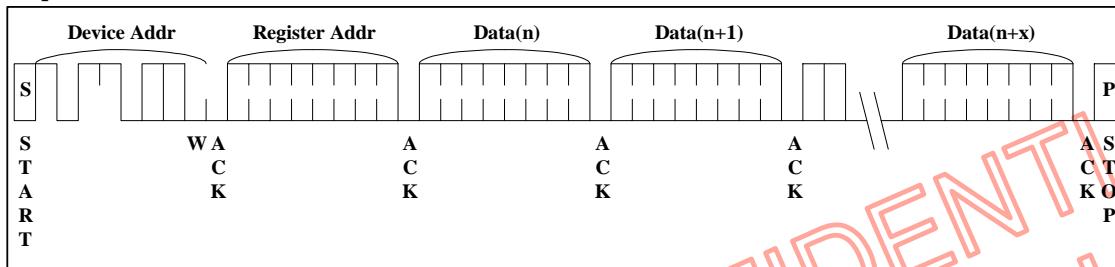
Byte Read
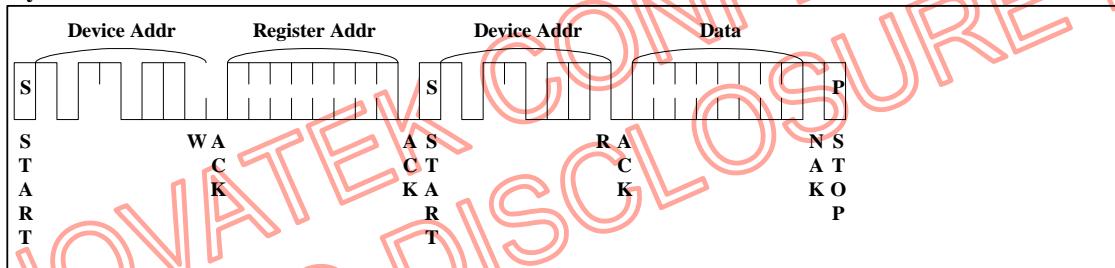
Sequential Read
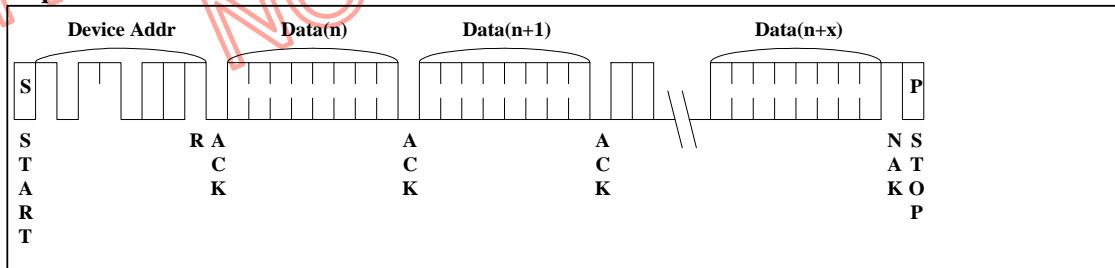
Figure 6.14-1 I2C General Register Read/Write Protocol

Index Port Access R/W

Index Port Write Access
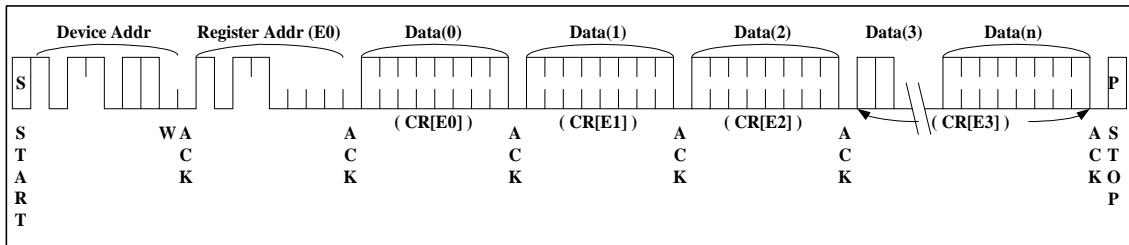
Index Port Read Access
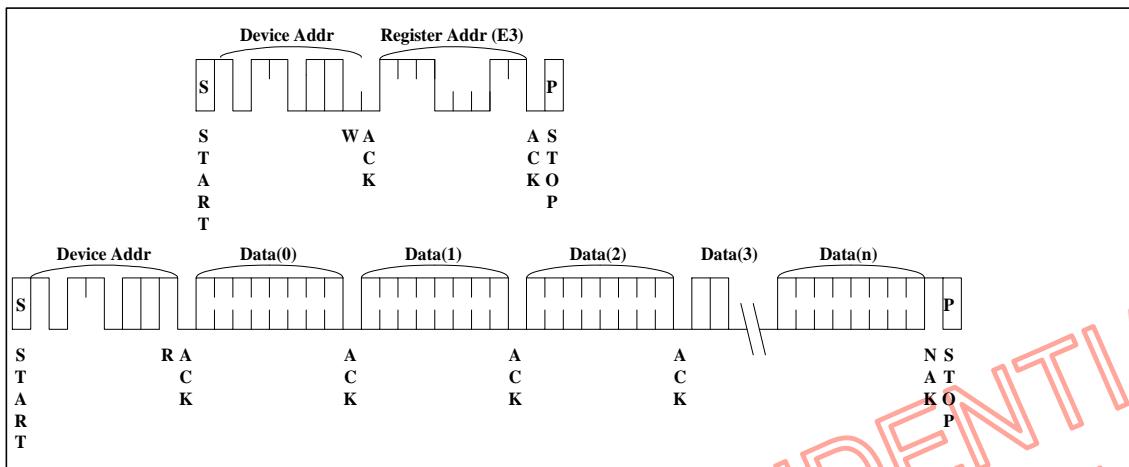
Figure 6.14-2 I2C Index Port Data Access Protocol

6.14.2. IRQn Interrupt Sources

NT68665/NT68625 provides an interrupt request output pin IRQn. The following figure shows the detail structure of the IRQn sources.
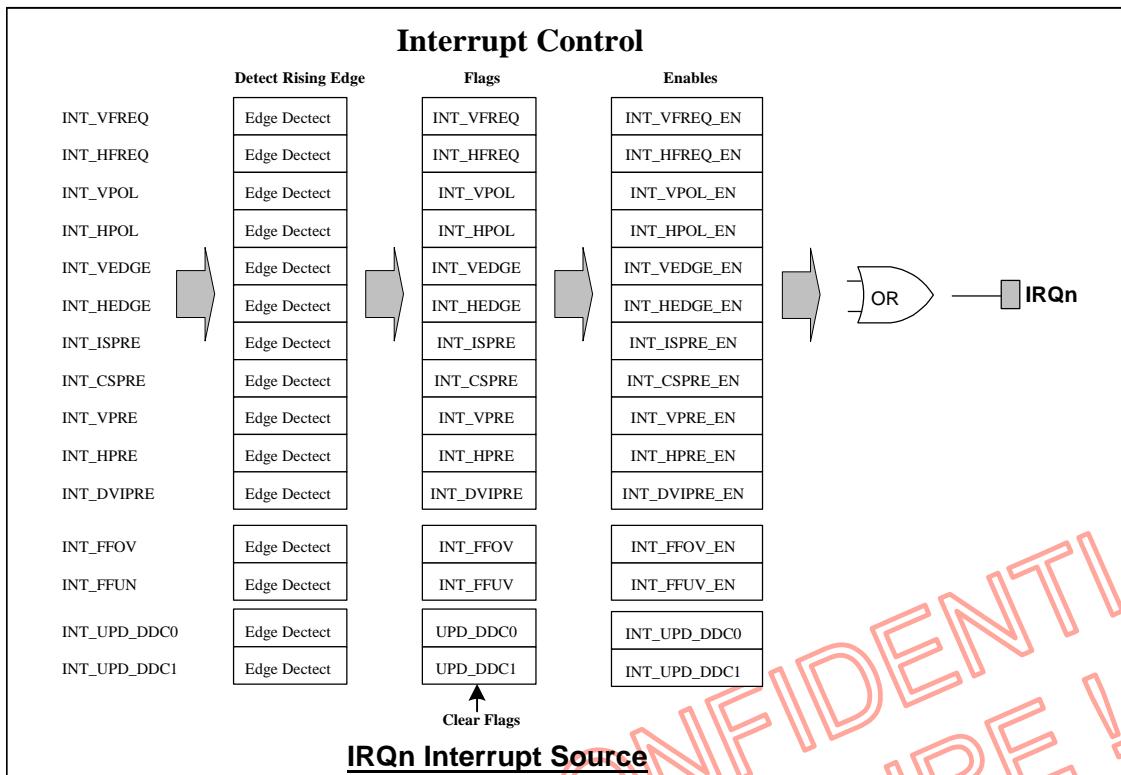
Figure 6.14-3 IRQn Interrupt Block Diagram

INTHV_IRQ	Meaning	Action
INT_VFREQ	Vsync Frequency Change	It will be activated when the Input frequency of Vsync changes.
INT_HFREQ	Hsync Frequency Change	It will be activated when the Input frequency of Hsync changes.
INT_VPOL	V-Polarity Change INT	It will be activated when the Input Polarity of Vsync changes.
INT_HPOL	H-Polarity Change INT	It will be activated when the Input Polarity of Hsync changes.
INT_VEDGE	Vsync Edge INT	It will be activated when the Vsync rising edge is occur.
INT_HEDGE	Hsync Edge INT	It will be activated when the Hsync rising edge is occur.
INT_ISPRE	Interlaced Sync INT	It will be activated when the Interlaced Sync is present.
INT_ CSPRE	Composite Sync INT	It will be activated when the Composite Sync is present.
INT_VPRE	Vsync Present INT	It will be activated when the Vsync is present.
INT_HPRE	Hsync Present INT	It will be activated when the Hsync is present.
INT_DVIPRE	DVI sync Present INT	It will be activated when the DVI sync is present.
INT_FFOV	FIFO Overflow INT	It will be activated when the FIFO is overflow

INT_ FFUV	FIFO Underflow INT	It will be activated when the FIFO is underflow
INT_UPD_DDC0	DDC0 updated INT	It will be activated when DDC0 Ram-Buffer contents updated.
INT_ UPD_DDC1	DDC1 updated INT	It will be activated when DDC1 Ram-Buffer contents updated.

Table 6.14-1 IRQn Interrupt

6.15. 8031 On-Chip Microcontroller

Reference application notice – "NT68665/NT68625 MCU APN v2.0.pdf"

7. Electrical Specifications

3.3V Supply voltage range, $V_{3.3}$ (see Note1)…………………………………-0.3V to 4V

1.8V Supply voltage range, V_{18} (see Note2)…………………………………-0.3V to 1.98V

Output voltage range, V_O……..………………………………………………-0.3V to V_{33} +0.3V

Input voltage range (5V Tolerant), V_I…………………………………………-0.3V to V_{5V} +0.3V

Electrostatic Discharge, V_{ESD}…………………………………………………$\pm$2.0kV

Ambient Operating temperature, T_A……………………………………….…..0°C to 70°C

Lead temperature 1, 6 mm (1/16 inch) from case for 10 seconds……………260°C

Junction Temperature……………………………………………………………150°C

Thermal resistance (Junction to Air) Natural Convection, θ_{JA}…..………….. 29°C/W

Thermal resistance (Junction to Case) Natural Convection, θ_{JC}…..………..13 °C/W

Storage temperature range, Tstg……………………………………..…..-40°C to 125°C

Storage humidity……………………………………………………….…………..< 60% HR

Storage Life (Storage Temperature < 30 ℃)………………………………….. 1 year

♦ Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.
♦ Note1: Includes pins ADC_VAA, AVCC, PVCC, DVDD.
♦ Note2: Includes pins CVDD, PLL_VDD

7.1. DC Electrical Characteristics

(T_A = 25°C, Oscillator freq. = 12.000MHz, unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
		Power Requirements				
V_{CVDD}	1.8 V digital power supply	1.71	1.8	1.89	V	CVDD
V_{PLL}	PLL power supply	1.71	1.8	1.89	V	PLL_VDD
V_{ADC}	R/G/B channel ADC analog power supply	3.15	3.3	3.47	V	ADC_VAA,
V_{TMDSA}	TMDS analog power supply	3.15	3.3	3.47	V	AVCC
V_{TMDSP}	TMDS PLL power supply	3.15	3.3	3.47	V	PVCC
V_{DDD}	Display interface power supply	3.15	3.3V	3.47	V	DVDD
V_{MCU}	MCU power supply	3.00	3.3V	3.60	V	MCU_VCC
I_{VDD}	1.8 V digital power supply current		130		mA	No Loading (Includes CVDD, PLL_VDD)
I_{ADC}	ADC power supply current		160		mA	No Loading
I_{TMDS}	TMDS power supply current		110		mA	No Loading
I_{DDD}	Display interface power supply current		50		mA	No Loading
I_{DD18} I_{DD33}	1.8 V Operating current (Total) 3.3 V Operating current (Total)		130 320		mA	No Loading

I$_{MCU}$	MCU Operating Current	-	20	-	mA	No Loading
I$_{DDPD18}$ I$_{DDPD33}$	1.8 V Power down current 3.3 V Power down current		2 10		mA	No Loading
Digital Outputs						
V$_{OH}$	Output high voltage	2.0		V$_{DD}$	V	DISP_DE, DISP_VS, DISP_HS, DISP_CLK, IRQn, IN_HSO, IN_VSO
V$_{OL}$	Output low voltage	GND		0.8	V	
V$_{OH}$	Output high voltage for PWM/DDC			5	V	PWM[1:0], DDC_SCL[1:0], DDC_SCL[1:0],
I$_{OZ}$	Tri-State Leakage Current	-25		25	uA	
I$_{OH1}$	Output high current	-16		-2	mA	(V$_{OH}$ = 2.5V) DISP_DE, DISP_VS, DISP_HS, DISP_CLK, REFCKO,
I$_{OL1}$	Output low current	2		16	mA	(V$_{OL}$ = 0.4V) DISP_DE, DISP_VS, DISP_HS, DISP_CLK, REFCKO
I$_{OH2}$	Output high current			-4	mA	(V$_{OH}$ = 2.5V) IRQn, IN_HSO, IN_VSO
I$_{OL2}$	Output low current	4			mA	(V$_{OL}$ = 0.4V) IRQn, IN_HSO, IN_VSO
LVDS Outputs						
|V$_{OD}$|	Differential Steady-state Output Voltage Magnitude	240			mV	R$_L$ = 100Ω, See Figure 7.1.1
△|V$_{OD}$|	Change in the Steady-state Differential Output Voltage Magnitude between Opposite binary States			35	mV	
V$_{OC(SS)}$	Steady-state Common-mode Output Voltage	1.125		1.475	V	See Figure 7.1.1
V$_{OC(PP)}$	Peak-to-peak Common-mode Output Voltage		80	150	mV	
I$_{OS}$	Short-circuit Output Current			±24	mA	V$_{O(TP)}$ = 0
				±12	mA	V$_{OD}$ = 0
I$_{OZ}$	Output Tri-State Current		±1		μA	V$_O$ = 0 to Vcc
RSDS Output						
V$_{OHDIF}$	Differential Voltage High Output	+200		+450	mV	

	Voltage					
V_{OLDIF}	Differential Voltage Low Output Voltage	-450		+200	mV	
V_{CM}	Differential Voltage Common Voltage	1.1	1.2	1.3	V	
Z_L	Differential load impedance	90	100	110	Ω	
Analog Input						
V_{IAMIN}	Minimum Input Voltage Range			0.55	V p-p	
V_{IAMAX}	Maximum Input Voltage Range	0.9			V p-p	V_{IAMAX}
DVI Input						
V_{ID}	Differential Input Voltage	150		1200	mV	See Figure 7.1.3
V_{ICOM}	Input Common Mode Voltage	AVCC-300mV		AVCC-37mV	mV	See Figure 7.1.3
V_{BTD}	Behavior when Transmitter is disabled	AVCC-10mV		AVCC+10mV	mV	See Figure 7.1.3
Digital Input						
V_{IH}	Input high voltage	2.0		V_{DD}	V	Y[7:0],
V_{IL}	Input low voltage	GND		0.8	V	
$V_{T+(HSYNC)}$	Schmitt Trigger Positive Going Threshold Voltage for HSYNC Inputs	1.5	1.6	2.2	V	HSYNCI0, HSYNCI1
$V_{T-(HSYNC)}$	Schmitt Trigger Negative Going Threshold Voltage for HSYNC Inputs	0.7	1.1	1.4	V	HSYNCI0, HSYNCI1
$V_{T+(VSYNC)}$	Schmitt Trigger Positive Going Threshold Voltage for VSYNC Inputs		1.8	2.0	V	VSYNCI0, VSYNCI1
$V_{T-(VSYNC)}$	Schmitt Trigger Negative Going Threshold Voltage for VSYNC Inputs	0.8	1.5		V	VSYNCI0, VSYNCI1
V_{IHC}	Clock high voltage	2.0		V_{DD}	V	YUV_CLK,
V_{ILC}	Clock low voltage	GND		0.4	V	
I_{IH}	Input high current	-25		25	μA	(V_{IH} = 2.5V)
I_{IL}	Input low current	-25		25	μA	(V_{IL} = 0.4V)

Micro-controller						
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
IDD	Operating Current	-	20	-	mA	No Loading
I/O Port						
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**

$V_{UT(PORT)}$	Schmitt Upper-Threshold Voltage for I/O Ports	1.9	-	2.3	V	PA0~PA3;PA4*~ PA7*; PB0~PB3; PB4*/SCL0*;PB5*/SDA0*; PB6*/SCL1*;PB7*/SDA1* PC0*,PC1*,PC2~PC7; PD0~PD6; PE0~PE1; P30,P31,P34,P35; RSTB
$V_{LT(PORT)}$	Schmitt Lower-Threshold Voltage for I/O Ports	1	-	1.5	V	PA0~PA3;PA4*~PA7*; PB0~PB3; PB4*/SCL0*;PB5*/SDA0*; PB6*/SCL1*;PB7*/SDA1* PC0*,PC1*,PC2~PC7; PD0~PD6; PE0~PE1; P30,P31,P34,P35; RSTB

I/O Port						
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
V_{OH}	Output High Voltage for I/O Ports	2.5	-	-	V	PA0~PA3 @ I_{OH} = -4mA PB0~PB3 @ I_{OH} = -4mA PC2~PC7 @ I_{OH} = -4mA PD0~PD6 @ I_{OH} = -4mA PE0~PE1 @ I_{OH} = -4mA P30,P31,P34,P35 @ I_{OH} = -100uA
	Output High Voltage for Open-Drain Ports/PWMs	-	-	5	V	External Voltage for Open Drain Structure PA4*/PWM12*,PA5*/PWM13*, PA6*/PWM14*,PA7*/PWM15* PB4*/SCL0*;PB5*/SDA0* PB6*/SCL1*,PB7*/SDA1* PC0*,PC1*
$V_{OL(PORT)}$	Output Low Voltage for I/O Ports	-	-	0.4	V	PA0~ PA3 @ I_{OL} = +8mA PA4*~PA7* @ I_{OL} = +8mA PE0~PE1 @ I_{OL} = +8mA PB0~PB3 @ I_{OL} = +4mA PC0*,PC1*; PC2~PC7 @ I_{OL} = +4mA PD0~PD6 @ I_{OL} = +4mA PE0~PE1 @ I_{OL} = +8mA P30,P31,P34,P35 @ I_{OL} = +4mA
$V_{OL(IIC)}$	Output Low Voltage for I²C bus Ports	-	-	0.4	V	@ I_{OL}=+3mA · PB4*/SCL0*,PB5*/SDA0*, PB6*/SCL1*;PB7*/SDA1*
		-	-	0.6	V	@ I_{OL}=+6mA
R_{PH1}	Pull up Resistor @ Vi=1.5V	40	60	80	KΩ	PA0~PA3 PB0~PB3 PC2~PC7 PD0~PD5
Reset						
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
V_{LowPwr}	Low-Voltage Detect Voltage for Power	2.6	-	3.0		
V_{LVR}	Low-Voltage Reset Voltage for Power	2.0	-	2.8	V	Pulse Width > $t_{PW(LVR)}$
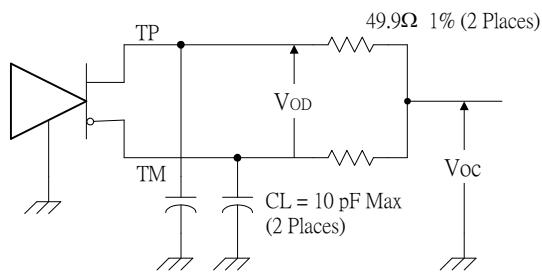
(a)SCHEMATIC
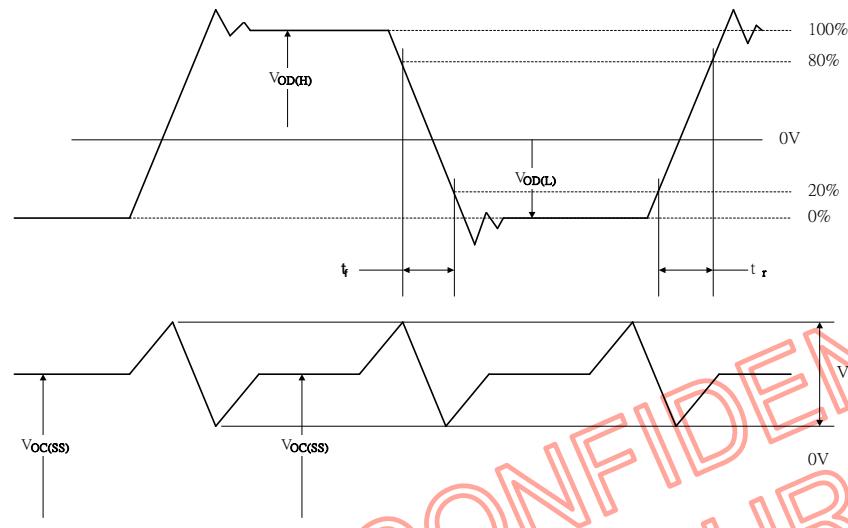
(b) WAVEFORMS

Figure 7.1-1 Test Load and Voltage Definitions for LVDS Outputs
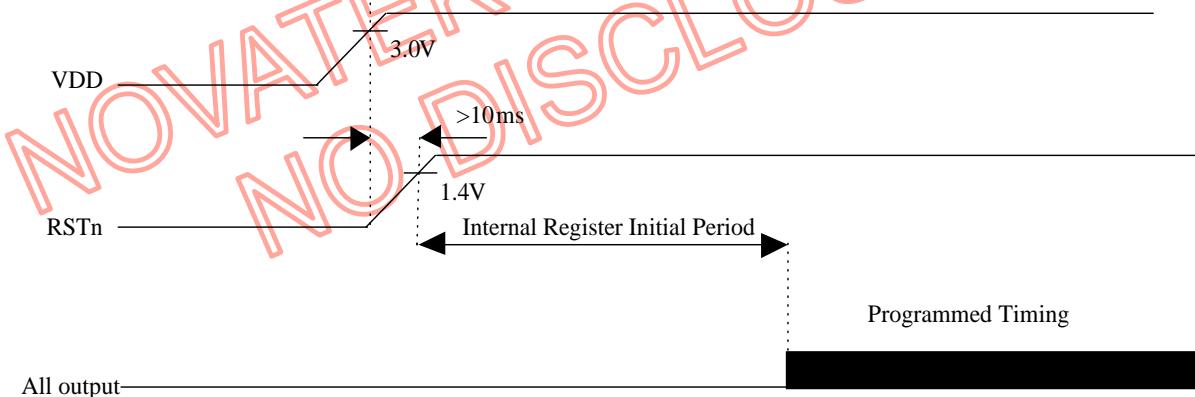
Power -up Sequence

Figure 7.1-2 Power-up Sequence
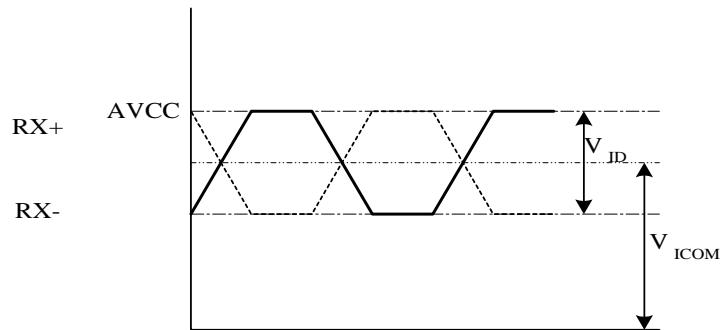
Figure 7.1-3 DVI Single-ended Differential Signal
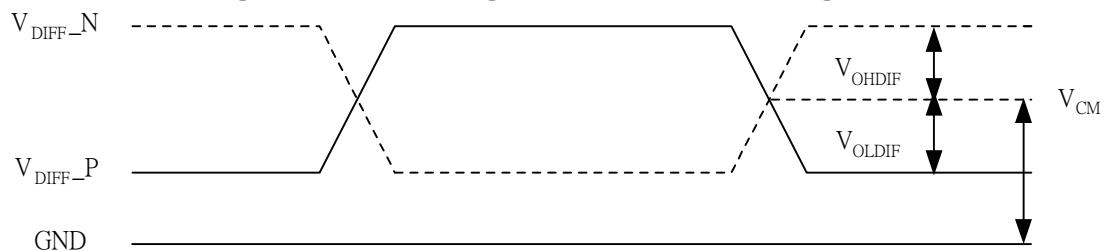
Figure 7.1-4 Voltage Definitions for RSDS Outputs

7.2. AC Electrical Characteristics

(VDD=3.3V, TA=25°C, Oscillator freq.=14.318MHz, unless otherwise specified)

ADCPLL

Phase-locked loop							
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**	
j$_{PLL}$	Short term jitter	fclkout=165MHz	-	-	120	ps	
	Long term jitter	fclkout=165MHz	-	-	1.2	ns	
DR	Divider ratio	-	2	-	4096		
f$_{CLKIN}$	Input clock frequency range	-	15	-	110	kHz	
f$_{CLKOUT}$	Output clock frequency range	XF type EF type	12 12	-	110 165	MHz	
t$_{COAST}$	Maximum coast mode time	-	-	-	3	ms	
t$_{CAP}$	PLL capture time	In start-up conditions	-	-	5	ms	
δ	CKOUT clock duty cycle	165 MHz output	45	50	55	%	

Clamping Pulse						
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
t$_{DELAY}$	Clamp pulse delay time	CLAMP_BEG<5:0>=0x00	-	0	-	4/CKOUT
		CLAMP_BEG<5:0>=0x0F	-	15	-	4/CKOUT
t$_{WIDTH}$	Clamp pulse width	CLAMP_WID<5:0>=0x01	-	1	-	4/CKOUT
		CLAMP_WID<5:0>=0x0F	-	15	-	4/CKOUT
t$_{COR1}$	Clamp correction time to within ±10 mV	±100mV black level input variation; clamp capacitor = 4.7nF	-	-	300	ns
t$_{COR2}$	Clamp correction time to less than 1 LSB	±100mV black level input variation; clamp capacitor = 4.7nF	-	-	10	Lines

Analog-to-Digital Converter						
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
fs	Sampling frequency	X type E type	10 10	-	110 165	MHz
B	Bandwidth	-	150	-	-	Mhz
G$_{MATCH}$	Channel to channel match	-	-	2	5	%
Vin(p-p)	Input signal voltage (peak-peak)	Corresponding to full scale output	0.55	0.7	0.9	V

DNL	DC differential non linearity	From analog input to digital output; ramp input;
		f$_{CLK}$ = 165 MHz (E type);
		f$_{CLK}$ = 110 MHz (X type);
			-	±0.5	+1.25/ - 1.0	LSB

INL	DC integral non	From analog input to digital	-	±0.6	±2.25	LSB

	linearity	output; ramp input; f_{CLK} = 165 MHz (E type); f_{CLK} = 110 MHz (X type);				
ENOB	Effective number of bits	From analog input to digital output;10KHz sine wave input; ramp input; f_{CLK} = 165MHz (E type); f_{CLK} = 110MHz (X type);	-	7	-	bits
THD		Input 1V(p-p) and 10MHz	-	-	1	%

No Missing Codes is guaranteed.

Signal-to-Noise Ratio						
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
S/N	Signal-to-noise ratio	Maximum gain X type -- f_{CLK}=110MHz E type -- f_{CLK}=165MHz	-	45	-	dB
		Minimum gain X type -- f_{CLK}=110MHz E type -- f_{CLK}=165MHz	-	44	-	dB

TMDS Receiver

TMDS Receiver						
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
f_{OP}	Operating Frequency range		25	-	165	MHz
t_{JJT}	Jitter tolerance		2	-	-	ns
t_{START}	Receiver Startup Time		-	-	10	ms
t_{DPS}	Intra-Pair (+ to -) Differential Input Skew	165MHz 1 pixel/clock			250	ps
t_{CCS}	Channel to Channel Differential Input Skew	165MHz 1 pixel/clock			5.0	ns
C_{IN}	TMDS Input Pin Capacitance		-	7	-	pF

Sync Processor (Oscillator freq.=12MHz)

H/V Sync Processor						
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
f_{VSYNC}	Vsync Input Frequency	Vsync Duty Cycle = 40%	15	-	250	Hz
f_{VCLK}	Vsync Input Frequency for DDC-1 Mode	Supply VCLK for DDC-1 mode only	-	-	25	KHz
t_{VPW}	VSYNC input Pulse Width	Vsync Duty Cycle < 40%	-	-	4.43	ms
f_{HSYNC}	Hsync Input Frequency	Hsync Duty Cycle = 40%	15	-	250	KHz
t_{HPW}	HSYNC input Pulse Width	Hsync Duty Cycle < 40%	-	-	8.66	us
$t_{HPW(COMP)}$	HSYNC input Pulse Width	Hsync Duty Cycle < 40%	-	-	8.66	us
$t_{HTTT(COMP)}$	Horizontal total time - $t_{HPW(COMP)}$		8.66			us

I2C Bus Timing

Symbol	Parameter	Min	Max	Unit
	I2C Bus Timing			
f$_{SCL}$	SCL clock frequency	0.00	400	kHz
t$_{SUSTO}$	STOP setup time	0.60		us
t$_{BUF}$	Bus free time between a STOP and START	1.30		us
t$_{HDSTA}$	START hold time	0.60		us
t$_{LOW}$	SCL clock pulse width low	1.30		us
t$_{IICR}$	IIC bus rise time		300	ns
t$_{HDDAT}$	DATA hold time	0.00		us
t$_{HIGH}$	SCL clock pulse width high	0.60		us
t$_{ICF}$	IIC bus fall time		300	ns
t$_{SUDAT}$	Data setup time	100		ns
t$_{SUSTA}$	START setup	0.60		us
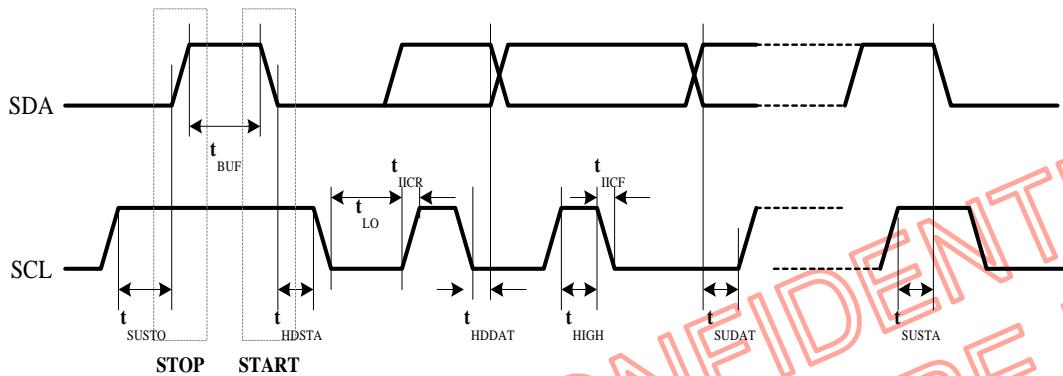
Figure 7.2-1 I2C Bus Timing

DDC Bus Timing
DDC1 Mode:

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t$_{VAA}$	Data Valid from the low-to-high edge of the VCLK	-	-	1000	ns	
t$_{MODE}$	Time for Transition to DDC2B Mode from DDC1	-	-	500	ns	

Note:

VCLK comes from Separate VSYNCI or is extracted from Composite Sync. The internal noise filter will cause a filter time delay of the VCLK.

DDC1 Timing

Figure 7.2-2

DDC Mode Transition

Figure 7.2-3

DDC2B Mode

Symbol	Parameter		Standard Mode		Fast Mode		Unit
			Min.	Max	Min	Max	
f_{SCL}	SCL Clock Frequency			100		400	KHz
t_{BUF}	Bus Free Between a STOP and START Condition		4.7		1.3		us
$t_{HD;STA}$	Hold Time for START Condition		4.0		0.6		us
t_{LOW}	LOW Period of The SCL Clock		4.7		1.3		us
t_{HIGH}	HIGH Period of The SCL Clock		4.0		0.6		us
$t_{SU;STA}$	Set-up Time for a Repeated START Condition		4.7		0.6		us
$t_{HD;DAT}$	Data Hold Time	Transmitter	0.1		0.1	0.9	us
		Receiver	0		0		
$t_{SU;DAT}$	Data Set-up Time		250		100		ns
t_r	Rise Time of Both SDA and SCL Signals			1000		300	ns
t_f	Fall Time of Both SDA and SCL Signals			300		300	ns
$t_{SU;STO}$	Set-up Time for STOP Condition		4.0		0.6		us
t_{SP}	Pulse Width of spikes which must be suppressed by the input filter		0	50	0	50	ns
C_I	Capacitance for each Bus Pin		-	10		10	pF
C_b	Capacitive load for each Bus Line		-	400		400	pF

DDC-Bus Timing

Figure 7.2-4

LCD Display Control Timing with TCON
RSDS Mode

Differential Mode AC Electronical Characteristics						
Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
t_{RCP}	Clock Period		14.8			ns
t_{RCHP}	Clock High Period		$0.4t_{CLK}$		$0.6t_{CLK}$	ns
t_{RCLP}	Clock Low Period		$0.4t_{CLK}$		$0.6t_{CLK}$	ns
t_{RSSTU}	Data setup time	$R_L=100\Omega$, $C_L=5pF$,Max f_{CLK}=95MHz	2			ns
t_{RSHLD}	Data hold time	$R_L=100\Omega$, $C_L=5pF$,Max f_{CLK}=95MHz	0.2			ns
t_{SPSTU}	Start pulse setup time	$C_L=20pF$, Max f_{CLK}=95MHz	3			ns
t_{SPHLD}	Start pulse hold time	$C_L=20pF$, Max f_{CLK}=95MHz	2			ns
t_{GPOSTU}	GPO setup time	$C_L=20pF$, Max f_{CLK}=95MHz	3			ns
t_{GPOHLD}	GPO hold time	$C_L=20pF$, Max f_{CLK}=95MHz	2			ns
t_{Rising}	Transition rising time		250	700	1500	ps
$t_{Falling}$	Transition falling time		250	700	1500	ps
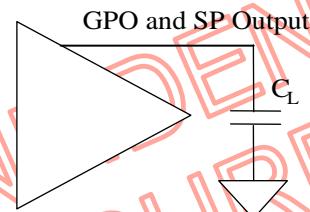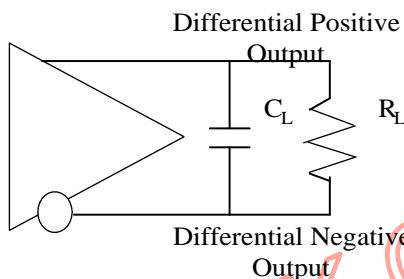
Figure 7.2-5
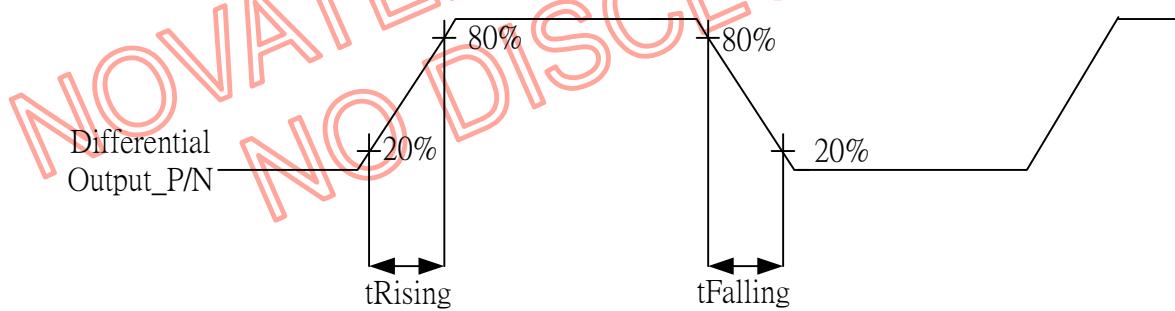
Figure 7.2-6

Figure 7.2-7

$tSKEW1 = tRCP$ (Min) - tRCHP (Min) - tRCLP (Min)

$tSKEW2 = tRCHP$ (Min) - tRSSTU (Min) - tRSHLD (Min) or

$tSKEW2 = tRCLP$ (Min) - tRSSTU (Min) - tRSHLD (Min)

**Differential Mode Transmitter
Skew Margin
Figure 7.2-8**
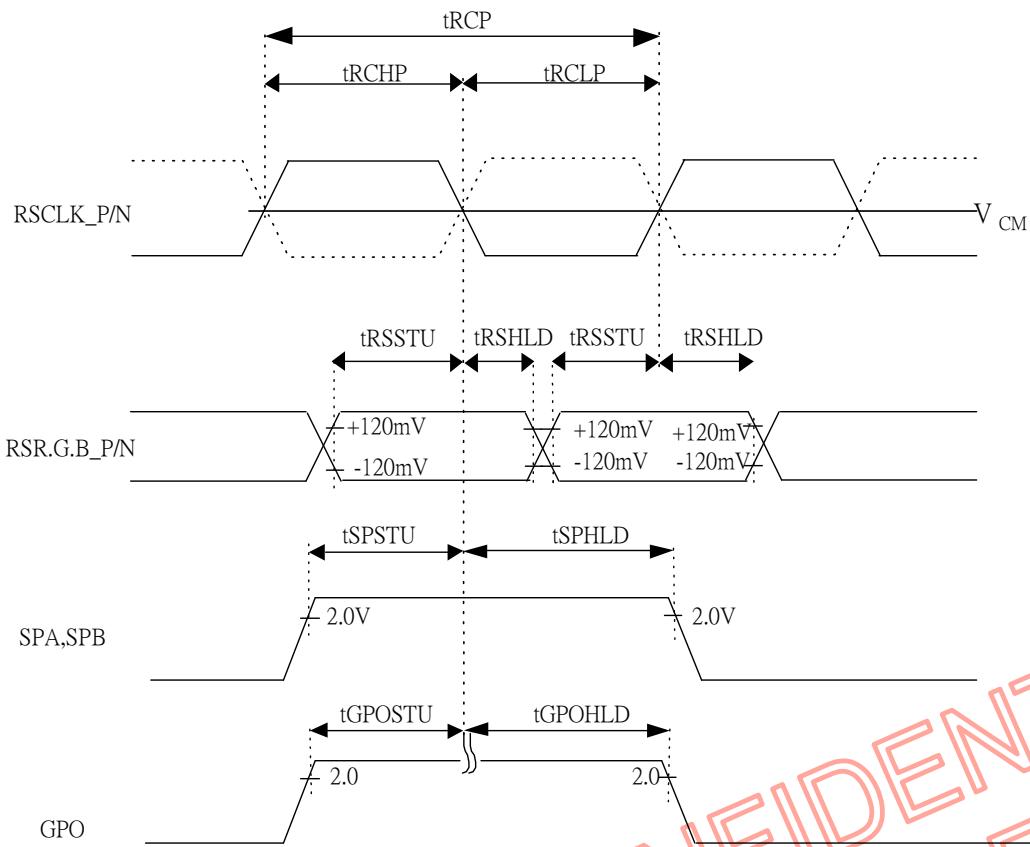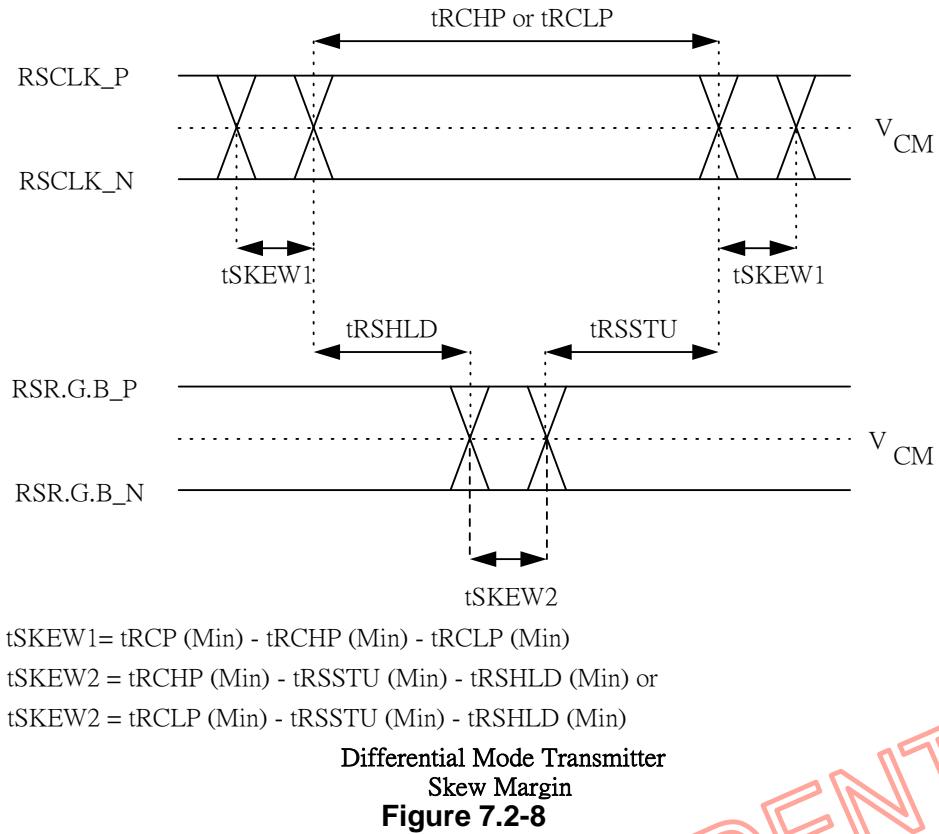
LCD Display Control Timing without TCON
LVDS Timing

Symbol	Parameter	Min.	Typ.*	Max.	Unit	Conditions
t_{d0}	Delay Time, TCLK↓ to Serial Bit Position 0	-0.20	0	0.20	ns	f = 65 MHz
t_{d1}	Delay Time, TCLK↓ to Serial Bit Position 1	2.00	2.20	2.40	ns	t_c =15.38 ns
t_{d2}	Delay Time, TCLK↓ to Serial Bit Position 2	4.20	4.40	4.60	ns	(±0.2%),
t_{d3}	Delay Time, TCLK↓ to Serial Bit Position 3	6.39	6.59	6.79	ns	See Figure
t_{d4}	Delay Time, TCLK↓ to Serial Bit Position 4	8.59	8.79	8.99	ns	7.2.10
t_{d5}	Delay Time, TCLK↓ to Serial Bit Position 5	10.79	10.99	11.19	ns	
t_{d6}	Delay Time, TCLK↓ to Serial Bit Position 6	12.99	13.19	13.39	ns	
t_{d0}	Delay Time, TCLK↓ to Serial Bit Position 0	-0.20	0	0.20	ns	f = 85 MHz
t_{d1}	Delay Time, TCLK↓ to Serial Bit Position 1	1.48	1.68	1.88	ns	t_c =11.76 ns
t_{d2}	Delay Time, TCLK↓ to Serial Bit Position 2	3.16	3.36	3.56	ns	(±0.2%),
t_{d3}	Delay Time, TCLK↓ to Serial Bit Position 3	4.84	5.04	5.24	ns	See Figure
t_{d4}	Delay Time, TCLK↓ to Serial Bit Position 4	6.52	6.72	6.92	ns	7.2.10
t_{d5}	Delay Time, TCLK↓ to Serial Bit Position 5	8.20	8.40	8.60	ns	
t_{d6}	Delay Time, TCLK↓ to Serial Bit Position 6	9.88	10.08	10.28	ns	
t_{d7}	Delay Time, CLKIN↑ or CLKIN ↓ to TCLK↑	3.0	4.2	5.5	ns	See Figure 7.2.6
t_{jcc}	Transmitter Jitter Cycel-to-Cycle		110	150	Ps	f = 85 MHz
			210	230	ps	f = 65 MHz

t_w	Pulse Duration, High-Level Output Clock	$0.35t_c$	$\frac{4}{7}t_c$	$0.65t_c$	ns	
t_t	Transition Time, Differential Output Voltage (t_r or t_f)	260	700	1500	ps	See Figure 7.2.6
t_{en}	Enable Time, $\overline{PWDN}\uparrow$ to Phase Lock (TCLK Valid)			10	ms	See Figure 7.2.7
t_{dis}	Disable Time, $\overline{PWDN}\downarrow$ to Off State (TCLK Low)			100	ns	See Figure 7.2.8

* All typical values are at VCC = 3.3V, T_A = 25°C
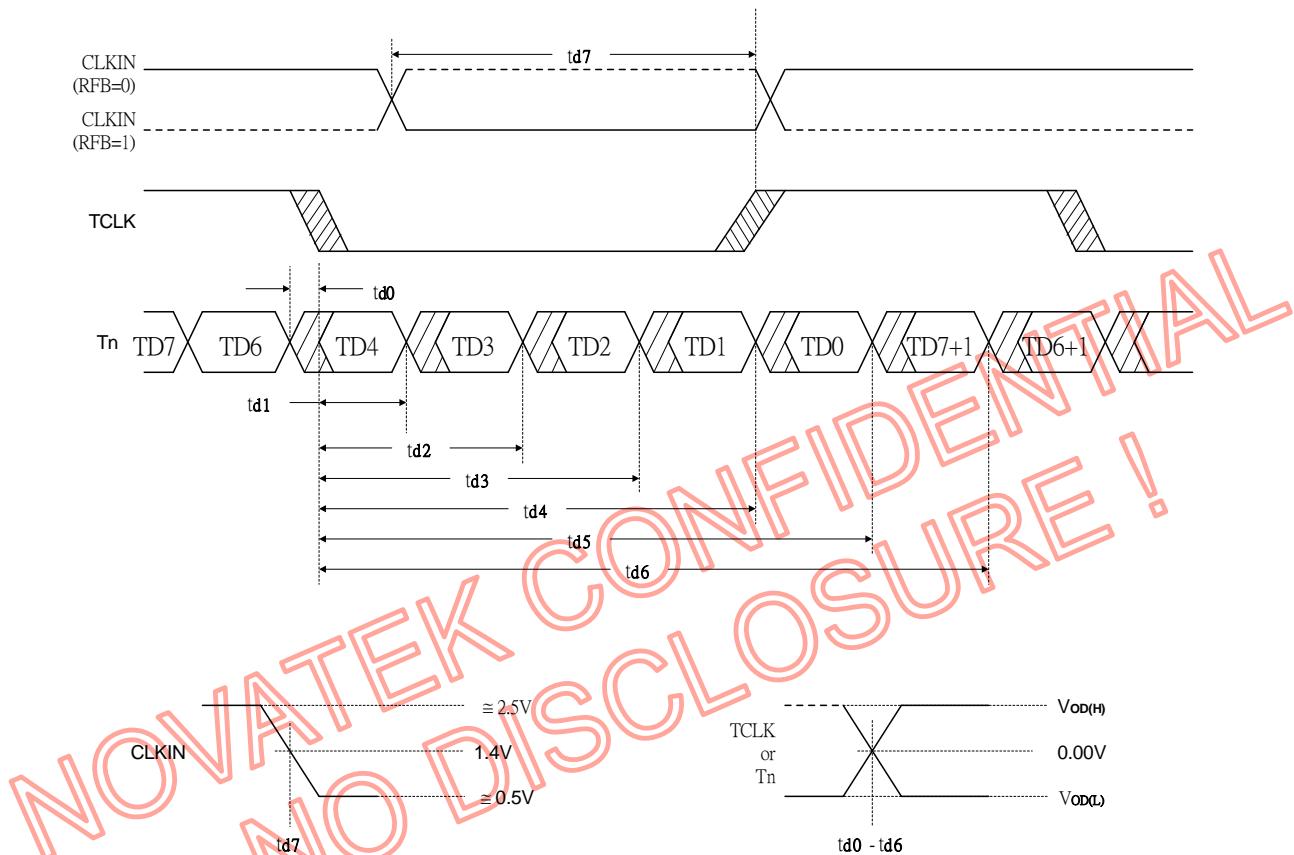
Figure 7.2-9 LVDS Timing Definitions
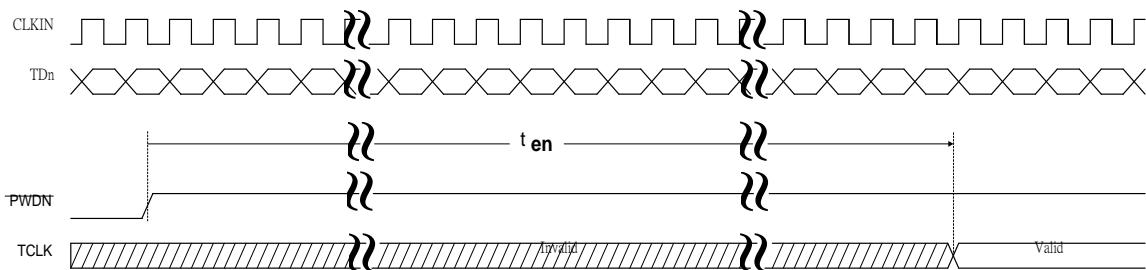
Figure 7.2-10 LVDS Enable Time Waveforms
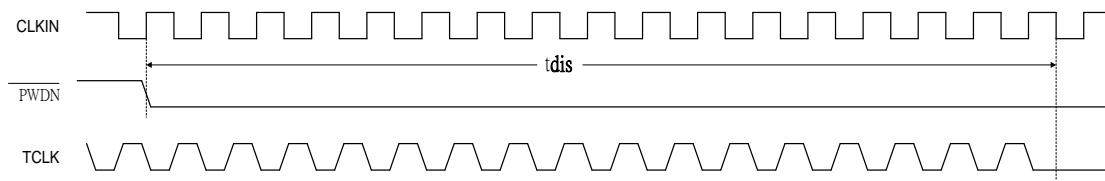
Figure 7.2-11 LVDS Disable Time Waveforms

MCU Electrical Characteristics

A/D Converter						
Symbol	*Parameter*	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
t_{CNVT}	A/D Conversion Time	-	-	15	us	
V_{OFFSET}	A/D Converter Error	-	-	1	LSB	
V_{LINEAR}	A/D Input Dynamic Range of Linearity Conversion	GND	-	MCU_VCC	V	
Reset Block						
Symbol	*Parameter*	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
$t_{PW(RSTB)}$	Active-Low External Reset Pulse Width	-	64	-	t_{OSC}	
$t_{RST(POR)}$	Internal Reset Interval for Power-On Reset	-	2^{16}	-	t_{OSC}	
$t_{RST(WDT)}$	Watch-Dog Reset Period	500	520	540	ms	f_{OSC} = 24MHz

DDC2B+ Mode

Symbol	Parameter		Standard Mode		Fast Mode		Unit
			Min.	**Max**	**Min**	**Max**	
f_{SCL}	SCL Clock Frequency			100		400	KHz
t_{BUF}	Bus Free Between a STOP and START Condition		4.7		1.3		us
$t_{HD;STA}$	Hold Time for START Condition		4.0		0.6		us
t_{LOW}	LOW Period of The SCL Clock		4.7		1.3		us
t_{HIGH}	HIGH Period of The SCL Clock		4.0		0.6		us
$t_{SU;STA}$	Set-up Time for a Repeated START Condition		4.7		0.6		us
$t_{HD;DAT}$	Data Hold Time	Transmitter	0.1		0.1	0.9	us
		Receiver	0		0		
$t_{SU;DAT}$	Data Set-up Time		250		100		ns
t_r	Rise Time of Both SDA and SCL Signals			1000		300	ns
t_f	Fall Time of Both SDA and SCL Signals			300		300	ns
$t_{SU;STO}$	Set-up Time for STOP Condition		4.0		0.6		us

t_{SP}	Pulse Width of spikes which must be suppressed by the input filter	0	50	0	50	ns
C_I	Capacitance for each Bus Pin	-	10		10	pF
C_b	Capacitive load for each Bus Line	-	400		400	pF

IIC-Bus Timing

Symbol	Parameter	Standard Mode		Fast Mode		Unit
		Min.	Max	Min	Max	
$V_{IL(I2C)}$	Low Level Input Voltage	-0.5	1	-0.5	1	V
$V_{IH(I2C)}$	High Level Input Voltage	2.3	MCU_VCC +0.5	2.3	MCU_VCC +0.5	V
$V_{LT(I2C)}$	Schmitt Lower-Threshold Voltage for I^2C bus	1	1.5	1	1.5	V
$V_{UT(I2C)}$	Schmitt Upper-Threshold Voltage for I^2C bus	1.9	2.3	1.9	2.3	V
$V_{OL1(I2C)}$	Low Level Output Voltage @Io=3mA	0	0.4	0	0.4	V
$V_{OL2(I2C)}$	Low Level Output Voltage @Io=6mA	0	0.6	0	0.6	V
t_{OF}	Output Fall Time @Co=400pF		250		250	ns
I_I	Input Current @Vi=0.4 ~ 0.9VCC	-10	10	-10	10	uA
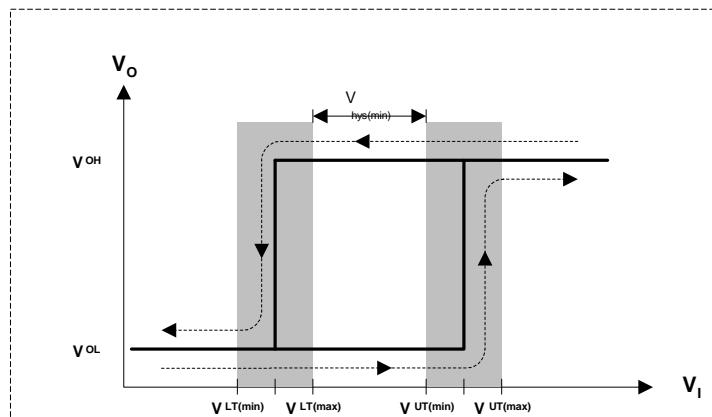
Schmitt Trigger Characteristics

2006-02-09

Ver. 0.40

8. Application Circuit
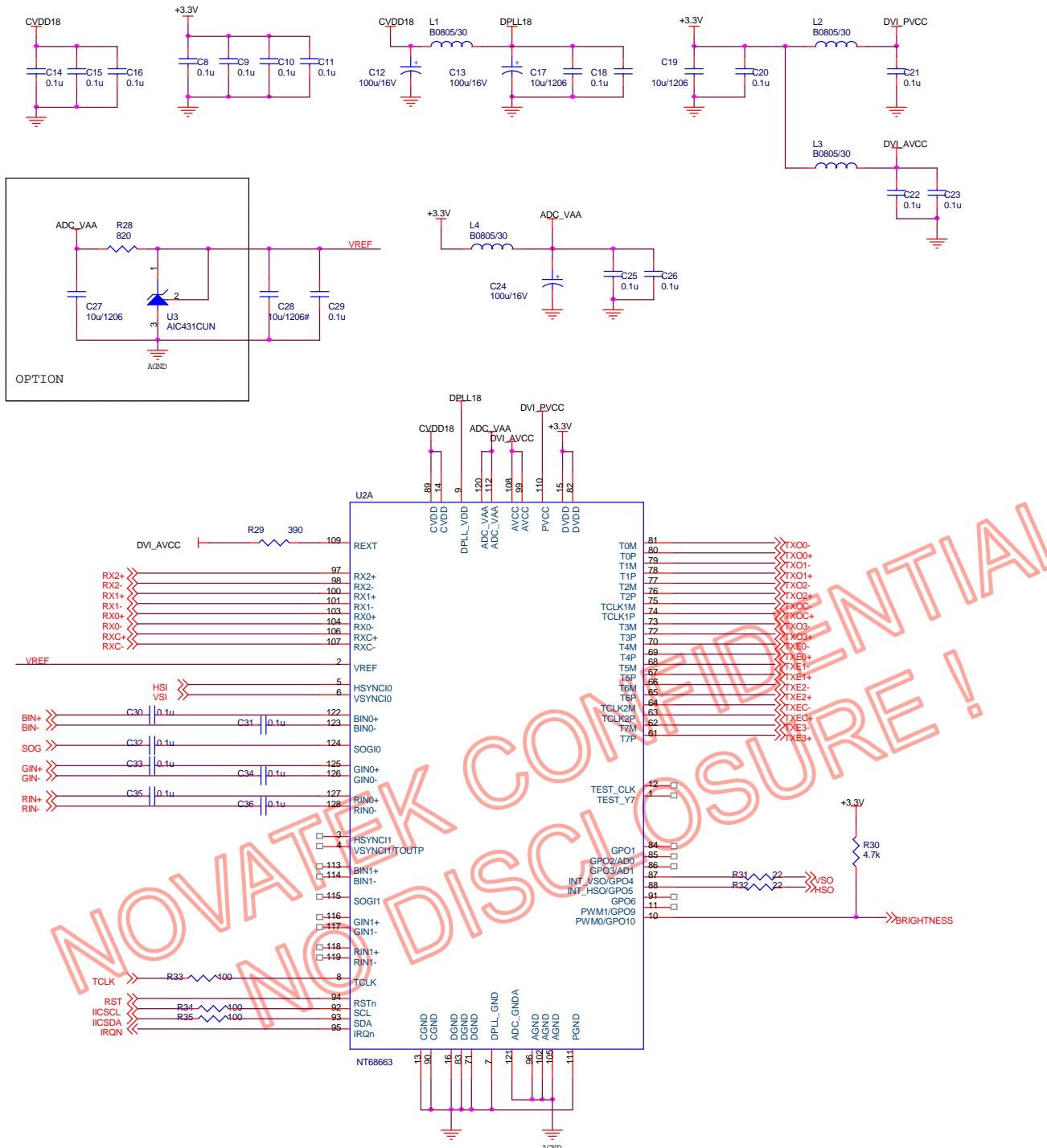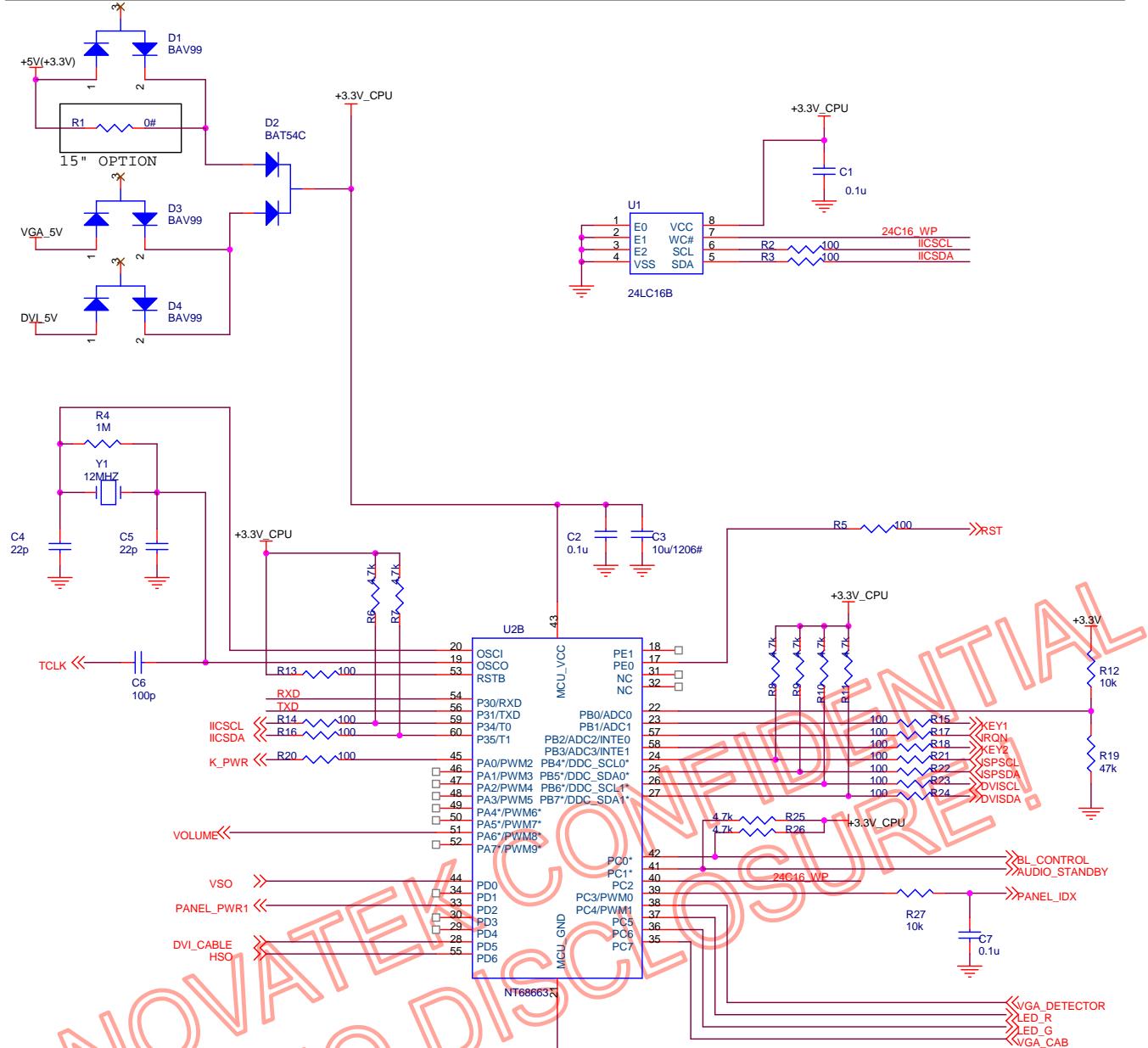
Figure 8-1 Application Circuit

9. Registers Mapping

	Block Name		Byte Offset	Size (bytes)	
	ADC PLL Interface	Page 0	0x000 ~ 0x017	32	
	DVI Input Control 1		0x018 ~ 0x01E		
	Graphic Port Control		0x020 ~ 0x03F	32	
	Video Port Control		0x040 ~ 0x05F	32	
	Back End Image Processing		0x060 ~ 0x064	4	
	NR Control		0x068 ~ 0x06F	8	
	GPIO Control		0x070 ~ 0x073	4	
	PWM Control		0x074 ~ 0x077	4	
	DDC Control		0x078 ~ 0x07D	6	
	OSD Control		0x080 ~ 0x0CF	80	
	Index Port Access Control		0x0E0 ~ 0x0E3	4	
	Misc. Access Control		0x0E5 ~ 0x0E6	2	
	HS Digital PLL		0x0D0 ~ 0x0DF 0x0E8 ~ 0x0EF	24	
	Display Digital PLL & SSC		0x0F0 ~ 0x0F7	8	
	Gauge Control		0x0F8 ~ 0x0FD	5	
	Page Control		0x0FF	1	
	Power Control	Page 1	0x101 ~ 0x102	2	
	Auto Tune		0x106 ~ 0x12F	32	
	Bright Frame Display		0x130 ~ 0x13B		
	Display General Control		0x150 ~ 0x18F	48	
	Sync Processor		0x196 ~ 0x1B0	27	
	sRGB Control		0x1D0 ~ 0x1DF	16	
	Test Mode		0x1E0 ~ 0x1FE	31	
	Page Control		0x1FF	1	

9.1. ADC Interface

0x000		ADCPLL Control	R/W
Bits	Name	Description	
7		Reserved	
6		Reserved	
5		Reserved	
4	HPLL_HSYNC_SEL	HPLL Hsync input signal selection 0: HSYNCI (pad sync from HSYNCI0 or HSYNCI1) 1: SYNC_HS (Internal signal from sync processor)	
3	HSYNC_SEL	PLL Hsync input signal selection 0: HSYNCI (HSYNCI0/HSYNCI1) 1: SOGI	
2		Reserved	
1	REG_VREF	ADCPLL reference voltage (2.5V) source select 0: External (from VREF pin) 1: Internal (from internal regulator)	
0		Reserved	

Default: 1010 0000B

0x001		Red Channel Gain Control	R/W
Bits	Name	Description	
7-0	RGAIN[8:1]	The RAGAIN[7:0] that sets the gain of the R channel. The ADC can accommodate input signals with a full-scale range of between 0.55V and 0.9Vp-p. Note that increasing RGAIN results in the picture having less contrast.	

Default: 1000 0000B

0x002		ADC test control	R/W
Bits	Name	Description	
7-3		Reserved	
2-0	CMCTL[2:0]		

Default: 0000 0010B

0x003		Red Channel DC Shift Control	R/W
Bits	Name	Description	
7-0	RCSC [7:0]	Control the R channel DC shift value to compensate the color excursion. Bigger value gives less brightness.	

Default: 0100 0000B

0x004		Green Channel Gain Control	R/W
Bits	Name	Description	
7-0	GGAIN[8:1]	The GAGAIN[7:0] that sets the gain of the G channel. The ADC can accommodate input signals with a full-scale range of between 0.55V and 0.9Vp-p. Note that increasing GGAIN results in the picture having less contrast.	

Default: 1000 0000B

0x005		ADC test control	R/W
Bits	Name	Description	

7-5		Reserved
4	CMP2I	
3-0	GNB[3:0]	

Default: 0000 0000B

0x006	Green Channel DC Shift Control		R/W
Bits	Name	Description	
7-0	GCSC [7:0]	Control the G channel DC shift value to compensate the color excursion. Bigger value gives less brightness.	

Default: 0100 0000B

0x007	Blue Channel Gain Control		R/W
Bits	Name	Description	
7-0	BGAIN[8:1]	The BAGAIN[7:0] that sets the gain of the B channel. The ADC can accommodate input signals with a full-scale range of between 0.55V and 0.9Vp-p. Note that increasing BGAIN results in the picture having less contrast.	

Default: 1000 0000B

0x008	ADC Channel and MID Clamp Control		R/W
Bits	Name	Description	
D7-4		Reserve	
3	YUV_SEL0	Input Type Select. 0: Analog (RGB) 1: Digital (YUV)	
2	CHANNEL_SEL	Input Mux Control. 0: Channel 0 1: Channel 1	
1	BMID	Blue Clamp Select 0: Clamp to ground 1: Clamp to midscale	
0	RMID	Red Clamp Select 0: Clamp to ground 1: Clamp to midscale	

Default: XXXX 0000B

0x009	Blue Channel DC Shift Control		R/W
Bits	Name	Description	
7-0	BCSC[7:0]	Control the B channel DC shift value to compensate the color excursion. Bigger value gives less brightness.	

Default: 0100 0000

0x00A	Reserved		R/W
Bits	Name	Description	
7-0		Reserved	

Default: XXXX 0110B

0x00B	Reserved		R/W
Bits	Name	Description	
7-0		Reserved	

Default: 1001 0111B

0x00C		Reserved	R/W
Bits	Name	Description	
7-0		Reserved	

Default: 0101 0101B

0x00D		Reserved	R/W
Bits	Name	Description	
7-6		Reserved	

Default: 0100 0000B

0x00E		ADC PLL Power-up Control	R/W
Bits	Name	Description	
7		Reserved	
6		Reserved	
5	BGAIN[0]	BGAIN bit 0	
4	GGAIN[0]	GGAIN bit 0	
3	RGAIN[0]	RGAIN bit 0	
2	PU_Badc1	1= Power-up B channel A2D converter.	
1	PU_Gadc1	1= Power-up G channel A2D converter.	
0	PU_Radc1	1= Power-up R channel A2D converter.	

Default: 1111 1111B

0x00F		ADC Status	R
Bits	Name	Description	
7-0		Reserved	

Default: 0000 0000B

0x00F		ADC Status	W
Bits	Name	Description	
7-0		Reserved	

Default: 0000 0000B

0x010		Analog Bandwidth Control	R/W
Bits	Name	Description	
7-4		Reserved	
3			
2-1	ADC_BW [1:0]	Analog bandwidth select 11 : 500 MHz 10 / 01: 300 MHz 00 : 75 MHz	
0		Reserved	

Default: XXXX X11XB

0x011		Reserved	R/W
Bits	Name	Description	
7-0		Reserved	

Default: XXXX XXXXB

0x012		SOG Slicer Control	R/W
Bits	Name	Description	

7-3	SOG_THR [4:0]	The comparator threshold of the Sync-on-Green Slicer to be adjusted. This register adjust it in steps of 10 mV, with the setting 10 mV <= SOG_THR <=330 mV
2	EN_SOG_SLICER	Enable internal SOG Slicer. 0 = Disable 1 = Enable
0-1		Reserved

Default: 0111 11XXB

0x013		White Balance Control	R/W
Bits	Name	Description	
7-2		Reserved	
1-0	VREF[1:0]	Select the signal source for VGA input. When VR1 or VR2 is selected, the PLL will go into free-run state. 00: VR0. Internal zero voltage. 01: Internal test mode 10: VR2. Internal reference voltage 2. (0.7V) 11: Normal. From external RGB input pin.	

Default: XXXX XX11B

0x014		Hsync Trigger Level Control	R/W
Bits	Name	Description	
6-4	HS_THR_H	The trigger level threshold of the sync high level to be adjusted. This register adjust it in steps of 100 mV, with the setting 1500 mV <= HS_THR_H <=2200 mV	
2-0	HS_THR_L	The trigger level threshold of the sync low level to be adjusted. This register adjust it in steps of 100 mV, with the setting 700 mV <= HS_THR _L<=1400 mV	

Default: X000 X000B

0x015		Reserved	R/W
Bits	Name	Description	
7-0			

Default: XXXX XXXXB

9.2. DVI Input Control 1

0x016		DVI Clock Detection	R
Bits	Name	Description	
7-0	DVI_CLK	DVI clock detection	

Default: XXXX XXXXB

0x017		DVI Control	R/W
Bits	Name	Description	
7-0			

Default: XXXX XXXXB

0x018		DVI Control 1	R/W
Bits	Name	Description	
7-6	DPLL_LOOP_FIT [1:0]	TMDS PLL loop filter control	

5	BSTREAM_CHK	Bit Stream error correction control 0 = Disable 1 = Enable
4	FSM_RST	DPLL FSM Disable 0 = Enable 1 = Disable
3	SYNC_SEL	Sync is generated from R channel or B channel 0 = From B Channel (RX0) 1 = From R Channel (RX2)
2	FORCE_BND_EEC	Force boundary error correction enable
1	BND_EEC_EN	Adaptive boundary error correction enable
0	DPLL_ACT	TMDS DPLL working mode selection

Default: 0000 0000B

0x019	DVI Control 2		R/W
Bits	Name	Description	
7-6	DVI_DET_CHANNEL [1:0]	Detection channel select 00: RX0 01: RX1 10: TX2 11: Reserved	
5-4	DVI_TRIG_SRC [1:0]	Detection trig point select 00: V Sync Other: Always trig	
3-2		Reserved	
1	DPLL_FSM_MOD	DPLL FSM mode select 0 = 3 state FSM 1 = 5 state FSM	
0	EXT_UDCHK_EN	Extend up/down check enable	

Default: 0000 0000B

0x01A	DVI Control 3		R/W
Bits	Name	Description	
7-6	DVI_DET_LEN [1:0]	DVI detection length 00: 32 01: 64 10: 96 11: 128	
5-4	DVI_DET_TYPE [1:0]	DVI detection type	
3		Reserved	
2	DVI_DET_SYNC_POL	DVI detection sync polarity invert 0 = Normal 1 = Inverted	
1	DVI_DET_RDY	DVI detection data ready 0 = No data 1 = Ready	
0	DVI_DET_EN	DVI detection data enable	

Default: 0000 0000B

0x01B	DVI Control 4	R/W

Bits	Name	Description
7-0	DVI_DET_DATA [7:0]	DVI detection data

Default: 0000 0000B

0x01C	DVI Control 5	R/W

Bits	Name	Description
7-0	DVI_CLK_DLY	Control the delay of recovered clock

Default: 0000 0000B

0x01D	DVI Control 6	R/W

Bits	Name	Description
7	DVI_CLK_DLY_EN	Enable the delay of recovered clock
6-0	DVI_PLL_BW	Bandwidth control of PLL

Default: 0001 1111B

0x01E	DVI Control 7	R/W

Bits	Name	Description
7-0	DVI_EQ_DATA	Equalizer bias current control

Default: 0111 1000B

9.3. Pre-Pattern Control

0x01F		Pre-Pattern Control	R/W
Bits	Name	Description	
7	PRE_PATT_EN	Pre-Pattern Enable. 0 = Disable 1 = Enable	
6	PRE_INV	Pre-Pattern Data invert 0 = Normal 1 = Invert the RGB Data	
5	PRE_CBAR_EN	Paste a Cross Bar on the built-in Pre-pattern and the Bar's gray level is controlled via CBAR_FG[7:0] register (0x15A) 0 = Disable 1 = Enable	
4	PRE_PATT_BK	Built-in pre-pattern bank Select 0 = Bank 0 1 = Bank 1	

3-0	PRE_PATT_SEL [3:0]	Select built-in pre-pattern type
		Pattern number = 0~7
		
		If PRE_PATT_BK = Bank 0
		0000 = Reserved
		0001 = Dot Moiré
		0010 = Vertical Line Moire (1B1W)
		0011 = Vertical Line Moire (2B1W)
		0100 = Vertical Line Moire (2B2W)
		0101 = 256 V_Gray Bar
		0110 = 256 H_Gray Bar
		0111 = Horizontal Line Moire (1B1W)
		1000 = Horizontal Line Moire (2B1W)
		1001 = Horizontal Line Moire (2B2W)
		1010 = Chat Pattern
		1011 = White Pattern
		11xx = Rectangular pattern, outline width is defined by xx bits.
		  00 = 1 pixel
		  01 = 3 pixels
		  10 = 5 pixels
		  11 = 7 pixels
		
		If PATT_BK = Bank 1
		0000 = Black pattern
		0001~1111 = Reserved	

Default: 0000 0000B

9.4. Graphic Port Control

- ♦ ADC/TMDS/Digital input source selection
- ♦ Clamp pulse
- ♦ Interlace decision window
- ♦ Mask window
- ♦ Capture window

General Control

0x020		Graphic Port Control	R/W
Bits	Name	Description	
7	GI_VSYNC_EDGE	Select the V sync referenced edge. 0 = Leading edge 1 = Trailing edge	
6	GI_IFLD_INV	Invert the internal field reference signal for data merging priority 0 = Normal 1 = Invert	
5	GI_MKWIN_EN	Mask Window Enable. When GI_MKWIN_EN =1, GI_HMASK_BEG, GI_HMASK_END, GI_VMASK_BEG and GI_VMASK_END are used to set the window around the HSYNC and VSYNC during which the captured data is 0x000 and auto tune is ignored. This filters out noise occurring on the RGB channels around the HSYNC and VSYNC pulse. 0 = Disable 1 = Enable	
4	GI_WRAP_SEL	Wrap around method select. 0 = Wrap around 1 = Wrap black	
3	GI_HSYNC_EDGE	Select the H sync referenced edge. 0 = Leading edge 1 = Trailing edge	
2	GI_INTE_EN	Interlaced input enable. When GI_INTE_EN =1, the field status is reference to internal field detector. 0 = Non-interlaced 1 = Interlaced	
1	GI_SRC_SEL	Graphic input source select 0 = ADC 1 = TMDS/Digital	
0	GI_CAP_EN	Graphic input capture enable 0 = Disable 1 = Enable	

Default: 0000 0000B

0x021		Clamp Pulse Begin	R/W
Bits	Name	Description	
7	CLAMP_EDG	Clamp Pulse Reference Edge 0 = GHS rising edge 1 = GHS falling edge	
6	CLAMP_POL	Clamp Pulse Polarity. 0 = Active Low 1 = Active High	
5-0	CLAMP_BEG [5:0]	Clamp Pulse Begin. (Unit 4xCLP_REFCLK) CLAMP_BEG =5, means waiting 5 x 4CLP_REFCLK after GHS edge to begin the pulse.	

Default: 0000 0000B

0x022		Clamp Pulse Width	R/W
Bits	Name	Description	
7	CLAMP_EN	Clamp Pulse Enable 0 = Disable	

Free Datasheet http://www.datasheet4u.com/

		1 = Enable
6	CLP_CLK_SEL	Clamp Pulse Reference clock (CLP_REFCLK = Capture Clock) Select 0 = CLP_REFCLK 1 = 2 x CLP_REFCLK
5-0	CLAMP_WID [5:0]	Clamp Pulse Width.(unit 4xCLP_REFCLK) CLAMP_WID =5, means pulse width being 6 x 4CLP_REFCLK wide.

Default: 0000 1111B

0x023		Digital Port Input Control	R/W
Bits	Name	Description	
7	YPbPr_EN	YPbPr Input Enable	
6	CLAMP_SOURCE	Clamp source select. 0 = selects Row Hs to be used for clamping. 1 = selects Sync Separated Hsync to be used for clamping.	
5	HS_DEJITTER_EN	For TMDS input mode, This bit enables/disable the HSYNC De-jitter function. 0 = Disable 1 = Enable	
4	DEJITTER_RST	For TMDS input mode, De-jitter reset 0 = Normal 1 = Reset	
3	HCAP_DE_EN	For TMDS input mode, active data is enclosed by DE signal. Hardware can automatically capture the first data and bypass the setting of capture begin registers (0x034~0x035). This bit is effective if DVI_SYNC_SEL=1 (0x192 bit 7). 0 = According to horizontal capture registers 1 = According to DE signal	
2			
1	DVI_DE_INV	DVI DE auto detection control	
0	SYNC_SEL	Sync processor input path selection 0: Graphic 1: Video	

Default: 0000 0000B

0x024		ADCLK Delay Control	R/W
Bits	Name	Description	
7-0		Reserved	
3-0		Reserved	

Default: 0000 0000B

0x025		ADCLK Delay & Invert Control	R/W
Bits	Name	Description	
6	CLKI_INV	Internal data latch clock invert 0 = Normal 1 = Invert	
5		Reserved	
4		Reserved	
3-0	CLKI_DLY	Internal data latch clock delay (0.5nS/step) 0~15 step	

Default: X000 0000B

0x026		Data Delay & Swap Control	R/W
Bits	Name	Description	
7	CLAMP_MASK_EN	Clamping pulse mask enable	
6		Reserved	
5	CAP_RB_SWAP	Capture R/B channel swap 0 = Normal 1 = Swap	
4		Reserved	
3		Reserved	
2	CAP_BIT_SWAP	Capture data bit swap D7-D0 -> D0-D7 0 = Normal 1 = Swap	
1		Reserved	
0	CAP_DATA_DLY	Capture data delay 0 = Normal 1 = Delay 1 ADCLK	

Default: 0000 0000B

0x027		Vsync and DE Delay	R/W
Bits	Name	Description	
6-4	GI_DEDLY [2:0]	Delay the graphic port internal DE pulse by input pixel clock to avoid the unmatched data phase -4~+3 pixel clocks delay	
3-0	GI_VSDLY [3:0]	Delay the graphic port VSYNC pulse by input pixel clock to avoid the confusion of 1st HSYNC recognized following VSYNC leading edge. 0~15 pixel clocks delay	

Default: X011 0001B

0x028		Hsync edge detection control 1	R/W
Bits	Name	Description	
7-6		Reserved	
5-4		Reserved	
3-2		Reserved	
1		Reserved	
0		Reserved	

Default: 0000 0000B

0x029		Hsync edge detection control 2	R/W
Bits	Name	Description	
7		Reserved	
6		Reserved	
5-4		Reserved	
3		Reserved	
2		Reserved	
1-0		Reserved	

Default: 0000 0000B

Mask Window Define

0x02A		Horizontal Mask Window Begin	R/W
Bits	Name	Description	

| 7-0 | GI_HMASK_BEG [7:0] | Horizontal Mask Window Begin. When GI_MKWIN_EN =1, this register sets the number of clocks after the referenced edge of the HSYNC pulse in which the captured data is '0x00' and the auto-tune starts outside this window. |

Default: 0000 0000B

0x02B	Horizontal Mask Window End		R/W
Bits	Name	Description	
7-0	GI_HMASK_END [7:0]	Horizontal Mask Window End. When GI_MKWIN_EN =1, this register sets the number of clocks before the referenced edge of the HSYNC pulse in which the captured data is '0x00' and the auto-tune stops.	

Default: 0000 0000B

0x02C	Vertical Mask Window Begin		R/W
Bits	Name	Description	
7-0	GI_VMASK_BEG [7:0]	Vertical Mask Window Begin. When GI_MKWIN_EN =1, this register sets the number of lines after the referenced edge of the VSYNC pulse in which the captured data is '0x00' and auto-tune starts outside this window.	

Default: 0000 0000B

0x02D	Vertical Mask Window End		R/W
Bits	Name	Description	
7-0	GI_VMASK_END [7:0]	Vertical Mask Window End. When GI_MKWIN_EN =1, this register sets the number of lines before the referenced edge of the VSYNC pulse in which the captured data is '0x00' and the auto-tune stops.	

Default: 0000 0000B
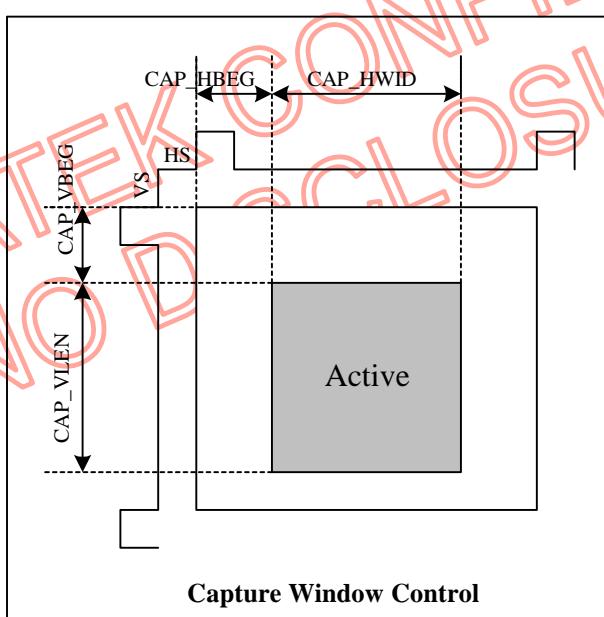
Figure 9.4-1

Capture Window Control

0x02E	Capture Vertical Begin for Odd Field -lo		R/W
Bits	Name	Description	
7-0	GI_CAP_VBEGO	Vertical Capture Begin for Odd Field. GI_CAP_VBEGO indicates how	

[7:0]		many lines to wait after referenced edge of VSYNC before starting image capture. GI_CAP_VBEGO =3, means waiting 3 lines to begin capture. This register is double-buffered.

Default: 0000 0000B

0x02F	**Capture Vertical Begin for Odd Field -hi**	**R/W**
Bits	Name	Description
2-0	GI_CAP_VBEGO [10:8]	MSB of GI_CAP_VBEGO. This register is double-buffered.

Default: XXXX X000B

0x030	**Capture Vertical Begin for Even Field -lo**	**R/W**
Bits	Name	Description
7-0	GI_CAP_VBEGE [7:0]	Vertical Capture Begin for Even Field. GI_CAP_VBEGE indicates how many lines to wait after referenced edge of VSYNC before starting image capture. GI_CAP_VBEGE =3, means waiting 3 lines to begin capture. This register is double-buffered.

Default: 0000 0000B

0x031	**Capture Vertical Begin for Even Field -hi**	**R/W**
Bits	Name	Description
2-0	GI_CAP_VBEGE [10:8]	MSB of GI_CAP_VBEGE. This register is double-buffered.

Default: XXXX X000B

0x032	**Capture Vertical Length -lo**	**R/W**
Bits	Name	Description
7-0	GI_CAP_VLEN [7:0]	Vertical Capture Length. GI_CAP_VLEN indicates how many lines to capture. GI_CAP_VLEN = 3, means capturing 3 lines. This register is double-buffered.

Default: 0000 0000B

0x033	**Capture Vertical Length –hi**	**R/W**
Bits	Name	Description
2-0	GI_CAP_VLEN [10:8]	MSB of GI_CAP_VLEN. This register is double-buffered.

Default: XXXX X000B

0x034	**Capture Horizontal Begin –lo**	**R/W**
Bits	Name	Description
7-0	GI_CAP_HBEG [7:0]	Horizontal Capture Begin. GH_CAP_HBEG indicates how many pixels to wait after referenced edge of HSYNC before starting image capture. GH_CAP_HBEG =3, means waiting 3 pixels to begin capture. This register is double-buffered.

Default: 0000 0000B

0x035	**Capture Horizontal Begin –hi**	**R/W**
Bits	Name	Description
3-0	GI_CAP_HBEG [11:8]	MSB of GI_CAP_HBEG. This register is double-buffered.

Default: XXXX 0000B

0x036		Capture Horizontal Width –lo	R/W
Bits	Name	Description	
7-0	GI_CAP_HWID [7:0]	Horizontal Capture Width. GI_CAP_HWID indicates how many pixels to capture. GI_CAP_HWID = 3, means capturing 3 pixels. This register is double-buffered.	

Default: 0000 0000B

0x037		Capture Horizontal Width –hi	R/W
Bits	Name	Description	
3-0	GI_CAP_HWID [11:8]	MSB of GI_CAP_HWID. This register is double-buffered.	

Default: XXXX 0000B

0x038		Alternate sampling control	R/W
Bits	Name	Description	
3	DE_MK_EN	For TMDS mask DE Mode enable	
2	CLK_MK_EN	Capture clock mask enable	
1	GI_ALT_INV	The alternate sampling reference frame signal polarity control 0 = Active Low 1 =Active High	
0	GI_ALT_EN	Input alternate sampling enable. This bit should be enabled for input graphic pixel rate lager than SXGA@75Hz, . 0 = Disable 1 = Enable	

Default: XXXX XX00B

0x039		Clock mask window control	R/W
Bits	Name	Description	
7-0	CLK_MASK_WID	Clock mask width. When CLK_MK_EN =1, this register sets the number of clocks after the internal de signal. Unit: 2 ADC sample clock	

0x03A~0x03B		Reserved	R/W
Bits	Name	Description	
7-0			

Default: XXXX XXXXB

0x03C		DVI Input Horizontal Active Width-lo	R
Bits	Name	Description	
7-0	DVI_CAP_HWID [7:0]	The active window horizontal width. The value is valid only for DVI interface is enabled and the SYNC input source is from DVI DE signal	

Default: 0000 0000B

0x03D		DVI Input Horizontal Active Width-hi	R
Bits	Name	Description	
3-0	DVI_CAP_HWID [11:8]	MSB of DVI_CAP_HWID	

Default: XXXX 0000B

0x03E		DVI Input Vertical Active Length-lo	R
Bits	Name	Description	

7-0	DVI_CAP_VLEN [7:0]	The active window vertical length. The value is valid only for DVI interface is enabled and the SYNC input source is from DVI DE signal

Default: 0000 0000B

0x03F	DVI Input Vertical Active Length-hi	R
Bits	Name	Description
2-0	DVI_CAP_VLEN [10:8]	MSB of DVI_CAP_VLEN

Default: XXXX X000B

9.5. Video Port Control

General Control

0x040		Video Port Control 1	R/W
Bits	Name	Description	
7		Reserved	
6:5	VI_BT656_EN	When Video port is active, select between 8-bit wide or 16-bit wide data capture. 00 = Reserved 01 = Reserved 1X = 8-bit wide BT656 processing from Video Port (YUV0 / YUV1)	
4	UV_SWAP	Swap the order of received UV data. 0 = Normal 1 = Swap	
3	YUV_PORT_SEL	YUV input port selection. 0 = YUV0 (Located from Pin55~62) 1 = YUV1 (Located from Pin30~37)	
2	EXFLD_EN	Select field indicator source. When VI_INTE_EN =1, this bit is in effect. 0 = From internal field detector 1 = From external EX_FIELD pin	
1	VI_INTE_EN	Interlaced input enable. When VI_INTE_EN =1, the field status is reference to internal field detector or external EXFLD input signal. 0 = Non-interlaced 1 = Interlaced	
0	VI_CAP_EN	Input capture enable 0 = Disabled 1 = Enabled	

Default: X000 0000B

0x041		Video Port Control 2	R/W
Bits	Name	Description	
5	VI_CAP_656_AUTO	For BT656 mode, when VI_CAP_656_AUTO = "1". Hardware referee to the setting of capture registers to capture the active data 0 = Disable 1 = Enable	
4	VI_MKWIN_EN	Mask Window Enable. When GI_MKWIN_EN =1, GI_HMASK_BEG, GI_HMASK_END, GI_VMASK_BEG and GI_VMASK_END are used to set the window around the HSYNC and VSYNC during which the captured data is 0x00 and auto tune is disabled. This filters out noise occurring on the RGB channels around the HSYNC and VSYNC pulse. 0 = Disable 1 = Enable	
3	VI_WRAP_SEL	Wrap around method select 0 = Wrap around 1 = Wrap black	
2	VI_SYNC_EDGE	Select the H/V sync reference edge. 0 = Leading edge 1 = Trailing edge	
1	VCAP_656_EN	For BT656 mode, active data is enclosed by SAV/EAV code. Hardware can automatically capture the active data and bypass the setting of capture registers except the Horizontal Capture Width.	

		0 = According to vertical capture registers 1 = According to SAV/EAV code
0	HCAP_656_EN	For BT656 mode, active data is enclosed by SAV/EAV code. Hardware can automatically capture the active data and bypass the setting of capture registers except the Horizontal Capture Width. 0 = According to horizontal capture registers 1 = According to SAV/EAV code

Default: XX00 0000B

0x042	Polarity Control		R/W
Bits	Name	Description	
5	VI_656CLK_INV	Invert the polarity of CLK for internal BT656 data processing unit 0 = Normal 1 = Invert	
4	VI_IFLD_INV	Invert the internal field reference signal for data merging priority 0 = Normal 1 = Invert	
3	VI_601CLK_INV	Invert the polarity of CLK for internal ITU601 data processing unit 0 = Normal 1 = Invert	
2		Reserved	
1		Reserved	
0		Reserved	

Default: XX00 0X00B

0x043	VSYNC Delay		R/W
Bits	Name	Description	
3-0	VI_VSDLY [3:0]	Delay the video port VSYNC pulse by input pixel clock to avoid the confusion of 1st HSYNC recognized following VSYNC trailing edge. 0~15 pixels delay	

Default: XXXX 0001B

Mask Window Define

0x047	Horizontal Mask Window Begin		R/W
Bits	Name	Description	
7-0	VI_HMASK_BEG [7:0]	Horizontal Mask Window Begin. When VI_MKWIN_EN =1, this register sets the number of clocks after the referenced edge of the HSYNC pulse in which the captured data is '0x00' and the auto-tune starts outside this window.	

Default: 0000 0000B

0x048	Horizontal Mask Window End		R/W
Bits	Name	Description	
7-0	VI_HMASK_END [7:0]	Horizontal Mask Window End. When VI_MKWIN_EN =1, this register sets the number of clocks before the referenced edge of the HSYNC pulse in which the captured data is '0x00' and the auto-tune stops.	

Default: 0000 0000B

0x049	Vertical Mask Window Begin		R/W
Bits	Name	Description	
7-0	VI_VMASK_BEG	Vertical Mask Window Begin. When VI_MKWIN_EN =1, this register sets	

	[7:0]	the number of lines after the referenced edge of the VSYNC pulse in which the captured data is '0x00' and auto-tune starts outside this window.

Default: 0000 0000B

| 0x04A		Vertical Mask Window End	R/W
Bits	Name	Description	
7-0	VI_VMASK_END [7:0]	Vertical Mask Window End. When VI_MKWIN_EN =1, this register sets the number of lines before the referenced edge of the VSYNC pulse in which the captured data is '0x00' and the auto-tune stops.	

Default: 0000 0000B

9.6. Color space conversion Control

Color Transfer Equation

$R = Y_{601} + COEFA*(Cr-128)/512$
$G = Y_{601} - COEFB*(Cr-128)/-512 - COEFC*(Cb-128)/-512$
$B = Y_{601} + COEFD*(Cb-128)/-512$

SDTV

$R = Y_{601} + 1.371(Cr-128)$
$G = Y_{601} - 0.698(Cr-128) - 0.336(Cb-128)$
$B = Y_{601} + 1.732(Cb-128)$

HDTV

$R = Y_{709} + 1.540(Cr-128)$
$G = Y_{709} - 0.459(Cr-128) - 0.183(Cb-128)$
$B = Y_{709} + 1.816(Cb-128)$

Color Transfer Coefficient

0x04B		Color Transfer Coefficient A -lo	R/W
Bits	Name	Description	
7-0	COEFA [7:0]	Video YUV/YPbPr to RGB Color Transfer Coefficient. 0~1023	

Default: 1011 1110B

0x04C		Color Transfer Coefficient A -hi	R/W
Bits	Name	Description	
1-0	COEFA [9:8]	MSB of COEFA	

Default: XXXX XX10B

0x04D		Color Transfer Coefficient B -lo	R/W
Bits	Name	Description	
7-0	COEFB [7:0]	Video YUV/YPbPr to RGB Color Transfer Coefficient. 0~1023	

Default: 0110 0101B

0x04E		Color Transfer Coefficient B -hi	R/W
Bits	Name	Description	
1-0	COEFB	MSB of COEFB	

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		[9:8]	

Default: XXXX XX01B

0x04F		Color Transfer Coefficient C -lo	R/W
Bits	Name	Description	
7-0	COEFC [7:0]	Video YUV/YPbPr to RGB Color Transfer Coefficient. 0~1023	

Default: 1010 1100B

0x050		Color Transfer Coefficient C -hi	R/W
Bits	Name	Description	
1-0	COEFC [9:8]	MSB of COEFC	

Default: XXXX XX00B

0x051		Color Transfer Coefficient D -lo	R/W
Bits	Name	Description	
7-0	COEFD [7:0]	Video YUV/YPbPr to RGB Color Transfer Coefficient. 0~1023	

Default: 0111 0111B

0x052		Color Transfer Coefficient D -hi	R/W
Bits	Name	Description	
1-0	COEFD [9:8]	MSB of COEFD	

Default: XXXX XX11B

9.7. Video Port Capture Control

Capture Window Control

0x053		Vertical Capture Begin for Odd Field -lo	R/W
Bits	Name	Description	
7-0	VI_CAP_VBEGO [7:0]	ODD Field Vertical Capture Begin. VI_CAP_VBEGO indicates how many lines to wait after referenced edge of VSYNC before starting image capture. VI_CAP_VBEGO =3, means waiting 3 lines to begin capture. **This register is double-buffered.**	

Default: 0000 0000B

0x054		Vertical Capture Begin for Odd Field -hi	R/W
Bits	Name	Description	
2-0	VI_CAP_VBEGO [10:8]	MSB of VI_CAP_BEG. **This register is double-buffered.**	

Default: XXXX X000B

0x055		Vertical Capture Begin for Even Field -lo	R/W
Bits	Name	Description	
7-0	VI_CAP_VBEGE [7:0]	Even Field Vertical Capture Begin. VI_CAP_VBEGE indicates how many lines to wait after referenced edge of VSYNC before starting image capture. VI_CAP_VBEGE =3, means waiting 3 lines to begin capture. **This register is double-buffered.**	

Default: 0000 0000B

0x056		Vertical Capture Begin for Even Field -hi	R/W
Bits	Name	Description	
2-0	VI_CAP_VBEGE [10:8]	MSB of VI_CAP_VBEGE. **This register is double-buffered.**	

Default: XXXX X000B

0x057		Vertical Capture Length -lo	R/W
Bits	Name	Description	
7-0	VI_CAP_VLEN [7:0]	Vertical Capture Length. VI_CAP_VLEN indicates how many lines to capture. VI_CAP_VLEN =3, means capturing 3 lines. **This register is double-buffered.**	

Default: 0000 0000B

0x058		Vertical Capture Length -hi	R/W
Bits	Name	Description	
2-0	VI_CAP_VLEN [10:8]	MSB of VI_CAP_VLEN. **This register is double-buffered.**	

Default: XXXX X000B

0x059		Horizontal Capture Begin -lo	R/W
Bits	Name	Description	
7-0	VI_CAP_HBEG [7:0]	Horizontal Capture Begin. VI_CAP_HBEG indicates how many pixels to wait after referenced edge of HSYNC before starting image capture. VI_CAP_HBEG =3, means waiting 3 pixels to begin capture. **This register is double-buffered.**	

Default: 0000 0000B

0x05A		Horizontal Capture Begin -hi	R/W
Bits	Name	Description	
3-0	VI_CAP_HBEG [11:8]	MSB of VI_CAP_HBEG. **This register is double-buffered.**	

Default: XXXX 0000B

0x05B		Horizontal Capture Width -lo	R/W
Bits	Name	Description	
7-0	VI_CAP_HWID [7:0]	Horizontal Capture Width. VI_CAP_HWID indicates how many pixels to capture. VI_CAP_HWID = 3, means capturing 3 pixels. **This register is double-buffered.**	

Default: 0000 0000B

0x05C		Horizontal Capture Width -hi	R/W
Bits	Name	Description	
3-0	VI_CAP_HWID [11:8]	MSB of VI_CAP_HWID **This register is double-buffered.**	

Default: XXXX 0000B

0x05D~0x05F		Reserved	R/W
Bits	Name	Description	
7-0			

Default: XXXX XXXXB

9.8. Back End Image Processing

♦ Back-end offset control
♦ Back-end gain control
♦ Back-end sharpness and smooth control

0x060		Back-end Horizontal Sharpness	R/W
Bits	Name	Description	
7		Reserved	
6	BK_H_ASRP	Graphic horizontal adaptive sharpness adjusting. 0 = Disable 1 = Enable	
5		HPLL test control	
4	BK_H_SRPSMO	Graphic horizontal back-end smooth and sharpness select. 0 = sharpness 1 = smooth	
3-0	BK_H_SRP [3:0]	Graphic horizontal back-end sharpness/smooth adjusting. 16 steps	

Default: X000 0000B

0x061		Color Channel Select	R/W
Bits	Name	Description	
3	GAIN_DITH_EN	Gain dithering enable	
2	GAIN_DITH_MODE	Gain dithering mode 0 = Static dithering 1 = Random dithering	
1-0	BK_CH_SEL [1:0]	Select color channel for offset and gain adjusting. 00 = R/G/B 01 = R 10 = G 11 = B	

Default: XXXX 0000B

0x062		Back-end Offset	R/W
Bits	Name	Description	
7-0	BK_OFFSET [7:0]	Back-end offset adjusting. -128~127 in 2's complement Display color = (Original value * GAIN) +OFFSET	

Default: 0000 0000B

0x063		Back-end Gain	R/W
Bits	Name	Description	
7-0	BK_GAIN [7:0]	Back-end gains adjusting. 0/128~255/128	

Default: 1000 0000B

0x064		Interpolation Control	R/W
Bits	Name	Description	

7-5	TEXT_EN [2:0]	Select the Text Mode type 000 = Normal Mode 001 = Level 1 Text Mode 010 = Level 2 Text Mode 011 = Level 3 Text Mode 1xx = Reserved
4-3	V_INTE_TYPE [1:0]	Select the Vertical interpolation type 00 = DSP (2-pixel) 01 = Bi-linear (2-pixel) 10 = Duplicate (2-pixel) 11 = Reserved
2-0	H_INTE_TYPE [2:0]	Select the Horizontal interpolation type 000 = Advanced DSP (4-pixel) 001 = Bi-linear (2-pixel) 010 = Duplicate (2-pixel) 011 = DSP (2-pixel) 100 = DSP (4-pixel) 101, 110, 111 = Reserved

Default: 0000 0000B

0x065	Gamma Control		R/W
Bits	Name	Description	
7	GAMMA_EN	Gamma Table Enable, When GAMMA_EN = 1, the Gamma Table can't read or write by host interface. When GAMMA_EN = 0 the display is bypass the Gamma table. 0 = Disable 1 = Enable	
6	TBL_8_10B_SEL	Used 8 bit gamma table or 10 bit gamma table for read/write 0 = 10 Bit Access 1 = 8 Bit Access	
5	BFW2_GAMMA_EN	Bright frame window 2 Gamma Table Enable 0 = Disable 1 = Enable	
4	BFW1_GAMMA_EN	Bright frame window 1 Gamma Table Enable 0 = Disable 1 = Enable	
3-0			

Default: 00XX XXXXB

0x066	Back-end Vertical Sharpness		R/W
Bits	Name	Description	
7-6			
5	V_INTE_SHIFT_EN	Vertical Interpolation shift enable 0 = Disable 1 = Enable	
4		Reserved	
2-0	BK_V_SRP [2:0]	Graphic vertical back-end sharpness adjusting. 8 steps	

Default: XXXX X000B

0x067	Reserved	R/W

Bits	Name	Description
7-0		

Default: XXXX XXXXB

9.9. Noise Reduction Filter Control

0x068	Noise Reduction Filter Control		R/W
Bits	Name	Description	
7		Reserved	
6	NR2_EN	Second Noise Reduction enable 0 = Disable 1 = Enable	
5	NR_ROUND	Noise Reduction round calculation enable 0 = Disable 1 = Enable	
4	NR_EDGE_DET	Noise Reduction edge detection enable 0 = Disable 1 = Enable	
3		Reserved	
2-0	NR_TYPE	Select the Noise Reduction Filter type 000 = Normal Mode (NR disable) 001 = Mode 1 010 = Mode 2 011 = Mode 3 1xx = Reserved	

Default: XX00 0000B

0x069	Noise Reduction threshold		R/W
Bits	Name	Description	
7-4	NR_EDGE_THR [3:0]	Edge Threshold of the noise reduction filter adjusting.	
3-0	NR_THR [3:0]	Threshold of the noise reduction filter adjusting.	

Default: 0000 0000B

0x06A	Jitter Correction Control		R/W
Bits	Name	Description	
7-6	JC_MAX_TYPE	Jitter Correction max type selection 00 = 1 frame 01 = 2 frame 10 = 4 frame 11 = Adaptive mode	
5		Reserved	
4	JC_EN	Jitter Correction Enable 0 = Disable 1 = Enable	
3-0	JC_LEVEL [3:0]	Jitter Correction Level	

Default: 0000 0001B

0x06B		Seconded Noise Reduction threshold	R/W
Bits	Name	Description	
7-6		Reserved	
5	NR3_EN	Third Noise Reduction enable	
4			
3-0	NR2_THR [3:0]	Threshold of the seconded noise reduction filter adjusting.	

Default: 0000 0000B

0x06C		Vertical Interpolation shift offset	R/W
Bits	Name	Description	
7-0	V_INTE_SHIFT_OFFSET		

Default: 0000 0000B

0x06D		Reserved	R/W
Bits	Name	Description	
7-0			

Default: 0000 0000B

0x06E		Reserved	R/W
Bits	Name	Description	
7-0			

Default: 0000 0000B

0x06F		Reserved	R/W
Bits	Name	Description	
7-0			

Default: 0000 0000B

9.10. General Purpose Input Output (GPIO)

0x070		GPIO Port Control	R/W
Bits	Name	Description	
5	PWMB_EN	PWMB output enable (open-drain) 0 = Disable 1 = PWMB Enable	
4	PWMA_EN	PWMA output enable (open-drain) 0 = Disable 1 = PWMA Enable	
3		Reserved	
2		Reserved	

Default: XX00 00XXB

0x071		GPIO Output / Input Data	R/W
Bits	Name	Description	
5			
4			
3			
2			
1			

0 | | |

Default: XX00 0000B

0x072		Bypass Sync Control	R/W
Bits	Name	Description	
4	BP_HSYNC_EN	This bit is used to Bypass the Hsync from pin to INT_HSO 0 = Disable 1 = Enable	
3		Reserved	
2	REFCKO_EN	Reference clock output enable 0 = Disable 1 = Enable	
1	BP_HSYNC_SEL	When BP_SYNC_EN = "1", this bit is used to select the output source. 0 = From the internal normal Hsync (RAW_HS) 1 = From the internal SOG Sync (SOG_HS)	
0	BP_VSYNC_EN	This bit is used to Bypass the sync from pin to INT_VSO 0 = Disable 1 = Enable	

Default: XXXX 0100B

0x073		GPIO Data Direction	R/W
Bits	Name	Description	
5			
4			
3			
2			
1			
0			

Default: XX00 0000B

9.11. PWM Output

♦ Frequency programmable
♦ Duty cycle programmable
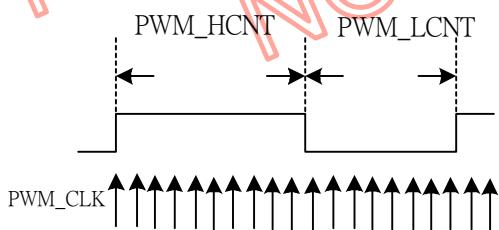
When clock source select from reference clock

$$F_{PWM\_CLK} = F_{REFCLK} / (PWM\_DIV\,1 \times PWM\_DIV\,2\,)$$

When clock source select from Display Hsync

$$F_{PWM\_CLK} = F_{DISP\_HS} / (PWM\_DIV\,1 \times PWM\_DIV\,2\,)$$

$$F_{PWM} = \frac{F_{PWM\_CLK}}{(PWM\_HCNT + PWM\_LCNT)}$$

$$Duty = \frac{PWM\_HCNT}{(PWM\_HCNT + PWM\_LCNT)}$$

$$PWM\_HCNT = \frac{Duty \times F_{PWM\_CLK}}{F_{PWM}}$$

$$PWM\_LCNT = \frac{(1 - Duty) \times F_{PWM\_CLK}}{F_{PWM}}$$

PWM_HCNT	PWM_LCNT	PWM Output
0	0	Tri-state
0	1~255	DC '0'
1~255	0	DC '1'
1~255	1~255	PWM pulse

0x074		PWMA Low Period Counter	R/W
Bits	Name	Description	
7-0	PWMA_LCNT [7:0]	PWMA pulse low period counter value. Double-buffered.	

Default: 0000 0000B

0x075		PWMA High Period Counter	R/W
Bits	Name	Description	
7-0	PWMA_HCNT [7:0]	PWMA pulse high period counter value. Double-buffered.	

Default: 0000 0000B

0x076		PWMB Low Period Counter	R/W
Bits	Name	Description	
7-0	PWMB_LCNT [7:0]	PWMB pulse low period counter value. Double-buffered.	

Default: 0000 0000B

0x077		PWMB High Period Counter	R/W
Bits	Name	Description	
7-0	PWMB_HCNT [7:0]	PWMB pulse high period counter value. Double-buffered.	

Default: 0000 0000B

0x078~0x07D		Reserved	R/W
Bits	Name	Description	
7-0			

Default: XXXX XXXXB

0x07E		PWM Control 1	R/W
Bits	Name	Description	

7	PWMB_VS_LOCK	PWMB counter lock to display vertical sync 0 = Roll PWM counter over continuously 1 = Load PWM on Display VS (DISP_VS) leading edge
6-5	PWMB_DIV1 [1:0]	First divider-- PWMB clock divide of the selected clock by 00 = 1; 01 = 2; 10 = 4; 11 = 8; when PWMB_DVI2 = "00"b 00 = 16; 01 = 32;10 = 64; 11 = 128; when PWMB_DVI2 = "01"b 00 = 256; 01 = 512;10 = 1024; 11 = 2048; when PWMB_DVI2 = "10"b 00 = 4096; 01 = 8192; 10 = 16384; 11 = 16384; when PMB_DVI2 = "11"b
4	PWMB_CLK	PWMB clock source select 0 = Reference Clock 1 = Display HS (DISP_HS)
3	PWMA_VS_LOCK	PWMA counter lock to display vertical sync 0 = Load PWM counter when high period counter 1 = Load PWM on Display VS (DISP_VS) leading edge
2-1	PWMA_DIV1 [1:0]	First divider-- PWMA clock divide of the selected clock by 00 = 1; 01 = 2; 10 = 4; 11 = 8; when PWMA_DVI2 = "00"b 00 = 16; 01 = 32;10 = 64; 11 = 128; when PWMA_DVI2 = "01"b 00 = 256; 01 = 512;10 = 1024; 11 = 2048; when PWMA_DVI2 = "10"b 00 = 4096; 01 = 8192; 10 = 16384;11=16384; when PWMA_DVI2 = "11"b
0	PWMA_CLK	PWMA clock source select 0 = Reference Clock 1 = Display HS (DISP_HS)

Default: 0000 0000B

0x07F	PWM Control 2	R/W
Bits	Name	Description
7	PWMB_VSRESET	PWMB reset counter on DSIP_VS leading edge 0 = Roll PWMB counter over continuously 1 = Reset PWMB on DISP_VS leading edge
6	PWMA_VSRESET	PWMA reset counter on DSIP_VS leading edge 0 = Roll PWMA counter over continuously 1 = Reset PWMA on DISP_VS leading edge
5-4		Reserved
3-2	PWMB_ DIV2	Second divider--PWMB clock divide of the selected clock by 00 = 1; 01 = 16 10 = 512; 11 = 4096
1-0	PWMA_DIV2 [1:0]	Second divider--PWMA clock divide of the selected clock by 00 = 1; 01 = 16 10 = 512; 11 = 4096

Default: 0000 0000B

9.12. On Screen Display Registers

OSD Control

0x080	OSD and Window Enable Control	R/W
Bits	Name	Description
7	ROT_EN	Rotation control.

		0: Normal
		1: Rotated
6	FLIP_EN	Flip control
		0: No flip
		1: Flip ON
5	MIR_EN	Mirror control
		0: No mirror
		1: Mirror ON
4	WIN4_EN	Enable Window 4
		0: Disable
		1: Enable
3	WIN3_EN	Enable Window 3
		0: Disable
		1: Enable
2	WIN2_EN	Enable Window 2
		0: Disable
		1: Enable
1	WIN1_EN	Enable Window 1
		0: Disable
		1: Enable
0	OSD_EN	Enable OSD
		0: Disable
		1: Enable

Default: 0000 0000B

0x081	OSD Frame Horizontal Start - Low byte		R/W
Bits	Name	Description	
7-0	OSD_HS [7:0]	OSD frame horizontal start low byte [7:0]. Specifies the horizontal starting position of the OSD in pixel units. This register is **double-buffered**.	

Default: 0000 0000B

0x082	OSD Frame Horizontal Start - High Byte		R/W
Bits	Name	Description	
7-4		Reserved	
3-0	OSD_HS [11:8]	OSD frame horizontal start high byte [11:8]. Specifies the horizontal starting position of the OSD in pixel units. This register is **double-buffered**.	

Default: XXXX 0000B

0x083	OSD Frame Horizontal Width		R/W
Bits	Name	Description	
7		Reserved	
5-0	OSD_HW [5:0]	Specifies the width of the OSD in font units. Range: 0~ 63 (OSD display width = 1~64)	

Default: XX00 0000B

0x084	OSD Frame Vertical Start Low byte		R/W
Bits	Name	Description	
7-0	OSD_VS [7:0]	OSD frame vertical start low byte [7:0]. Specifies the vertical starting position of the OSD in line units. This register is **double-buffered**.	

Default: 0000 0000B

0x085		OSD Frame Vertical Start High byte	R/W
Bits	Name	Description	
7-3		Reserved	
2-0	OSD_VS [10:8]	OSD frame vertical start high byte [10:8]. Specifies the vertical starting position of the OSD in line units. This register is **double-buffered**.	

Default: XXXX X000B

0x086		OSD Frame Vertical Height	R/W
Bits	Name	Description	
7-5		Reserved	
4-0	OSD_VH [4:0]	Specifies the height of the OSD in font units. Range: 0~31 (OSD display height = 1~32)	

Default: XXX0 0000B

0x087		OSD Shift Row Offset	R/W
Bits	Name	Description	
4-0	OSD_SHIFT_ROW	Specifies the row of the OSD shift offset. Range: 0~31	

Default: X000 0000B

0x088		OSD One Bit Font Address - Low Byte	R/W
Bits	Name	Description	
7-0	FONT1B_ADDR [7:0]	OSD one bit per pixel programmable font start address high byte [7:0]. Specifies the start address for the On-Chip programmable font. Default for this 12 bit register = 1000 (dec)	

Default: 1110 1000B

0x089		OSD One bit Font Address - High Byte	R/W
Bits	Name	Description	
3-0	FONT1B_ADDR [11:8]	OSD one bit per pixel programmable font start address high byte [11:8]. Specifies the start address for the On-Chip programmable font Default for this 12 bit register = 1000 (dec)	

Default: XXXX 0011B

0x08A		OSD Two Bit Font Address - Low Byte	R/W
Bits	Name	Description	
7-0	FONT2B_ADDR [7:0]	OSD two bit per pixel programmable font start address high byte [7:0]. Specifies the start address for the On-Chip programmable font. Default for this 12 bit register = 2656 (dec)	

Default: 0110 0000B

0x08B		OSD Two Bit Font Address - High Byte	R/W
Bits	Name	Description	
3-0	FONT2B_ADDR [11:8]	OSD two bit per pixel programmable font start address high byte [11:8]. Specifies the start address for the On-Chip programmable font Default for this 12 bit register = 2656 (dec)	

Default: XXXX 1010B

0x08C		OSD Four Bit Font Address - Low Byte	R/W
Bits	Name	Description	

7-0	FONT4B_ADDR [7:0]	OSD four bit per pixel programmable font start address high byte [7:0]. Specifies the start address for the On-Chip programmable font. Default for this 12 bit register = 3808 (dec)

Default: 1110 0000B

0x08D	OSD Four Bit Font Address - High Byte	R/W
Bits	Name	Description
3-0	FONT4B_ADDR [11:8]	OSD four bit per pixel programmable font start address high byte [11:8]. Specifies the start address for the On-Chip programmable font Default for this 12 bit register = 3808 (dec)

Default: XXXX 1110B

OSD Fade in/out Control

0x08E	OSD Fade-in / Fade-out Step	R/W
Bits	Name	Description
7-4	FAD_V_STEP [3:0]	OSD Vertical side Fade-in / Fade-out Step (4 pixel/step) 0~15 step
3-0	FAD_H_STEP [3:0]	OSD Horizontal side Fade-in / Fade-out Step (4 pixel/step) 0~15 step

Default: 0000 0000B

0x08F	OSD Fade-in / Fade-out Frequency	R/W
Bits	Name	Description
7	FAD_EN	Fade-in / Fade-out function enable. 0: Fade-in / Fade-out disable 1: Fade-in / Fade-out enable
6-4	FAD_VFREQ [2:0]	OSD Fade-in / Fade-out Vertical Frequency for every step
3-0	FAD_HFREQ [3:0]	OSD Fade-in / Fade-out Horizontal Frequency for every step

Default: 0000 0000B

OSD Zoom Control

0x090	OSD Zoom Control	R/W
Bits	Name	Description
7-4		Reserved
3	VROW_ZMEN	Vertical Row Zoom Enable; Vertical zoom for all characters in one row defined in Reg 0x09A ~ 0x09D. 0: Disable 1: Enable.
2	HROW_ZMEN	Horizontal Row Zoom Enable; Horizontal zoom for all characters in one row defined in Reg 0x096 ~ 0x099. 0: Disable 1: Enable.
1	VGLOB_ZMEN	Vertical Global Zoom Enable; Vertical zoom for all characters in OSD frame. 0: Disable 1: Enable.
0	HGLOB_ZMEN	Horizontal Global Zoom Enable; Horizontal zoom for all characters in OSD frame. 0: Disable

| | | 1: Enable. | |

Default: XXXX 0000B

0x091		OSD Font Horizontal Global Zoom Pattern - Low Byte	R/W
Bits	Name	Description	
7-0	HZM_PATN [7:0]	Least significant 8 bits (7:0) of the horizontal zoom pattern. This is a user definable zoom pattern. Pixels with '1' pattern are duplicated according to the zoom range.	

Default: 0000 0000B

0x092		OSD Font Horizontal/Vertical Global Zoom Pattern - High Byte	R/W
Bits	Name	Description	
7-6		Reserved	
5-4	VZM_PATN [17:16]	Most significant 2 bits (17:16) of the vertical zoom pattern. This is a user definable zoom pattern. Pixels with '1' pattern are duplicated according to the zoom range.	
3-0	HZM_PATN [11:8]	Most significant 4 bits (11:8) of the horizontal zoom pattern. This is a user definable zoom pattern. Pixels with '1' pattern are duplicated according to the zoom range.	

Default: XX00 0000B

0x093		OSD Font Vertical Global Zoom Pattern - Low Byte	R/W
Bits	Name	Description	
7-0	VZM_PATN [7:0]	Least significant 8 bits (7:0) of the vertical zoom pattern. This is a user definable zoom pattern. Pixels with '1' pattern are duplicated according to the zoom range.	

Default: 0000 0000B

0x094		OSD Font Vertical Global Zoom Pattern - Mid Byte	R/W
Bits	Name	Description	
7-0	VZM_PATN [15:8]	Bits (15:8) of the vertical zoom pattern. This is a user definable zoom pattern. Pixels with '1' pattern are duplicated according to the zoom range.	

Default: 0000 0000B

0x095		OSD Font Global Zoom Range	R/W
Bits	Name	Description	
7-6	VGLOB_ZMRNG1 [1:0]	Vertical Global Zoom Pattern (Reg 0x092 ~ 0x094) '1' Zoom Range 00: No Zoom 01: Vertical Zoom Pattern '1' bits are duplicated once 10: Vertical Zoom Pattern '1' bits are duplicated twice 11: Vertical Zoom Pattern '1' bits are duplicated three times	
5-4	HGLOB_ZMRNG1 [1:0]	Horizontal Global Zoom Pattern (Reg 0x091 ~ 0x092) '1' Zoom Range 00: No Zoom 01: Horizontal Zoom Pattern '1' bits are duplicated once 10: Horizontal Zoom Pattern '1' bits are duplicated twice 11: Horizontal Zoom Pattern '1' bits are duplicated three times	
3-2	VGLOB_ZMRNG0 [1:0]	Vertical Global Zoom Pattern (Reg 0x092 ~ 0x094) '0' Zoom Range 00: No Zoom 01: Vertical Zoom Pattern '0' bits are duplicated once 10: Vertical Zoom Pattern '0' bits are duplicated twice.	

		11: Vertical Zoom Pattern '0' bits are duplicated three times.
1-0	HGLOB_ZMRNG0 [1:0]	Horizontal Global Zoom Pattern (Reg 0x091 ~ 0x092) '0' Zoom Range 00: No Zoom 01: Horizontal Zoom Pattern '0' bits are duplicated once 10: Horizontal Zoom Pattern '0' bits are duplicated twice 11: Horizontal Zoom Pattern '0' bits are duplicated three times

Default: 0000 0000B

0x096		Horizontal Row Zoom Control Row 7 - 0	R/W
Bits	Name	Description	
7-0	HROW_ZMPN [7:0]	Horizontal Row Zoom Pattern 7-0 Zooms each row horizontally defined as zoom range according to each bit. Each bit controls a row correspondingly. Reg 0x090 [2] must be set to '1'.	

Default: 0000 0000B

0x097		Horizontal Row Zoom Control Row 15 - 8	R/W
Bits	Name	Description	
7-0	HROW_ZMPN [15:8]	Horizontal Row Zoom Pattern 15-8 Zooms each row horizontally defined as zoom range according to each bit. Each bit controls a row correspondingly. Reg 0x090 [2] must be set to '1'.	

Default: 0000 0000B

0x098		Horizontal Row Zoom Control Row 23 - 16	R/W
Bits	Name	Description	
7-0	HROW_ZMPN [23:16]	Horizontal Row Zoom Pattern 23-16 Zooms each row horizontally defined as zoom range according to each bit. Each bit controls a row correspondingly. Reg 0x090 [2] must be set to '1'.	

Default: 0000 0000B

0x099		Horizontal Row Zoom Control Row 31 - 24	R/W
Bits	Name	Description	
7-0	HROW_ZMPN [31:24]	Horizontal Row Zoom Pattern 31-24 Zooms each row horizontally defined as zoom range according to each bit. Each bit controls a row correspondingly. Reg 0x090 [2] must be set to '1'.	

Default: 0000 0000B

0x09A		Vertical Row Zoom Control Row 7 - 0	R/W
Bits	Name	Description	
7-0	VROW_ZMPN [7:0]	Vertical Row Zoom Pattern 7-0 Zooms each row vertically defined as zoom range according to each bit. Each bit controls a row correspondingly. Reg 0x090 [3] must be set to '1'.	

Default: 0000 0000B

0x09B		Vertical Row Zoom Control Row 15 - 8	R/W
Bits	Name	Description	
7-0	VROW_ZMPN [15:8]	Vertical Row Zoom Pattern 15-8 Zooms each row vertically defined as zoom range according to each bit. Each bit controls a row correspondingly. Reg 0x090 [3] must be set to '1'.	

Default: 0000 0000B

0x09C		Vertical Row Zoom Control Row 23 - 16	R/W

Bits	Name	Description
7-0	VROW_ZMPN [23:16]	Vertical Row Zoom Pattern 23-16 Zooms each row vertically defined as zoom range according to each bit. Each bit controls a row correspondingly. Reg 0x090 [3] must be set to '1'.

Default: 0000 0000B

0x09D	Vertical Row Zoom Control Row 31 - 24	R/W

Bits	Name	Description
7-0	VROW_ZMPN [31:24]	Vertical Row Zoom Pattern 31-24 Zooms each row vertically defined as zoom range according to each bit. Each bit controls a row correspondingly. Reg 0x090 [3] must be set to '1'.

Default: 0000 0000B

0x09E	OSD Font Row Zoom Range	R/W

Bits	Name	Description
7-4		Reserved
3-2	VROW_ZMRNG [1:0]	Vertical Row Zoom Range; The rows assigned by Vertical Row Zoom Control registers will be zoomed up. 00: Vertical Zoom 1x for all fonts in the row 01: Vertical Zoom 2x for all fonts in the row 10: Vertical Zoom 3x for all fonts in the row 11: Vertical Zoom 4x for all fonts in the row
1-0	HROW_ZMRNG [1:0]	Horizontal Row Zoom Range; The rows assigned by Horizontal Row Zoom Control registers will be zoomed up. 00: Horizontal Zoom 1x for all fonts in the row 01: Horizontal Zoom 2x for all fonts in the row 10: Horizontal Zoom 3x for all fonts in the row 11: Horizontal Zoom 4x for all fonts in the row

Default: XXXX 0000B

0x09F	Reserved	R/W

Bits	Name	Description

Default: 0000 0000B

OSD Translucent and Blinking Control

0x0A0	OSD Blink Control	R/W

Bits	Name	Description
7		Reserved
6	OSD_BLINK	Blink 1=OSD frame blink enable, don't care the attribute bit 0. 0=Blink control from font attribute bit 0.
5	BS_BLINK	Mask Border/Shadow at Blink 1=Character border/shadow will not blink with the foreground of the character. 0= Character border/shadow will blink with the foreground of the character.
4-2	BLINK_FREQ [2:0]	Blink Frequency 000: Character foreground's blinking period is 4 frames. 001: Character foreground's blinking period is 8 frames. 010: Character foreground's blinking period is 16 frames. 011: Character foreground's blinking period is 32 frames.

		100: Character foreground's blinking period is 64 frames.
1-0	BLINK_RATE [1:0]	Blink Rate 00: Character foreground is turned 25% on / 75% off. 01: Character foreground is turned 50% on / 50% off. 10: Character foreground is turned 75% on / 25% off. 11: reserved.

Default: X000 0001B

0x0A1	OSD Character Translucent Level		R/W
Bits	Name	Description	
5-3	TP_LEVEL_TWO [2:0]	When the attribute BG_Index is set to "0001", these 3-bits set the translucent level of the character background color. Translucent level refers to the percentage of color composition that is OSD. "111" = 0% "110" = 12.25% "101" = 25% "100" = 37.5% "011" = 50% "010" = 62.5% "001" = 75% "000" = 87.5%	
2-0	TP_LEVEL_ONE [2:0]	When the attribute BG_Index is set to "0000" ~ "1111" except "0001", these 3-bits set the translucent level of the character background color. Translucent level refers to the percentage of color composition that is OSD. "111" = 0% "110" = 12.25% "101" = 25% "100" = 37.5% "011" = 50% "010" = 62.5% "001" = 75% "000" = 87.5%	

Default: XX00 0000B

OSD Spacing Control

0x0A2	OSD Space		R/W
Bits	Name	Description	
7	V_FS_SEL	Vertical Font size selection 0: 18 font size for Vertical 1: 16 font size for Vertical	
6	H_FS_SEL	Horizontal Font size selection 0: 12 font size selected for Horizontal 1: 10 font size selected for Horizontal	
5-3	VSPACE [2:0]	OSD vertical space. These 3 bits define the vertical scan pixel of background color added to above and below of each character. Range: 0~7	
2-0	HSPACE [2:0]	OSD horizontal space. These 3 bits define the horizontal scan pixel of background color added to left and right of each character. Range: 0~7	

Default: 0000 0000B

0x0A3~0x0A4	Reserved		R/W
Bits	Name	Description	

Default: 0000 0000B

OSD Window Control

0x0A5		OSD Window Select	R/W
Bits	Name	Description	
7	WIN8_EN	Enable Window 8 0: Disable 1: Enable	
6	WIN7_EN	Enable Window 7 0: Disable 1: Enable	
5	WIN6_EN	Enable Window 6 0: Disable 1: Enable	
4	WIN5_EN	Enable Window 5 0: Disable 1: Enable	
3		Reserved	
2-0	WIN_SEL [2:0]	This register is used to select which window is to be accessed or modified. It is programmed prior to accessing the registers Reg 0x0A6h ~ 0x0AFh "000" = Window1 "001" = Window2 "010" = Window3 "011" = Window4 "100" = Window5 "101" = Window6 "110" = Window7 "111" = Window8	

Default: 0000 X000B

0x0A6		OSD Window Horizontal Start	R/W
Bits	Name	Description	
7-6		Reserved	
5-0	WIN_HS [5:0]	Horizontal starting position relative to the OSD for the selected window. The unit is in font. Range: 0~63	

Default: XX00 0000B

0x0A7		OSD Window Horizontal End	R/W
Bits	Name	Description	
7-6		Reserved	
5-0	WIN_HE [5:0]	Horizontal ending position relative to the OSD for the selected window. The unit is in font. The OSD Window Horizontal Width = (WIN_HE+1) - WIN_HS Range: 0~63	

Default: XX00 0000B

0x0A8		OSD Window Vertical Start	R/W
Bits	Name	Description	
4-0	WIN_VS [4:0]	Vertical starting position relative to the OSD for the selected window. The unit is in font. Range: 0~31	

Default: XXX0 0000B

0x0A9		OSD Window Vertical End	R/W
Bits	Name	Description	

7-5		Reserved
4-0	WIN_VE [4:0]	Vertical ending position relative to the OSD for the selected window. The unit is in font. The OSD Window 1 Vertical Height = (WIN1_VE+1) - WIN1_VS Range: 0~31

Default: XXX0 0000B

0x0AA		OSD Window Attribute	R/W
Bits	Name	Description	
7	WIN_BLEN	Window bevel enable Bevel size is specified in WIN_BL_HWID [2:0] and WIN_BL_VHEI[2:0]	
6-5	WIN_BL_TYPE	Window bevel type 00: Type 1 01: Type 2 10: Type 3 11: Type 4	
4	WIN_MIX	Window translucent enable for the selected window 0 - Normal 1 - Translucent ((1- TP_LEVEL_ONE) * Display + (TP_LEVEL_ONE) * OSD_BG)	
3-2	WIN_SDSZ [1:0]	Shadow Size for the selected window when window shadow enable 00: 2 pixels in width and 2 lines in height. 01: 4 pixels in width and 4 lines in height. 10: 6 pixels in width and 6 lines in height. 11: 8 pixels in width and 8 lines in height.	
1	WIN_SDEN	Window Shadow Enable for the selected window Shadow size is specified in bits 3:2. 1= Shows a shadow for Window. 0= No shadow	
0		Reserved	

Default: 0000 000XB

0x0AB		OSD Window Color	R/W
Bits	Name	Description	
7-0	WIN_CL [7:0]	Color index for the selected OSD Window. This color will cover the character background color when Window is enabled.	

Default: 0000 0000B

0x0AC		OSD Window Shadow Color	R/W
Bits	Name	Description	
7-0	WIN_SDCL [7:0]	Color index for all eight window's shadow	

Default: 0000 0000B

0x0AD		OSD Window Bevel Width	R/W
Bits	Name	Description	
7-4		Reserved	
2-0	WIN_BL_VWID [2:0]	Specifies the width of the window bevel units. Range: 1~8	

Default: 0000 0000B

0x0AE	OSD Window Bevel Right Color	R/W

Bits	Name	Description
7-0	WIN_BL_RCL [7:0]	Color index for all eight window's right side bevel

Default: 0000 0000B

0x0AF	OSD Window Bevel Left Color	R/W

Bits	Name	Description
7-0	WIN_BL_LCL [7:0]	Color index for all eight window's left side bevel

Default: 0000 0000B

OSD Border And Shadow Control

0x0B0	OSD Shadow Control Row 7 - 0	R/W

Bits	Name	Description
7-0	OSD_SCR [7:0]	Character Row Shadow Enable for 7-0. Each bit controls each row correspondingly. Used only in one bit per pixel font. 1= Enable shadow for a row.

Default: 0000 0000B

0x0B1	OSD Shadow Control Row 15 - 8	R/W

Bits	Name	Description
7-0	OSD_SCR [15:8]	Character Row Shadow Enable for 15-8. Each bit controls each row correspondingly. Used only in one bit per pixel font. 1= Enable shadow for a row.

Default: 0000 0000B

0x0B2	OSD Shadow Control Row 23 - 16	R/W

Bits	Name	Description
7-0	OSD_SCR [23:16]	Character Row Shadow Enable for 23-16. Each bit controls each row correspondingly. Used only in one bit per pixel font. 1= Enable shadow for a row.

Default: 0000 0000B

0x0B3	OSD Shadow Control Row 31 - 24	R/W

Bits	Name	Description
7-0	OSD_SCR [31:24]	Character Row Shadow Enable for 31-24. Each bit controls each row correspondingly. Used only in one bit per pixel font. 1= Enable shadow for a row.

Default: 0000 0000B

0x0B4	OSD Border Control Row 7 - 0	R/W

Bits	Name	Description
7-0	OSD_BCR [7:0]	Character Row Border Enable for 7-0. Each bit controls each row correspondingly. Used only in one bit per pixel font. 1= Enable border for a row.

Default: 0000 0000B

0x0B5	OSD Border Control Row 15-8	R/W

Bits	Name	Description

7-0	OSD_BCR [15:8]	Character Row Border Enable for 15-8. Each bit controls each row correspondingly. Used only in one bit per pixel font. 1= Enable border for a row.

Default: 0000 0000B

0x0B6	OSD Border Control Row 23-16		R/W
Bits	Name	Description	
7-0	OSD_BCR [23:16]	Character Row Border Enable for 23-16. Each bit controls each row correspondingly. Used only in one bit per pixel font. 1= Enable border for a row.	

Default: 0000 0000B

0x0B7	OSD Border Control Row 31-24		R/W
Bits	Name	Description	
7-0	OSD_BCR [31:24]	Character Row Border Enable for 31-24. Each bit controls each row correspondingly. Used only in one bit per pixel font. 1= Enable border for a row.	

Default: 0000 0000B

0x0B8	OSD Border & Shadow Color Row 1 - 0		R/W
Bits	Name	Description	
7-4	OSD_BSCR1 [3:0]	Character Border/Shadow Color Index For Row 1. Used only in one bit per pixel font.	
3-0	OSD_BSCR0 [3:0]	Character Border/Shadow Color Index For Row 0. Used only in one bit per pixel font.	

Default: 0000 0000B

0x0B9	OSD Border & Shadow Color Row 3 - 2		R/W
Bits	Name	Description	
7-4	OSD_BSCR3 [3:0]	Character Border/Shadow Color Index For Row 3. Used only in one bit per pixel font.	
3-0	OSD_BSCR2 [3:0]	Character Border/Shadow Color Index For Row 2. Used only in one bit per pixel font.	

Default: 0000 0000B

0x0BA	OSD Border & Shadow Color Row 5 - 4		R/W
Bits	Name	Description	
7-4	OSD_BSCR5 [3:0]	Character Border/Shadow Color Index For Row 5. Used only in one bit per pixel font.	
3-0	OSD_BSCR4 [3:0]	Character Border/Shadow Color Index For Row 4. Used only in one bit per pixel font.	

Default: 0000 0000B

0x0BB	OSD Border & Shadow Color Row 7- 6		R/W
Bits	Name	Description	
7-4	OSD_BSCR7 [3:0]	Character Border/Shadow Color Index For Row 7. Used only in one bit per pixel font.	
3-0	OSD_BSCR6 [3:0]	Character Border/Shadow Color Index For Row 6. Used only in one bit per pixel font.	

Default: 0000 0000B

0x0BC		OSD Border & Shadow Color Row 9 - 8	R/W
Bits	Name	Description	
7-4	OSD_BSCR9 [3:0]	Character Border/Shadow Color Index For Row 9. Used only in one bit per pixel font.	
3-0	OSD_BSCR8 [3:0]	Character Border/Shadow Color Index For Row 8. Used only in one bit per pixel font.	

Default: 0000 0000B

0x0BD		OSD Border & Shadow Color Row 11 - 10	R/W
Bits	Name	Description	
7-4	OSD_BSCR11 [3:0]	Character Border/Shadow Color Index For Row 11. Used only in one bit per pixel font.	
3-0	OSD_BSCR10 [3:0]	Character Border/Shadow Color Index For Row 10. Used only in one bit per pixel font.	

Default: 0000 0000B

0x0BE		OSD Border & Shadow Color Row 13 - 12	R/W
Bits	Name	Description	
7-4	OSD_BSCR13 [3:0]	Character Border/Shadow Color Index For Row 13. Used only in one bit per pixel font.	
3-0	OSD_BSCR12 [3:0]	Character Border/Shadow Color Index For Row 12. Used only in one bit per pixel font.	

Default: 0000 0000B

0x0BF		OSD Border & Shadow Color Row 15 - 14	R/W
Bits	Name	Description	
7-4	OSD_BSCR15 [3:0]	Character Border/Shadow Color Index For Row 15. Used only in one bit per pixel font.	
3-0	OSD_BSCR14 [3:0]	Character Border/Shadow Color Index For Row 14. Used only in one bit per pixel font.	

Default: 0000 0000B

0x0C0		OSD Border & Shadow Color Row 17 - 16	R/W
Bits	Name	Description	
7-4	OSD_BSCR17 [3:0]	Character Border/Shadow Color Index For Row 17. Used only in one bit per pixel font.	
3-0	OSD_BSCR16 [3:0]	Character Border/Shadow Color Index For Row 16. Used only in one bit per pixel font.	

Default: 0000 0000B

0x0C1		OSD Border & Shadow Color Row 19 - 18	R/W
Bits	Name	Description	
7-4	OSD_BSCR19 [3:0]	Character Border/Shadow Color Index For Row 19. Used only in one bit per pixel font.	
3-0	OSD_BSCR18 [3:0]	Character Border/Shadow Color Index For Row 18. Used only in one bit per pixel font.	

Default: 0000 0000B

0x0C2H		OSD Border & Shadow Color Row 21 - 20	R/W
Bits	Name	Description	

| 7-4 | OSD_BSCR21 [3:0] | Character Border/Shadow Color Index For Row 21. Used only in one bit per pixel font. |
| 3-0 | OSD_BSCR20 [3:0] | Character Border/Shadow Color Index For Row 20. Used only in one bit per pixel font. |

Default: 0000 0000B

0x0C3	OSD Border & Shadow Color Row 23- 22	R/W
Bits	Name	Description
7-4	OSD_BSCR23 [3:0]	Character Border/Shadow Color Index For Row 23. Used only in one bit per pixel font.
3-0	OSD_BSCR22 [3:0]	Character Border/Shadow Color Index For Row 22. Used only in one bit per pixel font.

Default: 0000 0000B

0x0C4	OSD Border & Shadow Color Row 25 - 24	R/W
Bits	Name	Description
7-4	OSD_BSCR25 [3:0]	Character Border/Shadow Color Index For Row 25. Used only in one bit per pixel font.
3-0	OSD_BSCR24 [3:0]	Character Border/Shadow Color Index For Row 24. Used only in one bit per pixel font.

Default: 0000 0000B

0x0C5	OSD Border & Shadow Color Row 27 – 26	R/W
Bits	Name	Description
7-4	OSD_BSCR27 [3:0]	Character Border/Shadow Color Index For Row 27. Used only in one bit per pixel font.
3-0	OSD_BSCR26 [3:0]	Character Border/Shadow Color Index For Row 26. Used only in one bit per pixel font.

Default: 0000 0000B

0x0C6	OSD Border & Shadow Color Row 29 – 28	R/W
Bits	Name	Description
7-4	OSD_BSCR29 [3:0]	Character Border/Shadow Color Index For Row 29. Used only in one bit per pixel font.
3-0	OSD_BSCR28 [3:0]	Character Border/Shadow Color Index For Row 28. Used only in one bit per pixel font.

Default: 0000 0000B

0x0C7	OSD Border & Shadow Color Row 31 - 30	R/W
Bits	Name	Description
7-4	OSD_BSCR31 [3:0]	Character Border/Shadow Color Index For Row 31. Used only in one bit per pixel font.
3-0	OSD_BSCR30 [3:0]	Character Border/Shadow Color Index For Row 30. Used only in one bit per pixel font.

Default: 0000 0000B

OSD Splitting Control

0x0C8	OSD Horizontal Splitting Control	R/W
Bits	Name	Description
7	H_SPL_EN	Horizontal Splitting Enable 0: Disable

		1: Enable
6-0	SPL_HP [6:0]	Splitting horizontal begin position relative to the OSD frame for the selected window. The unit is in 1 horizontal font size. Range: 0~127

Default: 0000 0000B

0x0C9		OSD Horizontal Splitting width Control	R/W
Bits	Name	Description	
7-0	SPL_HW [7:0]	Splitting horizontal width relative to the OSD frame. The unit is in 8 pixels. Range: 0~255	

Default: 0000 0000B

0x0CA		OSD Vertical Splitting Control	R/W
Bits	Name	Description	
7	V_SPL_EN	Vertical Splitting Enable 0: Disable 1: Enable	
6		Reserved	
5-0	SPL_VP [5:0]	Splitting vertical begin position relative to the OSD frame. The unit is in 1 vertical font size. Range: 0~64	

Default: 0000 0000B

0x0CB		OSD Vertical Splitting Height Control	R/W
Bits	Name	Description	
7-0	SPL_VH [7:0]	Splitting vertical height relative to the OSD frame. The unit is in 8 lines. Range: 0~255	

Default: 0000 0000B

OSD Attribute Control and OSD Fast Clear Control

0x0CC		OSD Attribute LSB	R/W
Bits	Name	Description	
7-0	OSD_ATTR [7:0]	OSD Attribute LSB. The register OSD_ATTR [15:0] is use for fast clear and update code from host and attribute from Register. This value is appended with the character font code. When update OSD SRAM code from host and "attribute from Reg 0x0CC ~ 0x0CD is selected in Reg 0x0E0 [7:4]. If fast clear is enable, the hardware will fill the entire SRAM with the values in Reg 0x0CE (Code) and Reg 0x0CC ~ 0x0CD (Attribute).	

Default: 0000 0000B

0x0CD		OSD Attribute MSB	R/W
Bits	Name	Description	
7-0	OSD_ATTR [15:8]	OSD attribute MSB. The register OSD_ATTR [15:0] is use for fast clear and update code from host and attribute from Register. This value is appended with the character font code. When update OSD SRAM code from host and "attribute from Reg 0x0CC ~ 0x0CD is selected in Reg 0x0E0 [7:4]. If fast clear is enable, the hardware will fill the entire SRAM with the values in Reg 0x0CE (Code) and Reg 0x0CC ~ 0x0CD (Attribute).	

Default: 0000 0000B

0x0CE		OSD SRAM Code Value For Fast Clear	R/W
Bits	Name	Description	
7-0	CODE_FC [7:0]	SRAM code for fast clear.	

Default: 0000 0000B

0x0CF		Fast Clear and Fade Mode Control	R/W
Bits	Name	Description	
7-6	FADE_MODE	Fade-in/Fade-out mode select 00:Left-Top corner 01:Right-Top corner 10:Left-Bottom corner 11:Right-Bottom corner	
5	BG_MIX_EN	Background translucent enables.	
4	FG_MIX_EN	Foreground translucent enables.	
3	BS_MIX_EN	Border/Shadow translucent enable.	
2	WIN_MIX_EN	Windows translucent enable.	
1	FC_MASK	Fast Clear area mask 0: SRAM on OSD frame 1: SRAM on 0x0000 to One bit Font Address	
0	FC_EN (W)/ FC_RDY (R)	Fast Clear Enable, When enable this bit, the hardware will fill the entire SRAM with the values in Reg 0x0CE (Code) and Reg 0x0CC ~ 0x0CD (Attribute). 1: Enable the fast clear. If fast clear is finished, this bit FC_RDY will be clear to '0'. 0: No Effect	

Default: 0000 0000B

9.13. Source Hsync Digital PLL Control

0x0D0		HS DDS PLL Control	R/W
Bits	Name	Description	
7	HSDDS_DEBUG_MODE		
6	VER_DOUB_BYPASS	Vertical double buffer bypass 0: Normal 1: Bypass	
5	DBL_EN	Double buffer Load Data at VSYNC Blanking 0: Disable 1: Enable	
4	PHASE_COM_EN	Phase heat compensation enable	
3	HSDDS_RST	HS DDS Reset 0: Normal 1: Reset	
2	OCLK_DIV	Oscillator Clock divide 0: Normal 1: Divide 2	
1	HSDDS_UNLOCK_CHK	HS PLL unlock check 0: Disable 1: Enable	
0	DDS_EN	Reserved	

Default: 0000 0000B

0x0D1		HS Frequency Control	R/W
Bits	Name	Description	
6-4	HSDDS_LOOP_FILTER [2:0]	HS DDS loop filter control	
3	HSDDS_DIV_CTRL	HS DDS Divide control 0: Enable 1: Disable	
2		Reserved	
1-0	HPLL_FREQ_RANGE [1:0]	HS DDS output frequency range control 00: 100~200MHz 01: 50~100MHz 10: 25~50MHz 11: 12.5~25MHz	

Default:X001 0000B

0x0D2		HS PLL Frequency Control Ratio – lo	R/W
Bits	Name	Description	
7-0	HSDDS_RATIO [7:0]	HS PLL frequency control ration	

Default: 0000 0000B

0x0D3		HS PLL Frequency Control Ratio - mi	R/W
Bits	Name	Description	
7-0	HSDDS_RATIO [15:8]	HS PLL frequency control ration	

Default: 0000 0000B

0x0D4		HS PLL Frequency Control Ratio – hi	R/W
Bits	Name	Description	
5-0	HSDDS_RATIO [21:16]	HS PLL frequency control ration	

Default: 0000 1010B

0x0D5		HS PLL phase lock control	R/W
Bits	Name	Description	
7-5		Reserved	
4		Reserved	
3	HS_INV	HSYNC Invert 0: Normal 1: Inverted	
2	HPLL_OP_LOOP	HS PLL open loop control 0: Disable 1: Enable	
1	HS_QUICK_UNLOCK_CHK	HS PLL quick unlock check 0: Disable 1: Enable	
0	HPLL_EN	HS PLL DDS enable 0: Disable 1: Enable	

Default: 1000 0011B

0x0D6	HS PLL control		R/W
Bits	Name	Description	
7	HPLL_LOCK_EN	HS PLL phase lock enable	
6-5	HPLL_PLOOP_FIT [1:0]	HS PLL phase lock error correction ratio	
4-3	HPLL_FLOOP_FIT0 [1:0]	HS PLL frequency lock mode long time adjust level select 00: 16 01: 32 10: 64 11: 128	
2-0	HPLL_FLOOP_FIT1 [2:0]	HS PLL phase lock mode long time adjust duration select 000: 1 001: 2 010: 4 011: 8 100: 16 101: 32 110: 64 111:128	

Default: 0011 1111B

0x0D7	HS PLL divider - lo		R/W
Bits	Name	Description	
7-0	HSDDS_DIVIDER [7:0]	Clock divides value in the feedback loop of the HS PLL. The HS PLL reference is the input Hsync signal.	

Default: 1001 0111B

0x0D8	HS PLL divider - hi		R/W
Bits	Name	Description	
3-0	HSDDS_ DIVIDER [11:8]	The low byte [7:0] of HS PLL divider value. The register is **double-buffered**. Divider = HSDDS_ DIVIDER <11:0> + 1	

Default: XXXX 0110B

0x0D9	HS PLL phase control 1		R/W
Bits	Name	Description	
7-6	CLK_DLY_SEL	Select clock channel with clock delay adjusting. 00 = R 01 = G 10 = B 11 = Reserved	
5-0	HS_PHASE_STEP [5:0]	HS PLL 64 step phase adjust	

Default: 0000 0000B

0x0DA	HS PLL Phase control 2		R/W
Bits	Name	Description	
7-6		Reserved	
5	ADC_CKI_INV		
4	ADC_CKD_INV		
3-0	ADC_CK_DELAY[3:0]	To ADC Clock delay control	

Default: 0000 0000B

0x0DB	HS PLL Line count Select		R/W

Bits	Name	Description
7-5		Reserved
4-0	HS_LINE_CNT_SEL [4:0]	Horizontal Sync Line Count Select 00000: 1 Line 00001: 2 Line 00010: 4 Line 00100: 8 Line 01000: 16 Line 10000: 32 Line

Default: 0000 0100B

0x0DC	HS_DDS DPLL Output Control		R/W
Bits	Name	Description	
7-4	ADC_CK_DUTY [3:0]	To ADC clock duty control	
3	TMDS_CK_EN	Clock input to TMDS PLL enable 0: Disable 1: Enable	
2	HSDDS_COAST_EN	HS PLL coast enable 0: Disable 1: Enable	
1	CAP_CKO_INV	Capture clock output polarity invert 0: Normal 1: Inverted	
0	EXT_CKIN_EN	External clock input enable 0: Disable 1: Enable	

Default: 0000 0000B

0x0DD	HS DPLL Frequency Read back– lo		R
Bits	Name	Description	
7-0	HS_CNT_RESULT [7:0]	HS DPLL Frequency read back [7:0]	

Default: 0000 0000B

0x0DE	HS DPLL Frequency Read back - mi		R
Bits	Name	Description	
7-0	HS_CNT_RESULT [15:8]	HS DPLL Frequency read back [15:8]	

Default: 0000 0000B

0x0DF	HS DPLL Frequency Read back – hi		R
Bits	Name	Description	
5-0	HS_CNT_RESULT [21:16]	HS DPLL Frequency read back [21:16]	

Default: 0000 0000B

9.14. Index Port Access Control

0x0E0	Index Access Port		R/W
Bits	Name	Description	

7-4	TBL_SEL	Table Select
	INDEX_ADDR [7:0]	0000: Red Gamma Table (Read/Write) (10 bits/word)
	INDEX_ADDR [7:0]	0001: Green Gamma Table (Read/Write) (10 bits/word)
	INDEX_ADDR [7:0]	0010: Blue Gamma Table (Read/Write) (10 bits/word)
	INDEX_ADDR [7:0]	0011: R/G/B Gamma Tables modified simultaneously (Write only) (10 bits/word)
	INDEX_ADDR [11:0]	0100: OSD SRAM code only (Read/Write) (8 bits/word)
	INDEX_ADDR [11:0]	0101: OSD SRAM attribute MSB (Read/Write) (8 bits/word)
	INDEX_ADDR [11:0]	0110: OSD SRAM attribute LSB (Read/Write) (8 bits/word)
	INDEX_ADDR [11:0]	0111: OSD SRAM attribute (Read/Write) (16 bits/word)
	INDEX_ADDR [11:0]	1000: OSD SRAM code and attribute (Read/Write) (24 bits/word)
	INDEX_ADDR [11:0]	1001: OSD SRAM code from host and attribute from Reg 0x0CC ~ 0x0CD (Read/Write) (8 bits/word)
	INDEX_ADDR [9:0]	1010: OSD Programmable 1 Bit Color Font (Read/Write) (24 bits/word)
	INDEX_ADDR [7:0]	1011: OSD Programmable 2 Bit Color Font (Read/Write) (24 bits/word)
	INDEX_ADDR [7:0]	1100: OSD Programmable 4 Bit Color Font (Read/Write) (24 bits/word)
	INDEX_ADDR [7:0]	1101: OSD Palette (Read/Write) (16 bits/word)
	INDEX_ADDR [7:0]	1110: HDCP Data(Read/Write) (8 bits/word)
	INDEX_ADDR [7:0]	1111: Reserved
3	PORT_RW	Port Read/Write 0: Write 1: Read
2	DISP_ACCESS	SRAM write access enable when normal display 0: Disable 1: Enable
1-0		Reserve

Default: 0000 00XXB

0x0E1		Index Address Port - Low Byte	R/W
Bits	Name	Description	
7-0	INDEX_ADDR [7:0]	Table Address – low bits	

Default: 0000 0000B

0x0E2		Index Address Port - High Byte	R/W
Bits	Name	Description	
7-0	INDEX_ADDR [15:8]	Table Address – upper bits	

Default: 0000 0000B

0x0E3		Index Data Port	R/W
Bits	Name	Description	
7-0	PORT_DATA [7:0]	Data port for the SRAM, Palette, and Programmable Font.	

Default: 0000 0000B

Note: 1. If The Index Port's access is over 8 bit data length, the host interface will transfer or receive data from LSB to MSB.

9.15. Misc. Access Control

0x0E5	Host Interface Type Status	R

Bits	Name	Description
7-3		Reserve
2-1	I2C_ADDR	I2C Address Bit [2:1]
0	BUSTYPE	Host Interface Select 0: Parallel bus access 1: I2C bus access

Default: 0000 0001B

9.16. Auto Gain/Gauge Access Window Control

0x0E6	Auto Gain/Gauge Window Odd field Vertical Begin -lo	R/W

Bits	Name	Description
7-0	GI_CAP_VBEGO [7:0]	Vertical Capture Begin for Odd Field. GI_CAP_VBEGO indicates how many lines to wait after referenced edge of VSYNC before starting image capture. GI_CAP_VBEGO =3, means waiting 3 lines to begin capture. This register is double-buffered.

Default: 0000 0000B

0x0E7	Auto Gain/Gauge Window Odd field Vertical Begin -hi	R/W

Bits	Name	Description
2-0	GI_CAP_VBEGO [10:8]	MSB of GI_CAP_VBEGO. This register is double-buffered.

Default: XXXX X000B

0x0E8	Auto Gain/Gauge Window Even field Vertical Begin -lo	R/W

Bits	Name	Description
7-0	GI_CAP_VBEGE [7:0]	Vertical Capture Begin for Even Field. GI_CAP_VBEGE indicates how many lines to wait after referenced edge of VSYNC before starting image capture. GI_CAP_VBEGE =3, means waiting 3 lines to begin capture. This register is double-buffered.

Default: 0000 0000B

0x0E9	Auto Gain/Gauge Window Even field Vertical Begin -hi	R/W

Bits	Name	Description
2-0	GI_CAP_VBEGE [10:8]	MSB of GI_CAP_VBEGE. This register is double-buffered.

Default: XXXX X000B

0x0EA	Auto Gain/Gauge Window Vertical Length -lo	R/W

Bits	Name	Description
7-0	GI_CAP_VLEN [7:0]	Vertical Capture Length. GI_CAP_VLEN indicates how many lines to capture. GI_CAP_VLEN = 3, means capturing 3 lines. This register is double-buffered.

Default: 0000 0000B

0x0EB	Auto Gain/Gauge Window Vertical Length –hi	R/W

Bits	Name	Description
2-0	GI_CAP_VLEN [10:8]	MSB of GI_CAP_VLEN. This register is double-buffered.

Default: XXXX X000B

0x0EC		Auto Gain/Gauge Window Horizontal Begin –lo	R/W
Bits	Name	Description	
7-0	GI_CAP_HBEG [7:0]	Horizontal Capture Begin. GH_CAP_HBEG indicates how many pixels to wait after referenced edge of HSYNC before starting image capture. GH_CAP_HBEG =3, means waiting 3 pixels to begin capture. This register is double-buffered.	

Default: 0000 0000B

0x0ED		Auto Gain/Gauge Window Horizontal Begin –hi	R/W
Bits	Name	Description	
3-0	GI_CAP_HBEG [11:8]	MSB of GI_CAP_HBEG. This register is double-buffered.	

Default: XXXX 0000B

0x0EE		Auto Gain/Gauge Window Horizontal Width –lo	R/W
Bits	Name	Description	
7-0	GI_CAP_HWID [7:0]	Horizontal Capture Width. GI_CAP_HWID indicates how many pixels to capture. GI_CAP_HWID = 3, means capturing 3 pixels. This register is double-buffered.	

Default: 0000 0000B

0x0EF		Auto Gain/Gauge Window Horizontal Width –hi	R/W
Bits	Name	Description	
3-0	GI_CAP_HWID [11:8]	MSB of GI_CAP_HWID. This register is double-buffered.	

Default: XXXX 0000B

9.17. Display Digital PLL Control

0x0F0		Display DDS PLL Control	R/W
Bits	Name	Description	
7	DDDS_DEBUG_MODE		
6-4			
3	DDDS_RST	Display DDS Reset 0: Normal 1: Reset	
2			
1	DDDS_UNLOCK_CHK	Display PLL unlock check 0: Disable 1: Enable	
0	DDDS_EN	Display DDS enable 0: Disable 1: Enable	

Default: 0000 0001B

0x0F1		Display Frequency Control	R/W
Bits	Name	Description	
6-4	DDDS_LOOP_FILTER [2:0]	Display DDS loop filter control	

3-2		Reserved
1-0	DPLL_FREQ_DIV [1:0]	Display DDS output frequency divider 00: Divide 1 (80~180MHz) 01: Divide 2 (40~80MHz) 10: Divide 4 (20~40MHz) 11: Divide 8 (10~20MHz)

Default: 0001 0000B

0x0F2	Display PLL Frequency Control Ratio – lo		R/W
Bits	Name	Description	
7-0	DDDS_RATIO [7:0]	Display DDS frequency control ration	

Default: 0000 0000B

0x0F3	Display PLL Frequency Control Ratio - mi		R/W
Bits	Name	Description	
7-0	DDDS_RATIO [15:8]	Display DDS frequency control ration	

Default: 0000 0000B

0x0F4	Display PLL Frequency Control Ratio – hi		R/W
Bits	Name	Description	
5-0	DDDS_RATIO [21:16]	Display DDS frequency control ration	

Default: 0000 1010B

0x0F5	SSC Control		R/W
Bits	Name	Description	
7-5	SSC_MOD_FREQ	Display PLL spread spectrum modulation frequency control "111" = REFCLK/4 "110" = REFCLK/8 "101" = REFCLK/16 "100" = REFCLK/32 "011" = REFCLK/64 "010" = REFCLK/128 "001" = REFCLK/256 "000" = REFCLK/512	
4-1	SSC_RATIO	DDDS PLL spread spectrum ratio "1000" = 1/4 "0111" = 1/8 "0110" = 1/16 "0101" = 1/32 "0100" = 1/64 "0011" = 1/128 "0010" = 1/256 "0001" = 1/512 "0000" = 1/1024	
0	SSC_EN	DDS PLL spread spectrum enable 0: Disable 1: Enable	

Default: 0000 1010B

0x0F6	Reserved		R/W
Bits	Name	Description	

Default: 0000 0000B

9.18. Graphic Input Gauge

0x0F7	Gauge Control 1	R/W

Bits	Name	Description
7-1		
0	GAUGE_MOD_SEL	Gauge Detection Area mode select 0 = Detecting area is defined by capture registers 1 = Detecting area is defined by Auto Gain/Gauge window registers.

Default: XXXX XXX0B

0x0F8	Gauge Control 2		R

Bits	Name	Description
7	GAUGE_EN	To Gauge the distribution of input data. When GAUGE_EN set "1", the function is enable, then if the gauge is finished this bit is cleared to "0". 0 = Disable 1 = Enable
6-5		Reserved
4-3	GAUGE_SEL	Gauge Source Select 00: Blue Channel 01: Green Channel 10: Red Channel 11: Reserved
2-0	GAUGE_STEP [7:0]	The step of gauge Data 000: 1 Step 100: 16 Step 001: 2 Step 101: 32 Step 010: 4 Step 110: Reserved 011: 8 Step 111: Reserved

Default: 00X0 0000B

0x0F9	Gauge Result Read Back Area Select		R/W

Bits	Name	Description
7-3		Reserved
2-0	GAUGE_AREA	The Gauge Result Read back area select 0~7

Default: XXXX X000B

0x0FA	Gauge Offset		R/W

Bits	Name	Description
7-0	GAUGE_OFFSET	The level of Y/R/G/B Input when Gauge function is enable

Default: XXX0 0000B

0x0FB	Gauge Result - lo		R

Bits	Name	Description
7-0	GAUGE_RESULT [7:0]	The gauge result of input data in capture window

Default:

0x0FC	Gauge Result - mi		R

Bits	Name	Description
7-0	GAUGE_RESULT [15:8]	The gauge result of input data in capture window

Default:

0x0FD	Gauge Result - hi		R

Bits	Name	Description
7-0	GAUGE_RESULT [23:16]	The gauge result of input data in capture window

Default:

0x0FE	Reserved		R/W
Bits	Name	Description	

Default: 0000 0000B

0x0FF	Accessing Register Page Enable		R/W
Bits	Name	Description	
D7-2		Reserve	
D1-0	REG_PAGE_SEL	Register Page Enable 00: Enable register Page0. 01: Enable register Page1. 10: Enable register Page2. 11: Reserved	

Default: XXXX XX00B

9.19. Product ID

0x100	Product ID		R
Bits	Name	Description	
7-4	REV_NO	IC revision number	
3-0	CHIP_ID	Chip ID = 0111	

9.20. Power Control

0x101	Power Control		R/W
Bits	Name	Description	
7		Reserved	
6	PU_LVDSA	LVDS A Port power up control. 0 = Power down 1 = Power up	
5	WARM_RST	Chip Warm Reset. When WARM_RST=1, all state machines will be reset other than the all of register's value. 0 = Normal 1 = Reset	
4		Reserved	
3	GCLK_OFF	Graphic Port Clock Off. When GCLK_OFF=1, Graphic Port clock is disabled to conserve power. This bit is reset only by external reset pin.	
2	VCLK_OFF	Video Port Clock Off. When VCLK_OFF=1, Video Port clock is disabled to conserve power. This bit is reset only by external reset pin.	
1		Reserved	
0	DCLK_OFF	Display Clock Off. When DCLK_OFF=1, display clock is disabled to conserve power. This bit is reset only by external reset pin.	

Default: 0000 11X1B

0x102	Power Down Control 2		R/W
Bits	Name	Description	
7		Reserved	

6	PU_PLL	ADCPLL Power up frequency PLL. 0 = Power down 1 = Power up
5	PU_HPLL (hpll_en)	HPLL Power up control. 0 = Power down 1 = Power up
4	PU_TSEN	ADCPLL Power up on chip temperature sensor. 0 = Power down 1 = Power up
3	PU_ADC	ADC Power up control. 0 = Power down 1 = Power up
2		
1	PU_TMDS	TMDS PD power up mode. When PU_TMDS = '0', TMDS circuit will go into power down state. 0 = Power down 1 = Power up
0		Reserved

Default: 1101 1000B

0x103~0x105		Reserved	R/W
Bits	Name	Description	

Default: 0000 0000B

9.21. Auto Tune

Graphic Auto Tune Control

0x106		Graphic Auto Tune Control	R/W
Bits	Name	Description	
7	GI_AGPD_MOD	Auto Gain and Phase Detection Area mode select 0 = Normal/ Original 1 = Detecting area is defined by Auto Gain/Gauge window registers.	
6	GI_AUTO_MASK	Gain and Phase Detection Area masking when GI_GAINPHS_AREA = "1" 0 = Detecting area is whole frame 1 = Detecting area is defined by mask window registers.	
5	GI_GAINPHS_AREA	Gain and Phase Detection Area Define Enable. 0 = Detecting area is over one frame except the area defined by mask window registers. 1 = Detecting area is defined by capture registers.	
4	GI_POS_DE	Enable Position Detection depending on DE signal when TMDS is enabled. If GI_POS_DE =1, 0xFF data is input to RGB channel for position detection instead of data from graphic port when DE is '1'.	
3-2	GI_GAINPHS_SEL [1:0]	Graphic Input Gain and Phase Detection Type Select. 00 = Phase Tune 1 01 = Phase Tune 2 10 = Min RGB Gain 11 = Max RGB Gain	
1	GI_GAINPHS_EN/ GI_GAINPHS_RDY	Graphic Input Gain and Phase Detection Enable. When GI_GAINPHS_EN = 1, detection will start from next VSYNC. When	

		detection is finished, this bit is cleared to '0'. 0 = Disable 1 = Enable
0	GI_POS_EN/ GI_POS_RDY	Graphic Input Active Window Position Detection Enable. When GI_POS_EN = 1, detection will start from next VSYNC. When detection is finished, this bit is cleared to '0'. 0 = Disable. 1 = Enable

Default: 0001 1100B

Graphic Auto Position

0x107	Auto Position Black Threshold	R/W
Bits	Name	Description
7-0	GI_POS_THR [7:0]	Graphic data lager then GI_POS_THR will be considered to be non-black pixel for position detecting.

Default: 0000 1111B

0x108	Auto Position Vertical Begin for Odd Field –lo	R
Bits	Name	Description
7-0	GI_POS_VBEGO [7:0]	Active Window Vertical Begin for Odd Field. GI_POS_VBEGO= 3 means there are 3 blanking lines.

0x109	Auto Position Vertical Begin for Odd Field –hi	R
Bits	Name	Description
2-0	GI_POS_VBEGO [10:8]	MSB of GI_POS_VBEGO

0x10A	Auto Position Vertical Begin for Even Field –lo	R
Bits	Name	Description
7-0	GI_POS_VBEGE [7:0]	Active Window Vertical Begin for Even Field. GI_POS_VBEGE= 3 means there are 3 blanking lines.

0x10B	Auto Position Vertical Begin for Even Field –hi	R
Bits	Name	Description
2-0	GI_POS_VBEGE [10:8]	MSB of GI_POS_VBEGE

0x10C	Auto Position Vertical Length –lo	R
Bits	Name	Description
3-0	GI_POS_VLEN [7:0]	The active window vertical length. GI_POS_VLEN = 3 means there are 3 active lines.

0x10D	Auto Position Vertical Length –hi	R
Bits	Name	Description
2-0	GI_POS_VLEN [10:8]	MSB of GI_POS_VLEN

0x10E	Auto Position Horizontal Begin –lo	R

Bits	Name	Description
7-0	GI_POS_HBEG [7:0]	The active window horizontal begin. GI_POS_HBEG = 3 means there are 3 blanking pixels.

0x10F		Auto Position Horizontal Begin –hi	R
Bits	Name	Description	
3-0	GI_POS_HBEG [11:8]	MSB of GI_POS_HBEG	

0x110		Auto Position Horizontal Width –lo	R
Bits	Name	Description	
3-0	GI_POS_HWID [7:0]	The active window horizontal width. GI_POS_HWID = 3 means there are 3 active pixels.	

0x111		Auto Position Horizontal Width –hi	R
Bits	Name	Description	
3-0	GI_POS_HWID [11:8]	MSB of GI_POS_HWID	

Graphic Auto Phase and Gain

0x112		Auto Phase Bit Mask	R/W
Bits	Name	Description	
2-0	GI_PHS_MASK [2:0]	Decide how many LSB bits will be masked out, and then the difference between adjacent pixels will be added to the sum of difference accumulator.	

Default: XXXX X100B

0x113		Auto Phase Sum of Difference –lo	R
Bits	Name	Description	
7-0	GI_PHS_SDIFF [7:0]	Auto Phase Sum of Difference (LSB). GI_PHS_SDIFF specifies how the phase locking quality in ADCPLL block.	
	R_MINMAX [7:0]	The minimum or maximum value of red channel data in one frame.	

0x114		Auto Phase Sum of Difference – 2'nd	R
Bits	Name	Description	
7-0	GI_PHS_SDIFF [15:8]	Second byte of GI_PHS_SDIFF	
	G_MINMAX [7:0]	The minimum or maximum value of green channel data in one frame.	

0x115		Auto Phase Sum of Difference – 3'rd	R
Bits	Name	Description	
7-0	GI_PHS_SDIFF [23:16]	Third byte of GI_PHS_SDIFF	
	B_MINMAX [7:0]	The minimum or maximum value of blue channel data in one frame.	

0x116		Auto Phase Sum of Difference -hi	R
Bits	Name	Description	
7-0	GI_PHS_SDIFF [31:24]	MSB of GI_PHS_SDIFF	

Graphic Auto Clock

0x117		Auto Clock Reference Width -lo	R/W
Bits	Name	Description	
7-0	GI_CLK_REF [7:0]	Auto Clock Reference Width. This register provides the reference value for calibrating the frequency of sampling clock in ADCPLL block.	

Default: 0000 0000B

0x118		Auto Clock Reference Width -hi	R/W
Bits	Name	Description	
3-0	GI_CLK_REF [11:8]	MSB of AUTO_CLK_REF	

Default: XXXX 0000B

0x119		Auto Clock Detecting Result	R
Bits	Name	Description	
7-6	GI_CLK_COMP [1:0]	Auto Clock Comparing Relation. GI_CLK_COMP specifies the comparing relation between GI_POS_HWID and GI_CLK_REF 00: GI_POS_HWID = GI_CLK_REF 01: GI_POS_HWID < GI_CLK_REF 10: GI_POS_HWID > GI_CLK_REF 11: Reserved	
5-0	GI_CLK_DIFF [5:0]	Difference of |GI_POS_HWID - GI_CLK_REF| The difference value is clamped to 0x3F if difference $\geq$ 0x3F	

0x11A			R/W
Bits	Name	Description	
7-0		Reserved	

Video Auto Tune Control

0x11B		Video Auto Tune Control	R/W
Bits	Name	Description	
5	VI_AUTO_MASK	Gain Detection Area masking when VI_GAIN_AREA = "1" 0 = Detecting area is whole frame 1 = Detecting area is defined by mask window registers.	
4	VI_AUTO_HREF	Video auto tune according to YUV_HREF signal 0 = Disable 1 = Enable	
3	VI_GAIN_AREA	Gain Detection Area Define Enable. 0 = Detecting area is over one frame except the area defined by mask window registers. 1 = Detecting area is defined by capture registers.	
2	VI_GAIN_SEL	Video Input Gain Type Select	

Free Datasheet http://www.datasheet4u.com/

		0 = Min Y Gain
		1 = Max Y Gain
1	VI_GAIN_EN/ VI_GAIN_RDY	Video Input Y Min/Max Data Detection Enable. When VI_MINMAX_EN = 1, detection will start from next VSYNC. When detection is finished, this bit is cleared to '0'. 0 = Disable 1 = Enable
0	VI_POS_EN/ VI_POS_RDY	Video Input Active Window Position Detection Enable. When VI_POS_EN = 1, detection will start from next VSYNC. When detection is finished, this bit is cleared to '0'. 0 = Disable 1 = Enable

Default: XX00 0000B

Video Auto Position

0x11C	Auto Position Black Threshold	R/W
Bits	Name	Description
7-0	VI_POS_THR [7:0]	Video data lager than VI_POS_THR will be considered to be non-black pixel for position detecting.

Default: 0000 1111B

0x11D	Auto Position Vertical Total -lo	R
Bits	Name	Description
7-0	VI_VTOTAL [7:0]	Vertical Period Total. VI_VTOTAL =99 means total 99 lines.

0x11E	Auto Position Vertical Total -hi	R
Bits	Name	Description
2-0	VI_VTOTAL [10:8]	MSB of VI_VTOTAL.

0x11F	Auto Position Vertical Begin for Odd Field -lo	R
Bits	Name	Description
7-0	VI_POS_VBEGO [7:0]	Active Window Vertical Begin for Odd Field. VI_POS_VBEGO =9 means 9 blanking lines.

0x120	Auto Position Vertical Begin for Odd Field -hi	R
Bits	Name	Description
2-0	VI_POS_VBEGO [10:8]	MSB of VI_POS_VBEGO.

0x121	Auto Position Vertical Begin for Even Field -lo	R
Bits	Name	Description
7-0	VI_POS_VBEGE [7:0]	Active Window Vertical Begin for Even Field. VI_POS_VBEGE =9 means 9 blanking lines.

0x122H	Auto Position Vertical Begin for Even Field -hi	R
Bits	Name	Description

2-0	VI_POS_VBEGE [10:8]	MSB of VI_POS_VBEGE.

0x123	Auto Position Vertical Length -lo		R
Bits	Name	Description	
7- 0	VI_POS_VLEN [7:0]	Active Window Vertical Length. VI_POS_VLEN =99 means 99 active lines.	

0x124	Auto Position Vertical Length -hi		R
Bits	Name	Description	
2-0	VI_POS_VLEN [10:8]	MSB of VI_POS_VLEN.	

Default:

0x125	Auto Position Horizontal Total -lo		R
Bits	Name	Description	
7-0	VI_HTOTAL [7:0]	Horizontal Period Total. VI_HTOTAL=99, means total 99 pixels.	

Default:

0x126	Auto Position Horizontal Total -hi		R
Bits	Name	Description	
3-0	VI_HTOTAL [11:8]	MSB of VI_HTOTAL.	

Default:

0x127	Auto Position Horizontal Begin -lo		R
Bits	Name	Description	
7-0	VI_POS_HBEG [7:0]	Active Window Horizontal Begin. VI_POS_HBEG =3 means 3 blanking pixels.	

Default:

0x128	Auto Position Horizontal Begin -hi		R
Bits	Name	Description	
3-0	VI_POS_HBEG [11:8]	MSB of VI_POS_HBEG	

Default:

0x129	Auto Position Horizontal Width -lo		R
Bits	Name	Description	
7-0	VI_POS_HWID [7:0]	Active Window Horizontal Width. VI_POS_HWID =99 means 99 active pixels.	

Default:

0x12A	Auto Position Horizontal Width -hi		R
Bits	Name	Description	
3-0	VI_POS_HWID [11:8]	MSB of VI_POS_HWID	

Video Auto Gain

0x12B	Video Min/Max Y Value		R
Bits	Name	Description	
7-0	Y_MINMAX [7:0]	The minimum or maximum value of Y channel data in one frame.	

0x12C~0x12F	Reserved		R/W
Bits	Name	Description	
7-0		Reserved	

9.22. Bright Frame Display Registers

Bright Frame Control
Note--When both Bright Frames are enabled and if two windows are overlapped frame2 has higher priority than frame 1.

0x130	Bright Frame Enable Control		R/W
Bits	Name	Description	
7-5			
4	BRIGHT_REF_CTL	Bright Frame Active reference 0: Front (Capture) 1: Post (Display)	
3-2		Reserved	
1	BRIGHT_FRM2_EN	Enable Bright Frame 2 0: Disable 1: Enable	
0	BRIGHT_FRM1_EN	Enable Bright Frame 1 0: Disable 1: Enable	

Default: XXXX XX00B

0x131	Bright Frame access index Select		R/W
Bits	Name	Description	
7-1		Reserved	
0	BRIGHT_FRM_SEL [0]	This register is used to select which frame is to be accessed or modified. It is programmed prior to accessing the registers Reg 0x132 ~ 0x13B "0" = Bright Frame 1 "1" = Bright Frame 2	

Default: XXXX XXX0B

0x132	Bright Frame Horizontal Start - Low byte		R/W
Bits	Name	Description	
7-0	BRIGHT_FRM_HS [7:0]	Bright Frame horizontal start low byte [7:0]. Specifies the horizontal starting position of the Bright Frame in pixel units. This register is **double-buffered**.	

Default: 0000 0000B

0x133	Bright Frame Horizontal Start - High Byte		R/W
Bits	Name	Description	
7-4		Reserved	
3-0	BRIGHT_FRM_HS	Bright Frame horizontal start high byte [11:8]. Specifies the horizontal	

[11:8]	starting position of the Bright Frame in pixel units. This register is **double-buffered**.

Default: XXXX 0000B

0x134	Bright Frame Horizontal Width - Low byte		R/W
Bits	Name	Description	
7-0	BRIGHT_FRM_HW [7:0]	Bright Frame horizontal Width low byte [7:0]. Specifies the width of the Bright Frame in pixel units. . This register is **double-buffered**.	

Default: 0000 0000B

0x135	Bright Frame Horizontal Width – High byte		R/W
Bits	Name	Description	
7-4		Reserved	
3-0	BRIGHT_FRM_HW [11:8]	Bright Frame horizontal Width low byte [11:8]. Specifies the width of the Bright Frame in pixel units. . This register is **double-buffered**.	

Default: XXXX 0000B

0x136	Bright Frame Vertical Start - Low byte		R/W
Bits	Name	Description	
7-0	BRIGHT_FRM_VS [7:0]	Bright Frame vertical start low byte [7:0]. Specifies the vertical starting position of the Bright Frame in pixel units. This register is **double-buffered**.	

Default: 0000 0000B

0x137	Bright Frame Vertical Start - High Byte		R/W
Bits	Name	Description	
7-4		Reserved	
3-0	BRIGHT_FRM_VS [10:8]	Bright Frame vertical start high byte [10:8]. Specifies the vertical starting position of the Bright Frame in pixel units. This register is **double-buffered**.	

Default: XXXX 0000B

0x138	Bright Frame Vertical Height - Low byte		R/W
Bits	Name	Description	
7-0	BRIGHT_FRM_VH [7:0]	Bright Frame vertical Width low byte [7:0]. Specifies the width of the Bright Frame in pixel units. . This register is **double-buffered**.	

Default: 0000 0000B

0x139	Bright Frame Vertical Height – High byte		R/W
Bits	Name	Description	
7-4		Reserved	
2-0	BRIGHT_FRM_VH [10:8]	Bright Frame vertical Width low byte [10:8]. Specifies the width of the Bright Frame in pixel units. . This register is **double-buffered**.	

Default: XXXX X000B

0x13A	Bright Frame Gain Control	R/W
Bits	Name	Description
7-0	BRIGHT_FRM_GAIN	Bright Frame gains adjusting

Default: 1000 0000B

0x13B	Bright Frame Offset Control	R/W

Bits	Name	Description
7-0	BRIGHT_FRM_OFFSET	Bright Frame offsets adjusting

Default: 0000 0000B

0x13C~0x13E	Reserved	R/W

Bits	Name	Description

Default: 0000 0000B

9.23. DVI Input Control 2

0x13F	DVI Control	R/W

Bits	Name	Description
7-0		

Default: 0000 0000B

0x140	DVI Control	R/W

Bits	Name	Description
7-0		

Default: 0000 0000B

0x141	DVI Control	R/W

Bits	Name	Description
7-0		

Default: 0000 0000B

0x142	DVI Control	R/W

Bits	Name	Description
7-0		

Default: 0000 0000B

0x143	DVI Control	R/W

Bits	Name	Description
7	TMDS_PLL_PD	TMDS PLL power down control
6	TMDS_VCO_5X	TMDS PLL VCO 5X mode
5-4	TMDS_LCPC	TMDS PLL lower charge pump current
3-1	TMDS_VCO_SV	Control reference swing voltage of TMDS PLL VCO
0	PMOS_RES_EN	PMOS resistor enable

Default: 0000 0000B

0x144	DVI Control	R/W

Bits	Name	Description
7-1		
0	TMDS_IPDS_PD	Power down control of three channel impedances

Default: 0000 0000B

0x145	DVI Control	R/W

Bits	Name	Description
7-0		

Default: 0000 0000B

0x146	DVI Control	R/W
Bits	Name	Description
7-0		

Default: 0000 0000B

0x147	DVI Control	R/W
Bits	Name	Description
7-0		

Default: 0000 0000B

0x148 ~ 0x149	Reserved	R/W
7-0	Reserved	

Default: 0000 0000B

9.24. Display Port Control

♦   Display timing control

♦   Single pixel or dual pixel output

♦   Output signals drive current and slew rate control

♦   Phase delay adjustment for accessing clock to external LCD

♦   Dithering function supports 24-bit quality for 18-bit panel

♦   Mute display control

Display Video Special mode Control

0x14C	Reserved	R
Bits	Name	Description
7-0		

0x14D	Reserved	R
Bits	Name	Description
3-0		

0x14E	Reserved	R/W
7-0	Reserved	

Default: 0000 0000B

0x14F	Reserved	R/W
Bits	Name	Description
7-0	Reserved	

Default: XXXX 0000B

Display General Control

0x150	Display Control	R/W
Bits	Name	Description
7	DP_BIT_SHF	When display bus is 6-bit/color, this bit enable will shift the data RA[7:2], GA[7:2], BA[7:2] to RA[5:0], GA[5:0], BA[5:0] and RB[7:2], GB[7:2], BB[7:2] to RB[5:0], GB[5:0], BB[5:0]. When display bus is 8-bit/color, this bit enable will rotate the data RA[7:0], GA[7:0], BA[7:0] and RB[7:0], GB[7:0], BB[7:0]

		to right 2 bits 0 = Normal 1 = Shift / Rotate
6		Reserved
5		Reserved
4		Reserved
3	DP_COLDEP	Display Color Depth 0 = 8-bit/color 1 = 6-bit/color
2	DP_BUSWID	Display Bus Width 0 = Double pixel 48-bit 1 = Single pixel 24-bit
1	DP_DE	Panel supports DE mode 0 = Panel supports Sync mode, display Hs/Vs signal is at normal state 1 = Panel supports DE mode, display Hs/Vs signal will be pulled low
0	DP_EN	Display Enable 0 = Disable. Tri-state control lines and data lines. 1 = Enable

Default: 011X 0000B

0x151		Reserved	R/W
Bits	Name	Description	
7-0			

Default: 0000 0000B

0x152		Reserved	R/W
Bits	Name	Description	
7-0			

Default: 0000 0000B

0x153		Reserved	R/W
Bits	Name	Description	
3-0			

Default: XXXX 0000B

0x154		Display Mute and Color Control	R/W
Bits	Name	Description	
7-4	DP_PATT [3:0]	Select built-in display pattern Pattern number = 0~15 If PATT_BK = Bank 0 0000 = Gamma Correction pattern 0001 = Dot Moiré 0010 = Vertical Line Moire (1B1W) 0011 = Vertical Line Moire (2B1W) 0100 = Vertical Line Moire (2B2W) 0101 = 256 V_Gray Bar 0110 = 256 H_Gray Bar 0111 = Horizontal Line Moire (1B1W) 1000 = Horizontal Line Moire (2B1W) 1001 = Horizontal Line Moire (2B2W)	

		1010 = Chat Pattern
		1011 = White Pattern
		11xx = Rectangular pattern, outline width is defined by xx bits.
		00 = 1 pixel
		01 = 3 pixels
		10 = 5 pixels
		11 = 7 pixels
		If PATT_BK = Bank 1
		0000 = Black pattern
		0001~1111 = Reserved
3	PATT_BK	Built-in pattern bank Select 0 = Bank 0 1 = Bank 1
2	CBAR_EN	Paste a Cross Bar on the built-in display pattern and the Bar's gray level is controlled via CBAR_FG[7:0] register (0x15A) 0 = Disable 1 = Enable
1-0	DP_MUTE [1:0]	Display Mute Mode Select 00 = Normal display, RGB channel output controlled via DP_RGB 01 = Mute input with output built-in display pattern, pattern color decided by DP_RGB registers. (Display free-run) 10 = Mute input with output OSD and background color, background color decided by DP_BG_R/G/B registers. (Display free-run) 11 = Pull low all display signals including data, clock and control lines

Default: 0000 0000B

0x155	Display Drive Control		R/W
Bits	Name	Description	
7	DCLK_SLEW	Select panel interface CLOCK slew rate 0: Fast 1: Slow	
6-4	DCLK_DRV [2:0]	Select panel interface CLOCK drive strength 000: 2mA 100: 10mA 001: 4mA 101: 12mA 010: 6mA 110: 14mA 011: 8mA 111: 16mA	
3	DOUT_SLEW	Select panel interface DATA slew rate 0: Fast 1: Slow	
2-0	DOUT_DRV [2:0]	Select panel interface DATA drive strength 000: 2mA 100: 10mA 001: 4mA 101: 12mA 010: 6mA 110: 14mA 011: 8mA 111: 16mA	

Default: 0100 0011B

0x156	Display Drive and Polarity Control		R/W
Bits	Name	Description	
7	DDE_POL	Display DE 1 = Active High	

6	DCLK_POL	Display Clock 0 = Normal 1 = Inverted
5	DHS_POL	Display Hsync 1 = Active High 0 = Active Low
4	DVS_POL	Display Vsync 1 = Active High 0 = Active Low
3	DCTRL_SLEW	Select panel interface HS/VS/DE slew rate 0 = Fast 1 = Slow
2-0	DCTRL_DRV [2:0]	Select panel interface HS/VS/DE drive strength 000 = 2mA 100 = 10mA 001 = 4mA 101 = 12mA 010 = 6mA 110 = 14mA 011= 8mA 111 = 16mA

Note: first partial row at top reads "0 = Active Low"

Default: 1011 0010B

0x157		Display Clock and Data Delay Control	R/W
Bits	Name	Description	
7	DOUT_STAG	When dual-pixel/clock display output is enabled, staggering output format is supported to reduce the ground bounce that affects EMI. 0 = Normal 1 = Stagger	
6-5	DCLK_SYNC_SEL	Display clock synchronous mode select 00 = Display clock free-run 01 = Display clock is synchronized to input(default by TCON enable) 10 = Display clock free-run and DISP_DE synchronized to DISP_CLK 11 = Reserved	
4-0	DCLK_DLY [4:0]	Select panel interface CLOCK delay time. (0.5nS/step) 0~32 step	

Default: 0010 0000B

0x158		Display Dithering Control	R/W
Bits	Name	Description	
7-4	DITH_MODE [3:0]	Dithering mode select	
3	GAMMA_DITH_EN	Gamma Dithering enable. 0 = Disable 1 = Enable	
2	DITH_8BIT/ GAMMA_RANDOM	Rounded 10 bit gamma data output to 8 bit for dithering 0 = Disable 1 = Enable 8 Bit dithering If GAMMA_DITH_EN = "1" (0x158[3]), this bit is for gamma dithering random mode control	
1	DITH_TURBO		
0	DITH_EN	Dithering enable. When DITH_EN =0, the LSB bits of display data will be truncated if display color depth is less than internal data resolution. 0 = Disable	

		1 = Enable

Default: 0000 0000B

0x159	Display Channel Select		R/W
Bits	Name	Description	
7	INT_FAST_EN	Mute mode with Free Run timing when graphic input sync fail 0: Disable 1: Enable	
6		Reserved	
5	MUTE_FR_EN	Mute mode with Free Run timing Enable, this display Horizontal sync timing reference to Reg. 0x179~0x17A. 0: Disable 1: Enable	
3		Reserved	
2-0	DP_RGB [2:0]	Select RGB channel for display 000 = RGB normal display 001 = R channel only 010 = G channel only 011 = B channel only 100 = R & G channels 101 = R & B channels 110 = G & B channels 111 = RGB inverted display	

Default: 00XX X000B

0x15A	Cross Bar Gray Level		R/W
Bits	Name	Description	
7-0	CBAR_FG [7:0]	Select the foreground gray level of Cross Bar for burn-in display pattern. R=G=B= 0~255	

Display Timing Control
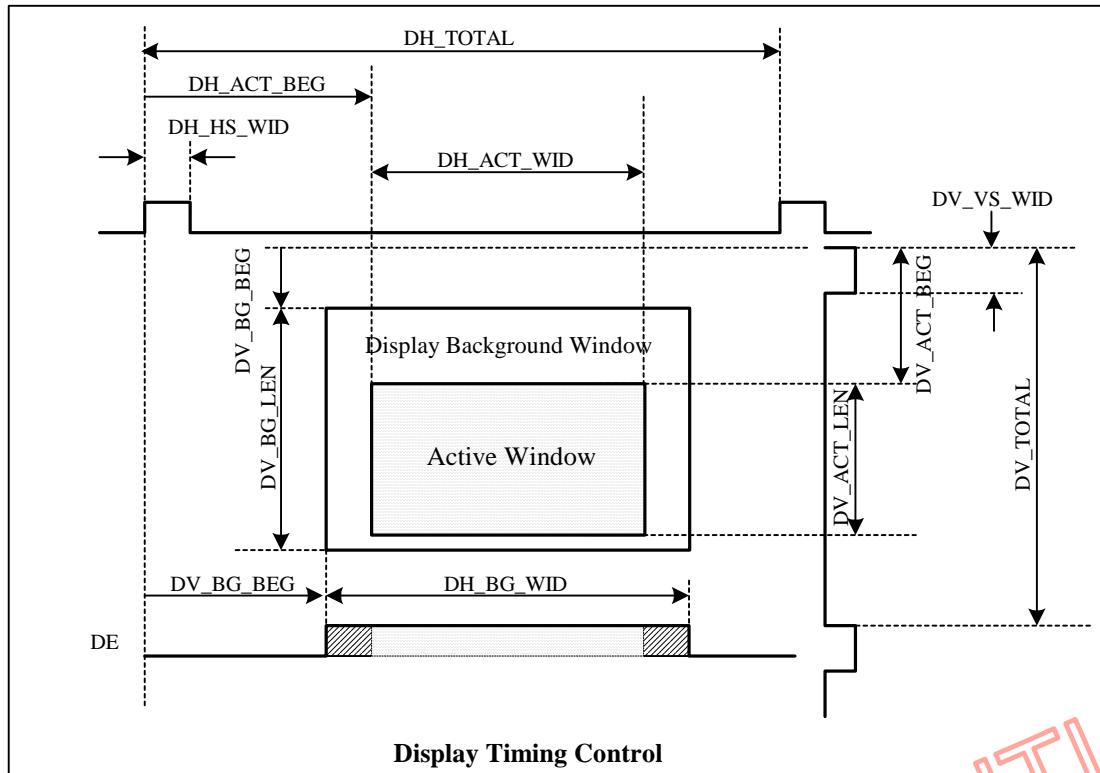
Figure 9.24-1 Display Timing

Display Sync Timing Control

0x15B		Display Vertical Total –lo	R/W
Bits	Name	Description	
7-0	DV_TOTAL [7:0]	Display Vertical Total Lines. DV_TOTAL = 3 means there are 4 total lines.	

Default: 0000 0000B

0x15C		Display Vertical Total –hi	R/W
Bits	Name	Description	
2-0	DV_TOTAL [10:8]	MSB of DV_TOTAL	

Default: XXXX X000B

0x15D		Display VSYNC Pulse Width	R/W
Bits	Name	Description	
7-0	DV_VS_WID [7:0]	Display VSYNC Pulse Width. DV_VS_WID =3, means pulse width is 3 lines wide.	

Default: 0000 0000B

0x15E		Display Horizontal Total –lo	R/W
Bits	Name	Description	
7-0	DH_TOTAL [7:0]	Display Horizontal Total Pixels. DH_TOTAL = 3 means there are 4 total pixels.	

Default: 0000 0000B

0x15F		Display Horizontal Total –hi	R/W

Bits	Name	Description
3-0	DH_TOTAL [11:8]	MSB of DH_TOTAL

Default: XXXX 0000B

0x160	Display HSYNC Pulse Width	R/W

Bits	Name	Description
7-0	DH_HS_WID [7:0]	Display HSYNC Pulse Width. DH_HS_WID =3, means pulse width is 3 pixels wide.

Default: 0000 0000B

0x161H		R/W

Bits	Name	Description
7-2		Reserved
1	DR_VUPDATE_EN	Display Registers update enable on next DVS when V_BOUBLE_EN = "1"
0	DR_VDOUBLE_EN	Display Registers update on next DVS enable, When this bit enable will causes display registers update on next DVS. Otherwise, display registers will direct update. 0 = Disable 1 = Enable

Default: 0000 0000B

Display Background Window Control

0x162	Display Background Window Vertical Begin –lo	R/W

Bits	Name	Description
7-0	DV_BG_BEG [7:0]	Display Background Window Vertical Begin. DV_BG_BEG indicates how many lines to wait after DVSYNC leading edge before starting image display. DV_BG_BEG =3, means waiting 3 lines to begin display.

Default: 0000 0000B

0x163	Display Background Window Vertical Begin –hi	R/W

Bits	Name	Description
2-0	DV_BG_BEG [10:8]	MSB of DV_BG_BEG

Default: XXXX X000B

0x164	Display Background Window Vertical Length –lo	R/W

Bits	Name	Description
7-0	DV_BG_LEN [7:0]	Display Background Window Vertical Length. DV_BG_LEN indicates how many lines to display. DV_BG_LEN =3, means displaying 3 lines.

Default: 0000 0000B

0x165	Display Background Window Vertical Length –hi	R/W

Bits	Name	Description
2-0	DV_BG_LEN [10:8]	MSB of DV_BG_LEN

Default: XXXX X000B

0x166	Display Background Window Horizontal Begin –lo	R/W

Bits	Name	Description

| 7-0 | DH_BG_BEG [7:0] | Display Background Window Horizontal Begin. DH_BG_BEG indicates how many pixels to wait after DHSYNC leading edge before starting image display. DH_BG_BEG =3, means waiting 3 pixels to begin display. |

Default: 0000 0000B

0x167	Display Background Window Horizontal Begin –hi		R/W
Bits	Name	Description	
3-0	DH_BG_BEG [11:8]	MSB of DH_BG_BEG	

Default: XXXX 0000B

0x168	Display Background Window Horizontal Width –lo		R/W
Bits	Name	Description	
7-0	DH_BG_WID [7:0]	Display Background Window Horizontal Width. DV_BG_WID indicates how many pixels to display. DV_BG_WID =3, means displaying 3 pixels.	

Default: 0000 0000B

0x169	Display Background Window Horizontal Width –hi		R/W
Bits	Name	Description	
3-0	DH_BG_WID [11:8]	MSB of DH_BG_WID	

Default: XXXX 0000B

0x16A			R/W
Bits	Name	Description	
7-5		Reserved	
4	DP_PORT_SWAP	A /B Port Swap Control 0: Normal 1: A/B Port Swap	
3	DP_BYTE_SWAPB	Display Bus Port B Byte Swap Control 0: Normal 1: B Port R/B Channel Byte Swap	
2	DP_BYTE_SWAPA	Display Bus Port A Byte Swap Control 0: Normal 1: A Port R/B Channel Byte Swap	
1	DP_BIT_SWAPB	Display Bus Port B Bit Swap Control 0: Normal 1: B Port Bit Swap	
0	DP_BIT_SWAPA	Display Bus Port A Bit Swap Control 0: Normal 1: Port A Bit Swap (RGB bit7~bit0 in 8 bit Mode, bit5~bit0 in 6 bit Mode)	

Default: XXX0 0000B

Display Background Color Control

0x16B	Display Background Color - Red		R/W
Bits	Name	Description	
7-0	DP_BG_R [7:0]	Display Background Window Red Color.	

Default: 0000 0000B

0x16C	Display Background Color - Green		R/W

Bits	Name	Description
7-0	DP_BG_G [7:0]	Display Background Window Green Color.

Default: 0000 0000B

0x16D	Display Background Color - Blue	R/W

Bits	Name	Description
7-0	DP_BG_B [7:0]	Display Background Window Blue Color.

Default: 0000 0000B

Graphic Display Active Window Control

0x16E	Graphic Display Window Control	R/W

Bits	Name	Description
7	VD_EN	Video Display Window Enable 0 = Disable 1 = Enable
6	GD_PRIO	When Graphic Display and Video Display are both enabled, the priority decides which one has higher priority to display for image overlap area. 0 = Graphic 1 = Video
5	GD_FRM_INV	Select the frame signal polarity to display for alternate sampling mode 0 = Normal 1 = Invert
4	GD_DEALT_SP	Spatial de-alternating mode enable 0 = Disable 1 = Enable
3	GD_DEALT	Display de-alternating function enable 0 = Disable 1 = Enable
2-1	GD_FLD [1:0]	Select the field to display for interlaced graphic input 00 = Display both odd and even field mode 01 = Display only odd field mode 10 = Display only even field mode 11 = Spatial Interpolation mode
0	GD_EN	Graphic Display Window Enable 0 = Disable 1 = Enable

Default: X000 0110B

0x16F	Graphic Display Active Window Vertical Begin –lo	R/W

Bits	Name	Description
7-0	GDV_ACT_BEG [7:0]	Graphic Display Active Window Vertical Begin. GDV_ACT_BEG indicates how many lines to wait after DVSYNC leading edge before starting graphic image display. GDV_BG_BEG =3, means waiting 3 lines to begin display.

Default: 0000 0000B

0x170	Graphic Display Active Window Vertical Begin –hi	R/W

Bits	Name	Description
2-0	GDV_ACT_BEG [10:8]	MSB of GDV_ACT_BEG

Default: XXXX X000B

0x171		Graphic Display Active Window Vertical Length –lo	R/W
Bits	Name	Description	
7-0	GDV_ACT_LEN [7:0]	Graphic Display Active Window Vertical Length. GDV_ACT_LEN indicates how many lines to display. GDV_ACT_LEN =3, means displaying 3 lines.	

Default: 0000 0000B

0x172		Graphic Display Active Window Vertical Length –hi	R/W
Bits	Name	Description	
2-0	GDV_ACT_LEN [10:8]	MSB of GDV_ACT_LEN	

Default: XXXX X000B

0x173		Graphic Display Active Window Horizontal Begin –lo	R/W
Bits	Name	Description	
7-0	GDH_ACT_BEG [7:0]	Graphic Display Active Window Horizontal Begin. GDH_ACT_BEG indicates how many pixels to wait after DHSYNC leading edge before starting graphic image display. GDH_ACT_BEG =3, means waiting 3 pixels to begin display.	

Default: 0000 0000B

0x174		Graphic Display Active Window Horizontal Begin –hi	R/W
Bits	Name	Description	
3-0	GDH_ACT_BEG [11:8]	MSB of GDH_ACT_BEG	

Default: XXXX 0000B

0x175		Graphic Display Active Window Horizontal Width –lo	R/W
Bits	Name	Description	
7-0	GDH_ACT_WID [7:0]	Graphic Display Active Window Horizontal Width. GDH_ACT_WID indicates how many pixels to display. GDH_ACT_WID =3, means displaying 3pixels.	

Default: 0000 0000B

0x176		Graphic Display Active Window Horizontal Width –hi	R/W
Bits	Name	Description	
3-0	GDH_ACT_WID [11:8]	MSB of GDH_ACT_WID	

Default: XXXX 0000B

0x177		Reserved	R
Bits	Name	Description	
7-0	LOCK_RD_H [7:0]	Lock H position read back low byte	

0x178		Reserved	R
Bits	Name	Description	
7-4	LOCK_RD_V [3:0]	Lock V position read back	

3-0	LOCK_RD_H [11:8]	Lock H position read back high byte

Free Run Htotal Control

0x179		Free Run Horizontal Total –lo	R/W
Bits	Name	Description	
7-0	FRH_TOTAL [7:0]	Free Run Horizontal Total Pixels. This register is used when MUTE_FR_EN = "1" (Reg. 0x159[5]). DH_TOTAL = 3 means there are 4 total pixels.	

Default: 0000 0000B

0x17A		Free Run Horizontal Total –hi	R/W
Bits	Name	Description	
3-0	FRH_TOTAL [11:8]	MSB of DH_TOTAL	

Default: XXXX 0000B

0x17B~0x181		Reserved	R/W
Bits	Name	Description	
7-0			

Default: 0000 0000B

Auto Control H-total Read Back

0x182		Reserved for Scaler	R
Bits	Name	Description	
7-0			

0x183		Reserved for Scaler	R
Bits	Name	Description	
3-0			

Residual Display HSYNC Control

0x184		Reserved for Scaler	R
Bits	Name	Description	
7-0			

0x185		Reserved for Scaler	R
Bits	Name	Description	
3-0			

0x186		Reserved for Scaler	R/W
Bits	Name	Description	
4			
3-2			
1			
0			

Default: XXX0 0000B

0x187		Reserved	R/W
Bits	Name	Description	

Default: 0000 0000B

0x188		VCR Control	R/W
Bits	Name	Description	
4	SC_MUTE_DIS	Scaler mute disable	
3-1			
0	VCR_EN	VCR input mode enable control 0 = Disable 1 = Enable	

Default: 0000 0000B

0x189		Reserved for Scaler	R/W
Bits	Name	Description	
7-0			

Default: 0000 0000B

0x18A		Reserved for Scaler	R/W
Bits	Name	Description	
3-0			

Default: XXXX 0000B

0x18B		Reserved for Scaler	R/W
Bits	Name	Description	
7-0			

Default: 0000 0000B

0x18C		Reserved for Scaler	R/W
Bits	Name	Description	
3-0			

Default: XXXX 0000B

0x18D		Residual DHS Average Increment	R/W
Bits	Name	Description	
5			
4	DHS_H_PORCH_SEL	Residual Display HSYNC Area Select 0 = Front Porch 1 = Back Porch	
3-2	DHS_TOTAL_SELECT [1:0]	Force Htotal control 00 = default auto Htotal 01 = force odd Htotal 10 = force even Htotal	

1-0	DHS_DIST_LEN [1:0]	When DHS_DIST = 10, this register indicates the increment value for average. 00 = 1-pixel 01 = 2-pixel 10 = 3-pixel 11 = 4-pixel

Default: XXX0 0000B

FIFO Over/Under-flow Interrupt

0x18E	FIFO Interrupt Flag		R
Bits	Name	Description	
1	INT_FFOV	FIFO over-flow interrupt flag	
0	INT_FFUN	FIFO under-flow interrupt flag	

0x18E	FIFO Interrupt Flag Clear		W
Bits	Name	Description	
1	CLR_FFOV	Writing '1' will clear INT_FFOV flag	
0	CLR_FFUN	Writing '1' will clear INT_FFUN flag	

Default: XXXX XX00B

0x18F	FIFO Interrupt Enable		R/W
Bits	Name	Description	
1	INT_FFOV_EN	FIFO over-flow interrupt enable	
0	INT_FFUN_EN	FIFO under-flow interrupt enable	

Default: XXXX XX00B

0x190	FIFO Control 1		R/W
Bits	Name	Description	
7-5			
4	FIFO_CLK_SWP	FIFO reference clock switch point 0 = End of the input active 1 = End of the output active	
3			
2	GR_VD_CLK_POL	0 = Normal 1 = Inverted	
1	GR_UP_CLK_POL	0 = Normal 1 = Inverted	
0	GR_BK_CLK_POL	0 = Normal 1 = Inverted	

Default: 0000 0000B

0x191	FIFO Control 2		R/W
Bits	Name	Description	
7	BP_VI	Bypass the VI data and power down the clock	
6	BP_HI	Bypass the HI data and power down the clock	
5	BP_SRGB	Bypass the SRGB data and power down the clock	
4	BP_VC	Bypass the VC data and power down the clock	

3	BP_HC	Bypass the HC data and power down the clock
2	GR_AUTO_CLK	FIFO reference clock control auto select enable 0 = Disable 1 = Enable
1-0	GR_FIFO_CLK_SEL [1:0]	FIFO reference clock control source select 00 = Graphic clock 01 = Video clock 10 = 11 =

Default: 0000 0100B

0x192	Reserved for Scaler		R
Bits	Name	Description	
7-0			

0x193	Reserved for Scaler		R
Bits	Name	Description	
7-4		Reserved	
3-0			

0x194	Reserved for Scaler		R
Bits	Name	Description	
7-0			

0x195	Reserved for Scaler		R
Bits	Name	Description	
7-4		Reserved	
3-0			

9.25. Sync Processor

♦ H/V sync frequency counter & polarity detection
♦ H/V sync frequency change detection
♦ Composite/separate auto-switch
♦ Interlaced/progressive input detection
♦ Programmable free-run H/V frequency
♦ Status change interrupt

Graphic Sync Processor Control

0x196	Graphic SYNC Processor Control 1	R/W
Bits	Name	Description
7	DVI_SYNC_SEL	Select the SYNC input source when DVI interface is enabled. 0 = From DVI DE signal 1 = From DVI HS/VS signal
6	GI_ADCHS_INV	Invert the ADC_HS polarity 0 = Normal 1 = Invert

5-4	GI_HS_SRC [1:0]	Select the HSYNC input source to sync processor and core logic. 00 = ADC_HS -> sync processor and core logic 01 = RAW_HS -> sync processor and core logic 10 = RAW_HS -> sync processor and ADC_HS -> core logic 11 = SOG_HS-> sync processor and core logic
3-2	GI_VCNT_BIT [1:0]	Select the bit number of GI_VCNT. 00 = 11-bit. Overflow freq = 27.32Hz 01 = 12-bit. Overflow freq = 13.66Hz 1X = 13-bit. Overflow freq = 6.83Hz
1-0	GI_SYNC_TYPE [1:0]	Graphic sync type select. 00 = Separate SYNC 01 = Composite SYNC 1X = Auto detection and switch

Default: 00010110B

0x197	Graphic SYNC Processor Control 2		R/W
Bits	Name	Description	
7	COAST_EN	COAST output enable for ADCPLL free run 0 = Disable 1 = Enable	
6	SYNC_OUT_SEL [0]	Internal SYNC signal selection	
5	GI_VRUN_EN	VSYNC output free run enable 0 = Disable 1 = Enable	
4	GI_HRUN_EN	HSYNC output free run enable 0 = Disable 1 = Enable	
3	GI_VSO_POL	VSYNC output polarity control 0 = Active low 1 = Active high	
2	GI_HSO_POL	HSYNC output polarity control 0 = Active low 1 = Active high	
1	GI_VSO_EN	VSYNC output enable 0 = Disable 1 = Enable	
0	GI_HSO_EN	HSYNC output enable 0 = Disable 1 = Enable	

Default: 1000 1111B

Interlace Detector Control

0x198	Graphic Field Decision Window	R/W
Bits	Name	Description
7-4	GI_FLD_WINEDN [3:0]	Define the end position of graphic field decision window.
3-0	GI_FLD_WINBEG [3:0]	The G_HS period is divided into 16 segments; a field decision window is defined by GI_FLD_WINBEG and GI_FLD_WINEND. GI_FLD_WINBEG defines the window begin position, and GI_FLD_WINEND defines the end position. If the G_VS reference edge locates inside the window, it means

		ODD field.

Default: 0100 1100B

0x199	Graphic SYNC Processor Control 3	R/W
Bits	Name	Description
6	SYNC_OUT_SEL [1]	Internal SYNC signal selection 0 = Disable 1 = Enable
5	HSYNC_CNT_MOD	Hsync period counter measurement mode. 0 = Counter mode 1 = Time mode
4-2		Reserved
1	GI_FLD_EDGE	Select the reference edge of VSYNC in Graphic Field Detector 0 = Leading edge 1 = Trailing edge
0	GI_FLD_INV	Invert the polarity of Graphic Field Detector output signal 0 = Normal 1 = Invert

Default: X00X XX00B

Sync Status

0x19A	Graphic Sync Processor Status	R
Bits	Name	Description
7	GI_VCNT_OV	GI_VCNT overflow flag 0 = Non-overflow 1 = Overflow
6	GI_HCNT_OV	GI_HCNT overflow flag 0 = Non-overflow 1 = Overflow
5	GI_CSPRE	Composite SYNC present flag 0 = Non-present 1 = Present
4	GI_VPRE	VSYNC present flag 0 = Non-present 1 = Present
3	GI_HPRE	HSYNC present flag 0 = Non-present 1 = Present
2	GI_INTE	Interlace input detected flag 0 = Progressive input 1 = Interlaced input
1	GI_VPOL	VSYNC polarity 0 = Active low 1 = Active high
0	GI_HPOL	HSYNC polarity 0 = Active low 1 = Active high
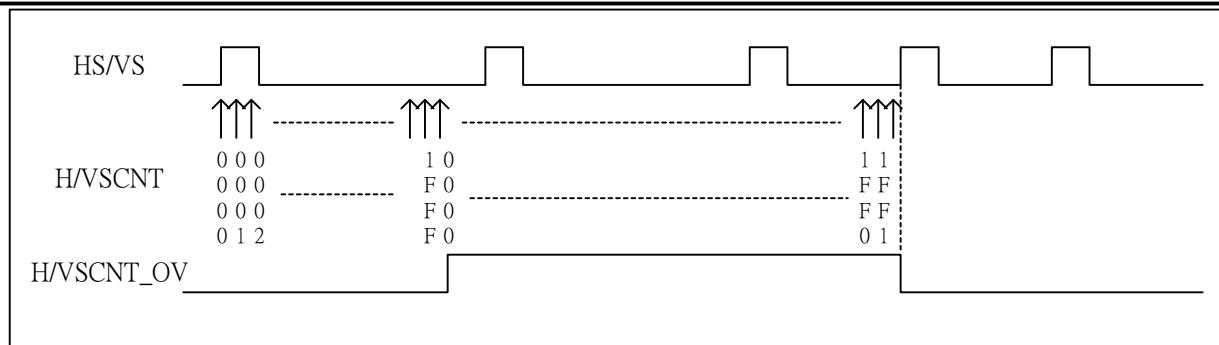
Figure 9.25-1

H/V Sync Counter

0x19B	Graphic HSYNC Counter -lo	R
Bits	Name	Description
7-0	GI_HCNT [7:0]	Hsync period counter. GI_HCNT is the number of clock (=REFCLK/4) in the period of 32x HSYNC. Hfreq = (REFCLK x 32)/(4 x GI_HCNT) Hz

0x19C	Graphic HSYNC Counter -hi	R
Bits	Name	Description
4-0	GI_HCNT [12:8]	MSB of GI_HCNT

0x19D	Graphic VSYNC Counter -lo	R
Bits	Name	Description
7-0	GI_VCNT [7:0]	Vsync period counter. GI_VCNT is a 12-bit counter; counter value is the number of clock (=REFCLK/256) between two VSYNC pulses. Vfreq = REFCLK/(256 x GI_VCNT)

0x19E	Graphic VSYNC Counter -hi	R
Bits	Name	Description
4-0	GI_VCNT [12:8]	MSB of GI_VCNT.

H/V Free Run Divider

0x19F	HSO Free Run Divider -lo	R/W
Bits	Name	Description
7-0	HFREE_DIV [7:0]	HSYNC output free-run divider value. HSYNC pulse width = 15x REFCLK Hfreq (free-run) = REFCLK/(HFREE_DIV+1) 0~511

Default: 0010 0111B

0x1A0	HSO Free Run Divider -hi	R/W
Bits	Name	Description
0	HFREE_DIV [8]	MSB of HFREE_DIV

Default: XXXX XXXX1B

0x1A1		VSO Free Run Divider -lo	R/W
Bits	Name	Description	
7-0	VFREE_DIV [7:0]	VSYNC output free-run divider value. VSYNC pulse width = 3x HFREE Vfreq (free-run) = Hfreq (free-run)/ (VFREE_DIV+1) 0~2048	

Default: 0010 0110B

0x1A2		VSO Free Run Divider -hi	R/W
Bits	Name	Description	
2-0	VFREE_DIV [10:8]	MSB of VFREE_DIV	

Default: XXXX X011B

H/V Present Threshold

0x1A3		HSYNC Present Low Count Threshold	R/W
Bits	Name	Description	
6-0	HPRE_THR_LO [6:0]	Hsync non-present counter threshold 1 (0H)~127 (7EH) Not-present when Hfreq < REFCLK / (4 x 8192 x HPRE_THR_LO) Hz	

Default: X010 1101B

0x1A4		HSYNC Present High Count Threshold	R/W
Bits	Name	Description	
6-0	HPRE_THR_HI [6:0]	Hsync present counter threshold 1 (0H)~127 (7EH) Present when Hfreq > REFCLK / (4 x 8x HPRE_THR_HI) Hz	

Default: X010 1100B

0x1A5		VSYNC Present Low Count Threshold	R/W
Bits	Name	Description	
6-0	VPRE_THR_LO [6:0]	Vsync non-present counter threshold 1 (0H)~127 (7EH) Not-present when Vfreq < REFCLK / (4 x 8192 x VPRE_THR_LO) Hz	

Default: X010 1100B

0x1A6		VSYNC Present High Count Threshold	R/W
Bits	Name	Description	
6-0	VPRE_THR_HI [6:0]	Vsync present counter threshold 1 (0H)~127 (7EH) Present when Vfreq > REFCLK / (4 x 2048x VPRE_THR_HI) Hz	

Default: X010 1100B

H/V Frequency Change Threshold

0x1A7		HSYNC Freq Change Threshold	R/W
Bits	Name	Description	
7-0	HCNT_THR [7:0]	HSYNC counter value change threshold for mode change detection. 1~256	

Default: 0000 0000B

0x1A8		VSYNC Freq Change Threshold	R/W

Bits	Name	Description
7-5	H_CHANG_CNT	The INT_HFREQ will occur if the times out of HSYNC frequency change time are more than CHANG_CNT setting. 000~111: 1, 4, 8, ~ 28 times
4-0	VCNT_THR [4:0]	VSYNC counter value change threshold for mode change detection. 1~32

Default: 0000 0000B

Interrupt Control

0x1A9		SYNC Interrupt Enable 1	R/W

Bits	Name	Description
7	INT_INV	Invert the polarity of IRQn output signal 0 = Normal 1 = Invert
5	INT_VFREQ_EN	VSYNC frequency change interrupt enable 0 = Disable 1 = Enable
4	INT_HFREQ_EN	HSYNC frequency change interrupt enable 0 = Disable 1 = Enable
3	INT_VPOL_EN	VSYNC polarity change interrupt enable 0 = Disable 1 = Enable
2	INT_HPOL_EN	HSYNC polarity change interrupt enable 0 = Disable 1 = Enable
1	INT_VEDGE_EN	VSYNC rising edge occur interrupt enable 0 = Disable 1 = Enable
0	INT_HEDGE_EN	HSYNC rising edge occur interrupt enable 0 = Disable 1 = Enable

Default: 0000 0000B

0x1AA		SYNC Interrupt Enable 2	R/W

Bits	Name	Description
4	INT_DVIPRE_EN	DVI SYNC present or non-present interrupt enable 0 = Disable 1 = Enable
3	INT_ISPRE_EN	Interlaced SYNC present or non-present interrupt enable 0 = Disable 1 = Enable
2	INT_CSPRE_EN	Composite SYNC present or non-present interrupt enable 0 = Disable 1 = Enable
1	INT_VPRE_EN	VSYNC present or non-present interrupt enable 0 = Disable 1 = Enable
0	INT_HPRE_EN	HSYNC present or non-present interrupt enable 0 = Disable 1 = Enable

Default: XXX0 0000B

0x1AB		SYNC Interrupt Flag 1	R
Bits	Name	Description	
5	INT_VFREQ	VSYNC frequency change interrupt	
4	INT_HFREQ	HSYNC frequency change interrupt	
3	INT_VPOL	VSYNC polarity change interrupt	
2	INT_HPOL	HSYNC polarity change interrupt	
1	INT_VEDGE	VSYNC rising edge occur interrupt	
0	INT_HEDGE	HSYNC rising edge occur interrupt	

Default: 0000 0000B

0x1AC		SYNC Interrupt Flag 2	R
Bits	Name	Description	
4	INT_DVIPRE	DVI SYNC present or non-present interrupt	
3	INT_ISPRE	Interlaced SYNC present or non-present interrupt	
2	INT_CSPRE	Composite SYNC present or non-present interrupt	
1	INT_VPRE	VSYNC present or non-present interrupt	
0	INT_HPRE	HSYNC present or non-present interrupt	

Default: XXX0 0000B

0x1AB		SYNC Interrupt Flag 1 Clear	W
Bits	Name	Description	
5	CLR_VFREQ	Writing '1' will clear INT_VFREQ flag	
4	CLR_HFREQ	Writing '1' will clear INT_HFREQ flag	
3	CLR_VPOL	Writing '1' will clear INT_VPOL flag	
2	CLR_HPOL	Writing '1' will clear INT_HPOL flag	
1	CLR_VEDGE	Writing '1' will clear INT_VEDGE flag	
0	CLR_HEDGE	Writing '1' will clear INT_HEDGE flag	

Default: 0000 0000B

0x1AC		SYNC Interrupt Flag 2 Clear	W
Bits	Name	Description	
4	CLR_DVIPRE	Writing '1' will clear INT_DVIPRE flag	
3	CLR_ISPRE	Writing '1' will clear INT_ISPRE flag	
2	CLR_CSPRE	Writing '1' will clear INT_CSPRE flag	
1	CLR_VPRE	Writing '1' will clear INT_VPRE flag	
0	CLR_HPRE	Writing '1' will clear INT_HPRE flag	

Default: XXX0 0000B

0x1AD		DVI Sync Status	R
Bits	Name	Description	
2	DVI_SQ	DVI signal quality 0 = lower than threshold 1 = higher than threshold	
1	DVI_DEPOL	DVI DE polarity. (Read Only) 0 = Active low 1 = Active high	

| 0 | DVI_SCDT | DVI Sync Detect. (Read Only)
0 = When DE is inactively, indicating the link is down
1 = When DE is actively toggling indicating that the link is alive.
The SCDT output itself, however, remains in the active mode at all times. |

Video Sync Processor Control

0x1AE		Video Sync Processor Status	R
Bits	Name	Description	
2	VI_INTE	Interlace input detected flag 0 = Progressive input 1 = Interlaced input	
1	VI_VPOL	VSYNC polarity 0 = Active low 1 = Active high	
0	VI_HPOL	HSYNC polarity 0 = Active low 1 = Active high	

0x1AF		HS Auto De-bouncing	R/W
Bits	Name	Description	
7		Front status	
6		Back status	
5		Manual delay enable	
4		Manual enable	
3		Faster V change interrupt mode enable	
2	DEBOUNCE_EN	De-bounce enable	
1		Faster H change interrupt mode enable	
0		Composite H insertion mode	

Default: 0100 1100B

0x1B0		Field Polarity Control	R/W
Bits	Name	Description	
1	VI_FLD_EDGE	Select the reference edge of VSYNC in Video Field Detector 0 = Leading edge 1 = Trailing edge	
0	VI_FLD_INV	Invert the polarity of Video Field Detector output signal or external EXFLD input signal. 0 = Normal 1 = Invert	

Default: XXXX XX00B

0x1B1		Hsync Pulse width counter	R/W
Bits	Name	Description	
7-0	GI_HS_WID [7:0]	Hsync pulse width counter. GI_HS_WID is the number of REFCLK in the period of HSYNC. Hpswid = (1/REFCLK x GI_HS_WID)	

Default: 0000 0000B

0x1B2		Vsync Pulse width counter	R/W

Bits	Name	Description
7-0	GI_VS_WID [7:0]	Vsync pulse width counter. GI_VS_WID is the number of clock in the period of HSYNC.

Default: 0000 0000B

0x1B3		R/W

Bits	Name	Description
7-0	PRE_COAST	Sets the number of Hsync periods that coast becomes active prior to Vsync.

Default: 0000 0000B

0x1B4		R/W

Bits	Name	Description
7-0	POS_COAST	Sets the number of Hsync periods that coast stays active following Vsync.

Default: 0000 0000B

0x1B5	Graphic VTotal Counter-lo	R

Bits	Name	Description
7-0	GI_VTOTAL [7:0]	Vertical total counter. GI_VTOTAL is an 11-bit counter, counter value is the number of Hsync between two VSYNC pulses.

Default: 0000 0000B

0x1B6	Graphic VTotal Counter-hi	R

Bits	Name	Description
2-0	GI_VTOTAL [10:8]	MSB of GI_VTOTAL

Default: 0000 0000B

0x1B7	Reserved	R/W

Bits	Name	Description

Default: 0000 0000B

9.26. LVDS Output Control

0x1B8	LVDS Output Control	R/W

Bits	Name	Description
7	LVDS_POL_SWAP	LVDS Channel Polarity Swap (Positive/Negative) 0 = Normal 1 = Enable
6	LVDS_CH_SWAP	LVDS Channel Swap 0 = Normal 1 = Enable, When enable, T0/T3 swap, TCLK1/T1 swap, T4/T7 swap, TCLK2/T5 swap
5-3	LVDS_LEVEL [2:0]	Fine tune LVDS output differential voltage 000: Standard output 200 mVp-p 001: Output 250 mVp-p 010: Output 300 mVp-p 011: Output 450 mVp-p 100~111: reserved

Bits	Name	Description
2-1	LVDS_ICO [1:0]	Charge pump current 00 : 100uA 01 : 200uA 10 : 400uA 11 : 800uA
0	LVDS_RFB	Data strobe edge selection 0 = falling edge strobe 1 = rising edge strobe

Default: 0000 0000B

0x1B9	Display Output Interface Control		R/W
Bits	Name	Description	
7-6			
5-2		Reserved	
1	DOS_SEL	Display output interface selection when timing controller disable 0 = LVDS 1 = Reseved	
0	TCON_EN	Timing controller enable 0 = Disable 1 = Enable	

Default: 0000 0000B

0x1BA~1BB		R/W
Bits	Name	Description

Default: 0000 0000B

9.27. Auto offset Control

0x1BC	Auto offset Control		R/W
Bits	Name	Description	
7	AO_LINE_MODE_RDY	Auto offset line mode ready, When detection is finished, this bit is set to "1"	
6	AO_LINE_MODE	Auto offset line mode enable 0 = Disable 1 = Enable	
5:4	AO_MODE[1:0]		
3	AO_POL		
2	AO_DIR	Reserved	
1	AO_ACC_EN	Auto offset 0 = Disable 1 = Enable	
0	AO_EN	Auto offset enable 0 = Disable 1 = Enable	

Default: 0000 0000B

0x1BD	Auto offset target value of Red channel		R/W
Bits	Name	Description	
7-0	AO_RVALUE		

Default: 0000 0000B

0x1BE	Auto offset target value of Green channel		R/W
Bits	Name	Description	
7-0	AO_GVALUE		

Default: 0000 0000B

0x1BF	Auto offset target value of Blue channel		R/W
Bits	Name	Description	
7-0	AO_RVALUE		

Default: 0000 0000B

0x1C0	Auto offset adjust value – Red channel		R/W
Bits	Name	Description	
7-0	AO_ADJ_RVALUE		

Default: 0000 0000B

0x1C1	Auto offset adjust value – Green channel		R/W
Bits	Name	Description	
7-0	AO_ADJ_GVALUE		

Default: 0000 0000B

0x1C2	Auto offset adjust value – Blue channel		R/W
Bits	Name	Description	
7-0	AO_ADJ_RVALUE		

Default: 0000 0000B

0x1C3	Auto offset mid filte read back – Red channel		R/W
Bits	Name	Description	
7-0	AO_MID_RVALUE		

Default: 0000 0000B

0x1C4	Auto offset mid value read back – Green channel		R/W
Bits	Name	Description	
7-0	AO_MID_GVALUE		

Default: 0000 0000B

0x1C5	Auto offset mid value read back – Blue channel		R/W
Bits	Name	Description	
7-0	AO_MID_RVALUE		

Default: 0000 0000B

0x1C6	Scaler Test Register		R/W
Bits	Name	Description	

Default: 0000 0000B

9.28. Data Tracking Control

0x1C7	Data Tracking Control		R/W
Bits	Name	Description	
7	DIT_TRACK4_EN	Dithering data output tracking enable 0: Disable	

Bits	Name	Description
		1: Enable
6	GAM_TRACK3_EN	Gamma data output tracking enable 0: Disable 1: Enable
5	OSD_TRACK2_EN	OSD data output tracking enable 0: Disable 1: Enable
4	GO_TRACK1_EN	Gain/Offset data output tracking enable 0: Disable 1: Enable
3-1		Reserved
0	DATA_TRACK1_EN	Scaler tracking enable One 0: Disable 1: Enable

Default: 0000 0000B

0x1C8~1CB	Data Tracking Mask	R/W
Bits	Name	Description
7-0	DATA_MASK [7:0]	

Default: 0000 0000B

0x1CC	Asynchronous Random dithering Control	R/W
Bits	Name	Description
7-3		Reserved
2	DP_ARD_EN	Display asynchronous random dithering enable
1	GA_ARD_EN	Gamma asynchronous random dithering enable
0	SRGB_ARD_EN	SRGB asynchronous random dithering enable

Default: 0000 0000B

0x1CD~1CF		R/W
Bits	Name	Description

Default: 0000 0000B

9.29. sRGB Control

0x1D0	sRGB Control	R/W
Bits	Name	Description
7	BF_SRGB_EN	Bright frame sRGB enable
6	SRGB_TBL_SEL	sRGB access select 0: Normal sRGB 1: Bright frame sRGB
5	SRGB_DITH_EN	SRGB dithering enable
4	RANDOM_DITH_EN	Random dithering enable
3	SRGB_FORCE_UPD	Force update sRGB 0: Disable 1: Force update the sRGB Coefficient to H/W
2-1	SRGB_BK_SEL	Select sRGB converting tristimulus values bank 00 = R 01 = G

| 10 = B |
| 11 = Reserved |

0	SRGB_En	sRGB Enable
		0: Disable
		1: Enable

Default: XXXX 1000B

0x1D1		sRGB Transfer Coefficient R Channel – lo	R/W
Bits	Name	Description	
7-0	SRGB_COEF_R [7:0]	sRGB Transfer R channel coefficient LSB -1024 ~ 1023	

Default: 0000 0000B

0x1D2		sRGB Transfer Coefficient R Channel – hi	R/W
Bits	Name	Description	
2-0	SRGB_COEF_R [10:8]	MSB of SRGB_COEF_R	

Default: 0000 0000B

0x1D3		sRGB Transfer Coefficient G Channel – lo	R/W
Bits	Name	Description	
7-0	SRGB_COEF_G [7:0]	sRGB Transfer GIN coefficient LSB -1024 ~ 1023	

Default: 0000 0000B

0x1D4		sRGB Transfer Coefficient G Channel – hi	R/W
Bits	Name	Description	
2-0	SRGB_COEF_G [10:8]	MSB of SRGB_COEF_G	

Default: 0000 0000B

0x1D5		sRGB Transfer Coefficient B Channel – lo	R/W
Bits	Name	Description	
7-0	SRGB_COEF_B [7:0]	sRGB Transfer BIN coefficient LSB -1024 ~ 1023	

Default: 0000 0000B

0x1D6		sRGB Transfer Coefficient B Channel – hi	R/W
Bits	Name	Description	
2-0	SRGB_COEF_B [10:8]	MSB of SRGB_COEF_B	

Default: 0000 0000B

0x1D7		sRGB Offset Coefficient	R/W
Bits	Name	Description	
2-0	SRGB_COEF_OFFSET [7:0]	The offset coefficient of sRGB matrix	

Default: 0000 0000B

0x1D8		sRGB Dithering Control 1	R/W
Bits	Name	Description	

7-6		Reserved
5-4	DITH_10	"10" dithering type
3		
2-0	DITH_01	"01" dithering type

Default: 0000 0000B

0x1D9	sRGB Dithering Control 2	R/W
Bits	Name	Description
3-0	DITH_OPT	

Default: 0000 0000B

0x1DA	Display Random Dithering Control	R/W
Bits	Name	Description
7-6		Reserved
5	MIX_DITH_EN	Display Mix mode Dithering Enable 0: Disable 1: Enable
4	RANDOM_EN	Random dithering mode enable
3-2	STATIC_CNT	Static dithering active period counter
1-0	RANDOM_CNT	Random dithering active period counter

Default: 0000 0000B

0x1DB	Gamma Dithering Control	R/W
Bits	Name	Description
7	RANDOM_EN	2D Random mode enable
6		Reserved
5-4	DITH_10	"10" dithering type
3		Reserved
2-0	DITH_01	"01" dithering type

Default: 0000 0000B

0x1DC	Scaler Misc. Odd Read Back and Control	R
Bits	Name	Description
7-0	MISC_O_RD [7:0]	Misc. odd read back low byte

0x1DD	Scaler Misc. Odd Read Back and Control	R/W
Bits	Name	Description
7	MISC_O_EN	Misc. odd control enable 0 = Disable 1 = Enable
3-0	MISC_O_RD [11:8]	Misc. odd read back low byte

0x1DE	Scaler Misc. Even Read Back and Control	R
Bits	Name	Description
7-0	MISC_E_RD [7:0]	Misc. even read back low byte

0x1DF	Scaler Misc. Even Read Back and Control		R/W
Bits	Name	Description	
7	MISC_E_EN	Misc. even control enable 0 = Disable 1 = Enable	
3-0	MISC_E_RD [11:8]	Misc. even read back low byte	

9.30. Test Mode

0x1E0H		Reserved	R/W
Bits	Name	Description	
7-0		Reserve	

Default :0000 0000B

0x1E1H		Reserved	R/W
Bits	Name	Description	
7-0		Reserve	

Default :0000 0000B

0x1E2		Test Mode Control 1	R/W
Bits	Name	Description	
7		Reserve	

Default：0000 0000B

0x1E3		Reserved	R/W
Bits	Name	Description	
7		Reserve	
6		Reserve	
5		Reserve	
4		Reserve	
3		Reserve	
2		Reserve	
1		Reserve	
0		Reserve	

Default：XX00 0X00B

0x1E4		Reserved	R/W
Bits	Name	Description	
7		Reserve	
6		Reserve	
5-4		Reserve	
3		Reserve	
2-1		Reserve	
0		Reserve	

Default：0000 0000B

0x1E5		Reserved	R/W
Bits	Name	Description	
7		Reserve	
6		Reserve	
5		Reserve	
4		Reserve	
3		Reserve	
2		Reserve	
1		Reserve	
0		Reserve	

Default：00XX 000B

0x1E6		ADC test mode Control	R/W
Bits	Name	Description	
7		Reserved	
6	SYNC_HS_SEL	Hsync2 selection 1: Hsync from sync process 0: Hsync from SOGI path	
5		Reserved	
4		Reserved	
3-0		Reserved	
0	RSTB	Reset ADC data to low	

Default：X000 XXX1B

0x1E7		Reserved	R/W
Bits	Name	Description	
7-0		Reserve	

Default：0100 XXXXB

0x1E8~1EA		Reserved	R/W
Bits	Name	Description	
7-0		Reserved	

Default：XXXX XXXXB

0x1EB		ADC Comparator Control	R/W
Bits	Name	Description	
7-2		Reserve	
1-0	Icomp[1:0]	ADC comparator current control 00: 100 % 01: 114 % 10: 133 % 11: 80 %	

Default：0000 0000B

0x1EC		ADC Test 1 Control	R/W
Bits	Name	Description	
7-0	Test1[7:0]	Test 1 Control	

Default：0000 0000B

0x1ED		Reserved	R/W
Bits	Name	Description	
7-0		Reserve	

Default：0000 0000B

0x1EE		Reserved	R/W
Bits	Name	Description	
7-0		Reserve	

Default：0000 0000B

0x1EF		Reserved	R/W
Bits	Name	Description	
7	HPLL_CK_TEST	HPLL clock reconstructed and phase-aligned by TMDS PLL	
6-0		Reserved	

Default：0000 0000B

0x1F0		Reserved	R/W
Bits	Name	Description	
7-0		Reserve	

Default：0000 0000B

0x1F1		Reserved	R/W
Bits	Name	Description	
7-6		Reserved	
5-4		Reserve	
3-2		Reserve	
1-0		Reserve	

Default：XX11 1111B

0x1F2		Reserved	R/W
Bits	Name	Description	
7-0		Reserve	

Default：0000 000xB

0x1F3		Reserved	R/W
Bits	Name	Description	
7-2		Reserved	
1		Reserve	
0		Reserve	

Default：0000 0011B

0x1F4		Reserved	R/W
Bits	Name	Description	
7-0		Reserve	

Default：1000 0010B

0x1F5		LVDS control 1	R/W
Bits	Name	Description	
7	Reg_125L		
6	Reg_125R		
5	EN_125		
4	PULL_LOW	Display output power down buffer control 0: Tri-state output 1: pull low output	
3	TEST		
2-0	T_S2 [2:0]		

Default：0000 0000B

0x1F6		LVDS control 2	R/W
Bits	Name	Description	
7-6	T_MON [1:0]		
5-3	T_S0 [2:0]		
2-0	T_S1 [2:0]		

Default：0000 0000B

0x1F7		LVDS control 3	R/W
Bits	Name	Description	
7	PD_LV1	LV1 power control 0: Power down 1: Power up	
6	PD_LV2	LV2 power control 0: Power down 1: Power up	
5-0		Reserve	

Default：0000 0000B

0x1F8		Reserved	R/W
Bits	Name	Description	
7-0		Reserve	

Default：0000 0000B

0x1F9		Reserved	R
Bits	Name	Description	
7-0		Reserve	

Default：0000 0000B

0x1FC		Reserved	R
Bits	Name	Description	
7-5		Reserved	
4		Reserve	
3		Reserve	
2		Reserve	
1		Reserve	
0		Reserve	

Default：XXX0 0000B

0x1FB		LVDS PLL divider control	R
Bits	Name	Description	
7-5		Reserved	
4		Reserve	
3		Reserve	
2-1	LVDS_PLL_DIV [1:0]	LVDS PLL frequency range 00: 80~180MHz 01: 40~80MHz	

		10: 20~40MHz
		11: 10~20MHz
0	LVDS_CLK_2X	Reserve

Default：XXXX X000B

0x1FF		Accessing Register Page Enable	R/W
Bits	Name	Description	
7-2		Reserve	
1-0	REG_PAGE_SEL	Register Page Enable	
		00: Enable register Page0.	
		01: Enable register Page1.	
		10: Enable register Page2.	
		11: Reserved	

Default: XXXX XX00B

9.31. Timing Controller control

0x200 ~ 0x206: Output Format Control

0x200		Output Format Control 1	R/W
Bits	Name	Description	
7	POL_INV	Polarity indication POL output polarity invert	
		0: Normal, POL output "High" when RGB data is inverted	
		1: Inverted, POL output "Low" when RGB data is inverted	
6	POL_EN	Polarity indication output enabled.	
		0: Disable	
		1: Enable	
5			
4	EXTRA_SP_HTOTAL		
3	SP_GPO_STUCK		
2-0	EXTRA_SP_CNT	Extra one start pulse count (0~7)	

Default: 0000 0000B

0x201		Output Format Control 2	R/W
Bits	Name	Description	
7	WHITE_DATA	0:No white data. RA, GA, BA=RB, GB, BB=24'000000, when vertical blanking	
		1:Enable white data. RA, GA, BA=RB, GB, BB=24'FFFFFF, when vertical blanking	
6	OUTPUT_POL_CRTL	0: POL output disable (internal pull low)	
		1: POL normal output	
5	OUTPUT_SP_CRTL	0: SP output disable (internal pull low)	
		1: SP normal output	
4	SPA_SPB_INV	Star pulse output polarity invert	
		0:Normal, (default is active high)	
		1:Inverted	
3	SP_RAISE_MODE	SP raise mode (1: posedge 0:negedge)	
2-0	SP_DUR[2:0]	Fine tune SPA, SPB pulse width with pixel clock count	

Default: 0000 0000B

0x202		Output Format Control 3	R/W
Bits	Name	Description	

Free Datasheet http://www.datasheet4u.com/

| 7-4 | SPB_OFFSET[3:0] | Data port B start pulse offset, active n clock before first RGB data |
| 3-0 | SPA_OFFSET[3:0] | Data port A start pulse offset, active n clock before first RGB data |

Default: 0000 0000B

0x203	Output Format Control 4		R/W
Bits	Name	Description	
7	RSDS_8BIT_EN	RSDS 8 bit data output enable when single port 0: Disable 1: Enable	
6		Reserved	
5	CLK_BLANK	0:CLKA, CLKB normal output 1:CLKA, CLKB blank (force to low) when GPO4 = 1	
4		Reserved	
3	CLKB_INV	0:CLKB/RSCLKB normal output 1:CLKB/RSCLKB invert	
2	CLKA_INV	0:CLKA/RSCLKA normal output 1:CLKA/RSCLKA invert	
1	CLKB_EN	0:CLKB/RSCLKB disable 1:CLKB/RSCLKB enable	
0	CLKA_EN	0:CLKA/RSCLKA disable 1:CLKA/RSCLKA enable	

Default: 0X00 0000B

0x204	Output Format Control 5		R/W
Bits	Name	Description	
7	BIT_SWAP_OPT	Bit swap option 0: 6 Bit 1: 8 Bit	
6	EN_MASK_VACT	Enable mask function 0: Disable 1: Enable	
5		Reserve	
4		Reserved	
3	RSDS_SEL	0:TCON output TTL mode 1:TCON output RSDS mode	
2-0	RSDS_LEVEL [2:0]	Fine tune RSDS output differential voltage 000: Standard output 200 mVp-p 001: Output 250 mVp-p 010: Output 300 mVp-p 011: Output 350 mVp-p 100: Output 400 mVp-p 101~111: Reserved	

Default: XXX0 0000B

0x205	Output Format Control 6		R/W
Bits	Name	Description	
7	RSDSB_POL	0: RSDS port B polarity normal operate 1: RSDS port B polarity inversion operate	
6	RSDSA_POL	0: RSDS port A polarity normal operate 1: RSDS port A polarity inversion operate	
5	PA_PB_SWAP	Port A and Port B data swap	

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		0: Normal output 1: RA, GA, and BA Swap with RB, GB, and BB. RSR_A, RSG_A, RSB_A swap with RSR_B, RSG_B, RSB_B
4	GA_GB_SWAP	0: Normal output 1: GA swap with GB RSG_A swap with RSG_B
3	PB_BYTE_SWAP	0: Normal output 1: RB, GB, BB change into BB, GB, RB RSR_B, RSG_B, RSB_B change into RSB_B, RSG_B, RSR_B
2	PB_BIT_SWAP	0: Normal output 1: RB[0:7], GB[0:7], BB[0:7] change into RB[7:0], GB [7:0], BB[7:0]; RSR_B[0:3], RSG_B[0:3], RSB_B[0:3] Change into RSR_B[3:0], RSG_B[3:0], RSB_B[3:0]
1	PA_BYTE_SWAP	0: Normal output 1: RA, GA, BA change into BA, GA, RA RSR_A, RSG_A, RSB_A change into RSB_A, RSG_A, RSR_A
0	PA_BIT_SWAP	0: Normal output 1: RA[0:7],GA[0:7],BA[0:7] change into RA[7:0], GA[7:0], BA[7:0]. RSR_A[0:3], RSG_A[0:3], RSB_A[0:3] Change into RSR_A[3:0], RSG_A[3:0], RSB_A[3:0]

Default: 0000 0000B

0x206	Output Format Control 7		R/W
Bits	Name	Description	
7-5		Reserved	
4-1	MODE1_GPO_SEL	GPO0~GPO8 select when Mode1 enable (Refer to 0x2□A)	
0	MODE1_HSTAER_HEND_SEL	0:HSTAR (Refer to 0x2□A) 1:HEND	

Default: 0000 0000B

0x207	Output Format Control 8		R/W
Bits	Name	Description	
7-4	RSDSB_CLKA_DELAY [4:0]	CLK / RSDS port B clock delay time. 0.5~16ns(0.5ns/step)	
3-0	RSDSA_CLKB_DELAY [4:0]	CLK / RSDS port A clock delay time. 0.5~16ns(0.5ns/step)	

Default: 0000 0000B

0x208	Output Format Control 9		R/W
Bits	Name	Description	
7			
6	GPO_DIV_MODE	0: Normal count 1: Divide clock count	
5	GPO_TRIGGER_EDGE	GPO trigger edge 0: posedge 1: negedge	
4	GPO_EN	GPO output enable 0: GPO disable (internal pull low) 1: GPO enable	
3	GPO_SLEW_RATE	0: Fast 1: Slow	

2-0	GPO_DRV_STRENGTH [2:0]	GPO driver strength
		000: 2mA 100: 10mA
		001: 4mA 101: 12mA
		010: 6mA 110: 14mA
		011: 8mA 111: 16mA

Default: 0000 0000B

0x209	Output Format Control 10	R/W
Bits	Name	Description
7-0	LINE_BUFFER_LSB [7:0]	Line buffer size LSB

Default: 0000 0000B

0x20A	Output Format Control 11	R/W
Bits	Name	Description
7	TCON_PD	TCON power down control 0: Power up 1: Power down
6	DE_MASK_EN	0: Disable 1: Enable
5	DE_MODE	0: DE mode 1: Sync mode
4		
1-0	LINE_BUFFER_MSB [9:8]	Line buffer size MSB This number define how many contiguous pixels are output, this mode used on dual source driver display at the same time

Default: XXXX XX00B

0x210 ~ 0x299: General Purpose Output Format Control
GPO0 : Reg.FFH = xxxx,xx10, Address = 10H ~ 19H
GPO1 : Reg.FFH = xxxx,xx10, Address = 20H ~ 29H
GPO2 : Reg.FFH = xxxx,xx10, Address = 30H ~ 39H
GPO3 : Reg.FFH = xxxx,xx10, Address = 40H ~ 49H
GPO4 : Reg.FFH = xxxx,xx10, Address = 50H ~ 59H
GPO5 : Reg.FFH = xxxx,xx10, Address = 60H ~ 69H
GPO6 : Reg.FFH = xxxx,xx10, Address = 70H ~ 79H
GPO7 : Reg.FFH = xxxx,xx10, Address = 80H ~ 89H
GPO8 : Reg.FFH = xxxx,xx10, Address = 90H ~ 99H

0x2☐0	Vertical Start - Low Byte	R/W
Bits	Name	Description
7-0	VSTART_LSB	Fine tune GPO pulse start position from vertical scan

Default: 0000 0000B

0x2☐1	Vertical Start - High Byte	R/W
Bits	Name	Description
3-0	VSTART_MSB	Fine tune GPO pulse start position from vertical scan

Default: XXXX 0000B

0x2□2		Vertical End - Low Byte	R/W
Bits	Name	Description	
7-0	VEND_LSB	Fine tune GPO pulse end position from vertical scan	

Default: 0000 0000B

0x2□3		Vertical End - High Byte	R/W
Bits	Name	Description	
3-0	VEND_MSB	Fine tune GPO pulse end position from vertical scan	

Default: XXXX 0000B

0x2□4		Horizontal Start - Low Byte	R/W
Bits	Name	Description	
7-0	HSTART_LSB	Fine tune GPO pulse start position from horizontal scan	

Default: 0000 0000B

0x2□5		Horizontal Start - High Byte	R/W
Bits	Name	Description	
3-0	HSTART_MSB	Fine tune GPO pulse start position from horizontal scan	

Default: XXXX 0000B

0x2□6		Horizontal End - Low Byte	R/W
Bits	Name	Description	
7-0	HEND_LSB	Fine tune GPO pulse end position from horizontal scan	

Default: 0000 0000B

0x2□7		Horizontal End - High Byte	R/W
Bits	Name	Description	
3-0	HEND_MSB	Fine tune GPO pulse end position from horizontal scan	

Default: XXXX 0000B

0x2□8		GPO Output Format Control 1	R/W
Bits	Name	Description	
7-6	GPO_H_DUR	GPO horizontal duration select 00:Horizontal duration in 1 H 01: Horizontal duration in 2 H 10: Horizontal duration in 3 H 11: Horizontal duration in 4 H	
5	HEND_EARLY	0:Hend early capability disable 1:Hend early capability enable	
4	HSTART_EARLY	0:Hstart early capability disable 1:Hstart early capability enable	
3	VEND_EARLY	0:Vend early capability disable 1:Vend early capability enable	
2	VSTART_EARLY	0:Vstart early capability disable 1:Vstart early capability enable	
1	GPO_TOGGLE	0:GPO toggle disable 1:GPO toggle enable	
0	GPO_POL_INV	GPO output signal polarity invert 0: Normal, (default GPO active high)	

		1: Inverted

Default: 0000 0000B

0x2□9		GPO Output Format Control 2	R/W
7	GPO_EN	GPO output enable 0: GPO enable 1: GPO disable (3-state)	
6	DOT_INV_SEL	Dot inversion selection 0: 1-line dot inversion enable 1: 2-line dot inversion enable	
5	RVS_RST_EN	RVS reset enable	
4	GPO_RST_EN	GPO reset enable	
3	GPO_MUTU	GPO mute 0: GPO mute disable 1: GPO mute enable, It depends on the register x8H Do to decide the polarity of each GPO output signal	
2	FAST_MUTE	Fast mute 0:H/W Fast mute disable 1:H/W Fast mute enable, when FAST_MUTE input pin active "high" then GPO will pull low	
1-0	GPO_COMB	00:Select GPO# as programmed 01:GPO#=GPO# "AND " GPO#--1 (reserve for GPO0) 10:GPO#=GPO# "OR" GPO#--1 (reserve for GPO0) 11: GPO#=GPO# "XOR" GPO#--1 (reserve for GPO0)	

Default: 0000 0000B

0x2□A		GPO HEND/ HSTRT Mode 1 control	R/W
Bits	Name	Description	
1	GPO_HEND_MODE1	0:Normal 1:HEND Mode 1 count reset from GPOx HSTAT or HEND (GPOx, refer to 0x206[4:1], HSTART or HEND refere to 0x206[0])	
0	GPO_HSTAR_MODE1	0:Normal 1:HSTAR Mode 1 count reset from GPOx HSTAT or HEND(GPOx, refer to 0x206[4:1], HSTART or HEND refere to 0x206[0])	

Default: XXXX 0000B

Table 1: GPO toggle horizontal duration select

Vertical Start	Vertical End	Horizontal Start	Horizontal End	GPO output
#a	#a	#c	#c	Stuck 1 when output polarity =0 Stuck 0 when output polarity =1
#a	#a	#c	#d (note)	Pulse is generated every line beginning at pixel #c and ending at pixel #d
#a	#b	#c	#c	Pulse begins at line #a, pixel #c and ends at line #b pixel #c
#a	#b	#c	#d	Pulse begins at line #a, pixel #c and ends at line #b pixel #d

Note: Pulse will cross horizontal blanking if d < c

0x2C8	GPO Output Format Control 1	R/W
Bits	Name	Description
7-6	GPO_DOT_INV_DUR	GPO Dot inversion line count selection 00:Horizontal duration in 1 H 01: Horizontal duration in 2 H 10: Horizontal duration in 3 H 11: Horizontal duration in 4 H
5-0		Reserved

Default: 0000 0000B

9.32. Flicker Detect Control

0x2D0	Flicker Detect Control	R/W
Bits	Name	Description
7	CKER_RESULT_LOCK	Flicker detection result lock.
6	FORCE_FLICKE	Force the detected pattern as flicker 0: Normal pattern(disable 2-line dot inversion) 1: Flicker pattern(enable 2-line dot inversion)
5	DE_FLICKER_MODE	De-flicker mode control 0: Manual 1: Auto
4	FRAME_MODE_EN	Frame mode pixel pattern accumulated enable
3	CONTIN_MODE_EN	Continuously detection enable
2	PIXEL_CKER_DET	Pixel pattern are accumulated enable
1	SUB_PIXEL_DET	Sub-pixel pattern are accumulated enable
0	FLICKER_DET_EN	Flicker pattern detection enable 0: Disable 1: Enable

Default: 1011 0110B

0x2D1	Flicker Detect Level Threshold	R/W
Bits	Name	Description
7-0	PIXEL_CKER_THR	Pixel pattern checker level threshold.

Default: 0001 0000B

0x2D2	Flicker Detect Dot Threshold	R/W
Bits	Name	Description
7-0	CKER_DOT_THR	Pixel pattern checker Dot threshold.

Default: 0000 1010B

0x2D2	Flicker Detect Line Threshold	R/W
Bits	Name	Description
7-0	CKER_LINE_THR	Pixel pattern checker line threshold.

Default: 0000 1111B

0x2D4	Frame mode Detection control	R/W
Bits	Name	Description
7-6		Reserved

| 5-4 | RESULT_CH_SEL [1:0] | The Color select of Dot Detection result
00 = R/G/B
01 = R
10 = G
11 = B |
| 3-0 | FRAME_DET_PARAM | Frame mode pixel pattern detection parameter. 1/16 ~16/16 |

Default: 0000 1000B

0x2D5		Dot Detect Result-lo	R
Bits	Name	Description	
7-0	CKER_RESULT [7:0]	The Dot Detection result	

Default: 0000 0000B

0x2D6		Dot Detect Result-mi	R
Bits	Name	Description	
7-0	CKER_RESULT [15:8]	The Dot Detection result	

Default: 0000 0000B

0x2D7		Dot Detect Result-hi	R
Bits	Name	Description	
7-0	CKER_RESULT [23:16]	The Dot Detection result	

Default: 0000 0000B

0x2FF		Accessing Register Page Enable	R/W
Bits	Name	Description	
7-2		Reserve	
1-0	REG_PAGE_SEL	Register Page Enable 00: Enable register Page0. 01: Enable register Page1. 10: Enable register Page2. 11: Reserved	

Default: XXXX XX00B

9.33. High-bandwidth Digital Content Protection System

HDCP Index Port Access Control

See section 9.14 Index Port Access Control

HDCP Control Register Map (MCU I2C side)

ADDRESS	R/W	Register Name	Description
0x300 ~ 0x301 ~ 0x302 ~ 0x303 ~ 0x304	R	BKSV[7:0] BKSV[15:8] BKSV[23:16] BKSV[31:24] BKSV[39:32]	Video receiver KSV. This value must always be available for reading, and may be used to determine that the video receiver is HDCP capable. Valid KSVs contain 20 ones and 20 zeros, a characteristic that must be verified by video transmitter hardware before encryption is enable.
0x305 ~ 0x307	R	RSVD	Reserved All bytes read as 0x00
0x308 ~ 0x309	R	Ri'[7:0] Ri'[15:8]	Link verification response. Updated every 128 th frame. It is recommended that graphics systems protect against errors in the I2C transmission by reading this value when unexpected values are received. This value must be available at all times between updates. R0' must be available a maximum of 100ms after AKSV is received. Subsequent Ri' values must be available a maximum of 128 pixel clocks following the assertion of CTL3
0x30A	R	Pj'	Enhanced Link Verification Response. Updated upon receipt of first video pixel received when frame counter value (j mod 16) == 0. The value is the XOR of the decrypted byte on channel zero of the first video pixel with the least significant byte of Rj. Rj is derived from the output function in the same manner as Ri, but is captured every 16th counted frame (rather than every 128th counted frame).
0x30B~0x30F	R	RSVD	Reserved All bytes read as 0x00
0x310 ~ 0x311 ~ 0x312 ~ 0x313 ~ 0x314	R/W	AKSV[7:0] AKSV[15:8] AKSV[23:16] AKSV[31:24] AKSV[39:32]	HDCP Transmitter KSV. Writes to this multi-byte value are written least significant byte first. The final write to 0x14 triggers the authentication sequence in the HDCP Receiver, and the current *Ainfo* value is copied from the port, takes effect, and the port is reset to the default value of zero.
0x315	W	Ainfo	Bits 7-2: Reserved zeros. Bit 1: ENABLE_1.1_FEATURES. This bit enables the Advance Cipher option. If in DVI mode, it also enables the Enhanced Encryption Status Signaling (EESS) (in HDMI mode, EESS is enabled regardless of this bit setting). This bit resets to default zero when the HDCP Receiver becomes attached or active, or is reset, or the last byte of Aksv is written. A write to the last byte of Aksv copies the port value and causes it to take effect, and then resets the port value to the default value of zero. Thus the options must be explicitly enabled prior to each authentication. Bit 0: Reserved (must be zero).
0x316~0x317	R	RSVD	Reserved All bytes read as 0x00
0x318 ~ 0x319 ~ 0x31A ~ 0x31B ~ 0x31C ~ 0x31D ~	R/W	An[7:0] An[15:8] An[23:16] An[31:24] An[39:32] An[47:40]	Session random number. This multi-byte value must be written by the HDCP Transmitter before the KSV is written.

0x31E ~ 0x31F		An[55:48] An[63:56]	
0x320~0x323	R	V'.H0	H0 part of SHA–1 hash value used in the second part of the authentication protocol for HDCP Repeaters. (NOTE: port 0x20 is the least significant byte of the H0 value, as all ports are little-endian byte order).
0x324~0x327	R	V'.H1	H1 part of SHA-1 hash value V'.
0x328~0x32B	R	V'.H2	H2 part of SHA-1 hash value V'.
0x32C~0x32F	R	V'.H3	H3 part of SHA-1 hash value V'.
0x330~0x333	R	V'.H4	H4 part of SHA-1 hash value V'.
0x334~0x33F	R	RSVD	All bytes read as 0x00
0x340	R	Bcaps	Bit 7: HDMI_RESERVED 　Use of this bit is reserved. HDCP Receivers not capable of supporting HDMI must clear this bit to 0. Bit 6: REPEATER, HDCP Repeater capability. 　When set to one, this HDCP Receiver supports downstream connections as permitted by the Digital Content Protection LLC license. This bit does not change while the HDCP Receiver is active. Bit 5: READY, KSV FIFO ready. 　When set to one, this HDCP Repeater has built the list of attached KSVs and computed the verification value *V'*. This value is always zero during the computation of *V'*. Bit 4: FAST. 　When set to one, this device supports 400 KHz transfers. When zero, 100 KHz is the maximum transfer rate supported. Note that 400KHz transfers are not permitted to any device unless all devices on the I2C bus are capable of 400KHz transfer. The transmitter may not be able to determine if the EDID ROM, present on the HDCP Receiver, is capable of 400KHz operation. This bit does not change while the HDCP Receiver is active. Bits 3-2: Reserved (must be zero). Bit 1: 1.1_FEATURES. 　When set to one, this HDCP Receiver supports Enhanced Encryption Status Signaling (EESS), Advance Cipher, and Enhanced Link Verification options. For the HDMI protocol, Enhanced Encryption Status Signaling (EESS) capability is assumed regardless of this bit setting. This bit does not change while the HDCP Receiver is active. Bit 0: FAST_REAUTHENTICATION. 　When set to 1, the receiver is capable of receiving (unencrypted) video signal during the session re-authentication. All HDMI-capable receivers shall be capable of performing the fast re-authentication even if this bit is not set. This bit does not change while the HDCP Receiver is active. Default: 8'h11
0x341 ~ 0x342	R	Bstatus[7:0] Bstatus[15:8]	This device does not support repeater capability. Bit15 ~ 14: Reserved Bit13: Reserved for future possible zero Bit12: HDMI Mode. When set to one, the HDCP Receiver has transitioned from DVI Mode to HDMI Mode. This has occurred

			because the HDCP Receiver has detected HDMI bus conditions on the link. This bit must not be cleared when the HDCP Transmitter and HDCP Receiver are connected and both are operating in an active HDMI mode. This bit must be cleared upon power-up, reset, unplug or plug of an HDCP Transmitter or anytime that the HDCP Receiver has not seen at least one Data Island within 30 video frames. Bit11: Topology error indicator. When set to one, more than seven levels of video repeater have been cascaded together. Bit10 ~ 8: Three-bit repeater cascade depth. This value gives the number of attached levels through The connection topology. Bit7: Topology error indicator. When set to one, more than 127 downstream devices, or the capacity of the KSV FIFO, are attached. Bit6 ~ 0: Total number of attached downstream devices. Always zero for HDCP Receivers. This count does not include the HDCP Repeater itself, but only downstream devices downstream from the HDCP Repeater. All bytes read as 0x00.
0x343	R	Ri' Frame count	Frame count status for Ri' update Default: 8'h00
0x344	R	Frame Pj'	Pj' value for every frame Default: 8'h00
0x345	R	Frame Ri'(l)	Ri' low byte value for every frame Default: 8'h00
0x346	R	Frame Ri'(h)	Ri' high byte value for evrery frame Default: 8'h00
0x347	R	MISC CTRL Status	Bit 7~ 4: Frame count status for Pj' update Bit 3: Authentication ok Bit 2: Km calculation finished Bit 1: Aksv bytes are all received Bit 0: Ainfo in effect Default: 8'h00
0x348	R	Mi' byte0	Mi' byte0 value for every frame Default: 8'h00
0x349	R	Mi' byte1	Mi' byte1 value for every frame Default: 8'h00
0x34A	R	Mi' byte2	Mi' byte2 value for every frame Default: 8'h00
0x34B	R	Mi' byte3	Mi' byte3 value for every frame Default: 8'h00
0x34C	R	Mi' byte4	Mi' byte4 value for every frame Default: 8'h00
0x34D	R	Mi' byte5	Mi' byte5 value for every frame Default: 8'h00
0x34E	R	Mi' byte6	Mi' byte6 value for every frame Default: 8'h00
0x34F	R	Mi' byte7	Mi' byte7 value for every frame Default: 8'h00
0x350	R	Ks' byte0	Ks' byte0 value of session key

			Default: 8'h00
0x351	R	Ks' byte1	Ks' byte1 value of session key Default: 8'h00
0x352	R	Ks' byte2	Ks' byte2 value of session key Default: 8'h00
0x353	R	Ks' byte3	Ks' byte3 value of session key Default: 8'h00
0x354	R	Ks' byte4	Ks' byte4 value of session key Default: 8'h00
0x355	R	Ks' byte5	Ks' byte5 value of session key Default: 8'h00
0x356	R	Ks' byte6	Ks' byte6 value of session key Default: 8'h00
0x357	R	Ki' byte0	Ki' byte0 for every frame Default: 8'h00
0x358	R	Ki' byte1	Ki' byte1 for every frame Default: 8'h00
0x359	R	Ki' byte2	Ki' byte2 for every frame Default: 8'h00
0x35A	R	Ki' byte3	Ki' byte3 for every frame Default: 8'h00
0x35B	R	Ki' byte4	Ki' byte4 for every frame Default: 8'h00
0x35C	R	Ki' byte5	Ki' byte5 for every frame Default: 8'h00
0x35D	R	Ki' byte6	Ki' byte6 for every frame Default: 8'h00
0x35E	R/W	Authentication Built in Self Test Status	Bit 7: Self test done Bit 6: BIST is working Bit 5: R0' fault Bit 4: M0' fault Bit 3: Ks' fault Bit 2: Km' fault Bit 1: Self test fault happens due to Bit5~Bit2 faults Bit 0: Authentication BIST enable Default: 8'h00
0x35F	R/W	Key set pair select for Authentication Built in Self Test	Bit7~Bit2: RSVD Bit1~0: 00: A1-B1 key pair 01: A1-B2 key pair 10: A2-B1 key pair 11: A2-B2 key pair Default: 8'h00
0x360	R/W	HDCP Input Control	Bit 7: HDCP clk input from 1: Ref clk 0: pixel clk(TMDS) Bit 6: HDCP clk input invert mode 1: clk inverted 0: clk non-inverted Bit 5~3: HDCP input DE pipe delay selection 000: no delay

			001: 1T delay 010: 2T delay 011: 3T delay 100: 4T delay others: 5T delay Bit 2~0: HDCP input data pipe delay selection 000: no delay 001: 1T delay 010: 2T delay 011: 3T delay 100: 4T delay others: 5T delay Default: 8'h80
0x361	R/W	HDCP Input Sync Selection	Bit 7~4: RSVD Bit 3 : HDCP Key Set Decryption Bit 2 : HDCP pad swap (this signal must be paired with 0x65 byte to swap the hdcp ddc pad) 1: enable 0: disable Bit 1 : V Sync selection from separated sync or decomposed sync 1: decomposed sync 0: separated sync Bit 0 : H Sync selection from separated sync or decomposed sync 1: decomposed sync 0: separated sync default : 8'h00
0x362	R	SRAM Status0	Bit7~0: SRAM address[7:0] for SRAM access Default: 8'h00
0x363	R	SRAM_Status1	Bit0: SRAM address[8] for SRAM access Bit1: SRAM Arbitration 1: Servicing for HDCP cipher machine request 0: Servicing for MCU read/write request Default: 8'h00
0x364	R/W	Ri Update Frame Count	Bit7:0 For every this (Ri_update_frame_count+1) value is reached, the Ri value will be updated for constantly link check, for example, if 127 is set, then for every 128th frame count, the Ri value will be updated Default : 8'h7F
0x365	R/W	HDCP Pad Swap Matching Value	Bit 7:0 When this byte is set to be 8'hAA and Bit 2 of 0x61 is set to be enable, then the HDCP ddc pad is swapped to another configuration Default : 8'h00
0x365~0x367	R	RSVD	
0x368	R/W	HDCP Slave Address	Bit7~0: HDCP Slave Address on DDC I2C bus Defaut: 0x74
0x369	R/W	HDCP Status	Bit 7: TMDS control status bit 3 Bit 6: TMDS control status bit 2 Bit 5: TMDS control status bit 1 Bit 4: TMDS control status bit 0 Bit 3: HDCP enable 1: HDCP clock enable

| | | | 0: HDCP clock disable
Bit 2: HDCP interrupt enable
1: interrupt enable
0: interrupt disable
Bit 1: Authentication done flag, write '1' to this bit will clear this flag to 0
Bit 0: AKSV transfer done flag, write '1' to this but will clear this flag to 0
Default: 8'h00 |
0x36A	R/W	Window of Opportunity Lower Bound	Bit 7~0: Low byte of window of opportunity lower bound for eess Default: 8'h00
0x36B	R/W	Window of Opportunity Lower Bound	Bit 7~0: High byte of window of opportunity lower bound for eess Default: 8'h02
0x36C	R/W	Window of Opportunity Upper Bound	Bit 7~0: Low byte of window of opportunity upper bound for eess Default: 8'h10
0x36D	R/W	Window of Opportunity Upper Bound	Bit 7~0: High byte of window of opportunity upper bound for eess Default: 8'h02

9.34. Dithering Function 2

0x370		Dither block blending control	R/W
Bits	Name	Description	
7	LSB10_BLEND_TYPE	0: Static and dynamic ordered blending . 1: Random and dynamic ordered blending .	
6	LSB01/11_BLEND_TYPE	0: Static and dynamic ordered blending . 1: Random and dynamic ordered blending .	
5	LSB10_BLEND_EN	0: Disable . 1: Enable .	
4-3	LSB10_BLEND_LOGIC_OP	00: Or . 01: Xor . 10: Xor . 11: And .	
2	LSB01/11_BLEND_EN	0: Disable . 1: Enable .	
1-0	LSB01/11_BLEND_LOGIC_OP	00: Or . 01: Xor . 10: Xor . 11: And .	

Default: 0000 0000B

0x371		Dither Toggle Control	R/W
Bits	Name	Description	
7-1	Reserved		
0	BLOCK_TOGGLE_EN	0: Disable . 1: Enable .	

Default: XXXX XXX0B

9.35. Horizontal Non-Linear Scaling Function
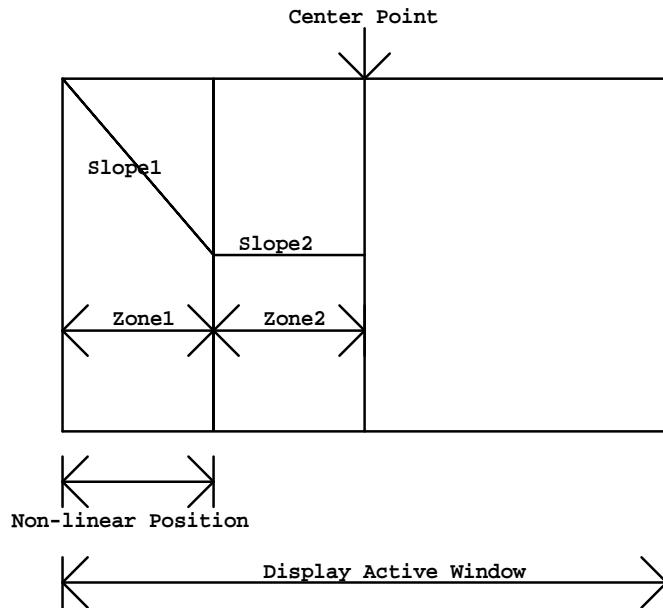
0x380		Horizontal non-linear scaling Control	R/W
Bits	Name	Description	
7-1		Reserved	
0	NL_SCALING_EN	0 = normal linear scaling applied to entire image. 1 = enable non-linear scaling.	

Default: XXXX XXX0B

0x381		Non-linear scaling Offset Adjust	R/W
Bits	Name	Description	
7-0	NL_OFF[7:0]	Adjust the error for scaling factor.	

Default: 0000 0000B

0x382		Non-linear scaling Factor Zone1 end - Low Byte	R/W
Bits	Name	Description	
7-0	NL_ZONE1_END [7:0]	Sets the Scaling Factor in the first non-linear scaling region (ZONE1).	

Default: 0000 0000B

0x383		Non-linear scaling Factor Zone1 end - High Byte	R/W
Bits	Name	Description	
7-0	NL_ZONE1_END [15:8]	Sets the Scaling Factor in the first non-linear scaling region (ZONE1).	

Default: 0000 0000B

0x384		Non-linear scaling Zone1 Slope - Low Byte	R/W

Bits	Name	Description
7-0	NL_SLOPE1 [7:0]	Sets the Slope Factor in the first non-linear scaling region (ZONE1).

Default: 0000 0000B

0x385	Non-linear scaling Zone1 Slope - High Byte	R/W

Bits	Name	Description
7-0	NL_SLOPE1 [15:8]	Sets the Slope Factor in the first non-linear scaling region (ZONE1).

Default: 0000 0000B

0x386	Non-linear scaling Factor Zone2 end - Low Byte	R/W

Bits	Name	Description
7-0	NL_ZONE2_END [7:0]	Sets the Scaling Factor in the first non-linear scaling region (ZONE2).

Default: 0000 0000B

0x387	Non-linear scaling Factor Zone2 end - High Byte	R/W

Bits	Name	Description
7-0	NL_ZONE2_END [15:8]	Sets the Scaling Factor in the first non-linear scaling region (ZONE2).

Default: 0000 0000B

0x388	Non-linear scaling Zone2 Slope - Low Byte	R/W

Bits	Name	Description
7-0	NL_SLOPE2 [7:0]	Sets the Slope Factor in the first non-linear scaling region (ZONE2).

Default: 0000 0000B

0x389	Non-linear scaling Zone2 Slope -High	R/W

Bits	Name	Description
7-0	NL_SLOPE2 [15:8]	Sets the Slope Factor in the first non-linear scaling region (ZONE2).

Default: 0000 0000B

0x38A	Non-linear Position - Low Byte	R/W

Bits	Name	Description
7-0	NL_CBEG [7:0]	Sets the Position of ZONE1 and ZONE2.

Default: 0000 0000B

0x38B	Non-linear Position - High Byte	R/W

Bits	Name	Description
7-0	NL_CBEG [15:8]	Sets the Position of ZONE1 and ZONE2. .

Default: 0000 0000B

9.36. Bright Frame Border Function

0x390	Bright Frame Windows Border control	R/W

Bits	Name	Description
7	BF1_BORDER_ EN	0 = disable BF1 border. 1 = enable BF1 border.
6	BF2_BORDER_ EN	0 = disable BF2 border. 1 = enable BF2 border.
5	Reserved	
4	GAMMA_POSITION_SW	Switching Gamma position.

3	BF2_ YUV2RGB _EN	0 = disable. 1 = enable BF2 YUV to RGB color space.
2	BF2_RGB2YUV_ EN	0 = disable. 1 = enable BF2 RGB to YUV color space.
1	BF1_YUV2RGB _EN	0 = disable. 1 = enable BF1 YUV to RGB color space.
0	BF1_RGB2YUV_ EN	0 = disable. 1 = enable BF1 RGB to YUV color space.

Default: 00X0 0000B

0x391	Bright Frame Border R color control		R/W
Bits	Name	Description	
7-0	BF_BORDER_R[7:0]	Bright frame border color R[7:0] .	

Default: 0000 0000B

0x392	Bright Frame Border G color control		R/W
Bits	Name	Description	
7-0	BF_BORDER_G[7:0]	Bright frame border color G[7:0] .	

Default: 0000 0000B

0x393	Bright Frame Border B color control		R/W
Bits	Name	Description	
7-0	BF_BORDER_B[7:0]	Bright frame border color B[7:0] .	

Default: 0000 0000B

0x394	Bright Frame Border enable control		R/W
Bits	Name	Description	
2	BF_BORDER_TOP/BOT	Bright frame top/bottom border enable control, 1:enable.	
1	BF_BORDER_RIGHT	Bright frame right border enable control, 1:enable.	
0	BF_BORDER_LEFT	Bright frame left border enable control, 1:enable.	

Default: XXXX X000B

9.37. Y/C Peaking Control

0x3A0	Y/C Peaking Function Control		R/W
Bits	Name	Description	
7-6	Reserved		
5	CHROMA_PEAK_MEDIAN_EN	These bits set the chroma median peaking control. 0: disabled , 1: enabled	
4	CHROMA_PEAK_EN	These bits set the chroma peaking control. 0: disabled , 1: enabled	
3-1	Reserved		
0	LUMA_PEAK_EN	This bit enables the luma horizontal peaking control , 0: disabled , 1: enabled	

Default: XX00 XXX0B

0x3A1	Luma Peaking Range Control		R/W
Bits	Name	Description	
7-D4	YCORING[3:0]	To control Luma Signal throshold .	

3-D2	YGAIN[1:0]	To control Luma Gain range .
1-D0	YFREQ[1:0]	To control Luma freq range .

Default: 0000 0000B

0x3A2		Chroma Peaking Range Control	R/W
Bits	Name	Description	
7-4	CCORING[3:0]	To control Chroma Signal throshold .	
3-2	CGAIN[1:0]	To control Chroma Gain range .	
1-0	CFREQ[1:0]	To control Chroma freq range .	

Default: 0000 0000B

9.38. ACE   Control

0x3B0		ACE Function Control	R/W
Bits	Name	Description	
7-5	Reserved		
4	HIST_MODE	0: Mode 0 , pixel number accumulation mode . 1: Mode 1 ,frame number accumulation mode .	
3-2	ACE_MODE[1:0]	00: 4 area histogram / I – Gamma curve . 01: 8 area histogram / I – Gamma curve . 10: 16 area histogram / I – Gamma curve . 11: reserved	
1	BF1_I-GAMMA_EN	1: enable BF1 , I-Gamma function , 0:disable .	
0	BF2_I-GAMMA_EN	1: enable BF2 , I-Gamma function , 0:disable .	

Default: XXX0 0000B

0x3B1		ACE Function Control	R/W
Bits	Name	Description	
7	I-GAMMA_UPDATE	1: for update I-Gamma curve data .	
6	I-GAMMA_RW	0: for read I-Gamma curve . 1: for write I-Gamma curve .	
5	WINSEL	0 : for BF1 access . 1 : for BF2 access .	
4	DATA_PORT_SEL	1: for I-Gamma curve R/W ,0: for histogram read .	
3-1	FRAME_MODE[2:0]	000 ~ 111: for 1 to 255 frame calculation .	
0	HIST_EN/HIST_RDY	1: enable histogram 0: histogram Read ready .	

Default: 0000 0000B

0x3B2		ACE R/W Data port	R/W
Bits	Name	Description	
7-0	DATA_PORT[7:0]	Ace r/w data port[7:0]	

Default: 0000 0000B

0x3B3		Frame mode threshold – Low Byte	R/W
Bits	Name	Description	
7-0	FRAME_THRESHOLD[7:0]	Mode 1 threshold [7:0]	

Default: 0000 0000B

0x3B4		Frame mode threshold – Mid Byte	R/W
Bits	Name	Description	
7-0	FRAME_THRESHOLD[15:8]	Mode 1 threshold [15:8]	

Free Datasheet http://www.datasheet4u.com/

Default: 0000 0000B

0x3B5		Frame mode threshold – High Byte	R/W
Bits	Name	Description	
7-0	FRAME_THRESHOLD[23:16]	Mode 1 threshold[23:16]	

Default: 0000 0000B

9.39. Color Management

0x3C0		CM Color Adjustment Control	R/W
Bits	Name	Description	
7	CM_UPDATE_FLAG	The status of updating new coefficients to controller right after any write to brightness, contrast, intensity, hue, and saturation. This flag is read-only bit. 0: Done,　1: Busy	
6	CM_BRIGHT_EN	Brightness Adjust Function Enable, update adjustment in Vsync 0: Disable,　1: Enable	
5	CM_CONTRAST_EN	Contrast Adjust Function Enable, update adjustment in Vsync 0: Disable,　1: Enable	
4	CM_HUE_EN	Hue Adjust Function Enable, update adjustment in Vsync 0: Disable,　1: Enable	
3	CM_SATURATION_EN	Saturation Adjust Function Enable, update adjustment in Vsync 0: Disable,　1: Enable	
2	CM_INTENSITY_EN	Intensity Adjust Function Enable, update adjustment in Vsync 0: Disable,　1: Enable	
1-0	Reserved		

Default: 0000 00XXB

0x3C1		CM Brightness coefficient for Red	R/W
Bits	Name	Description	
7-0	CM_BRIGHTNESS_R	This parameter is active when CM_BRIGHT_EN is active. The value is from –128 to 127 in 2's complement, power on default is 0. R Display color = (Original value * Contrast coef.) + Brightness coef.	

Default: 0000 0000B

0x3C2		CM Brightness coefficient for Green	R/W
Bits	Name	Description	
7-0	CM_BRIGHTNESS_G	This parameter is active when CM_BRIGHT_EN is active. The value is from –128 to 127 in 2's complement, power on default is 0. G Display color = (Original value * Contrast coef.) + Brightness coef.	

Default: 0000 0000B

0x3C3		CM Brightness coefficient for Blue	R/W
Bits	Name	Description	
7-0	CM_BRIGHTNESS_B	This parameter is active when CM_BRIGHT_EN is active. The value is from –128 to 127 in 2's complement, power on default is 0. B Display color = (Original value * Contrast coef.) + Brightness coef.	

Default: 0000 0000B

0x3C4		CM Contrast Ratio coefficient for R	R/W
Bits	Name	Description	

7-0	CM_CONTRAST_R	This parameter is active when CM_CONTRAST_EN is active. The value is from 0(00 h) to2 (FF h), power on default is 1 (80h)..

Default: 1000 0000B

0x3C5	CM Contrast Ratio coefficient for G		R/W
Bits	Name	Description	
7-0	CM_CONTRAST_G	This parameter is active when CM_CONTRAST_EN is active. The value is from 0(00 h) to2 (FF h), power on default is 1 (80h).	

Default: 1000 0000B

0x3C6	CM Contrast Ratio coefficient for B		R/W
Bits	Name	Description	
7-0	CM_CONTRAST_B	This parameter is active when CM_CONTRAST_EN is active. The value is from 0(00 h) to2 (FF h), power on default is 1 (80h).	

Default: 1000 0000B

0x3C7	CM Hue coefficient		R/W
Bits	Name	Description	
7-0	CM_HUE	This parameter is active when CM_HUE_EN is active. The value is from 00h to 7Fh, one step means 180/128 degree. Bit 7 is sign bit: 0: clockwise (negative rotation), 1: counterclockwise (positive rotation)	

Default: 1000 0000B

0x3C8	CM Hue coefficient		R/W
Bits	Name	Description	
7-0	CM_SATURATION	This parameter is active when CM_SATURATION_EN is active. The value is from 00 h to FF h.	

Default: 1000 0000B

0x3C9	CM Hue coefficient		R/W
Bits	Name	Description	
7-0	CM_INTENSITY	This parameter is active when CM_INTENSITY_EN is active. The value is from 00 h to FF h. (0~2)	

Default: 1000 0000B

0x3CC	CM Color Enhancement Configuration		R/W
Bits	Name	Description	
7	HH_MAP_EN	Hue-Hue map, 0: disable , 1: enable	
6	HS_MAP_EN	Hue-Saturation map, 0: disable , 1: enable	
5	SS_MAP_EN	Saturation-Saturation map, 0: disable , 1: enable	
4-2		Reserved	
1	MAP_LOAD_EN	Mapping table load enable , 1: enable	
0	CM_CE_EN	CM Color Enhancement enable , 0: disable, 1: enable	

Default: 000X XX00B

0x3CD	CM Index Access Port Control		R/W
Bits	Name	Description	
7-2	Reserved		

1-0	CM_INDEX_SEL	Table Select: 00 : no access, 01 : Hue-Hue Table, 10: Hue-Saturation Table, 11: Saturation-Saturation Table

Default: XXXX XX00B

0x3CE		CM Index Access Port Address	R/W
Bits	Name	Description	
7-5	Reserved		
4-0	CM_INDEX_ ADDR	Table Address: Hue-Hue address: 0~23 (24 entries), each step means 15 degree Hue-Saturation address: 0~23 (24 entries), each step means 15 degree Saturation-Saturation address: 0~16 (17 entries), each step means 1/16 full saturation scale	

Default: XXX0 0000B

0x3CF		CM Index Access Port	R/W
Bits	Name	Description	
7-0	CM_INDEX_PORT	Hue-Hue Data Port: The value is from 00h to 7Fh, one step means 30/128 degree. Bit 7: 0 is clockwise, 1 is counterclockwise. Power on default is 00h. Hue-Saturation Data Port: The value is from 00h to FFh. (0~2). Power on default is 80h (1). Saturation-Saturation Data Port: The value is from 00 h to FF h. (0~1). Power on default is FFh (1).	

Default: 0000 0000B(HH), 1000 0000B(HS),1111 1111B(SS)

10. Ordering Information

Order Code	Application	High Quality ADC	Ultra-Reliable DVI	RSDS Tx	LVDS Tx	MCU Flash	Package	Note
NT68625MEFG-64	SXGA	○		2	2	64K Byte	QFP 128L	Green Product (Pb-free)
NT68625MEFG-128	SXGA	○		2	2	128K Byte	QFP 128L	Green Product (Pb-free)
NT68665MEFG-64	SXGA	○	○	2	2	64K Byte	QFP 128L	Green Product (Pb-free)
NT68665MEFG-128	SXGA	○	○	2	2	128K Byte	QFP 128L	Green Product (Pb-free)

11. Package Information
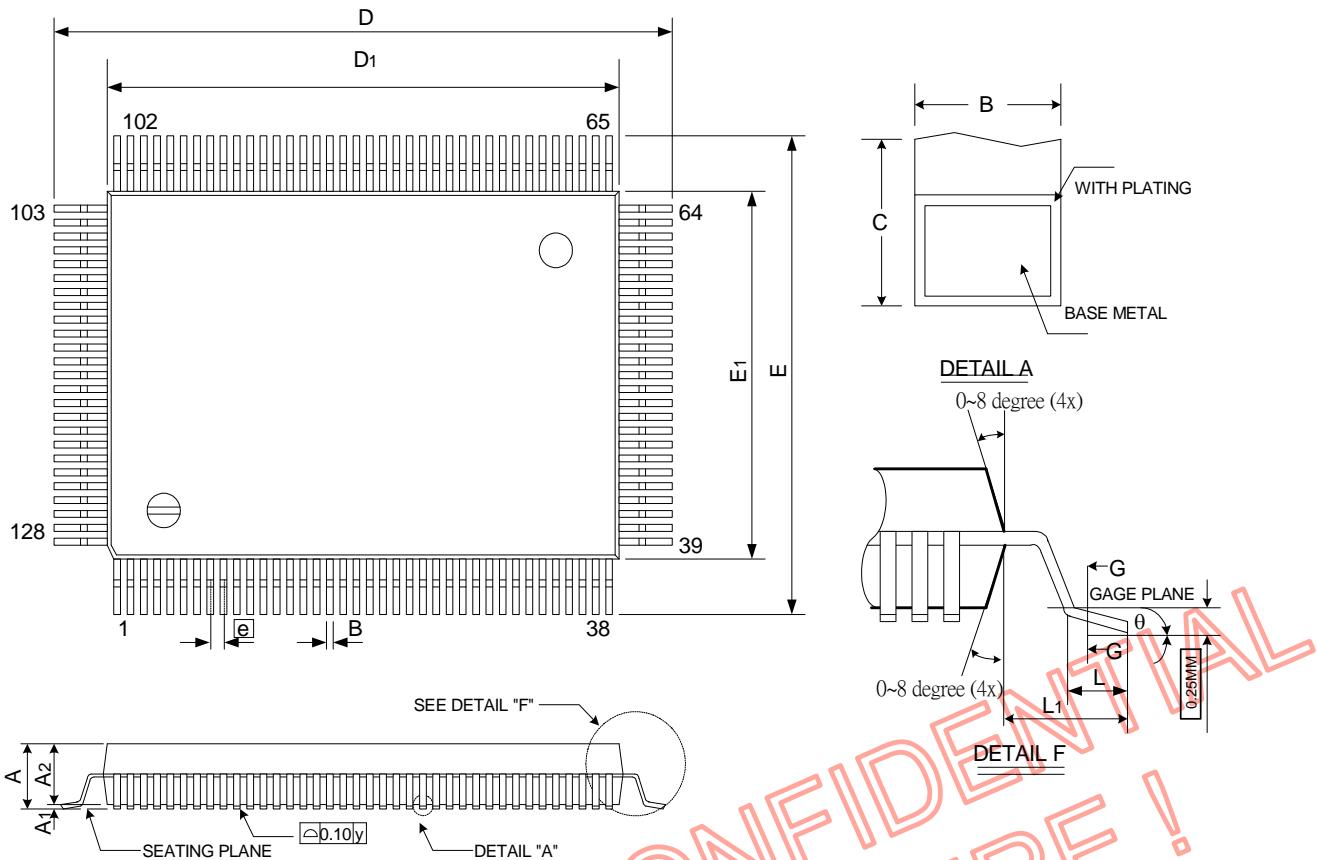
QFP 128L Outline Dimensions   **unit: inches/mm**

Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	--	--	0.134	--	--	3.40
A1	0.010	--	--	0.25	--	--
A2	0.101	0.112	0.117	2.57	2.85	2.97
B	0.005	0.009	0.011	0.13	0.22	0.27
C	0.004	--	0.008	0.09	--	0.20
D	0.906	0.913	0.921	23.00	23.20	23.40
D1	0.783	0.787	0.791	19.90	20.00	20.10
E	0.669	0.667	0.685	17.00	17.20	17.40
E1	0.547	0.551	0.555	13.90	14.00	14.10
e	0.020 BSC			0.5 BSC		
L	0.029	0.035	0.041	0.73	0.88	1.03
L1	0.063 BSC			1.60 BSC		
Y	--	--	0.004	--	--	0.10
θ	0°	--	7°	0°	--	7°

Notes: 1. Dimensions D & E do not include resin fins.

2. Dimensions F, G**D** & G**E** are for PC Board surface mount pad pitch design reference only