TOSHIBA MOS MEMORY PRODUCT

262,144 WORD × 1 BIT DYNAMIC RAM
N-CHANNEL SILICON GATE MOS

TMM41256P/T-12
TMM41256P/T-15

DESCRIPTION

The TMM41256P/T is the new generation dynamic RAM organized 262,144 words by 1 bit, it is successor to the industry standard TMM4164AP.

The TMM41256P/T utilizes TOSHIBA's N-channel Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user.

Multiplexed address inputs permit the TMM-41256P/T to be packaged in a standard 16 pin plastic DIP and 18 pin plastic leaded chip carrier. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment.

System oriented features include single power supply of 5V ±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

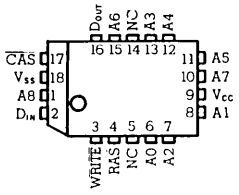
- 262,144 words by 1 bit organization
- Fast access time and cycle time

DEVICE	t_{RAC}	t_{CAC}	t_{RC}
TMM41256P/T-12	120 ns	60 ns	220 ns
TMM41256P/T-15	150 ns	75 ns	260 ns

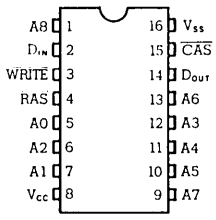
- Single power supply of 5V ±10% with a built-in V_{BB} generator
- Low Power:
  330mW Operating (MAX.) (TMM41256P/T-12)
  275mW Operating (MAX.) (TMM41256P/T-15)
  28mW Stand by (MAX.)
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "EARLY WRITE" operation
- Read-Modify-Write, $\overline{RAS}$-only refresh, Hidden refresh, and Page Mode capability.
- All inputs and output TTL compatible
- 256 refresh cycles/4ms
- Package
  Plastic DIP : TMM41256P
  Plastic Leaded Chip Carrier : TMM41256T

PIN CONNECTION (TOP VIEW)

• Plastic LCC



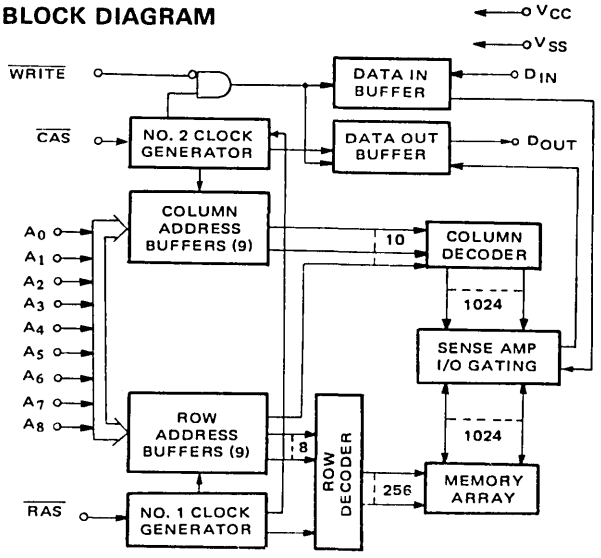
• Plastic DIP



PIN NAMES

$A_0 \sim A_8$	Address Inputs
$\overline{CAS}$	Column Address Strobe
D_{IN}	Data In
D_{OUT}	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WRITE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM MATIGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input and Output Voltage	V_{IN}, V_{OUT}	−1 ~ 7	V	1
Power Supply Voltage	V_{CC}	−1 ~ 7	V	1
Operating Temperature	T_{OPR}	0 ~ 70	°C	1
Storage Temperature	T_{STG}	−55 ~ 150	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITDONS (T_a = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	–	6.5	V	2
V_{IL}	Input Low Voltage	−1.0	–	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_a = 0 ~ 70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = t_{RC} MIN.)	TMM41256P T-12	–	60	mA	3, 4
		TMM41256P T-15	–	50		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		–	5	mA	
I_{CC3}	REFRESH CURRENT Average Power Supply Current, Refresh Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH} : t_{RC} = t_{RC} MIN.)	TMM41256P T-12	–	45	mA	3
		TMM41256P T-15	–	40		
I_{CC4}	PAGE MODE CURRENT Average Power Supply Current, Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling : t_{PC} = t_{PC} MIN.)	TMM41256P T-12	–	45	mA	3, 4
		TMM41256P T-15	–	40		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (OV ≦ V_{IN} ≦ 6.5V, All Other Pins Not Under Test = OV)		−10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, OV ≦ V_{OUT} ≦ +5.5V)		−10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = −5mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRIAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0 ~ 70 C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	TMM41256P-12		TMM41256P-15		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	220	—	260	—	ns	
t_{RWC}	Read-Write Cycle Time	240	—	285	—	ns	
t_{RMW}	Read-Modify-Write Cycle Time	260	—	310	—	ns	
t_{PC}	Page Mode Cycle Time	120	—	145	—	ns	
t_{PRWC}	Page Mode Read-Write Cycle Time	140	—	170	—	ns	
t_{PRMW}	Page Mode Read-Modify-Write Cycle Time	160	—	195	—	ns	
t_{RAC}	Access Time from $\overline{RAS}$	—	120	—	150	ns	8,10
t_{CAC}	Access Time from $\overline{CAS}$	—	60	—	75	ns	9,10
t_{OFF}	Output Buffer Turn-Off Delay	0	35	0	40	ns	11
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	6
t_{RP}	$\overline{RAS}$ Precharge Time	90	—	100	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	120	10,000	150	10,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	60	—	75	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	120	—	150	—	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	60	10,000	75	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	60	25	75	ns	13
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	—	10	—	ns	
t_{CPN}	$\overline{CAS}$ Precharge Time	25	—	25	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time (for Page Mode Cycle Only)	50	—	60	—	ns	
t_{ASR}	Row Address Set-Up Time	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	15	—	15	—	ns	
t_{ASC}	Column Address Set-Up Time	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	25	—	30	—	ns	
t_{AR}	Column Address Hold Time Reference to $\overline{RAS}$	95	—	120	—	ns	
t_{RCS}	Read Command Set-Up Time	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time Reference to $\overline{CAS}$	0	—	0	—	ns	12
t_{RRH}	Read Command Hold Time Reference to $\overline{RAS}$	15	—	20	—	ns	12
t_{WCH}	Write Command Hold Time	35	—	45	—	ns	
t_{WCR}	Write Command Hold Time Reference to $\overline{RAS}$	95	—	120	—	ns	
t_{WP}	Write Command Pulse Width	35	—	45	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	35	—	45	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	35	—	45	—	ns	
t_{DS}	Data-In Set-Up Time	0	—	0	—	ns	14
t_{DH}	Data-In Hold Time	35	—	45	—	ns	14
t_{DHR}	Data-In Hold Time Reference to $\overline{RAS}$	95	—	120	—	ns	
t_{REF}	Refresh Period	—	4	—	4	ms	
t_{WCS}	Write Command Set-Up Time	−10	—	−10	—	ns	15
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay	40	—	50	—	ns	15
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay	100	—	125	—	ns	15

CAPACITANCE

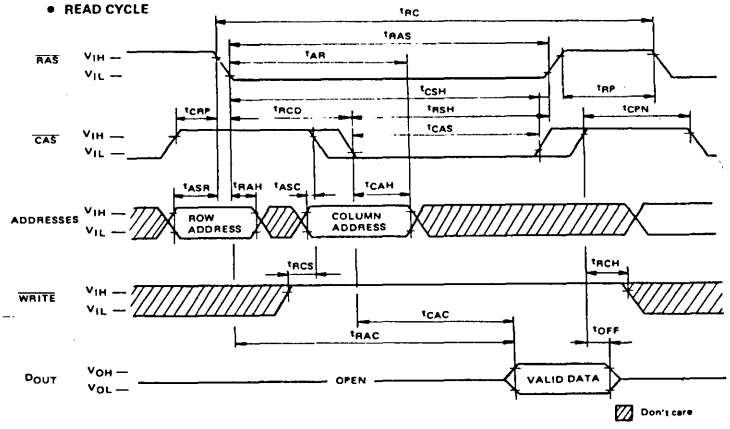
(V_{CC} = 5V ±10%, f = 1MHz, Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
C_{I1}	Input Capacitance ($A_0 \sim A_8$, D_{IN})	–	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$)	–	7	pF
C_O	Output Capacitance (D_{OUT})	–	7	pF

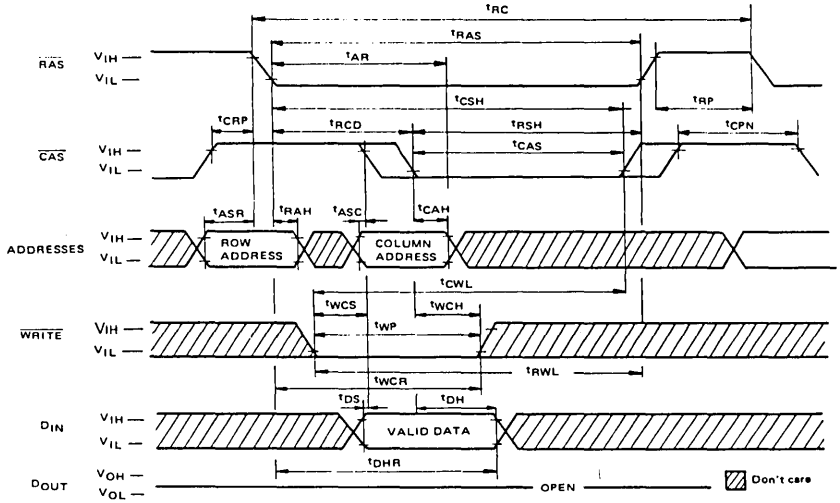
NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
6. AC measurements assume t_T = 5 ns.
7. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Assumes that $t_{RCD} \leqq t_{RCD}$ (max.). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
9. Assumes that $t_{RCD} \geqq t_{RCD}$ (max.)
10. Measured with a load equivalent to 2 TTL loads and 100pF.
11. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
13. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
14. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-write or read-modify-write cycles.
15. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{CWD} \geqq t_{CWD}$ (min.) and $t_{RWD} \geqq t_{RWD}$ (min.), the cycle is a read-write cycle or read-modify-write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

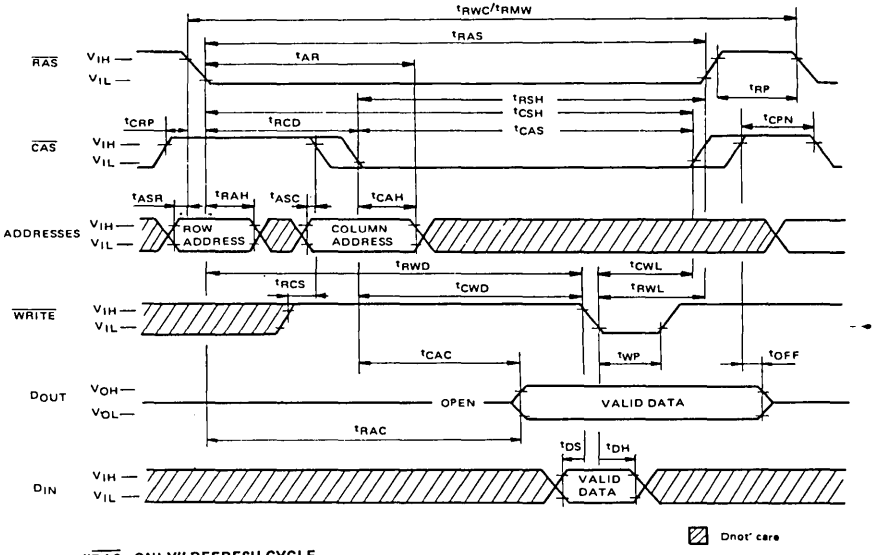
TIMING WAVEFORMS



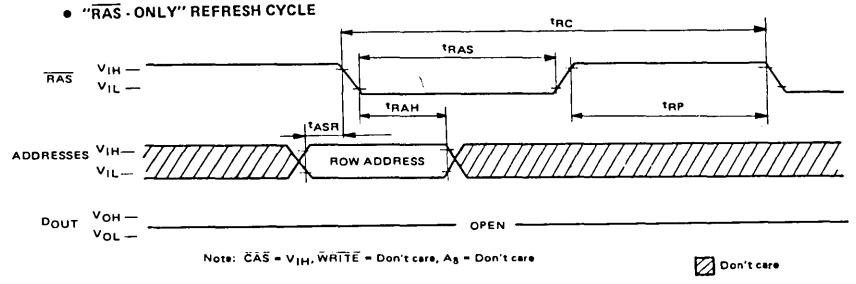
• WRITE CYCLE (EARLY WRITE)



•READ-WRITE/READ-MODIFY-WRITE CYCLE



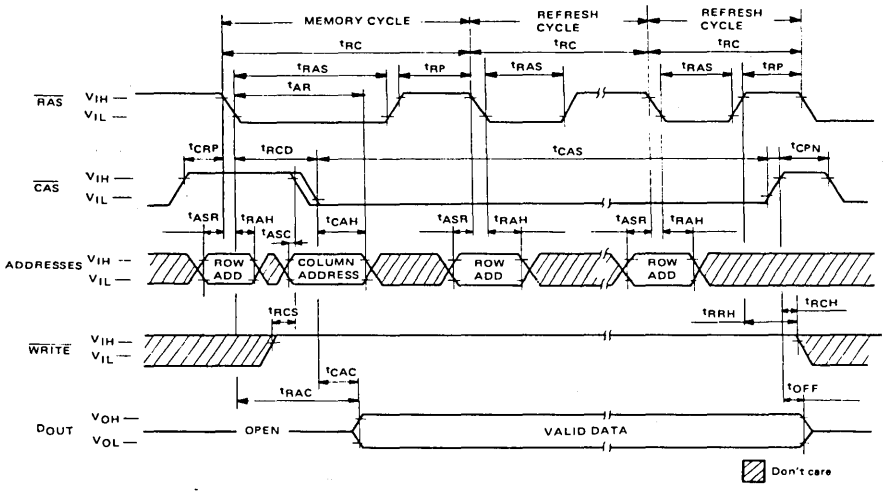
• "$\overline{RAS}$-ONLY" REFRESH CYCLE



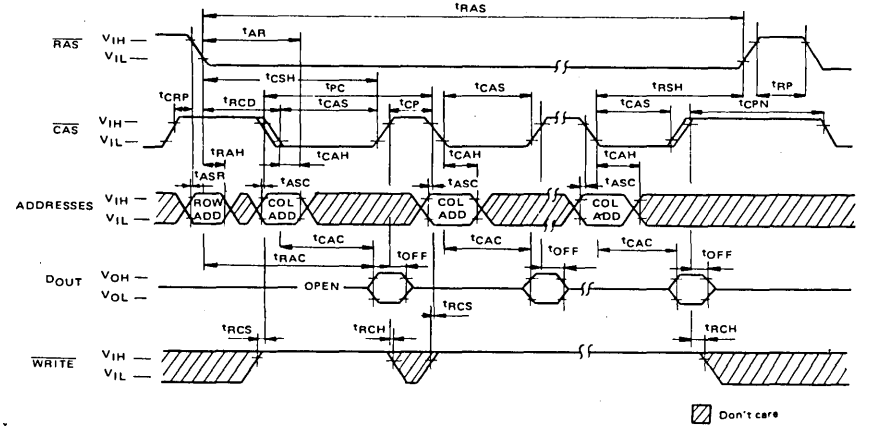
Note: $\overline{CAS}$ = V_{IH}, $\overline{WRITE}$ = Don't care, A_8 = Don't care

Don't care

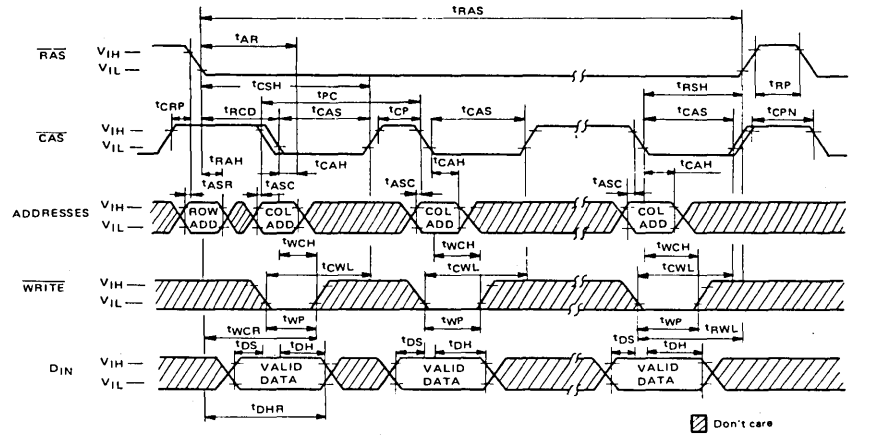
• HIDDEN REFRESH CYCLE



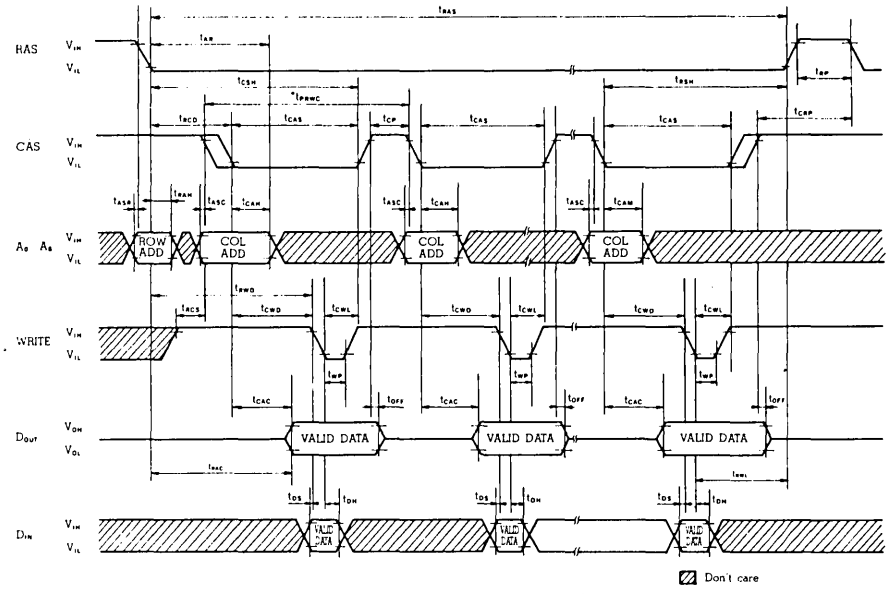
• PAGE MODE READ CYCLE



• PAGE MODE WRITE CYCLE



● PAGE MODE READ-WRITE/READ-MODIFY-WRITE CYCLE



APPLICATION INFORMATION

ADDRESSING

The 18 address bits required to decode 1 of the 262,144 cell locations within the TMM41256P/T are multiplexed onto the 9 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 9 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 9 column address bits into the chip. Each of these signals, $\overline{RAS}$ and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. This "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active. The later of the signals ($\overline{WRITE}$ or $\overline{CAS}$) to make its negative transition is the strobe for the Data In (D_{IN}) register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low (active) prior to $\overline{CAS}$, the D_{IN} is strobed by $\overline{CAS}$ and the set-up and hold times are referenced to $\overline{CAS}$. If the input data is not available at $\overline{CAS}$ time or if it is desired that the cycle be a read-write cycle, the $\overline{WRITE}$ signal will be delayed until after $\overline{CAS}$ has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than $\overline{CAS}$. (To illustrate this feature, D_{IN} is referenced to $\overline{WRITE}$ in the timing diagrams depicting the read-write and page mode write cycles while the "early write" cycle diagram shows D_{IN} referenced to $\overline{CAS}$).

Data is retrieved from the memory in a read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cycle in which $\overline{CAS}$ is active (low). Data read from the selected cell will be available at the output within the specified access time.

DATA OUTPUT CONTROL

The normal condition of the Data Output (D_{OUT}) of the TMM41256P/T is the high impedance (open circuit) state. This is to say, anytime $\overline{CAS}$ is at a high level, the D_{OUT} pin will be floating. The only time the output will turn on and contain either a logic 0 or logic 1 is at access time during a read cycle. D_{OUT} will remain valid from access time until $\overline{CAS}$ is taken back to the inactive (high level) condition.

PAGE MODE

The "Page-Mode" feature of the TMM41256P/T allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and maintaining the $\overline{RAS}$ signal at a logic 0 throughout all successive memory cycles in which the row address is common. This "Page Mode" of operation will not dissipate the power associated with the negative going edge of $\overline{RAS}$. Also, the time required for strobing in a new row address is eliminated, thereby decreasing the access and cycle times.

REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 256 row address ($A_0 \sim A_7$) within each 4 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this funciton is most easily accomplished with "$\overline{RAS}$ - only" cycles, $\overline{RAS}$ only refresh results in a substantial reduction in operating power. This reduction in power is reflected in the I_{CC3} specification.

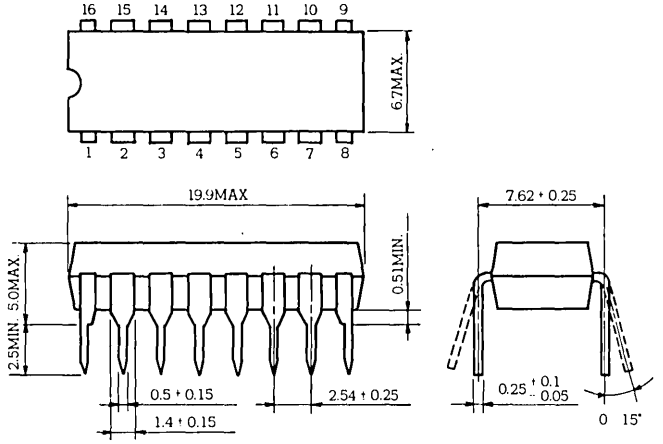
HIDDEN REFRESH

An optional feature of the TMM41256P/T is that refresh cycles may be performed while maintaining valid data at the output pin. This is referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a "$\overline{RAS}$ - only" refresh cycle, but with $\overline{CAS}$ held low

OUTLINE DRAWINGS

● Plastic DIP

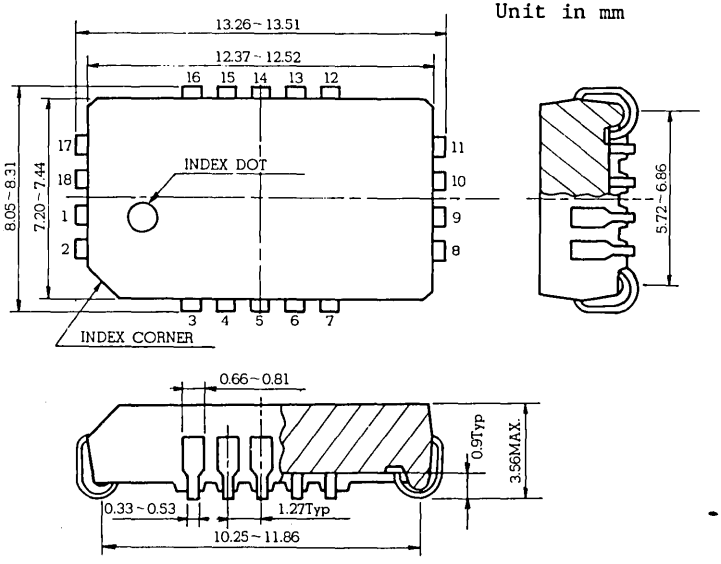
Unit in mm



Note : Each lead pitch is 2.54 mm. All leads are located within 0.25 mm of their true longitudinal position with respect to No. 1 and No. 16 leads. All dimensions are in millimeters.

● Plastic LCC

Unit in mm



Note : Each lead pitch is 1.27mm.