TEXAS INSTRUMENTS

SN74CB3T3245

SCDS136C – OCTOBER 2003 – REVISED MAY 2018

SN74CB3T3245 8-Bit FET Bus Switch
2.5-V and 3.3-V Low-Voltage With 5-V-Tolerant Level Shifter

1 Features

- Standard '245-Type Pinout
- Output Voltage Translation Tracks V_{CC}
- Supports Mixed-Mode Signal Operation on All Data I/O Ports
  - 5-V Input Down to 3.3-V Output Level Shift With 3.3-V V_{CC}
  - 5-V/3.3-V Input Down to 2.5-V Output Level Shift With 2.5-V V_{CC}
- 5-V-Tolerant I/Os With Device Powered Up or Powered Down
- Bidirectional Data Flow With Near-Zero Propagation Delay
- Low ON-State Resistance (r_{on}) Characteristics (r_{on} = 5 Ω Typical)
- Low Input/Output Capacitance Minimizes Loading ($C_{io(OFF)}$ = 5 pF Typical)
- Data and Control Inputs Provide Undershoot Clamp Diodes
- Low Power Consumption (I_{CC} = 40 μA Maximum)
- V_{CC} Operating Range From 2.3 V to 3.6 V
- Data I/Os Support 0- to 5-V Signaling Levels (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V, 5 V)
- Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs
- I_{off} Supports Partial-Power-Down Mode Operation

- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
- Ideal for Low-Power Portable Equipment

2 Applications

- Supports Digital Applications: Level Translation, PCI Interface, USB Interface, Memory Interleaving, Bus Isolation
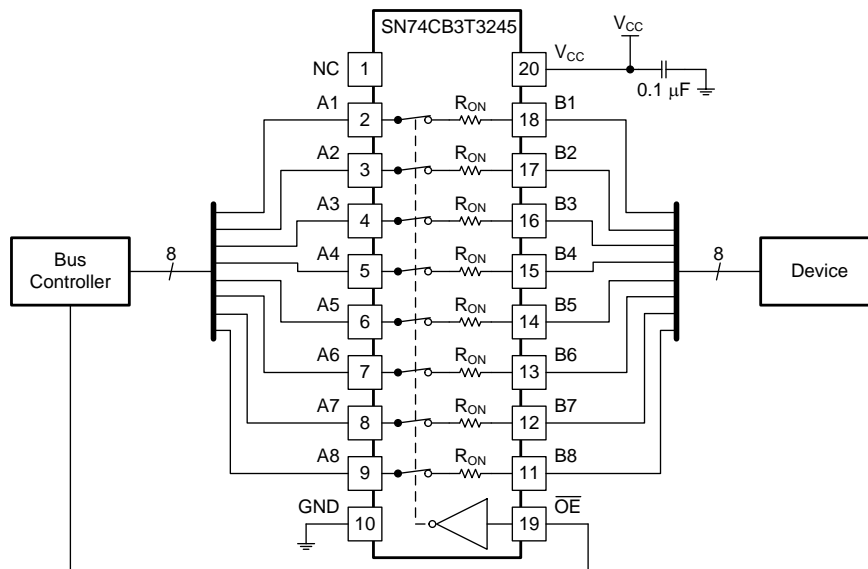
3 Description

The SN74CB3T3245 device is a high-speed TTL-compatible 8-bit FET bus switch with low ON-state resistance (r_{on}), allowing for minimal propagation delay. The device fully supports mixed-mode signal operation on all data I/O ports by providing voltage translation that tracks V_{CC}.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74CB3T3245DBQ	SSOP (20)	8.65 mm × 3.90 mm
SN74CB3T3245DGV	TVSOP (20)	5.00 mm × 4.40 mm
SN74CB3T3245DW	SOIC (20)	12.80 mm × 7.50 mm
SN74CB3T3245PW	TSSOP (20)	6.50 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Functional Diagram

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (June 2015) to Revision C   **Page**

- Changed the pin out image appearance 3
- Changed I_O = 1 mA To: I_O = 1 µA in Figure 9 and Figure 10 11

Changes from Revision A (August 2012) to Revision B   **Page**

- Added *Applications*, *Device Information* table, *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1
- Removed *Ordering Information* table. 1

Changes from Original (March 2005) to Revision A   **Page**

- Updated graphic note and picture in Figure 1. 8

Product Folder Links: *SN74CB3T3245*

5 Pin Configuration and Functions

DBQ, DGV, DW, and PW Package
20-Pin SSOP, TVSOP, SOIC, TSSOP
Top View

NC	1	20	VCC
A1	2	19	$\overline{OE}$
A2	3	18	B1
A3	4	17	B2
A4	5	16	B3
A5	6	15	B4
A6	7	14	B5
A7	8	13	B6
A8	9	12	B7
GND	10	11	B8
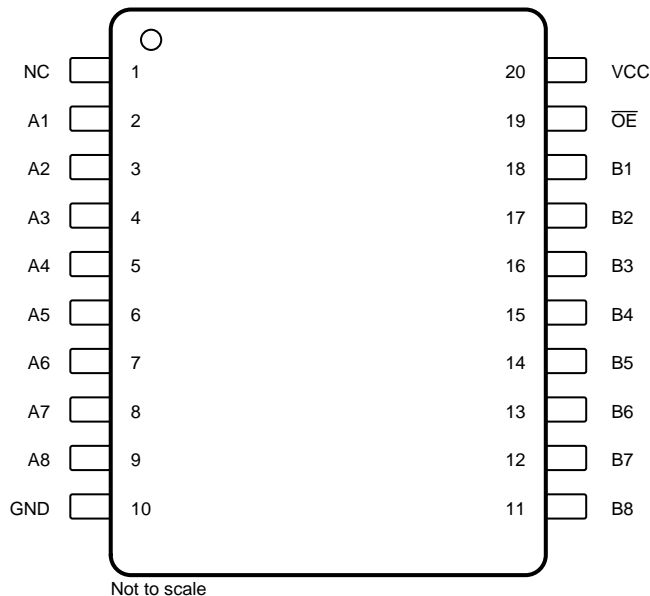
Not to scale

NC — No internal connection

Pin Functions

PIN NO.	NAME	I/O	DESCRIPTION
1	NC	—	Not internally connected
2	A1	I/O	Switch 1 A terminal
3	A2	I/O	Switch 2 A terminal
4	A3	I/O	Switch 3 A terminal
5	A4	I/O	Switch 4 A terminal
6	A5	I/O	Switch 5 A terminal
7	A6	I/O	Switch 6 A terminal
8	A7	I/O	Switch 7 A terminal
9	A8	I/O	Switch 8 A terminal
10	GND	—	Ground
11	B8	I/O	Switch 8 B terminal
12	B7	I/O	Switch 7 B terminal
13	B6	I/O	Switch 6 B terminal
14	B5	I/O	Switch 5 B terminal
15	B4	I/O	Switch 4 B terminal
16	B3	I/O	Switch 3 B terminal
17	B2	I/O	Switch 2 B terminal
18	B1	I/O	Switch 1 B terminal
19	$\overline{OE}$	I	Output enable, active low
20	V_{CC}	—	Power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage[2]		−0.5	7	V
V_{IN}	Control input voltage[2][3]		−0.5	7	V
$V_{I/O}$	Switch I/O voltage[2][3][4]		−0.5	7	V
I_{IK}	Control input clamp current	$V_{IN} < 0$		−50	mA
$I_{I/OK}$	I/O port clamp current	$V_{I/O} < 0$		−50	mA
$I_{I/O}$	ON-state switch current[5]			±128	mA
	Continuous current through V_{CC} or GND			±100	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		−65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) V_I and V_O are used to denote specific conditions for $V_{I/O}$.
(5) I_I and I_O are used to denote specific conditions for $I_{I/O}$.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	$V_{CC} = 2.3$ V to 2.7 V	1.7	5.5	V
		$V_{CC} = 2.7$ V to 3.6 V	2	5.5	
V_{IL}	Low-level control input voltage	$V_{CC} = 2.3$ V to 2.7 V	0	0.7	V
		$V_{CC} = 2.7$ V to 3.6 V	0	0.8	
$V_{I/O}$	Data input/output voltage		0	5.5	V
T_A	Operating free-air temperature		−40	85	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

6.4 Thermal Information

	THERMAL METRIC[1]	SN74CB3T3245				UNIT
		DBQ (SSOP)	DGV (TVSOP)	DW (SOIC)	PW (TSSOP)	
		20 PINS	20 PINS	20 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	68	92	58	83	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS		MIN	TYP[2]	MAX	UNIT
V_{IK}		V_{CC} = 3 V, I_I = −18 mA				−1.2	V
V_{OH}		See and Figure 1					
I_{IN}	Control inputs	V_{CC} = 3.6 V, V_{IN} = 3.6 V to 5.5 V or GND				±10	µA
I_I		V_{CC} = 3.6 V, Switch ON, V_{IN} = V_{CC} or GND	V_I = V_{CC} − 0.7 V to 5.5 V			±20	µA
			V_I = 0.7 V to V_{CC} − 0.7 V			−40	
			V_I = 0 to 0.7 V			±5	
I_{OZ}[3]		V_{CC} = 3.6 V, V_O = 0 to 5.5 V, V_I = 0, Switch OFF, V_{IN} = V_{CC} or GND				±10	µA
I_{off}		V_{CC} = 0, V_O = 0 to 5.5 V, V_I = 0,				10	µA
I_{CC}		V_{CC} = 3.6 V, $I_{I/O}$ = 0, Switch ON or OFF, V_{IN} = V_{CC} or GND	V_I = V_{CC} or GND			40	µA
			V_I = 5.5 V			40	
ΔI_{CC}[4]	Control inputs	V_{CC} = 3 V to 3.6 V, One input at V_{CC} − 0.6 V, Other inputs at V_{CC} or GND				300	µA
C_{in}	Control inputs	V_{CC} = 3.3 V, V_{IN} = V_{CC} or GND			4		pF
$C_{io(OFF)}$		V_{CC} = 3.3 V, $V_{I/O}$ = 5.5 V, 3.3 V, or GND, Switch OFF, V_{IN} = V_{CC} or GND			5		pF
$C_{io(ON)}$		V_{CC} = 3.3 V, Switch ON, V_{IN} = V_{CC} or GND	$V_{I/O}$ = 5.5 V or 3.3 V		5		pF
			$V_{I/O}$ = GND		13		
r_{on}[5]		V_{CC} = 2.3 V, TYP at V_{CC} = 2.5 V, V_I = 0	I_O = 24 mA		5	8.5	Ω
			I_O = 16 mA		5	8.5	
		V_{CC} = 3 V, V_I = 0	I_O = 64 mA		5	7	
			I_O = 32 mA		5	7	

(1) V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.
(2) All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.
(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.
(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.
(5) Measured by the voltage drop between A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.
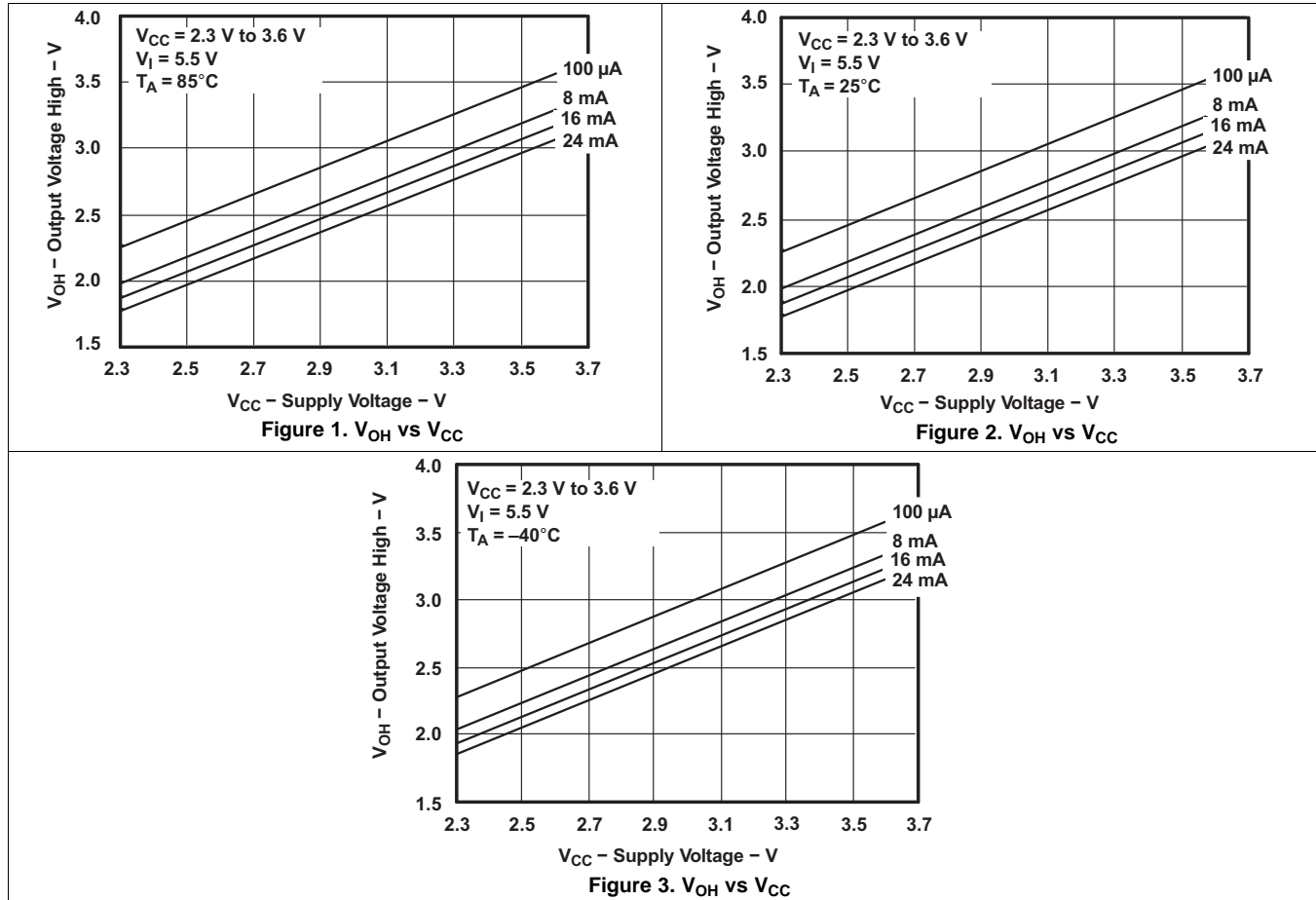
6.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}[1]	A or B	B or A		0.15		0.25	ns
t_{en}	$\overline{OE}$	A or B	1	10.5	1	8	ns
t_{dis}	$\overline{OE}$	A or B	1	5.5	1	7.5	ns

(1) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

6.7 Typical Characteristics

Figure 1. V$_{OH}$ vs V$_{CC}$

Figure 2. V$_{OH}$ vs V$_{CC}$

Figure 3. V$_{OH}$ vs V$_{CC}$

Product Folder Links: *SN74CB3T3245*

7 Parameter Measurement Information
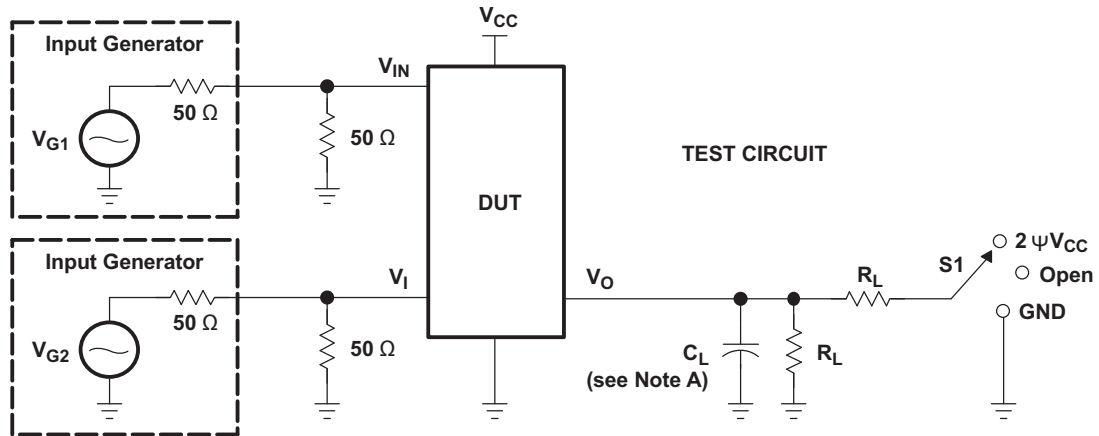
TEST	V_CC	S1	R_L	V_I	C_L	V_Δ
t_pd(s)	2.5 V ± 0.2 V	Open	500 Ω	3.6 V or GND	30 pF	
	3.3 V ± 0.3 V	Open	500 Ω	5.5 V or GND	50 pF	
t_PLZ/t_PZL	2.5 V ± 0.2 V	2 × V_CC	500 Ω	GND	30 pF	0.15 V
	3.3 V ± 0.3 V	2 × V_CC	500 Ω	GND	50 pF	0.3 V
t_PHZ/t_PZH	2.5 V ± 0.2 V	Open	500 Ω	3.6 V	30 pF	0.15 V
	3.3 V ± 0.3 V	Open	500 Ω	5.5 V	50 pF	0.3 V

VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES (t_pd(s))

VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
   B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
      Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
   C. All input pulses are supplied by generators having the following characteristics: PRR≤ 10 MHz, Z_O = 50 W, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
   D. The outputs are measured one at a time, with one transition per measurement.
   E. t_PLZ and t_PHZ are the same as t_dis.
   F. t_PZL and t_PZH are the same as t_en.
   G. t_PLH and t_PHL are the same as t_pd(s). The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance
      of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
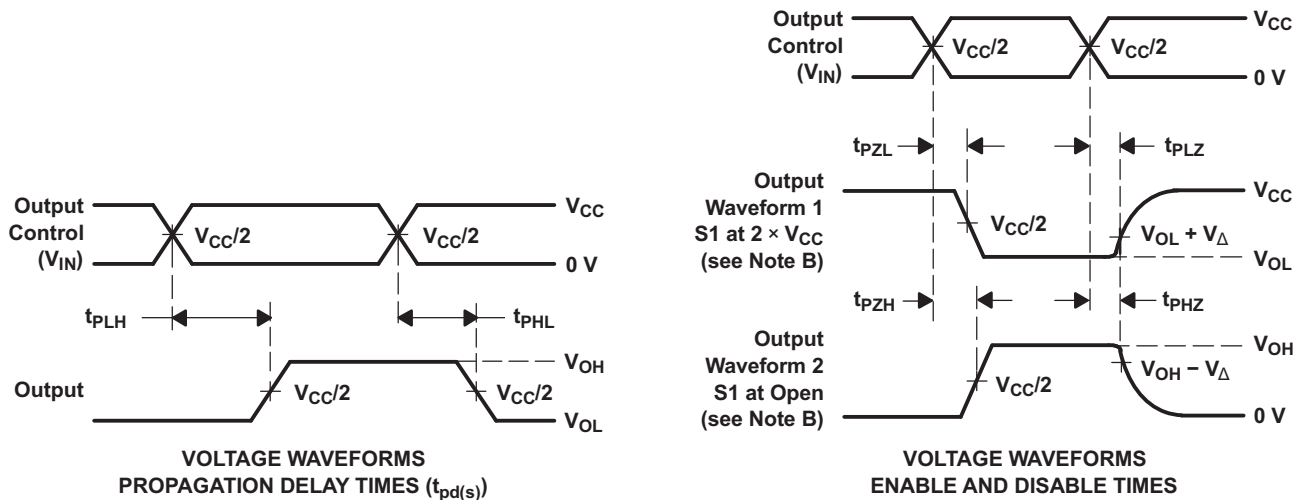   H. All parameters and waveforms are not applicable to all devices.

Figure 4. Test Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN74CB3T3245 device is a high-speed TTL-compatible FET bus switch with low ON-state resistance (r_{on}), allowing for minimal propagation delay. The device fully supports mixed-mode signal operation on all data I/O ports by providing voltage translation that tracks V_{CC}. The SN74CB3T3245 device supports systems using 5-V TTL, 3.3-V LVTTL, and 2.5-V CMOS switching standards, as well as user-defined switching levels (see Figure 5).

The SN74CB3T3245 device is an 8-bit bus switch with a single ouput-enable ($\overline{OE}$) input and a standard '245 pinout. When $\overline{OE}$ is low, the 8-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{OE}$ is high, the 8-bit bus switch is OFF, and a high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

8.2 Functional Block Diagram
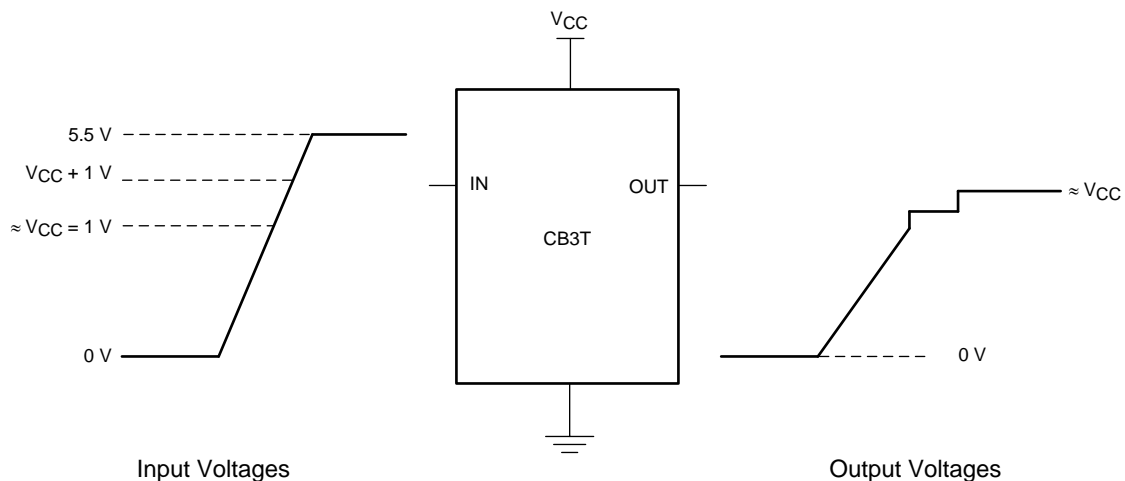
If the input high voltage (V_{IH}) level is greater than or equal to $V_{CC} + 1V$, and less than or equal to 5.5V, the output high voltage (V_{OH}) level will be equal to approximately the V_{CC} voltage level.

Figure 5. Typical DC Voltage Translation Characteristics
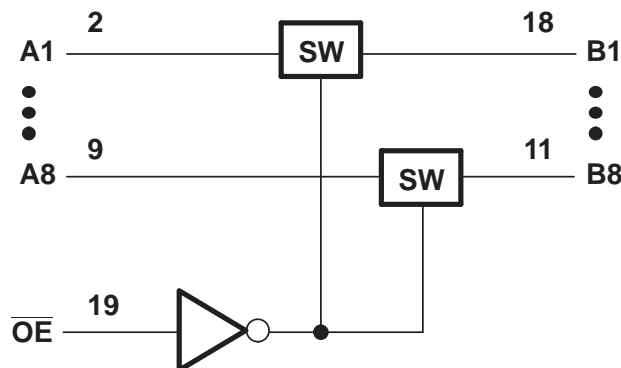
Figure 6. Logic Diagram (Positive Logic)

Product Folder Links: *SN74CB3T3245*

Functional Block Diagram (continued)

1) Gate Voltage (V_G) is approximately equal to $V_{CC} + V_T$ when the switch is ON and $V_I > (V_{CC} + V_T)$.
2) EN is the internal enable signal applied to the switch.

Figure 7. Simplified Schematic, Each FET Switch (SW)

8.3 Feature Description

The SN74CB3T3245 device uses the standard '245-type pinout. The output voltage tracks V_{CC}, allowing for easy down-translation. The device is ideal for low-power portable equipment.

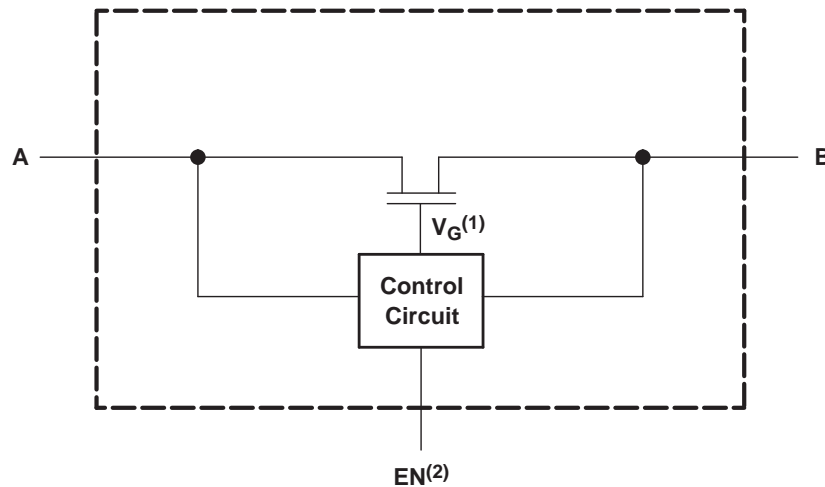Mixed-mode signal operation is supported on all data I/O ports. 5-V input down to 3.3-V output level shift with 3.3-V V_{CC} and 5-V/3.3-V input down to 2.5-V output level shift With 2.5-V V_{CC} are possible due to overvoltage tolerant inputs.

This part is friendly to partial power down systems. The I/Os are 5-V-tolerant with the device powered up or powered down and I_{off} supports partial-power-down mode operation

The SN74CB3T3245 has a bidirectional data flow with near-zero propagation delay.

The SN74CB3T3245 has low ON-state resistance (r_{on}) characteristics (r_{on} = 5 Ω Typical)

The SN74CB3T3245 has both low input and output capacitance minimizes loading ($C_{io(OFF)}$ = 5 pF Typical)

Data and control inputs provide undershoot clamp diodes.

The SN74CB3T3245 has low power consumption (I_{CC} = 40 μA Maximum)

The SN74CB3T3245 has a V_{CC} operating range from 2.3 V to 3.6 V.

The data I/Os support 0- to 5-V signaling levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)

Control inputs can be driven by TTL or 5-V/3.3-V CMOS outputs

8.4 Device Functional Modes

Table 1 lists the functional modes of the SN74CB3T3245.

Table 1. Function Table

INPUT $\overline{OE}$	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect

9 Application and Implementation

9.1 Application Information

This application is specifically to connect a 5-V bus to a 3.3-V device. It is assumed that communication in this particular application is one-directional, going from the bus controller to the device.

9.2 Typical Application
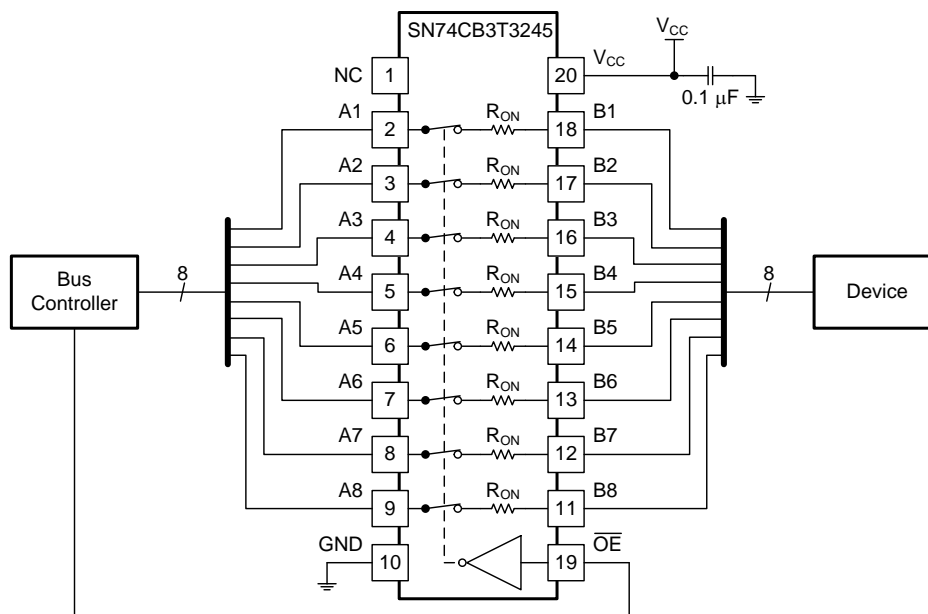
Figure 8. Typical Application Schematic

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits.

Because this design is for down-translating voltage, no pullup resistors are required.

9.2.2 Detailed Design Procedure

 1. Recommended Input conditions
    – Specified high and low levels. See (V_{IH} and V_{IL}) in *Recommended Operating Conditions*
    – Inputs are overvoltage tolerant allowing them to go as high as 7 V at any valid V_{CC}
 2. Recommend output conditions
    – Load currents should not exceed 128 mA on each channel

Typical Application (continued)

9.2.3 Application Curves

Figure 9. Data Output Voltage vs Data Input Voltage

Figure 10. Data Output Voltage vs Data Input Voltage
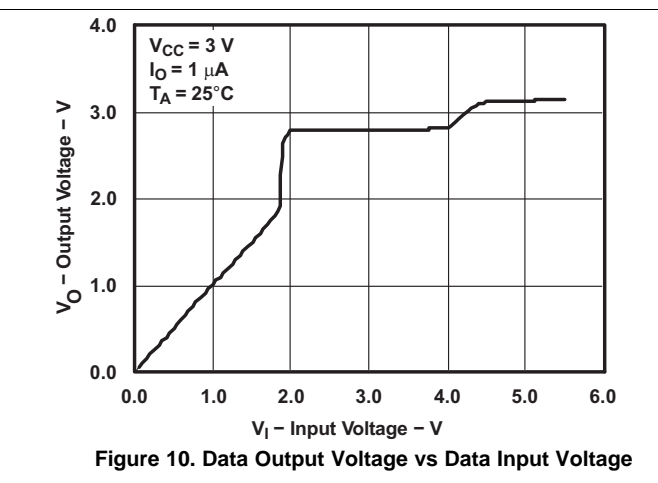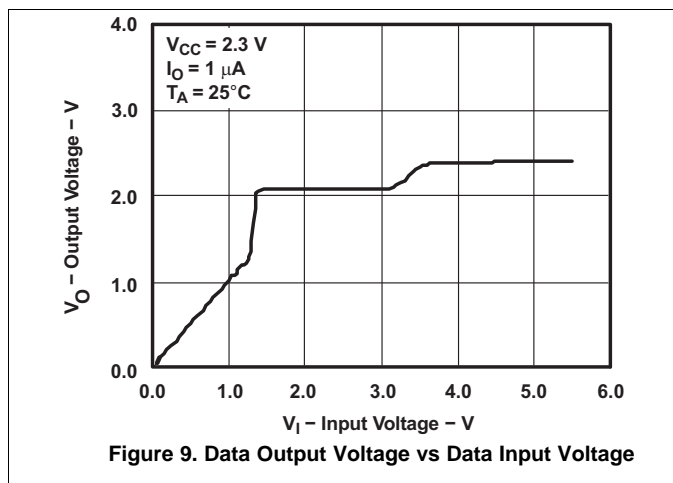
10   Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-μF bypass capacitor is recommended. If there are multiple pins labeled V_{CC}, then a 0.01-μF or 0.022-μF capacitor is recommended for each V_{CC} because the V_{CC} pins will be tied together internally. For devices with dual supply pins operating at different voltages, for example V_{CC} and V_{DD}, a 0.1-μF bypass capacitor is recommended for each supply pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-μF and 1-μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

11   Layout

11.1   Layout Guidelines

Reflections and matching are closely related to the loop antenna theory but are different enough to be discussed separately from the theory. When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. Figure 11 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

11.2   Layout Example
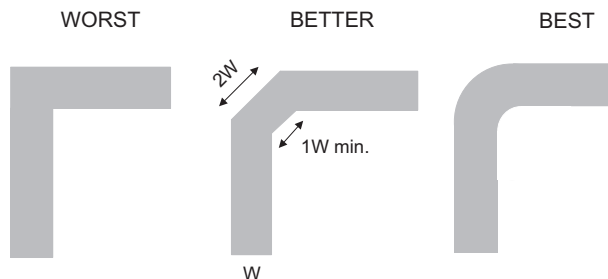
Figure 11. Trace Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

Implications of Slow or Floating CMOS Inputs, SCBA004

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74CB3T3245DBQR	ACTIVE	SSOP	DBQ	20	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CB3T3245	Samples
SN74CB3T3245DGVR	ACTIVE	TVSOP	DGV	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	KS245	Samples
SN74CB3T3245DW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3T3245	Samples
SN74CB3T3245DWG4	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3T3245	Samples
SN74CB3T3245DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3T3245	Samples
SN74CB3T3245DWRG4	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3T3245	Samples
SN74CB3T3245PW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	KS245	Samples
SN74CB3T3245PWG4	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	KS245	Samples
SN74CB3T3245PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	KS245	Samples
SN74CB3T3245PWRE4	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	KS245	Samples

[1] The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CB3T3245DBQR	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74CB3T3245DGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74CB3T3245DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74CB3T3245PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CB3T3245DBQR	SSOP	DBQ	20	2500	853.0	449.0	35.0
SN74CB3T3245DGVR	TVSOP	DGV	20	2000	367.0	367.0	35.0
SN74CB3T3245DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74CB3T3245PWR	TSSOP	PW	20	2000	853.0	449.0	35.0

TUBE

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74CB3T3245DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74CB3T3245DWG4	DW	SOIC	20	25	507	12.83	5080	6.6
SN74CB3T3245PW	PW	TSSOP	20	70	530	10.2	3600	3.5
SN74CB3T3245PWG4	PW	TSSOP	20	70	530	10.2	3600	3.5

4220206/A   02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

20X (1.5)

SYMM

1

20X (0.45)

(R0.05) TYP

20

SYMM

18X (0.65)

10

11

(5.8)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.05 MAX
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220206/A   02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

20X (1.5)

SYMM

(R0.05) TYP

1

20X (0.45)

20

18X (0.65)

SYMM

10

11

(5.8)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A   02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R—PDSO—G20)   PLASTIC SMALL OUTLINE

Example Board Layout

Based on a stencil thickness
of .127mm (.005inch).

18x0,65

20x0,25

1,55

5,6

5,6

18x0,65

Example
Non Soldermask Defined Pad

Example
Solder Mask Opening
(See Note E)

0,3

1,6

Pad Geometry

0,07
All Around

4211284-5/G   08/15

NOTES: A. All linear dimensions are in millimeters.
         B. This drawing is subject to change without notice.
         C. Publication IPC—7351 is recommended for alternate design.
         D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
             contact their board assembly site for stencil design recommendations. Refer to IPC—7525 for other stencil recommendations.
         E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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DBQ (R−PDSO−G20)   PLASTIC SMALL−OUTLINE PACKAGE

0.344 (8,75)
0.337 (8,55)

20   11

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)

Pin 1
Index Area

1   10

0.025 (0,635)

0.012 (0,30)
0.008 (0,20)

⊕ 0.005 (0,13) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°−8°

0.035 (0,89)
0.016 (0,40)
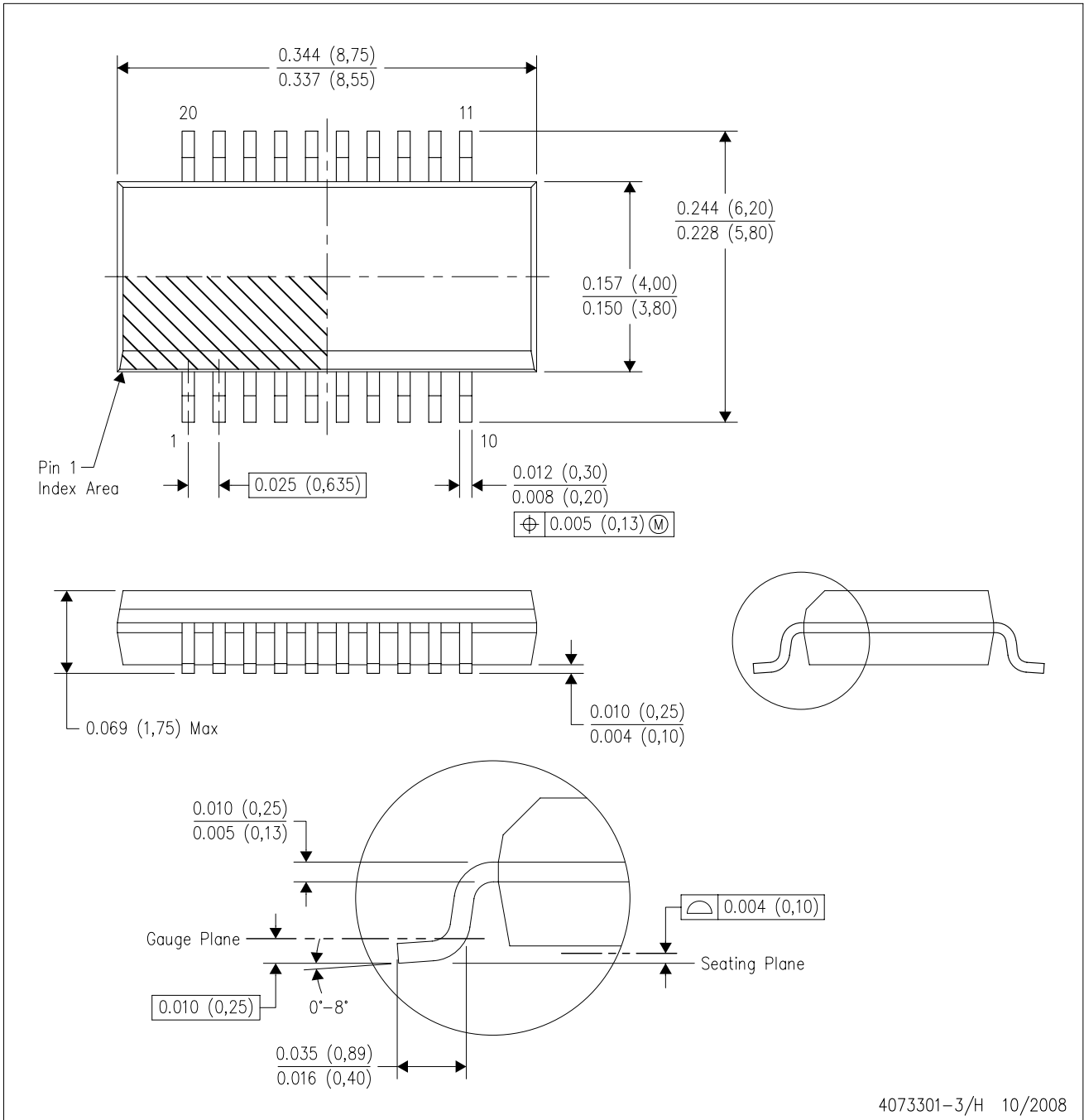
4073301−3/H   10/2008

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
         D.   Falls within JEDEC MO−137 variation AD.

C

SEATING PLANE

0.1 C

10.63 / 9.97 TYP

A

PIN 1 ID AREA

1

18X 1.27

20

13.0 / 12.6 NOTE 3

2X 11.43

10

11

2.65 MAX

B

7.6 / 7.4 NOTE 4

20X 0.51 / 0.31

⊕ 0.25 Ⓜ C A B

0.33 / 0.10 TYP

SEE DETAIL A

0.25 GAGE PLANE

1.27 / 0.40

0° - 8°

0.3 / 0.1

DETAIL A TYPICAL

4220724/A   05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

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20X (2)

SYMM

1

20

20X (0.6)

18X (1.27)

SYMM

(R0.05)
TYP

10

11

(9.3)

LAND PATTERN EXAMPLE
SCALE:6X

SOLDER MASK
OPENING

METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.07 MAX
ALL AROUND

0.07 MIN
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220724/A   05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

20X (2)

1

20X (0.6)

18X (1.27)

SYMM

20

SYMM

10

11

(9.3)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A   05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN

0,40

0,23
0,13 ⊕ | 0,07 Ⓜ

24   13

4,50
4,30   6,60
6,20

1   12

A

0,16 NOM

Gage Plane

0°−8°

0,25

0,75
0,50

1,20 MAX

0,15
0,05

Seating Plane

⌒ | 0,08

DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
  B. This drawing is subject to change without notice.
  C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
  D. Falls within JEDEC: 24/48 Pins – MO-153
    14/16/20/56 Pins – MO-194

TEXAS
INSTRUMENTS

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