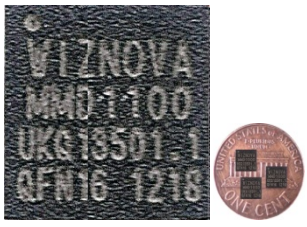
MMD1100 Data Sheet

Magnetic Card Reader IC

- UART Interface
- SPI Interface



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Jungjin clover co.,LTD

TEL : 02)896-7060
FAX : 02)896-7061

www.jclover.co.kr

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1 Introduction

1.1 Overview

The MMD1100(Non Encryption)chip integrates the magnetic card reader function. Upon reception of the magnetic head signals, the card data are recovered, and transferred to the external interfaces via universal asynchronous receiver and transmitter (UART) or serial peripheral interface (SPI). The chip supports up to 3 tracks card reading at the same time. Signal processing techniques are employed to recover F2F encoded data reliably from head signals with severe fluctuation of signal amplitude, widely varying bit interval, and jittery bit position. Fig. 1 shows the simplified block diagram of the chip.

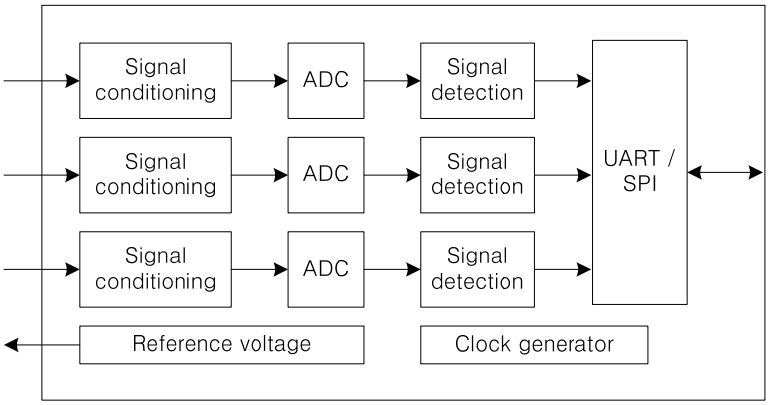


Figure 1: Block diagram.

1.2 Features

- 3 Tracks Support
- Signal Conditioning Adapted to wide range of amplitude and noise with Head Signal
- Digital Signal Processing for Superior Data Recovery Performance
- Flexible External Interface: UART or SPI
- Few External Component Required
- Wide range of card swipe speed : from 5 to 150 cm/s

1.3 Applications

- Point of Sale Terminal
- ATM Machine
- Card Key Entry System

2 External Interface

2.1 Pin configuration : 16 pin QFN package

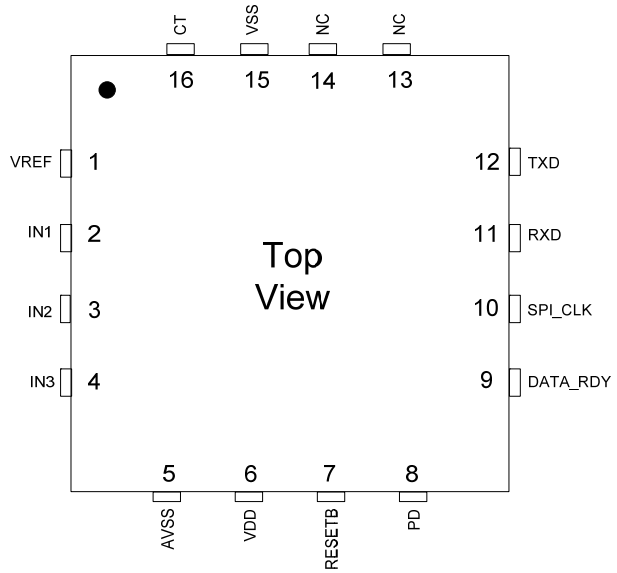


Figure 2: Pin configuration.

2.2 Pin description

Table 1: Pin description (14 pin QFN)

Pin name	Pin number	I/O	Description
VREF	1	Power	Reference voltage for head signal input (0.9V)
IN1	2	Input	Track 1 head signal, analog
IN2	3	Input	Track 2 head signal, analog
IN3	4	Input	Track 3 head signal, analog
AVSS	5	Power	Analog ground
VDD	6	Power	Power supply (3.3V)
RESETB[1)]	7	Input	External reset signal, active low
PD	8	Input	Tie to the ground VSS
DATA_RDY	9	Output	Data ready for SPI
SPI_CLK	10	Input	SPI clock: 10kHz ~ 100kHz
RXD	11	Input	UART/SPI receive data
TXD	12	Output	UART/SPI transmit data
NC	13	NC	Tie to the ground VSS
NC	14	NC	Tie to the ground VSS
VSS	15	Power	Digital ground
CT	16	Power	LDO external capacitor connect (20nF)

Note 1) It takes 600ms to be a restoration after reset signal.

3 Functional Description

3.1 Magnetic Head Interface

A magnetic head is connected to the MMD1100 as shown in Fig. 3. The track1, 2, and 3 signals are connected to the pin IN1, IN2, and IN3, respectively. The head common signal is connected with VREF to get the reference voltage of 0.9V. When a head with a fewer than 3 tracks is used, the input signal pin corresponding to the unused track should be tied to the VREF.

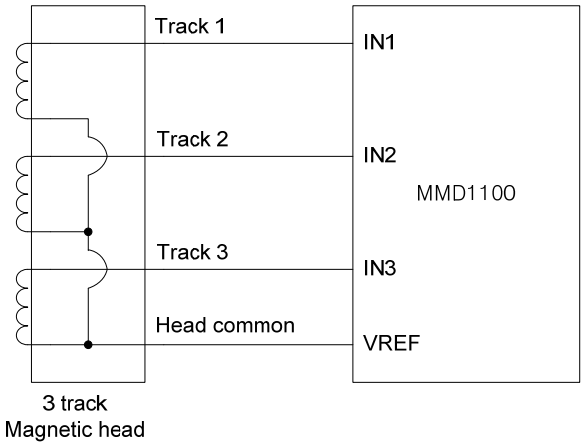


Figure 3: Magnetic head connection.

3.2 Signal Conditioning and Processing

The head signal input is amplified to fit the signal amplitude to the dynamic range of the circuit and filtered to remove the out of band noise before digital signal processing. The analog to digital converter (ADC) digitizes the incoming signal to generate a digital signal. The digital signal processing techniques adopted include acquisition and tracking of widely varying bit interval, signal amplitude tracking, minimizing jitter of bit position, removal of false peak and zero crossing, and sequential detection of F2F encoded data. The implemented analog signal conditioning and digital signal processing technology demonstrates a superior performance in the recovery of the magnetic card data.

3.3 UART and SPI

The external data interface either UART or SPI is selected by the state of the SPI_CLK input pin. The UART interface is selected as long as the SPI_CLK stays at the logical high state (3.3v) after the external reset signal input (RESETB=0V). The SPI interface is selected if the SPI_CLK is at the logical low state (0V) at least 3usec period after the external reset signal. Once the SPI is chosen, the SPI is assumed until the next external reset signal input

.

The UART interface supports the baud rate of 9.6, 19.2kbps. The frame structure is shown in Fig. 4. One start bit and at least one stop bit should be included in the frame. The data word consists of 8 bits. The LSB of the data is transmitted first. (1 start bit + 8 data bits, 1 stop bit, none parity).

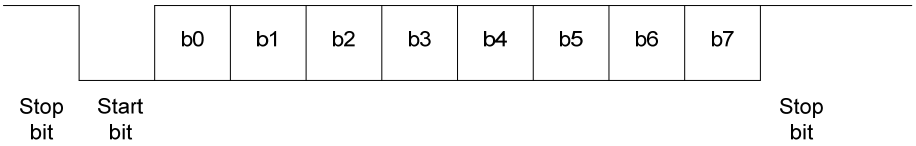


Figure 4: Frame format of UART interface.

The SPI interface uses SPI_CLK input as the timing reference to transmit or receive data through TXD and RXD, respectively. The supported data rate is from 10kbps to 100kbps. The data transmit and receive timing diagrams are shown in Fig. 5 and 6, respectively. The DATA_RDY output pin is asserted to notify the external device of the data availability. Once the DATA_RDY is asserted, the external device provides SPI_CLK to the chip and can latch the TXD signal at the falling edge of SPI_CLK. The chip receives bits through RXD and latches the signal at the falling edge of the SPI_CLK. Note that if there is no SPI_CLK input for 500msec after the DATA_RDY assertion, the DATA_RDY signal is de-asserted.

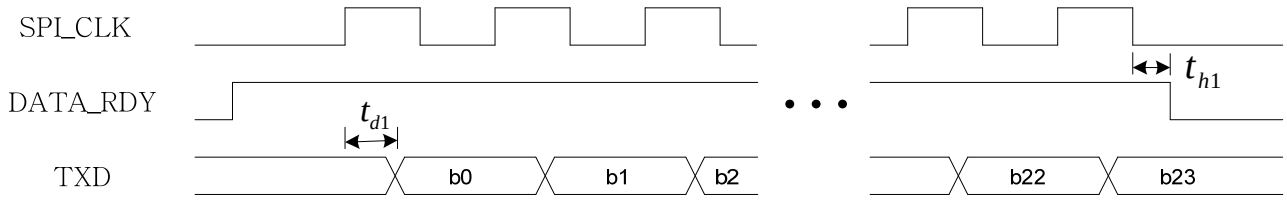


Figure 5: Timing diagram of SPI transmit data.

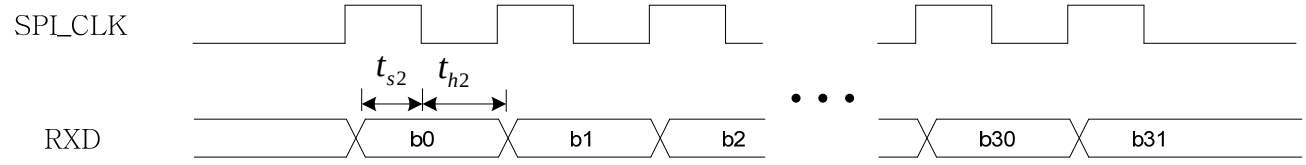


Figure 6: Timing diagram of SPI receive data.

3.4 Commands

Various commands are implemented to read data out of the chip, to set the initial encryption key and the operating mode of the chip, etc. These commands are provided to the chip via the UART or SPI. The response from the chip to each command can be used to check the effectiveness of the command. The command from the external device to the chip consists of the various fields as shown below.

Command format

STX (1byte)	Class (1byte)	Function (1byte)	Length (1byte)	TX Data (n byte)	ETX (1byte)	BCC (1byte)

* STX : Command Start Character (0x02)
* Class : Class of command
* Function : Requested function for the chip to conduct
* Length : Number of bytes in Data field
* TX Data : Data
* ETX : End Character (0x03)
* BCC : Check Sum (Exclusive OR value from STX to ETX)

Response format

STX (1byte)	Class (1byte)	Function (1byte)	Length (1byte)	Status (1byte)	RX Data (n byte)	ETX (1byte)	BCC (1byte)

* STX : Start Character for Response (0x02)
* Class : Re-transmission of the Class sent in the command
* Function : Re-transmission of the Function sent in the command
* Length : Number of bytes in RX Data field
* Status : Status Check Byte
  ACK (0x06): Successful execution of the command
  NAK (0x15): Failed execution of the command
* RX Data : Response Value and error code as response
* ETX : End Character for response (0x03)
* BCC : Check sum (Exclusive OR value from STX to ETX)

The commands are listed in Table 2.

Table 2: List of commands

Type	Class	Function	Length	Data	Remark
Get Version	0x10	0x31	0x00	-	Retrieve the version information of the chip
Load User Parameters	0x12	0x31	0x04	TX Mode (1byte) Reserved (1byte) All Track Error (1byte) Reserved (1byte)	Set the operating mode of the chip
UART Calibration	0x13	0x31	0x05	0xAAAAAAAAAA (5byte)	UART calibration
OTP Write (UART calibration)	0x15	0x33	0x00	-	OTP write of UART calibration result **(OTP write maximum 4 times)**
Get Status	0x16	0x31	0x00	-	Get the current setting of the chip
Read Data Retry	0x17	0x31	0x00	-	Re-read the data frame retrieved the most recent
Software Reset [1)]	0x18	0x31	0x00	-	Initialize the chip

Note 1) It takes 50 ms to complete the command.

The responses to the commands are listed in Table 3.

Table 3: List of responses

Type	Class	Function	Length	Status	Data	Remark
Get Version	0x10	0x31	0x10	0x06	MMD1000 VER:1.00	Current chip versions information return
			0x01	0x15	Error Code	Error code return
Load User Parameter	0x12	0x31	0x04	0x06	TX Mode (1byte) Reserved (1byte) All Track Error (1byte) Reserved (1byte)	Current operating mode return
			0x01	0x15	Error Code	Error code return
UART Calibration	0x13	0x31	0x01	0x06	Calibration Value (1byte)	UART calibration result return
			0x01	0x15	Error Code	Error code return
OTP Write (UART calibration)	0x15	0x33	0x01	0x06	Calibration Value (1byte)	UART calibration result OTP write
			0x01	0x15	Error Code	Error code return
Get Status	0x16	0x31	0x06	0x06	TX Mode (1byte) Reserved (1byte) All Track Error (1byte) Reserved(1byte) Reserved (1byte) UART Calibration (1byte)	Current setting information return
			0x01	0x15	Error Code	Error code return
Read Data Retry	Un-encrypted Most Recent Data Frame					Re-read of the most recent un-encrypted data frame
	0x17	0x31	0x01	0x15	Error Coder	Error code return
Software Reset						No response for successful initialization
	0x18	0x31	0x01	0x15	Error Code	Error code return

- The error codes carried in the response TX Data field are summarized in Table 4.

Table 4: List of error codes

Error Code	Description
0x51	Preamble error in card read data
0x52	Postamble error in card read data
0x53	LRC error in card read data
0x54	Parity error in card read data
0x55	Blank track
0x61	STX/ETX error in command communication
0x62	Class/Function un-recognizable in command
0x63	BCC error in command communication
0x64	Length error in command communication
0x65	No data available to re-read
0x71	No more space available for OTP write
0x72	OTP write try without data
0x73	CRC error in read data from OTP
0x74	No data stored in OTP

- The TX Mode is set as follow

Table 5: Data transmit mode

TX Mode	Transmit Mode
MODE2(0x02)	Binary data format (binary low data LSB first)

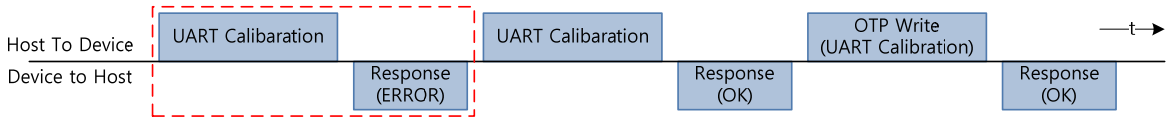
- The all track error field is set as follow

Table 6: all track error response setting

all track error	all track error response setting
0x00	all track error report :

- If the “Software Rest” command is issued without any error, all the registers of the chip are set to their initial values and user setting are retrieved from the OTP memory. The error type for the “Software Rest” command is limited to the communication error and unknown command error.

- To set the baud rate of the UART interface, use the “UART calibration” command as the first command after the power-up or reset. The chip will automatically tune the baud rate to the incoming bit period of the data field of the command (9.6kbps ~ 19.2kbps).



- The data frame formats are shown in Fig. 7.

						<-LEN1->				<-LEN2->				<-LEN3->		
TX MODE 2 Binary Mode	STX	MODE	1 TRK ID	LEN 1	STATUS	DATA	2 TRK ID	LEN 2	STATUS	DATA	3 TRK ID	LEN 3	STATUS	DATA	ETX	BCC
	0x02	0x33	0x25	n Byte	0x06	MS Data	0x3F	n Byte	0x06	MS Data	0x5E	n Byte	0x06	MS Data	0x03	1 Byte
					0x15	Error Code			0x15	Error Code			0x15	Error Code		

Figure 7: TX Data frame format

- The mode field of the data frame is generated by 0x31 + TX Mode.

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Parameter	Symbol	Limits	Units
Supply Voltage	VDD	-0.3 to +3.6	V
Input Voltage	VIN	-0.3 to VDD+0.3	V
Storage Temperature	ST	-65 to +150	℃
Maximum Junction Temperature	MJT	-20 to 125	℃

4.2 Operating conditions

Parameter	Symbol	Minimum	Typical	Maximum	Units
Supply voltage	VDD	3.0	3.3	3.6	V
Operating Temperature	OT	-20		+70	℃

4.3 DC electrical characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Units	Test Conditions
Input Voltage High	V_{IH}	2.0	-	3.6	V	
Input Voltage Low	V_{IL}	-0.3	-	0.8	V	
Output Voltage High	V_{OH}	2.4	-	3.6	V	I_{OH}=2mA
Output Voltage Low	V_{OL}	0.0	-	0.4	V	I_{OL}=-2mA
Input Current	I_I	-1	-	1	uA	
VDD Supply Current (normal mode)	I_{DD}	-	1.7	2	mA	PD=0V
LDO Output Voltage	V_{LDO}	1.6	1.8	2.0	V	VDD=3.3V
VREF Voltage	V_{vref}	1.0	0.9	0.8	V	VDD=3.3V

4.4 AC electrical characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Units	Test Conditions
TXD signal delay	t_{d1}	-	-	3	usec	SPI interface mode
DATA_RDY hold time	t_{h1}	2	-	-	usec	SPI interface mode
RXD setup time	t_{s2}	1	-	-	usec	SPI interface mode
RXD hold time	t_{h2}	3	-	-	usec	SPI interface mode

5 Application Schematic

5.1 SPI Mode Circuit (Triple Track)

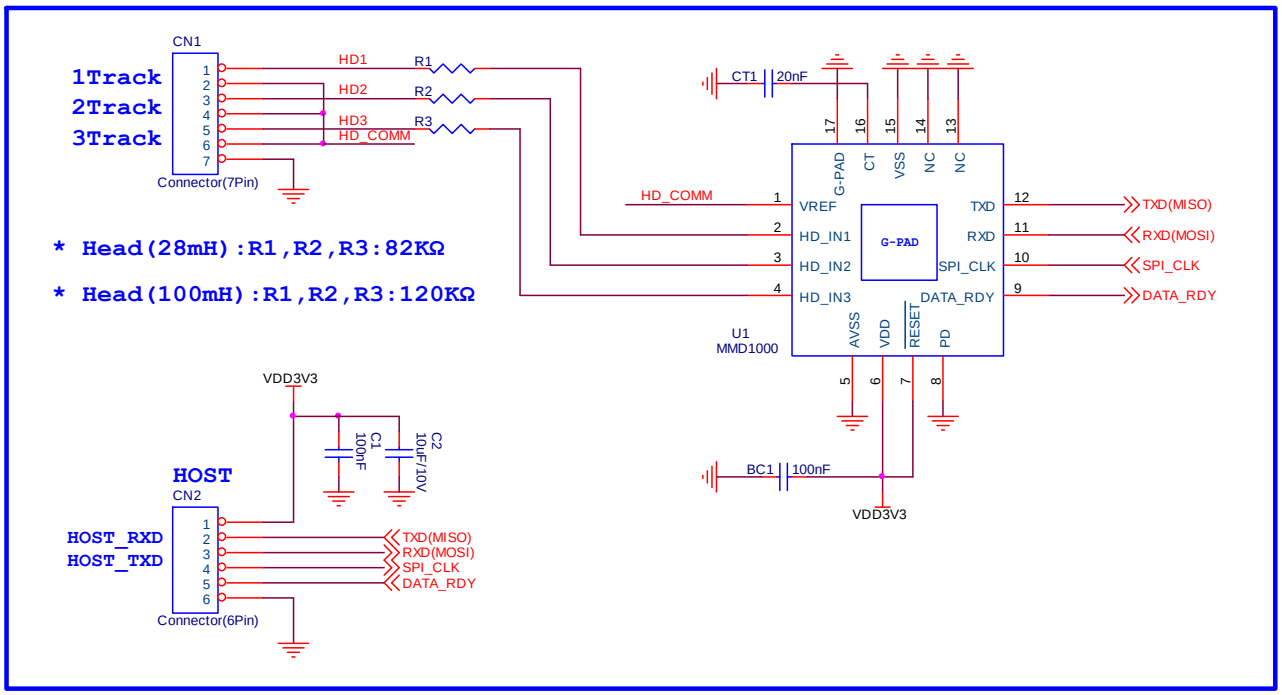


Figure 8: Triple Track Circuit (SPI Mode)

5.2 SPI Mode Circuit (Dual Track)

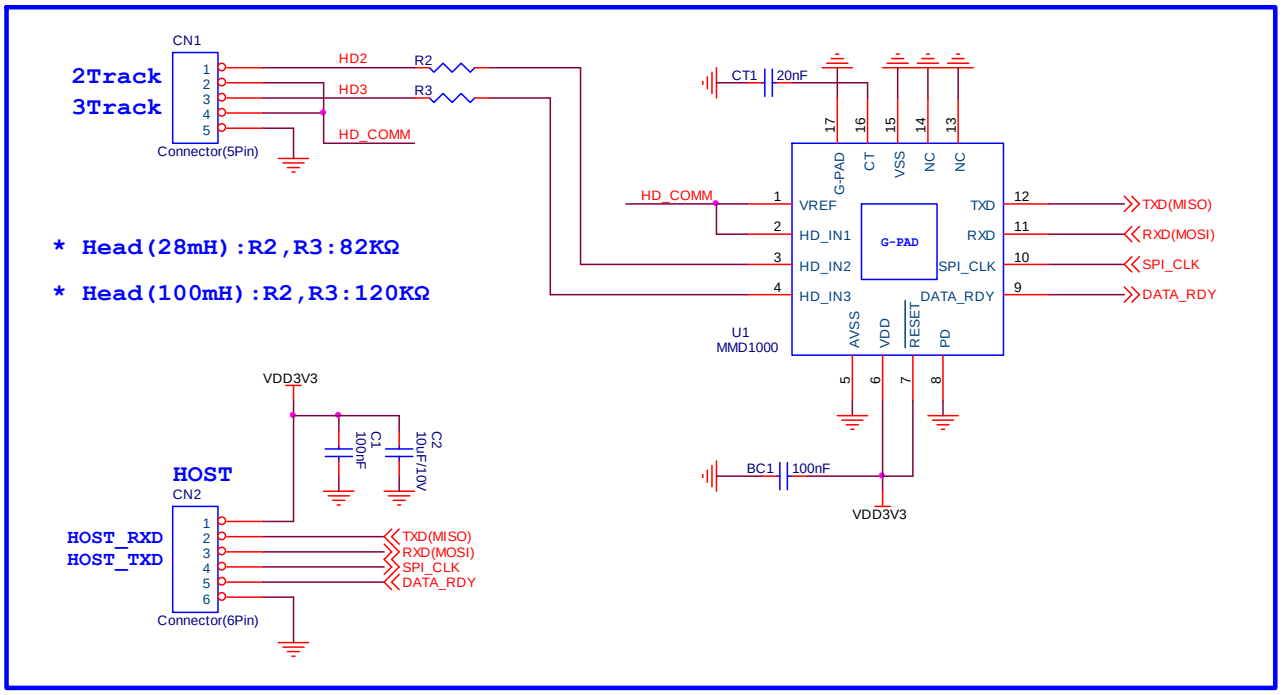


Figure 9: Dual Track Circuit (SPI Mode)

5.3 UART Mode Circuit (Triple Track)

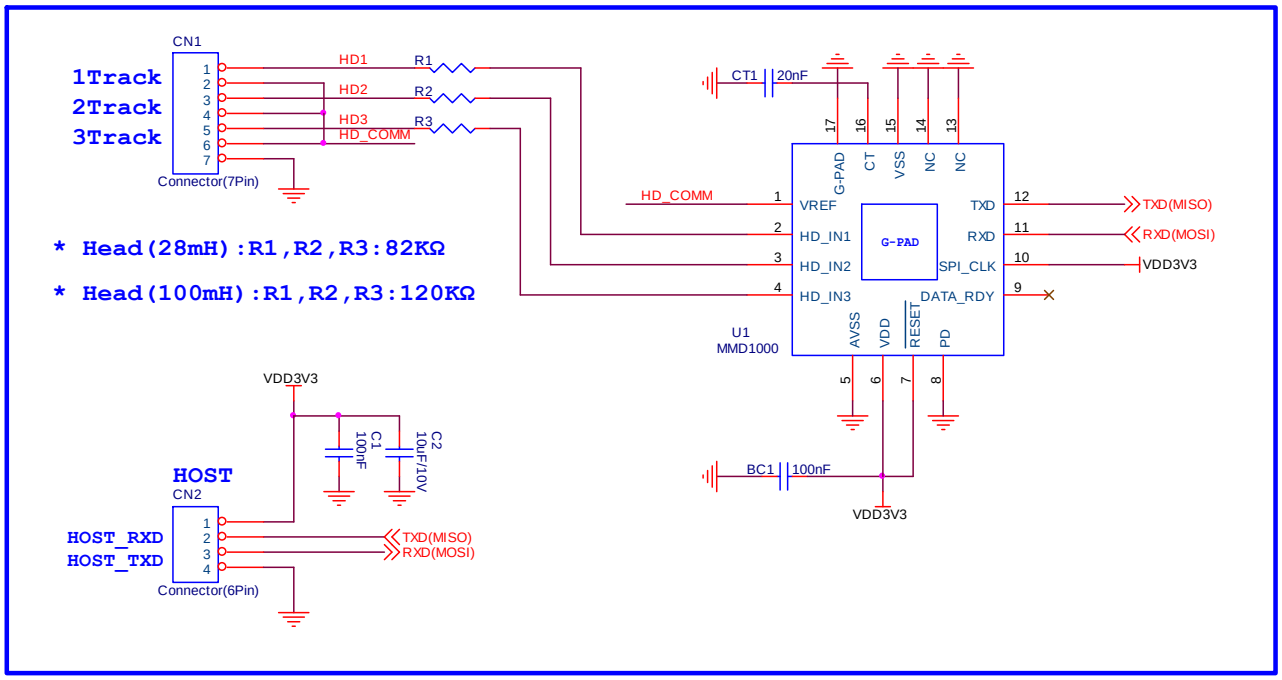


Figure 10: Triple Track Circuit (UART Mode)

5.4 UART Mode Circuit (Dual Track)

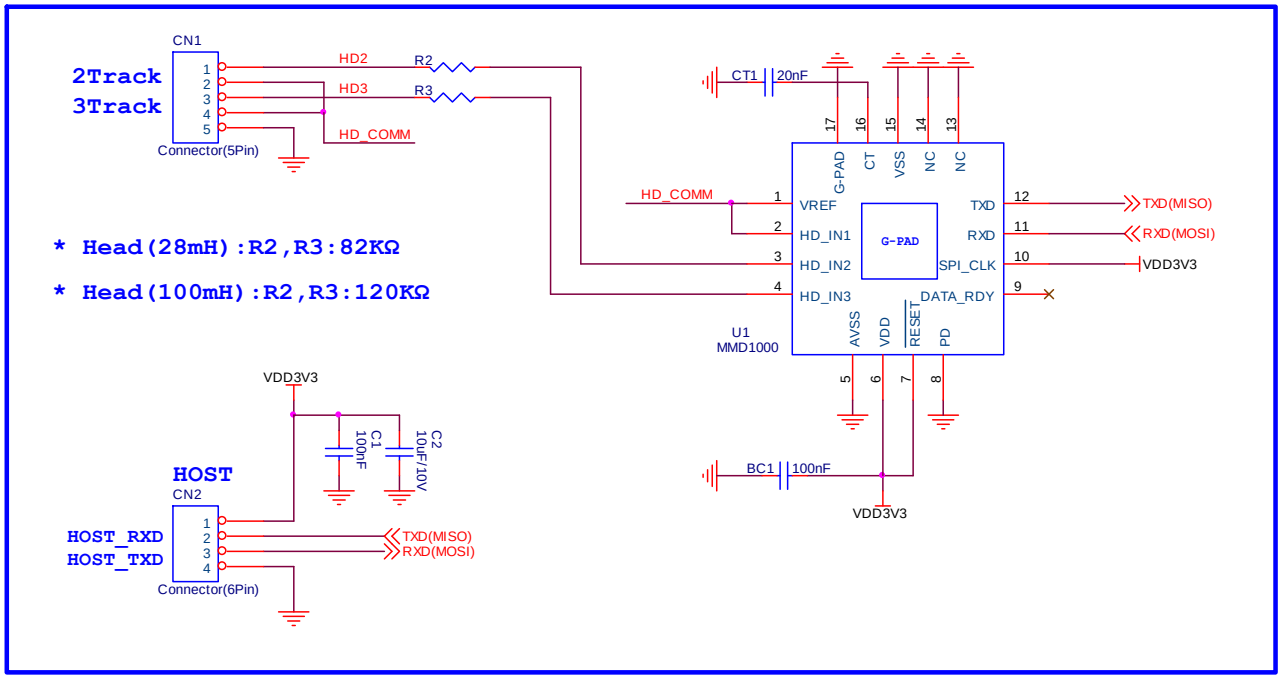
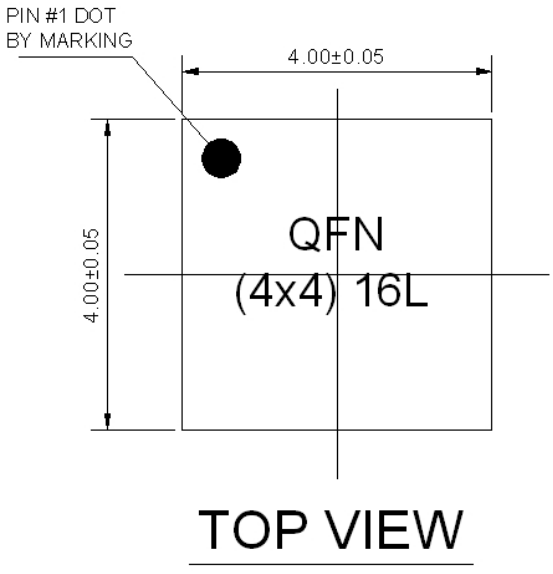
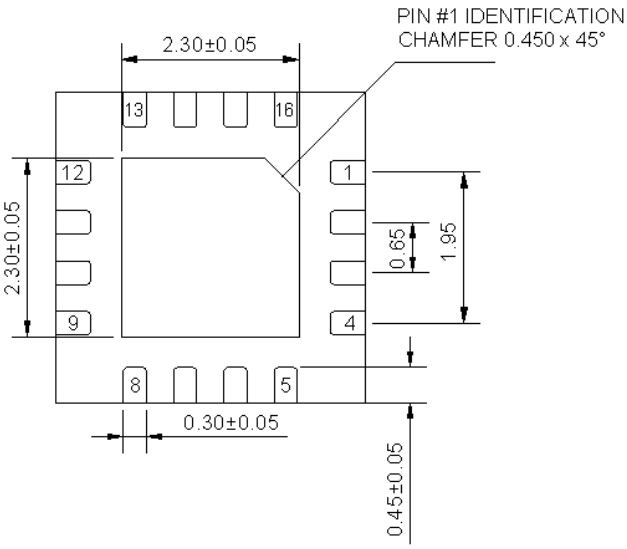


Figure 11: Dual Track Circuit (UART Mode)

6 Package Information: 4mm x 4mm, 16pin-QFN



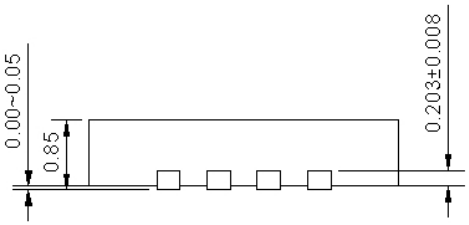
TOP VIEW



BOTTOM VIEW

NOTES

1. ALL DIMENSINS ARE IN MM UNLESS OTHERWUSE SPECIFIED



SIDE VIEW

7 Revision History

Revision number	Date	Remarks
A	05/11/2012	1. First draft
B	11/26/2012	2.Change application schematic
C	04/03/2013	3. Change Table6 contents
D	05/06/2013	4. Change normal current consumption
E	06/19/2013	5. Change Tx mode, operation temp and inform a restoration time of reset.