TSB43AA82 Storage Reference Design

Connectivity Solutions

ABSTRACT

A common application of TSB43AA82 (iSphynxII) is a 1394-enabled storage device. While there are solutions on the market targeted specifically at mainstream 1394 hard disk drives, iSphynxII is different in that it provides the system designer additional flexibility. This makes it ideal for non-standard storage solutions, such as MP3 players.

This document shows a simple iSphynxII-based storage solution. It includes a schematic, discusses design decisions, and identifies the software components necessary to complete the design.

References

1. TSB43AA82 (iSphynxII) Data Manual (SLLS461B)
2. Selection and Specification of Crystals for Texas Instruments IEEE 1394 Physical Layers (SLLA051)
3. Recommendation for PHY Layout (SLLA020A)
4. IEEE 1394 EMI Board Design and Layout Guidelines (SLLA117)
5. IEEE1394-1995 Specification and 1394a Amendment
6. Information Technology – AT Attachment with Packet Interface – v6 (ATA specification v6)
7. Serial Bus Protocol 2 (SBP-2) Specification
8. TI iSphynxII (TSB43AA82) Lynxsoft Firmware: Programmer's Guide (SLLU061)

1 Introduction

The TSB43AA82 iSphynxII device is a high-performance link layer controller with integrated PHY that can be used to implement an interface to the IEEE1394 serial bus. It is compliant with the IEEE 1394-1995 and IEEE1394.a-2000 specifications.

iSphynxII is designed for applications that require the rapid movement of bulk data – that is, data that does not require real-time streaming. In 1394 terminology, this type of transfer is referred to as *asynchronous* – that is, data that is not time-sensitive, but requires guaranteed delivery and accuracy. In contrast, *isochronous* data has guaranteed latency and bandwidth, but is not necessarily guaranteed delivery or accuracy.

A high-speed, 8/16-bit DMA interface called the *bulky data interface* equips iSphynxII with a way to communicate with memory devices. The bulky interface has several modes, allowing it to connect to various memory devices. However, one of the most useful is the ATA mode, which allows it to connect to hard disk drives (HDDs) and any other device that uses ATA's ultraDMA mode. Large transmit/receive FIFOs are employed. With a fast processor, an iSphynxII HDD storage system can achieve transfer rates of 15-25MB/s when interfaced to a typical PC, depending on the implementation**.**

Serial Bus Protocol-2 (SBP2) is an industry-standard way to exchange bulk data across the 1394 serial bus with storage devices such as disk drives, printers, etc., in peer-to-peer fashion. It is used to carry SCSI Reduced Block Commands (RBC) between an initiator (the PC) and a target (iSphynxII-based storage system). iSphynxII contains several SBP2 agents and accelerators in hardware that reduce processing load on the host MCU processor.

The host MCU is needed to conduct register reads/writes and PIO transfers with the ATA interface, as well as configure iSphynxII and oversee DMA transfers. Depending on the end application, the MCU may also serve other functions. For example, an MP3 player most likely will use a DSP such as TI's TMS320C55x platform to play MP3 files with audio circuitry after reading them from the hard drive via PIO.

It should be noted that iSphynxII does not implement the 16-bit CRC value required at the end of ATA ultraDMA transfers. There are two ways to deal with this. The first is to use HDDs that allow transfers to continue even if the correct CRC value is not received. The second is to insert an ASIC/PLD between iSphynxII and the HDD that calculates the CRC as the transfer is taking place and drives it to the drive at the appropriate time. This reference design assumes the HDD does not require the CRC.

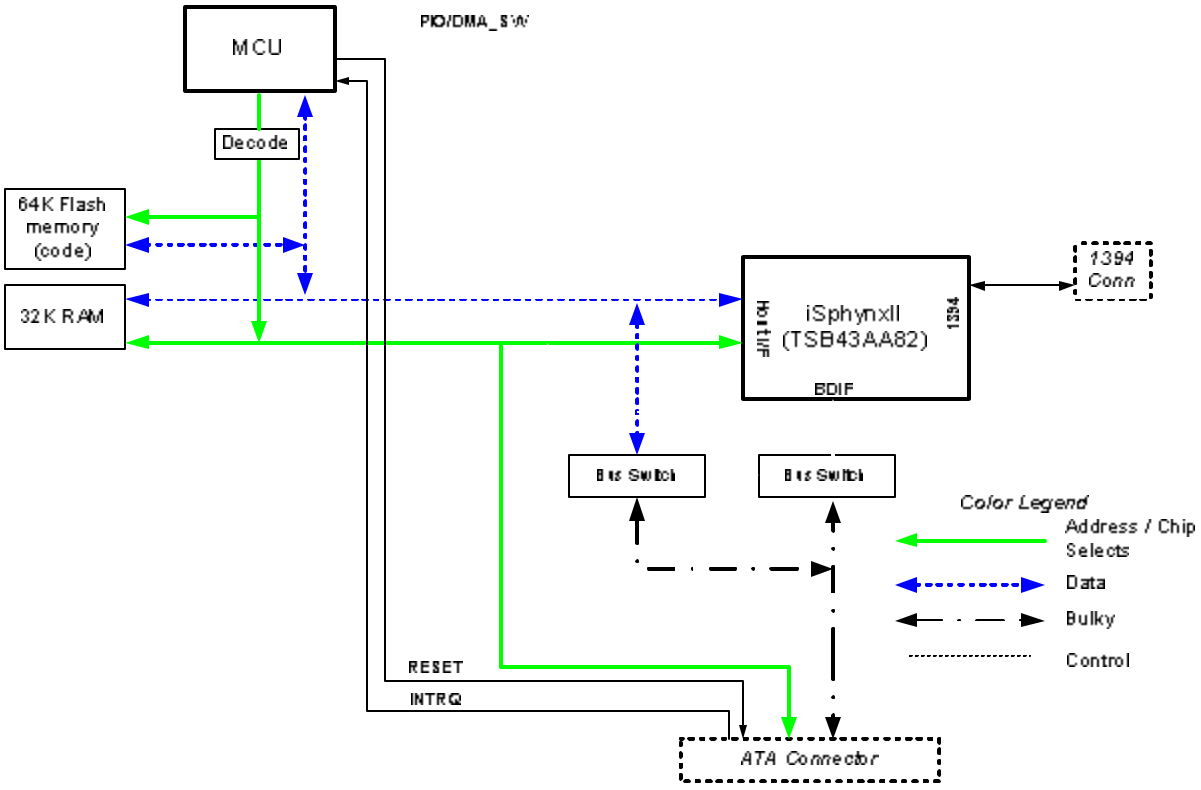
This document provides an example reference schematic for an iSphynxII storage interface. Design rationale is provided to assist the system engineer in understanding various points of the design, and thereby customizing it for the end application.

Note that this design has not been implemented as-is. However, it is based on designs built and tested by TI.

For other resources on IEEE1394, see http://www.ti.com/1394.

2 System Overview and Scope

The design implements a basic ATA interface. A block diagram for this system is shown in Figure 1.



Two specialized applications are described in the following sections.

2.1 MP3 Player

This design can be part of an MP3 player equipped with a 1394 interface. The most likely implementation would involve replacing the 8051-based MCU in this design with a DSP capable of processing the MP3 files, such as TI's TMS320C55x.

An MP3 player must be able to play files and transfer them with other devices. In the playback function, the DSP pulls the files from the HDD using PIO transfers and plays them back via on-board audio hardware. In the file transfer function, the DSP oversees the transfer of files to/from the HDD via iSphynxII.

2.2 CompactFlash

The "true IDE mode" of the CompactFlash specification is similar to ATA, and therefore can be used with iSphynxII. A notable limitation of true IDE mode is that it only supports PIO mode; no DMA transfers take place. For this reason, the connections between the iSphynxII bulky interface and the ATA connector shown in this design can be eliminated. Instead, when conducting transfers with other 1394 devices, the host processor must exchange data between the CompactFlash device and the host interface of iSphynxII. Throughput in this implementation is limited to PIO speeds.

3 Detailed Description

In the following descriptions, refer to Appendix A, which presents the schematic.

3.1 iSphynxII

This design only uses one of iSphynxII's two 1394 ports. The other one is terminated. TI's 1394a PHYs are terminated by leaving all port pins (TPA+/-, TPB+/-, and TPBIAS) open.

Note the placement of diode D1 on the CPS pin. On most TI PHYs, this diode is not necessary. It should be used with iSphynxII to deal with a device errata, and it can be any ordinary, small-signal diode capable of handling a forward continuous current of 75uA.

iSphynxII uses 1.8V for its digital core, and it has an on-chip 1.8-V regulator to derive it from the 3.3-V supply. If this regulator is to be used, the /EN pin should be pulled low. If an external regulator is to be used, /EN should be pulled high, and the 1.8-V source should be connected to the PWTST and DVDn pins. However, if 1.8V is supplied externally, it is important that the 3.3V be raised first. At no point should the voltage on the 1.8-V rail exceed the voltage of the 3.3-V rail. See the data manual for more information.

LPS, PD, and PLLON are all tied to fixed values in this design, but since they control the low-power states of the device, these should be configured by power management logic in a real-world design.

PWRCLSn report the draw from, or contribution to, bus power on the 1394 bus. The bus manager uses this information to manage power distribution. Be sure to set these values correctly, as specified by the 1394a specification.

Oscillator frequency is very important in high-speed bus designs. See the *Selection and Specification of Crystals for Texas Instruments IEEE 1394 Physical Layers* document for information about crystal selection. Be sure to verify that the frequency is within the tolerance allowed by 1394 (24.576MHz +/-100ppm).

Several bulky interface signals are not used in ATA mode, such as BDOCLK, BDICLK, and BDOEN/BDRD. In this design, the unused inputs are tied to ground, and the unused outputs are left open. In addition, since it is possible to disable BDOCLK by tying BDOCLKDIS high, this action is taken.

Note that if power draw is an important consideration, and iSphynxII is to be placed in one of the low-power modes, it is very important that all input pins have pullups or pulldowns attached. (50-100kOhm should be sufficient.) If the inputs of a chip are left floating, they can increase the device's power draw on the order of milliamps. These are implemented in this design as RN1 and RN2 on the Power page (section A.5).

Note also that when iSphynxII is in a low power mode, BDOCLK reverts to an input. This means that if power draw is a concern, it is necessary to provide a pulldown here as well. If BDOCLKDIS is permanently tied high, disabling the BDOCLK output, BDOCLK can be connected directly to ground.

A fixed value of "010" is given to BDIF[2:0]. This is the value that should always be applied during ATA mode transfers.

See *Recommendation for PHY Layout (SLLA020A)* for information about correctly laying out the board around the device. This app note is targeted at discrete PHY applications, rather than integrated devices like iSphynxII, but most of the principles still apply. Note that there is no PHY/link interface in iSphynxII, which reduces the possibility of EMI problems.

3.2 MCU

This design shows connection to an 8051-based microcontroller, the Philips XA-G37. This is a 16-bit version of the standard 8051 architecture. Other processors can be used, such as a DSP for audio applications.

A fast processor can greatly enhance system throughput. This is clearly true with PIO transfers, where the processor handles every data word, but it is also true for large blocks of data involving multiple DMA transfers. This is because the processor must conduct register accesses to the storage volume and iSphynxII to set up each transfer. Therefore, minimizing the length of the gaps between DMA transfers is key to enhancing throughput.

Code storage is shown in the form of a 128KB flash memory device. TI's iSphynxII Lynxsoft Firmware requires less than 64KB of code space. A RAM device provides 32KB working memory.

The PIO/DMA_SW signal controls which device can talk to the ATA interface – the MCU (via register reads/writes and PIO transfers) or iSphynxII (via DMA transfers over the bulky data interface). This will be discussed in further detail in the next section.

Interrupts can be received from either iSphynxII or from ATA. Because ATA has active-high interrupts, and the 8051 architecture requires active-low, an inverter is used.

A decoder device is used to generate the three chip selects used in this system. (The 8051 architecture does not provide integrated chip selects.) One is for iSphynxII, while the other two form the CS1/0 signals specified by ATA. Conveniently, "00" is an unused state for CS1/0; therefore a '138 decoder device with inverted outputs can easily generate the signals from the address lines. A15, the most significant address bit, controls whether the MCU is talking to local RAM or to the rest of the system.

3.3 ATA

The connector shown is for a 2.5" ("laptop") hard drive (specifically the 50/44-pin connector shown in section A.4 of the ATA specification), but any drive can be used.

If the hard drive's logic is powered by 5V, it is necessary to level-shift these down to the 3.3-V rail used for iSphynxII. iSphynxII's I/Os are *not* 5V-tolerant. In actuality, many HDDs with 5V-powered logic drive less than 5V, often under 4V. The absolute maximum input level specified in the iSphynxII data manual is V_{DD} + 0.5V, which is a nominal 3.8V. However, even if the drive signals always stay under 3.8V, TI still does not recommend this configuration because the long-term effects of driving above VDD are unknown. It is best to either use a storage device that can be driven from a 3.3V supply, or use signal conditioning such as that utilized in this design.

As discussed earlier, the primary purpose of the bus switches is to control whether the host or iSphynxII has access to the ATA device and to isolate the other device from the bus. Since only one should be active at a time, they are controlled by a single signal, PIO/DMA_SW, with an inverter on one of them.

Pullups and pulldowns are provided on the ATA connector, as required by the ATA specification. (Pullups/downs are also provided for /DIOW, /DIOR and /DMACK. These ensure that no glitches occur while the bus switches are transitioning from one to the other.)

iSphynxII is designed primarily to use UltraDMA mode 2, as described in Table 57 of the ATA specification. Multiword transfers are not supported.

3.4 Power

This device is bus-powered, meaning it draws all necessary power from the 1394 bus. The PWRCLS pins reflect this. Specifically, a value of 110b indicates this device is bus-powered, draws no more than 3W when the link is powered down, and less than 6W when fully-powered. The circuitry in this system other than the HDD should consume well under 0.5W in all conditions. The HDD, which is the largest power draw in this system, is only activated when the system is fully-powered. Power consumption can vary widely among the various HDD types, but most 2.5" ("laptop") drives consume 3W or less.

Since 1394 bus power can range from 8-33V, the regulators must be capable of handling this level of input.

As discussed in section 3.1, the iSphynxII inputs must have pullup or pulldown resistors if power draw is a concern while in low-power modes. This is the purpose of RN1 and RN2.

3.5 Address Space

The following table shows the memory map. Reference the TSB43AA82 data manual and the ATA specification for detailed descriptions of the registers.

Table 1. Memory Map

Group	Detail	Address
Data RAM	Data RAM	0000h-7FFFh
iSphynxII	Defined in data manual	8000h-80FFh
Reserved	Reserved	8100h-8105h
ATA	Alternate Status Register / Device Control Register	8106h
	Reserved	8107h-81FFh
	Data Register	8200h
	Error Register / Features Register	8201h
	Sector Count Register	8202h
	Sector Number Register	8203h
	Cylinder Low Register	8204h
	Cylinder High Register	8205h
	Device/Head Register	8206h
	Command Register / Status Register	8207h
	Data Port	*
Reserved	Reserved	8208h-FFFFh

* The data port is accessed by writing to any of the addresses outside the ATA range.

4 Software

Two software needs must be addressed when designing an iSphynxII storage solution. The first is firmware for the host MCU. This firmware must handle the SBP2 commands from the PC, manage the DMA transfers, and configure both iSphynxII and the ATA device. TI provides a firmware codebase that can be the starting point of an iSphynxII-based storage system, called the iSphynxII Lynxsoft Firmware. It covers all basic SBP2 functions and SCSI commands, and once adapted to a particular platform, it allows the volume to mount on an SBP2 initiator-capable computer. The code does not provide error-handling functionality, and if any customized features are to be provided in the end application, this code will need to be added as well. For more information, reference the document TI iSphynxII (TSB43AA82) Lynxsoft Firmware: Programmer's Guide (SLLU061).

The second software need is for the PC itself (the SBP-2 "initiator"). As with any external 1394 or USB storage volume, the PC must be equipped with a compatible mass storage driver and application code that can talk to the volume. Windows 2000/ME/XP and Mac OS X provide native support for mounting an SBP2-compliant 1394 drive, and service packs for Windows 98/SE and Mac OS 9 include these drivers as well.

Appendix A. Reference Schematic

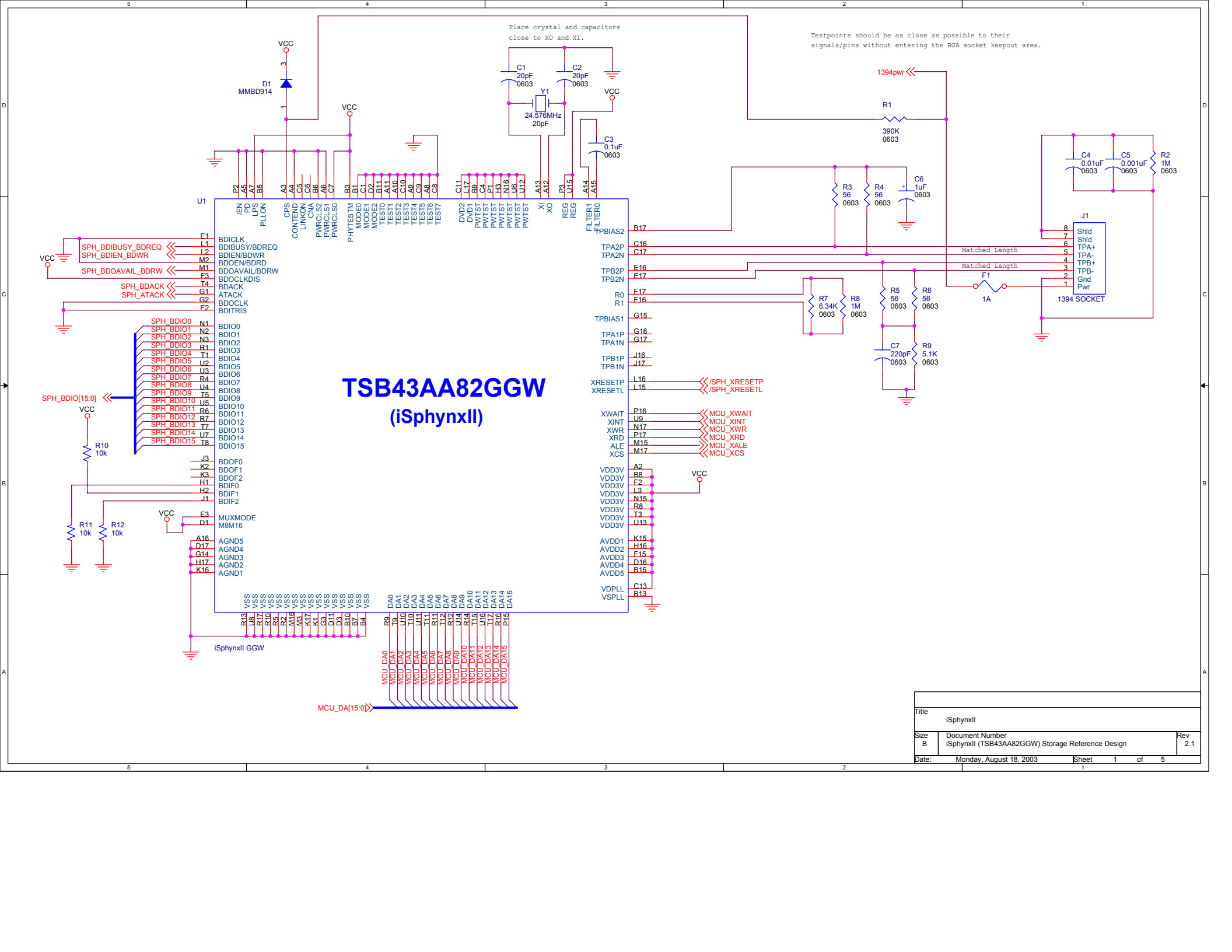
Figure A-1. iSphynxII

Figure A-2. iSphynxII Supporting Circuitry

Figure A-3. MCU

Figure A-4. ATA

Figure A-5. Power/Resets


Place crystal and capacitors close to XO and XI.
Testpoints should be as close as possible to their signals/pins without entering the BGA socket keepout area.
TSB43AA82GGW
(iSphynxII)
U1
D1
MMBD914
C1
20pF
0603
C2
20pF
0603
Y1
24.576MHz
20pF
C3
0.1uF
0603
R1
390K
0603
1394pwr
R2
1M
0603
C4
0.01uF
0603
C5
0.001uF
0603
R3
56
0603
R4
56
0603
C6
1uF
0603
R5
56
0603
R6
56
0603
R7
6.34K
0603
R8
1M
0603
C7
220pF
0603
R9
5.1K
0603
F1
1A
J1
1394 SOCKET
Matched Length
Matched Length
R10
10k
R11
10k
R12
10k
VCC
SPH_BDIBUSY_BDREQ
SPH_BDIEN_BDWR
SPH_BDOAVAIL_BDRW
SPH_BDACK
SPH_ATACK
SPH_BDIO[15:0]
/SPH_XRESETP
/SPH_XRESETL
MCU_XWAIT
MCU_XINT
MCU_XWR
MCU_XRD
MCU_XALE
MCU_XCS
MCU_DA[15:0]
iSphynxII GGW
Title
iSphynxII
Size
B
Document Number
iSphynxII (TSB43AA82GGW) Storage Reference Design
Rev
2.1
Date:
Monday, August 18, 2003
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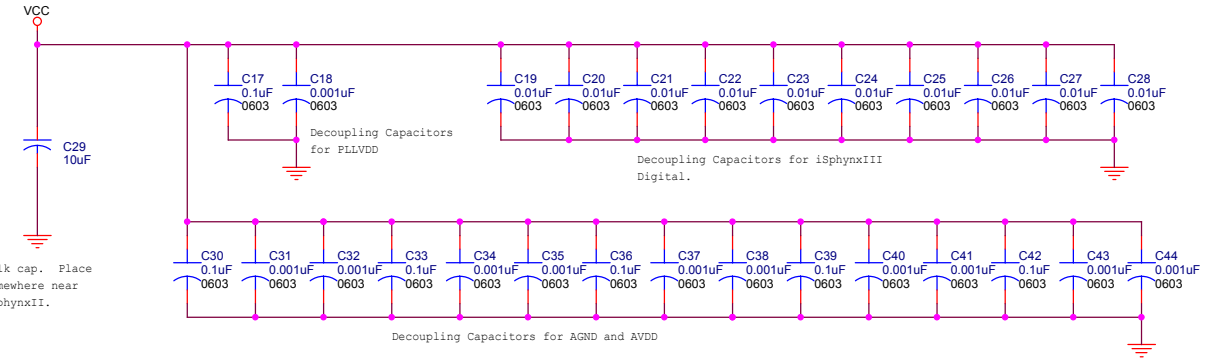
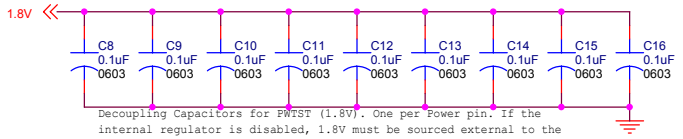
5

iSphynxII Capacitors





Title	iSphynxII Support	
Size B	Document Number iSphynxII (TSB43AA82GGW) Storage Reference Design	Rev 2.1
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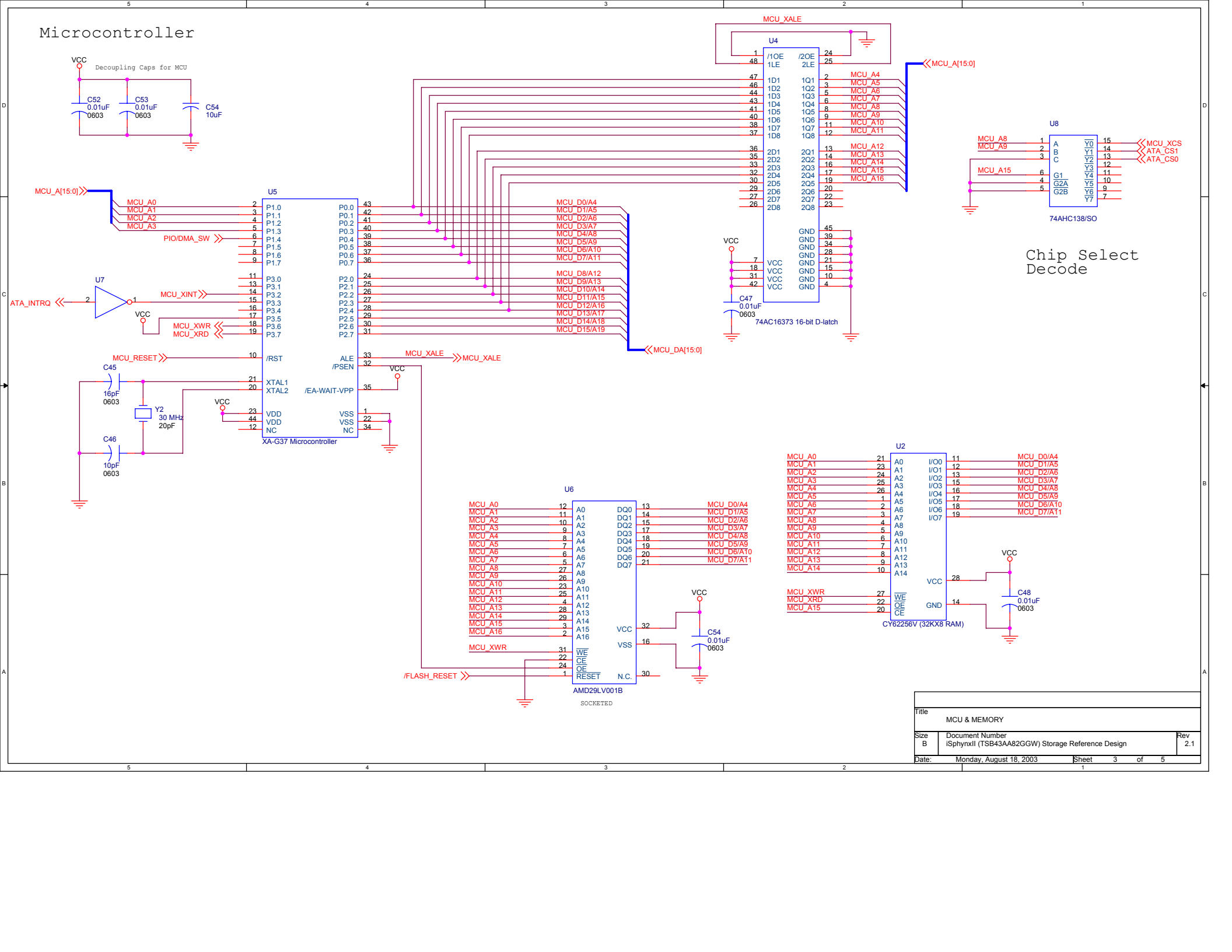
Microcontroller



Title	MCU & MEMORY	
Size B	Document Number iSphynxII (TSB43AA82GGW) Storage Reference Design	Rev 2.1
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2.5" ATAPI Connector (direct to Sphynx)

PIO Transfers

U9
SN74CBTD3861 10-bit
Level-Shifting Bus Switch

U10

DMA Transfers

U11
SN74CBTD16211

5V/3V Level-shifting
bus switches

Keep connector within 3" of iSphynxII
J2
44/50-PIN 2.5" ATA/ATAPI CONNECTOR
Place resistors as close to connector as possible

Bus Switch
Bypass Caps
(one per
device)

Title	50/44-pin ATA Connector
Size B	Document Number iSphynxII (TSB43AA82GGW) Storage Reference Design
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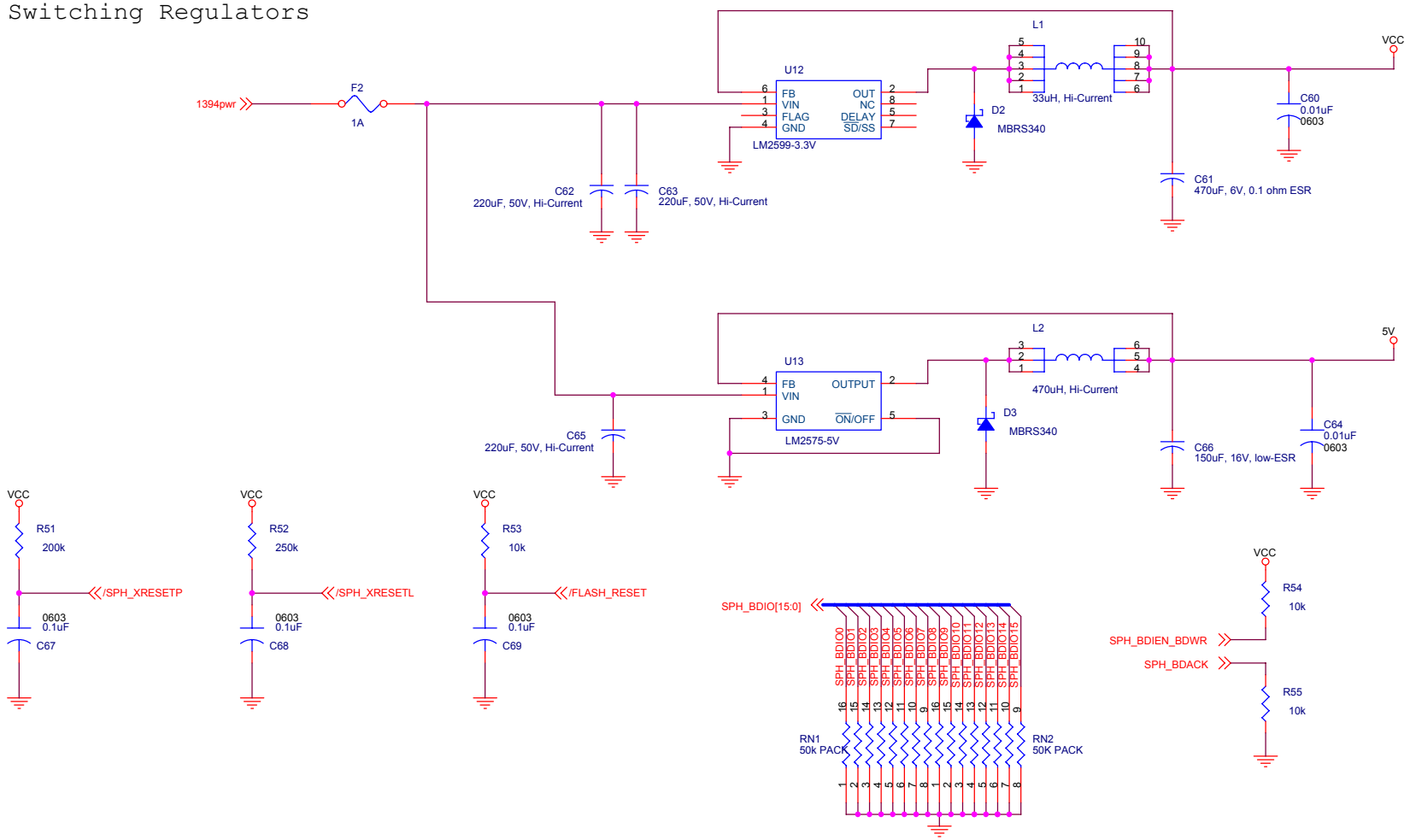
Switching Regulators



Title	POWER & RESET	
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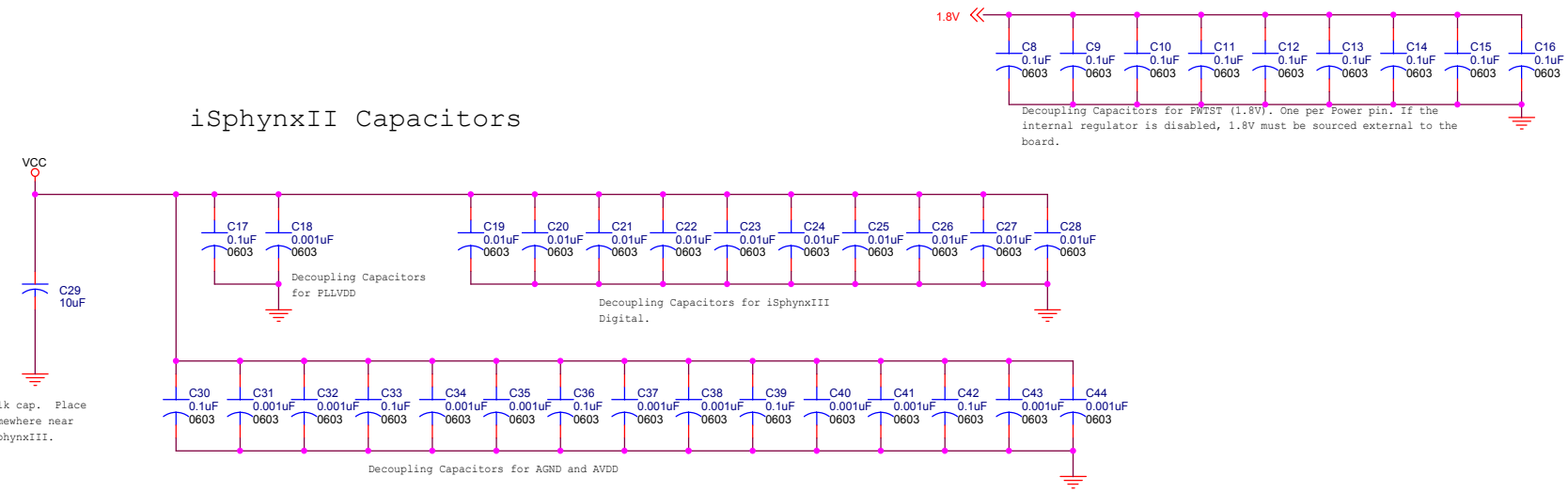
iSphynxII Capacitors



Title	iSphynxII Support	
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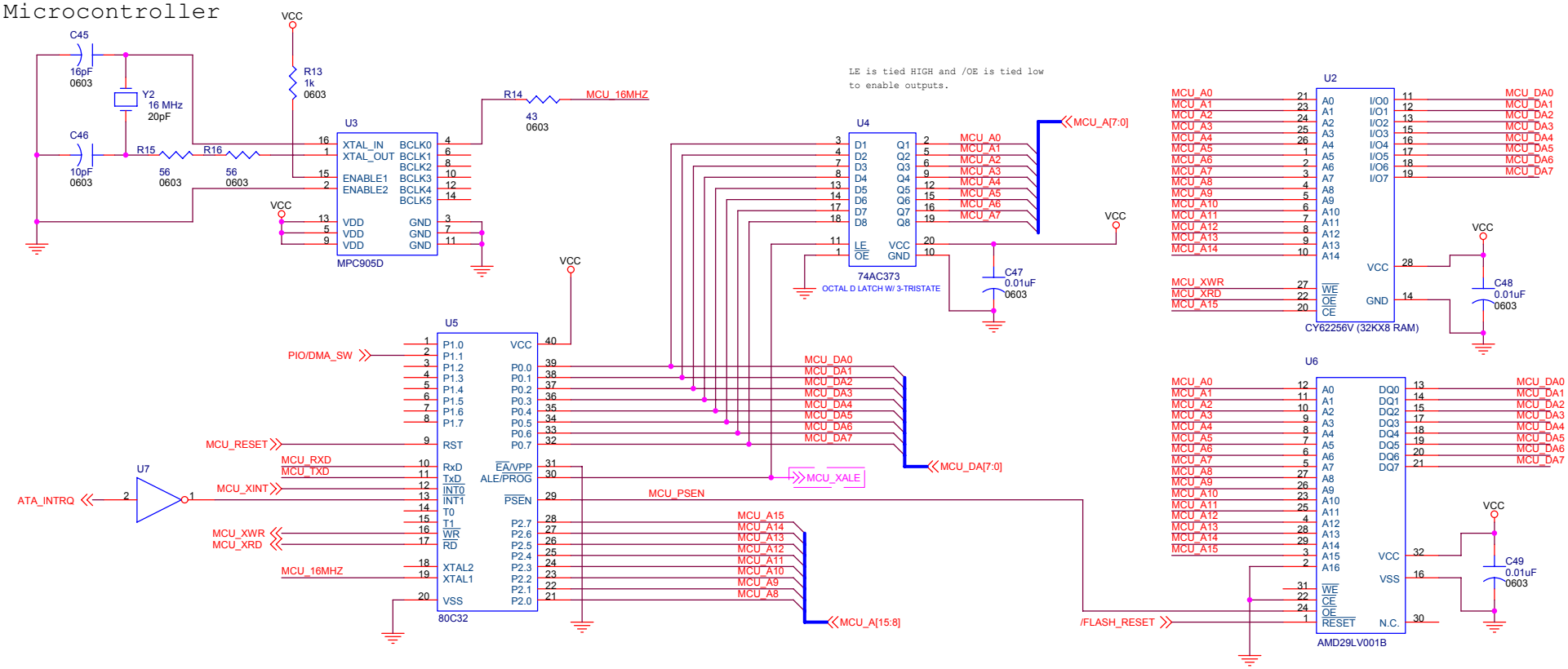
Microcontroller



Chip Select Decode

Title	MCU & MEMORY	
Size B	Document Number iSphynxII (TSB43AA82GGW) Storage Reference Design	Rev 2.1
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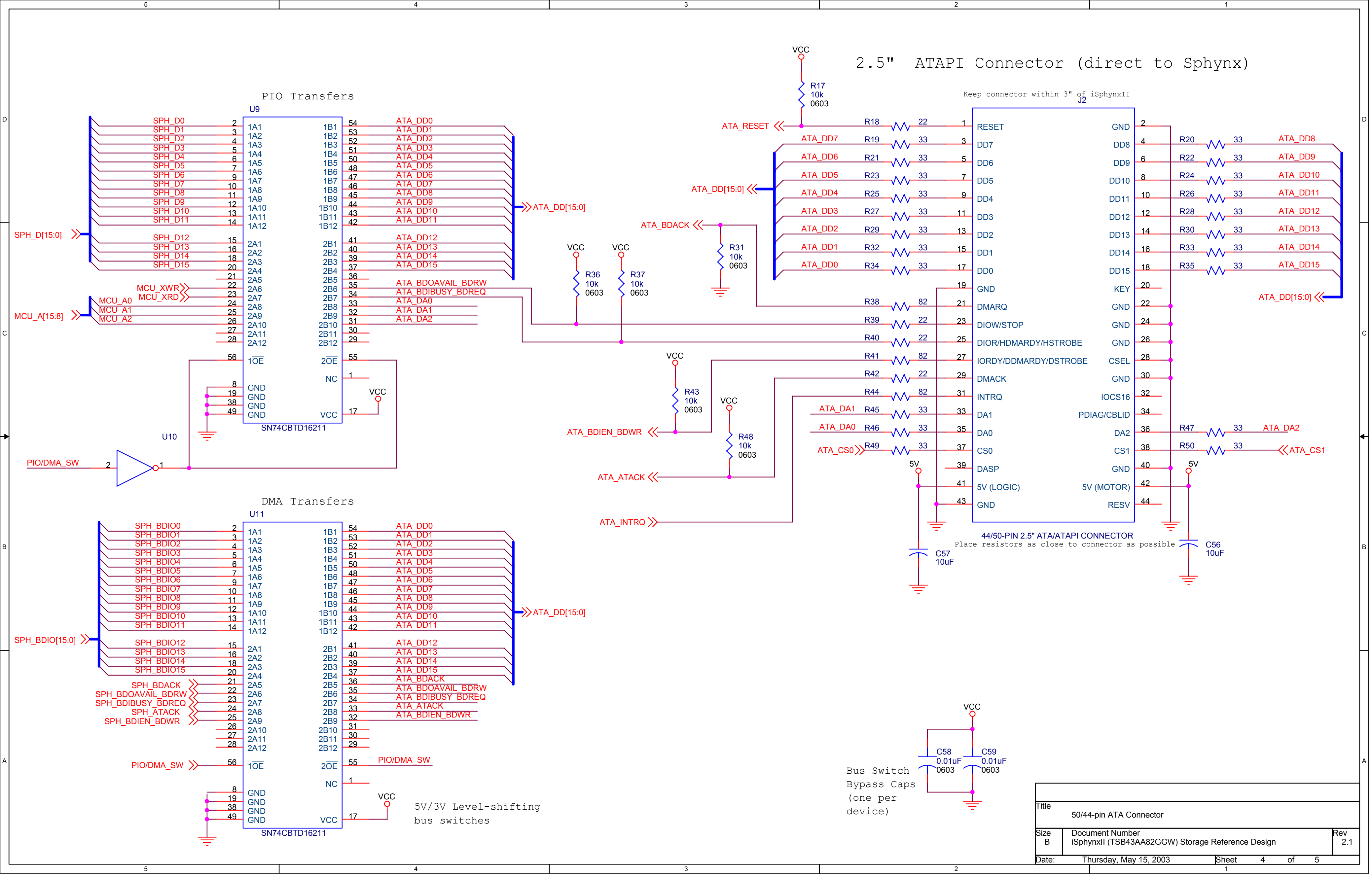

2.5" ATAPI Connector (direct to Sphynx)
Keep connector within 3" of iSphynxII
PIO Transfers
DMA Transfers
SN74CBTD16211
44/50-PIN 2.5" ATA/ATAPI CONNECTOR
Place resistors as close to connector as possible
Bus Switch Bypass Caps (one per device)
5V/3V Level-shifting bus switches
Title
50/44-pin ATA Connector
Size B
Document Number
iSphynxII (TSB43AA82GGW) Storage Reference Design
Rev 2.1
Date: Thursday, May 15, 2003
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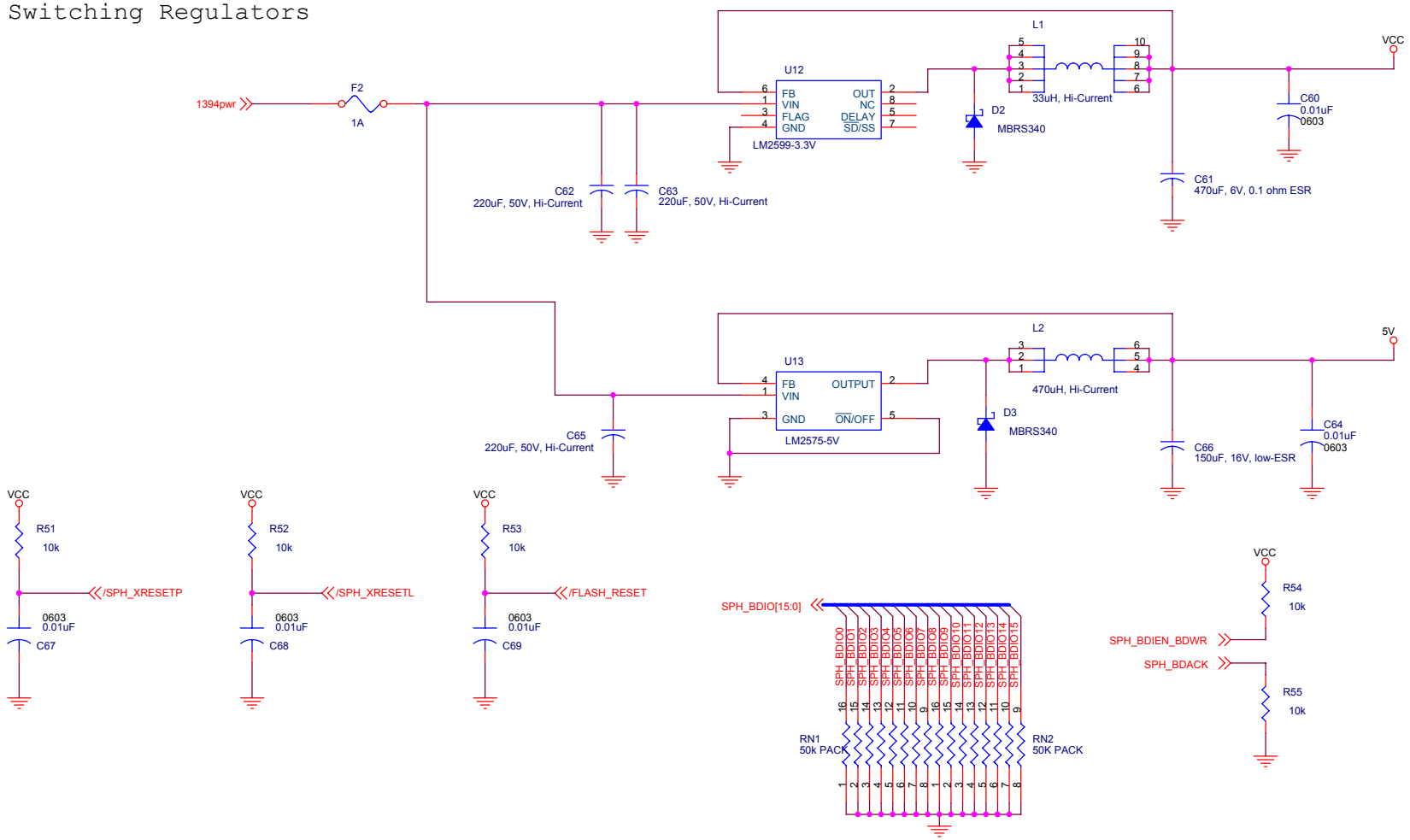
Switching Regulators



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