M74LS112AP

DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOPS WITH SET AND RESET

DESCRIPTION

The M74LS112AP is a semiconductor integrated circuit containing 2 J-K negative edge-triggered flip-flop circuits with discrete terminals for clock input $\overline{T}$, J and K inputs and direct set and reset inputs $\overline{S_D}$ and $\overline{R_D}$.

FEATURES

- Negative edge-triggering
- Independent input/output terminals for each flip-flop.
- Direct set and reset inputs
- Q and $\overline{Q}$ outputs
- Wide operating temperature range (T_a = -20 ~ +75°C)

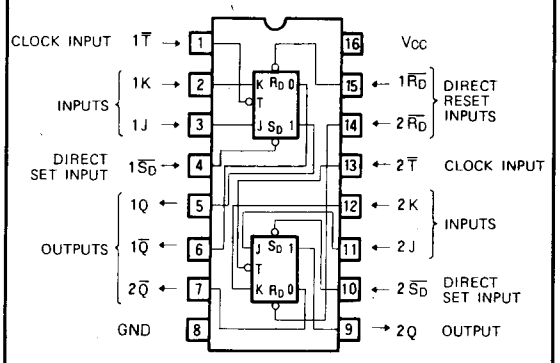
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

J and K signals of are read, while $\overline{T}$ is high. When $\overline{T}$ changes from high to low, the signals of J and K immediately before the change appear in outputs Q and $\overline{Q}$ in accordance with the function table. By using $\overline{S_D}$ and $\overline{R_D}$, this IC can be made into an direct R-S flip-flop. When both $\overline{S_D}$ and $\overline{R_D}$ are low, Q = $\overline{Q}$ = high. However, when both of them changed to high at the same time, the status of Q and $\overline{Q}$ cannot be anticipated. For use as a J-K flip-flop, keep $\overline{S_D}$ and $\overline{R_D}$ high. M74LS112AP is the same as M74LS76AP except for pin configuration.

PIN CONFIGURATION (TOP VIEW)



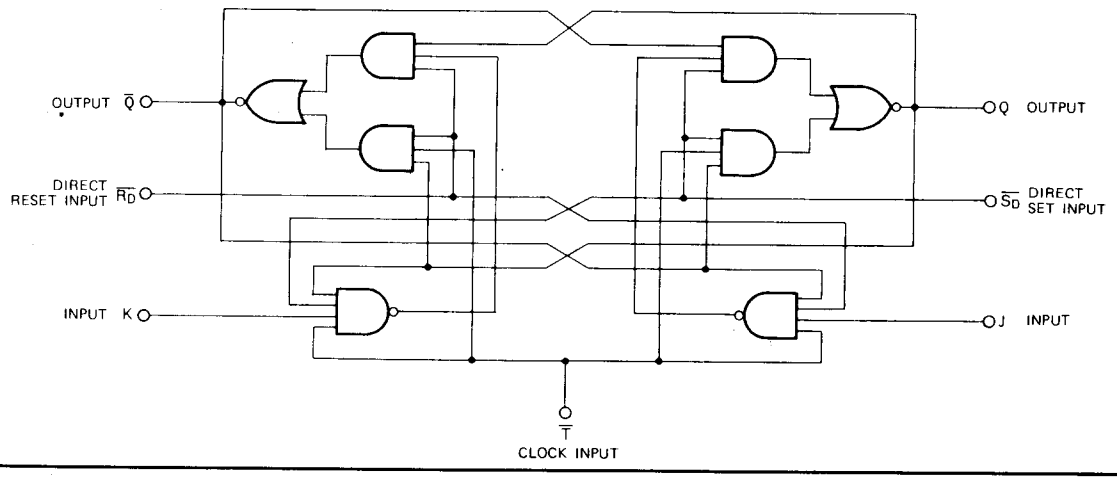
Outline 16P4

FUNCTION TABLE (Note 1)

$\overline{T}$	$\overline{S_D}$	$\overline{R_D}$	J	K	Q	$\overline{Q}$
X	L	H	X	X	H	L
X	H	L	X	X	L	H
X	L	L	X	X	H*	H*
↓	H	H	H	H	Toggle	
↓	H	H	L	H	L	H
↓	H	H	H	L	H	L
↓	H	H	L	L	Q^0	$\overline{Q^0}$
H	H	H	X	X	Q^0	$\overline{Q^0}$

Note 1. ↓ : transition from high to low-level
X : irrelevant
* : Q = $\overline{Q}$ = high when $\overline{S_D}$ = $\overline{R_D}$ = low and so when both $\overline{S_D}$ and $\overline{R_D}$ are set high, the status of Q and $\overline{Q}$ cannot be anticipated.
Q^0: level of Q before the indicated steady-state input conditions were established.
$\overline{Q^0}$: level of $\overline{Q}$ before the indicated steady-state input conditions were established.
Toggle : complement of previous state with ↓ transition of outputs

BLOCK DIAGRAM (EACH FLIP FLOP)



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DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOPS WITH SET AND RESET

ABSOLUTE MAXIMUM RATINGS (T_a = −20 ~ + 75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
T_{opr}	Operating free-air ambient temperature range		−20 ~ +75	°C
T_{stg}	Storage temperature range		−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS (T_a = −20 ~ + 75°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS (T_a = −20 ~ + 75°C, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ *	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage		V_{CC} = 4.75V, I_{IC} = −18mA				−1.5	V
V_{OH}	High-level output voltage		V_{CC} = 4.75V, V_I = 0.8V		2.7	3.4		V
			V_I = 2V, I_{OH} = −400μA					
V_{OL}	Low-level output voltage		V_{CC} = 4.75V	I_{OL} = 4mA		0.25	0.4	V
			V_I = 0.8V, V_I = 2V	I_{OL} = 8mA		0.35	0.5	V
I_{IH}	High-level input current	J, K	V_{CC} = 5.25V, V_I = 2.7V				20	μA
		$\overline{S_D}$, $\overline{R_D}$					60	
		$\overline{T}$					80	
		J, K	V_{CC} = 5.25V, V_I = 10V				0.1	mA
		$\overline{S_D}$, $\overline{R_D}$					0.3	
		$\overline{T}$					0.4	
I_{IL}	Low-level input current	J, K	V_{CC} = 5.25V, V_I = 0.4V				−0.4	mA
		$\overline{S_D}$, $\overline{R_D}$, $\overline{T}$					−0.8	
I_{OS}	Short-circuit output current (Note 3)		V_{CC} = 5.25V, V_O = 0V		−20		−100	mA
I_{CC}	Supply current		V_{CC} = 5.25V (Note 4)			4	6	mA

* : All typical values are at V_{CC} = 5V, Ta = 25°C.

Note 2: S_D and R_D should not both be set to 0.4V simultaneously.

Note 3: All measurements should be done quickly, and not more than one output should be shorted at a time.

Note 4: I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, $\overline{T}$ input is grounded.

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 15pF (Note 5)	30	45		MHz
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time from input $\overline{T}$ to output Q, $\overline{Q}$			6	20	ns
t_{PHL}				7	20	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{S_D}$, $\overline{R_D}$ to output Q, $\overline{Q}$			7	20	ns
t_{PHL}				7	20	ns

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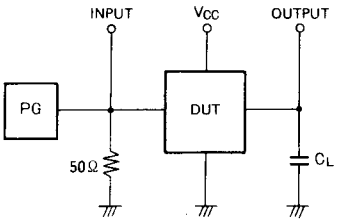
Note 4: Measurement circuit

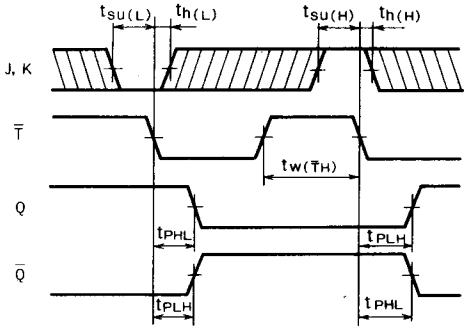


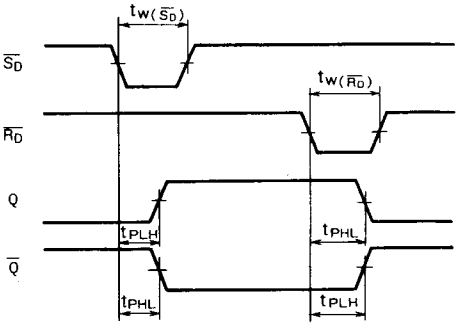
(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns,
V_P=3V_{P-P}, Z_O = 50Ω
(2) C_L includes probe and jig capacitance.

TIMING REQUIREMENTS (V_{CC} = 5V, T_a = 25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{w(\overline{T}H)}$	Clock input $\overline{T}$ high pulse width		20	12		ns
$t_{w(\overline{S_D},\overline{R_D})}$	Direct set and reset inputs $\overline{S_D}$, $\overline{R_D}$ pulse width		25	4		ns
t_r	Clock rise time			650	100	ns
t_f	Clock pulse fall time			900	100	ns
$t_{SU(H)}$	Setup time high J, K to $\overline{T}$		20	12		ns
$t_{SU(L)}$	Setup time low J, K to $\overline{T}$		20	12		ns
$t_{h(H)}$	Hold time high J, K to $\overline{T}$		0	−10		ns
$t_{h(L)}$	Hold time low J, K to $\overline{T}$		0	−6		ns

TIMING DIAGRAM (Reference level = 1.3V)





Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance.

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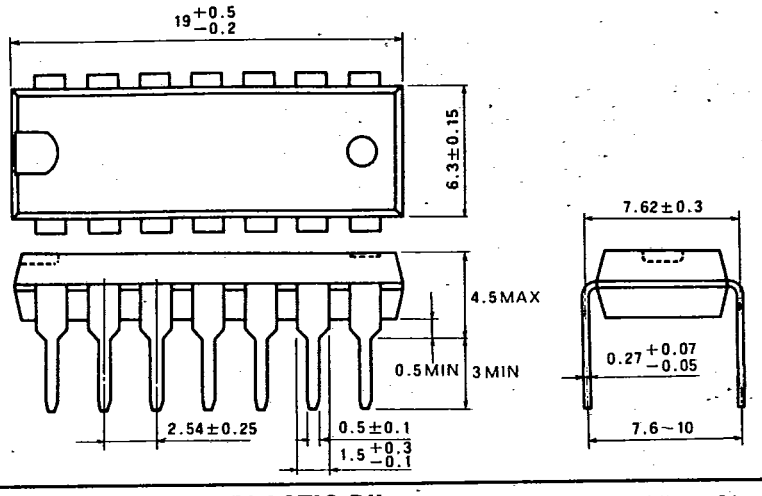
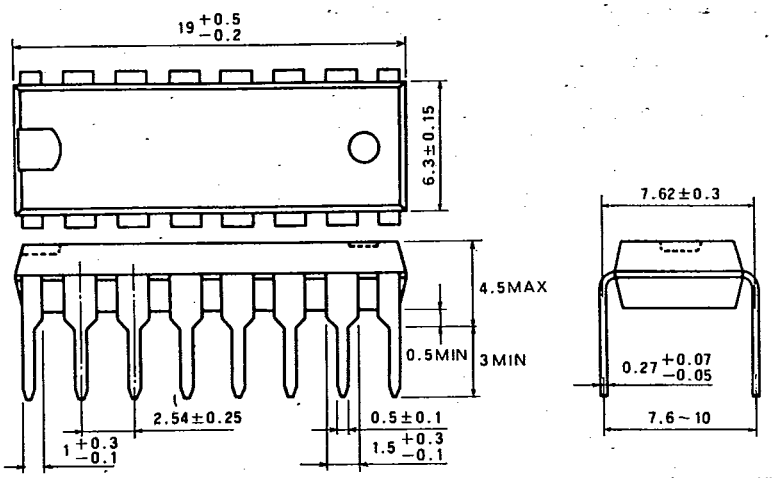
TYPE 14P4 14-PIN MOLDED PLASTIC DIL

Dimension in mm



TYPE 16P4 16-PIN MOLDED PLASTIC DIL

Dimension in mm



TYPE 20P4 20-PIN MOLDED PLASTIC DIL

Dimension in mm