

SERIES 15830, SERIES 15930 DTL INTEGRATED CIRCUITS

DTL SMALL-SCALE INTEGRATION (SSI)

Function	Operating Temperature		Packages*	
	Ranges		Dual-In-	
	-55°C to 125°C	0°C to 75°C	Line	Flat
GATES WITH 6-kΩ PULL-UP RESISTORS				
Expandable Dual 4-Input NAND Gates	SN 15930	SN 15830	J	N U
Quadruple 2-Input NAND Gates	SN 15946	SN 15846	J	N U
Triple 3-Input NAND Gates	SN 15962	SN 15862	J	N U
Dual 5-Input NAND Gates	SN 151900	SN 151800	J	N U
Expandable 8-Input NAND Gates	SN 151902	SN 151802	J	N U
10-Input NAND Gates	SN 151904	SN 151804	J	N U
Quadruple 2-Input AND Gates	SN 151906	SN 151806	J	N U
Quadruple 2-Input OR Gates	SN 151908	SN 151808	J	N U
Quadruple 2-Input NOR Gates	SN 151910	SN 151810	J	N U
Quadruple 2-Input Exclusive-OR Gates	SN 151912	SN 151812	J	N U
GATES WITH 2-kΩ PULL-UP RESISTORS				
Quadruple 2-Input NAND Gates	SN 15949	SN 15849	J	N U
Expandable Dual 4-Input NAND Gates	SN 15961	SN 15861	J	N U
Triple 3-Input NAND Gates	SN 15963	SN 15863	J	N U
Dual 5-Input NAND Gates	SN 151901	SN 151801	J	N U
Expandable 8-Input NAND Gates	SN 151903	SN 151803	J	N U
10-Input NAND Gates	SN 151905	SN 151805	J	N U
Quadruple 2-Input AND Gates	SN 151907	SN 151807	J	N U
Quadruple 2-Input OR Gates	SN 151909	SN 151809	J	N U
Quadruple 2-Input NOR Gates	SN 151911	SN 151811	J	N U
POWER/BUFFER GATES				
Expandable Dual 4-Input NAND Buffer Gates	SN 15932	SN 15832	J	N U
Expandable Dual 4-Input NAND Power Gates	SN 15944	SN 15844	J	N U
Quadruple 2-Input NAND Buffer Gates	SN 15957	SN 15857	J	N U
Quadruple 2-Input NAND Power Gates	SN 15958	SN 15858	J	N U
HEX INVERTERS				
6-kΩ Pull-Up Resistors	SN 15934	SN 15834	J	N U
Expandable (Open-Base) or Translator Inputs	SN 15935	SN 15835	J	N U
6-kΩ Pull-Up Resistors	SN 15936	SN 15836	J	N U
2-kΩ Pull-Up Resistors	SN 15937	SN 15837	J	N U
Open-Collector Outputs	SN 15938	SN 15838	J	N U
EXPANDERS				
Dual 4-Input Expanders	SN 15933	SN 15833	J	N U
FLIP-FLOPS				
Gated J-K/R-S (6-kΩ Pull-Up Resistors)	SN 15931	SN 15831	J	N U
Gated J-K/R-S (6-kΩ Pull-Up Resistors)	SN 15945	SN 15845	J	N U
Gated J-K/R-S (2-kΩ Pull-Up Resistors)	SN 15948	SN 15848	J	N U
Pulse-Triggered Binary (Active Pull-Up)	SN 15950	SN 15850	J	N U
Dual J-K, Individual Clocks and Presets (6-kΩ Pull-Up Resistors)	SN 159093	SN 158093	J	N U
Dual J-K, Individual Clocks and Presets (2-kΩ Pull-Up Resistors)	SN 159094	SN 158094	J	N U
Dual J-K, Common Clocks and Clears (2-kΩ Pull-Up Resistors)	SN 159097	SN 158097	J	N U
Dual J-K, Common Clocks and Clears (6-kΩ Pull-Up Resistors)	SN 159099	SN 158099	J	N U
MONOSTABLE MULTIVIBRATORS				
Gated, Negative-Edge-Triggered	SN 15951	SN 15851	J	N U

*For outline drawings of all packages, see Section 1.

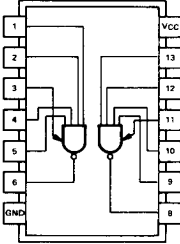
—SEE ORDERING INSTRUCTIONS PAGE 1-1—

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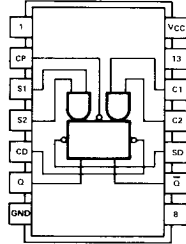
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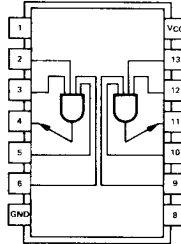
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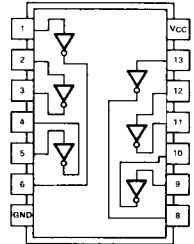
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(See Truth Tables 1 and 2)



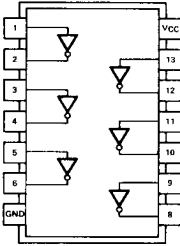
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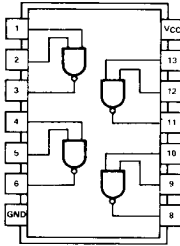
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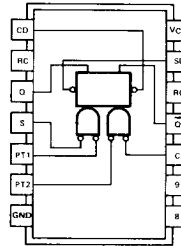
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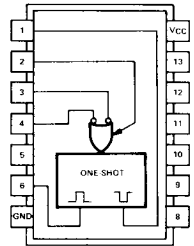


SN15850, SN15950
(See Truth Tables 3 and 4)



Each RC is a 1-kΩ resistor to VCC.

SN15851, SN15951
(See Notes A, B, and C)



TRUTH TABLE 1
R-S MODE

t_n				t_{n+1}	Q
S1	S2	C1	C2		
L	X	L	X		Q_n
L	X	X	L		Q_n
X	L	L	X		Q_n
X	L	X	L		Q_n
L	X	H	H		L
X	L	H	H		L
H	H	L	X		H
H	H	X	L		H
H	H	H	H		Indeterminate

TRUTH TABLE 2
J-K MODE

t_n		t_{n+1}	Q
S1	C1		
L	L		Q_n
L	H		L
H	L		H
H	H		\bar{Q}_n

TRUTH TABLE 3
SYNCHRONOUS

t_n				t_{n+1}	
PULSE INPUT				OUTPUT	
S	C	PT1	PT2	Q	\bar{Q}
H	X	X	H	Q_n	\bar{Q}_n
X	H	H	X	Q_n	\bar{Q}_n
L	H	L	X	H	L
L	X	L	H	H	L
H	L	X	L	L	H
X	L	H	L	L	H
L	L	L	L	Indeterminate	

TRUTH TABLE 4
ASYNCHRONOUS

DIRECT INPUT		OUTPUT	
SD	CD	Q	\bar{Q}
H	H	Q_n	\bar{Q}_n
L	H	L	H
H	L	H	L
L	L	H	H

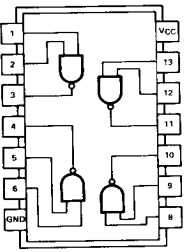
- NOTES: 1. t_n = bit time before clock pulse.
2. t_{n+1} = bit time after clock pulse.
3. H = high, L = low, X = irrelevant.
4. For operation in the J-K mode connect S2 to Q and C2 to \bar{Q} .

- NOTES: 5. Logical levels shown for pulse inputs PT1 and PT2 indicate that a transition to that level has just occurred.
6. Truth tables reflect individual conditions at the input. Either direct input may be used to inhibit its corresponding pulse input.

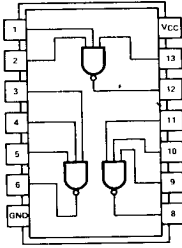
- NOTES: A. External timing resistor may be connected between pins 14 and 10 to control pulse width.
B. External timing capacitor may be connected between pins 10 and 11 to control pulse width.
C. Input sensitivity can be decreased by adding a capacitor from pin 5 to ground.

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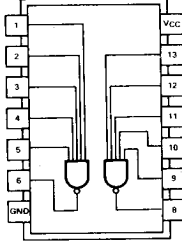
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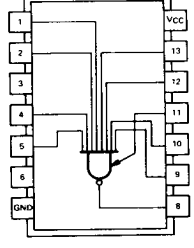
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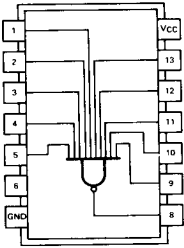
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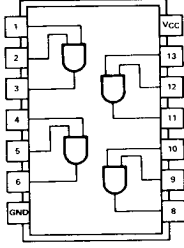
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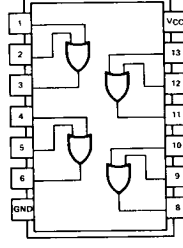
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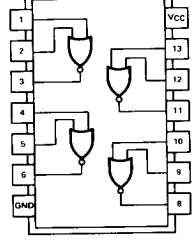
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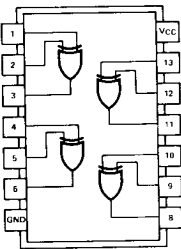
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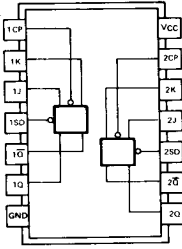
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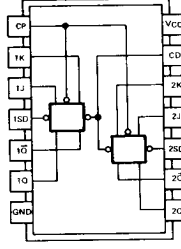
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**SN158093, SN158094,
SN159093, SN159094
(See Truth Table 5)**



**SN158097, SN158099,
SN159097, SN159099
(See Truth Table 5)**



TRUTH TABLE 5

	t_n	t_{n+1}	
	J	K	Q
L	L	L	Q _n
L	H	L	L
H	L	L	H
H	H	H	\bar{Q}_n

**SERIES 15830, SERIES 15930
DTL INTEGRATED CIRCUITS**

SERIES 15830 DTL FLIP-FLOPS

electrical and switching characteristics (unless otherwise noted, $V_{CC} = 5$)

PARAMETER	CONDITIONS	TA (°C)	SN15831		SN15845		SN15848		SN15850		SN158093		SN158097		SN158099		UNIT		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		MIN	MAX
VOL	IO = IOL MIN	0 and 25	0.45		0.45		0.45		0.45		0.45		0.45		0.45		0.45	V	
		75	0.5		0.5		0.5		0.5		0.5		0.5		0.5		0.5	V	
VOH	IO = IOH MIN	0 and 25	2.6		2.6		3.8		2.6		3.8		3.8		3.8		2.6	V	
		75	2.5		2.5		3.7		2.5		3.7		3.7		3.7		2.5	V	
VIL		0	1.2		1.2		1.2		1.2		1.2		1.2		1.2		1.2	V	
		25	1.1		1.1		1.1		1.1		1.1		1.1		1.1		1.1	V	
VIH		0	2		2		2		2		2		2		2		2	V	
		25	1.9		1.9		1.9		1.9		1.9		1.9		1.9		1.9	V	
IOL	VO = VOL MAX	0 and 25	10.5		16.8		15.4		12		16.8		15.4		15.4		16.8	mA	
		75	10.2		16		14.6		11.4		16		14.6		14.6		16	mA	
IOH	VO = VOH MIN	0, 25, and 75	-0.12		-0.12		-0.12		-1.5		-0.12		-0.12		-0.12		-0.12	mA	
		0	-0.59	-1.41	-1.77	-4.2	-13.7	-29										mA	
IOS	VO = 0 V	25			-0.59	-1.41	-1.77	-4.2	-13.7	-29								mA	
		75			-0.55	-1.38	-1.6	-4	-12.6	-28								mA	
IIL	VI = VOL MAX	DATA INPUTS	0 and 25	-1.05		-0.95		-0.95		-2.1		-0.95		-0.95		-0.95		mA	
			75	-1		-0.9		-0.9		-2		-0.9		-0.9		-0.9		mA	
		CLOCK INPUT	0 and 25	-2.8		-2.8		-2.24				-2.8		-2.8		-5.6		-5.6	mA
			75	-2.67		-2.67		-2.13				-2.67		-2.67		-5.34		-5.34	mA
		PRESET or CLEAR INPUT	0 and 25	-0.95		-2.1		-2.1		-1.6		-2.8		-2.8		-2.8	(1)	-2.8	mA
			75	-0.9		-2		-2		-1.52		-2.67		-2.67		-2.67		-2.67	mA
DATA INPUTS	0 and 25	5		5		5		5		5		5		5		5	μA		
	75	10		10		10		10		10		10		10		10	μA		
IiH	VI = 4 V	0 and 25	30		20		20		20		20		20		20		40	μA	
		75	40		30		30		30		30		30		30		60	μA	
ICC	VCC = 8 V	PRESET or CLEAR INPUT	0 and 25	5		5		5		5		5		5		5		μA	
			75	10		10		10		10		10		10		10		μA	
tPHL	FROM CLOCK TO OUTPUT	25	14		16		17.5		9.3		32		35		35		32	ns	
		75	18		18.5		22.5		19.6		37		45		45		37	ns	
tPLH	FROM CLOCK TO OUTPUT	25	36		75		15		65		5		32		15		65	ns	
		75	35		75		25		75		5		25		25		75	ns	

(1) Double the limit for the common clear input.

**SERIES 15830, SERIES 15930
DTL INTEGRATED CIRCUITS**

SERIES 15930 DTL FLIP-FLOPS

electrical and switching characteristics (unless otherwise noted, VCC = 5)

PARAMETER	CONDITIONS	TA (°C)	SN15931 MIN	SN15945 MAX	SN15948 MIN	SN15948 MAX	SN15950 MIN	SN15950 MAX	SN15903 MIN	SN15903 MAX	SN15904 MIN	SN15904 MAX	SN15907 MIN	SN15907 MAX	SN15909 MIN	SN15909 MAX	UNIT
VOL	IO = IOL MIN	-55 and 25	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	V
		125	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45	V
VOH	IO = IOH MIN	-55	2.5	2.6	3.8	3.8	3.8	3.8	2.5	2.6	3.8	3.8	3.8	2.6	2.5	2.5	V
		125	2.5	2.5	3.7	3.7	3.7	3.7	2.5	2.5	3.7	3.7	3.7	2.5	2.5	2.5	V
VIL		-55	1.1	1.1	1.4	1.4	1.4	1.4	1.4	1.1	1.1	1.1	1.1	1.4	1.1	1.1	V
		125	0.95	0.75	1.1	1.1	1.1	1.1	1.1	0.8	0.8	0.8	0.8	1.1	0.8	0.8	V
VIH		-55	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1	V
		125	1.9	1.9	1.9	1.9	1.9	1.9	1.9	1.9	1.9	1.9	1.9	1.9	1.9	1.9	V
IOL	VO = VOL MAX	-55	10	14.6	13	13	11.4	14.6	13	15.2	13	13.6	13.6	15.2	14.6	14.6	mA
		125	9.5	13.8	12.3	12.3	10.8	13.8	12.3	13.8	12.3	12.3	12.3	13.8	13.8	13.8	mA
IOH	VO = VOH MIN	-55	-0.12	-0.12	-0.12	-0.12	-1.5	-0.12	-0.12	-0.12	-0.12	-0.12	-0.12	-0.12	-0.12	-0.12	mA
		125	-0.12	-0.12	-0.12	-0.12	-1.5	-0.12	-0.12	-0.12	-0.12	-0.12	-0.12	-0.12	-0.12	-0.12	mA
IOS	VO = 0 V	-55 and 25	-0.7	-1.33	-2.1	-3.96	-15.7	-27	-0.7(1)	-2.4(1)	-2.1(1)	-5(1)	-2.1(1)	-5(1)	-0.7(1)	-2.4(1)	mA
		125	-0.62	-1.3	-1.86	-3.54	-14.6	-26	-0.7	-2.4	-2.1	-5	-2.1	-5	-0.7	-2.4	mA
IIL	VI = 0 V	-55 and 25	-1.07	-1.07	-1.07	-1.07	-2.4	-1.07	-1.07	-1.07	-1.07	-1.07	-1.07	-1.07	-1.07	-1.07	mA
		125	-1	-1	-1	-1	-2.25	-1	-1	-1	-1	-1	-1	-1	-1	-1	mA
IIL	CLOCK INPUT	-55 and 25	-3.4	-3.2	-2.56	-2.56			-3.2	-3.2	-3.2	-3.2	-6.4	-6.4	-6.4	-6.4	mA
		125	-3	-2.8	-2.2	-2.2			-3	-3	-3	-3	-6	-6	-6	-6	mA
IIL	PRESET or CLEAR INPUT	-55	-1.2	-2.4	-2.4	-2.4	-1.82	-2.4	-3.2	-3.2	-3.2	-3.2	(?)	-3.2	(?)	-3.2	mA
		125	-1.1	-2.1	-2.1	-2.1	-1.62	-2.1	-3.0	-3.0	-3.0	-3.0	-3.0	-3.0	-3.0	-3.0	mA
IIH	VI = 4 V	-55 and 25	2	2	2	2	2	2	2	2	2	2	2	2	2	2	μA
		125	5	5	5	5	5	5	5	5	5	5	5	5	5	5	μA
IIL	CLOCK INPUT	-55 and 25	20	10	10	10	10	10	10	10	10	10	10	20	20	20	μA
		125	30	20	20	20	20	20	20	20	20	20	20	40	40	40	μA
IIL	PRESET or CLEAR INPUT	-55 and 25	2	2	2	2	2	2	2	2	2	2	2	(?)	(?)	(?)	μA
		125	5	5	5	5	5	5	5	5	5	5	5	5	5	5	μA
ICC	VCC = 8 V	25	11	14	16.2	8.7	28	32	28	32	32	32	32	32	28	28	mA
		125	14.5	17	21.6	18.4	34	42	34	42	42	42	42	42	34	34	mA
IPLH	FROM CLOCK TO OUTPUT	25	35	75	15	75	15	65	5	32	15	75	15	65	15	75	ns
		125	35	75	25	75	25	75	25	75	25	75	25	75	25	75	ns

(1) 25°C only.
(2) Double the limit shown for common clear inputs.

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