Off-line Power Supply Controller

FEATURES

- Transformerless Off-line Applications

- Ideal Primary-side Bias Supply

- Efficient BiCMOS Design

- Wide Input Range

- Fixed or Adjustable Low Voltage Output

- Uses Low Cost SMD Inductors

- Short Circuit Protected

- Optional Isolation Capability

DESCRIPTION

The UCC1889 controller is optimized for use as an off-line, low power, low voltage, regulated bias supply. The unique circuit topology utilized in this device can be visualized as two cascaded flyback converters, each operating in the discontinuous mode, and both driven from a single external power switch. The significant benefit of this approach is the ability to achieve voltage conversion ratios of 400V to 12V with no transformer and low internal losses.
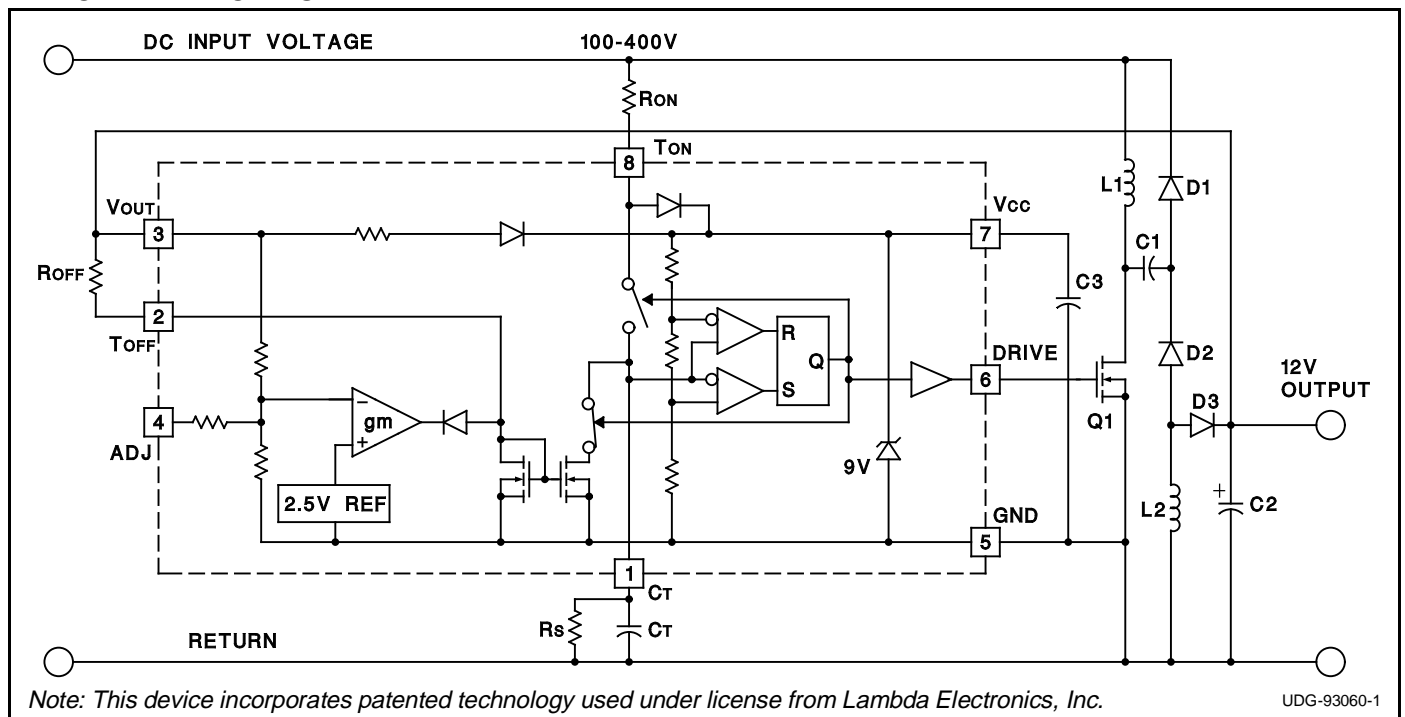
The control algorithm utilized by the UCC1889 is to force the switch on time to be inversely proportional to the input line voltage while the switch off time is made inversely proportional to the output voltage. This action is automatically controlled by an internal feedback loop and reference. The cascaded configuration allows a voltage conversion from 400V to 12V to be achieved with a switch duty cycle greater than 10%. This topology also offers inherent short circuit protection since as the output voltage falls to zero, the switch off time approaches infinity.

The output voltage can be easily set to 12V or 18V. Moreover, it can be programmed for other output voltages less than 18V with a few additional components. An isolated version can be achieved with this topology as described further in Unitrode Application Note U-149.

OPERATION

With reference to the application diagram below, when input voltage is first applied, the R_{ON} current into T_{ON} is directed to V_{CC} where it charges the external capacitor, C3, connected to V_{CC}. As voltage builds on V_{CC}, an internal undervoltage lockout holds the circuit off and the output at DRIVE low until V_{CC} reaches 8.4V. At this time, DRIVE goes high turning on the power switch, Q1, and redirecting the current into T_{ON} to the timing capacitor, C_T. C_T charges to a fixed threshold with a current $I_{CHG}=0.8 \cdot (V_{IN} - 4.5V)/R_{ON}$. Since DRIVE will only be high for as long as C_T charges, the power switch on time will be inversely proportional to line voltage. This provides a constant line voltage-switch on time product.

TYPICAL APPLICATION

Note: This device incorporates patented technology used under license from Lambda Electronics, Inc.

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OPERATION (cont.)

At the end of the on time, Q1 is turned off and the R$_{ON}$ current into T$_{ON}$ is again diverted to V$_{CC}$. Thus the current through R$_{ON}$, which charges C$_T$ during the on time, contributes to supplying control power during the off time.

The power switch off time is controlled by the discharge of C$_T$ which, in turn, is programmed by the regulated output voltage. The relationship between C$_T$ discharge current, I$_{DCHG}$, and output voltage is illustrated as follows:
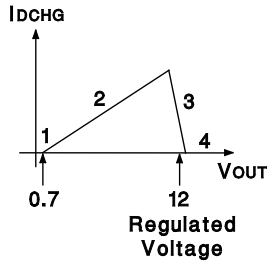
1. When V$_{OUT}$ = 0, the off time is infinite. This feature provides inherent short circuit protection. However, to ensure output voltage startup when the output is not a short, a high value resistor, R$_S$, is placed in parallel with C$_T$ to establish a minimum switching frequency.

2. As V$_{OUT}$ rises above approximately 0.7V to its regulated value, I$_{DCHG}$ is defined by R$_{OFF}$, and therefore is equal to:

$$I_{DCHG} = (V_{OUT} - 0.7V) / R_{OFF}$$

As V$_{OUT}$ increases, I$_{DCHG}$ increases resulting in the reduction of off time. The frequency of operation increases and V$_{OUT}$ rises quickly to its regulated value.

3. In this region, a transconductance amplifier reduces I$_{DCHG}$ in order to maintain V$_{OUT}$ in regulation.

4. If V$_{OUT}$ should rise above its regulation range, I$_{DCHG}$ falls to zero and the circuit returns to the minimum frequency established by R$_S$ and C$_T$.

The range of switching frequencies is established by R$_{ON}$, R$_{OFF}$, R$_S$, and C$_T$ as follows:

$$\text{Frequency} = 1/(T_{ON} + T_{OFF})$$

$$T_{ON} = R_{ON} \bullet C_T \bullet 4.6\text{ V}/(V_{IN} - 4.5\text{V})$$

$$T_{OFF} \text{ (max)} = 1.4 \bullet R_S \bullet C_T$$
$$\text{Regions 1 and 4}$$

$$T_{OFF} = R_{OFF} \bullet C_T \bullet 3.7\text{V} /(V_{OUT} - 0.7\text{V})$$
$$\text{Region 2, excluding the effects of } R_S$$
$$\text{which have a minimal impact on } T_{OFF}.$$

The above equations assume that V$_{CC}$ equals 9V. The voltage at T$_{ON}$ increases from approximately 2.5V to 6.5V while C$_T$ is charging. To take this into account, V$_{IN}$ is adjusted by 4.5V in the calculation of T$_{ON}$. The voltage at T$_{OFF}$ is approximately 0.7V.

DESIGN EXAMPLE

The UCC3889 regulates a 12 volt, 1 Watt nonisolated DC output from AC inputs between 80 and 265 volts. In this example, the IC is programmed to deliver a maximum on time gate drive pulse width of 2.4 microseconds which occurs at 80 VAC. The corresponding switching frequency is approximately 100kHz at low line, and overall efficiency is approximately 50%. Additional design information is available in Unitrode Application Note U-149.
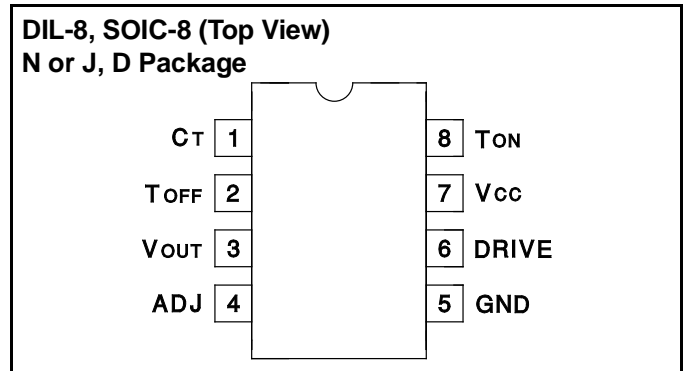

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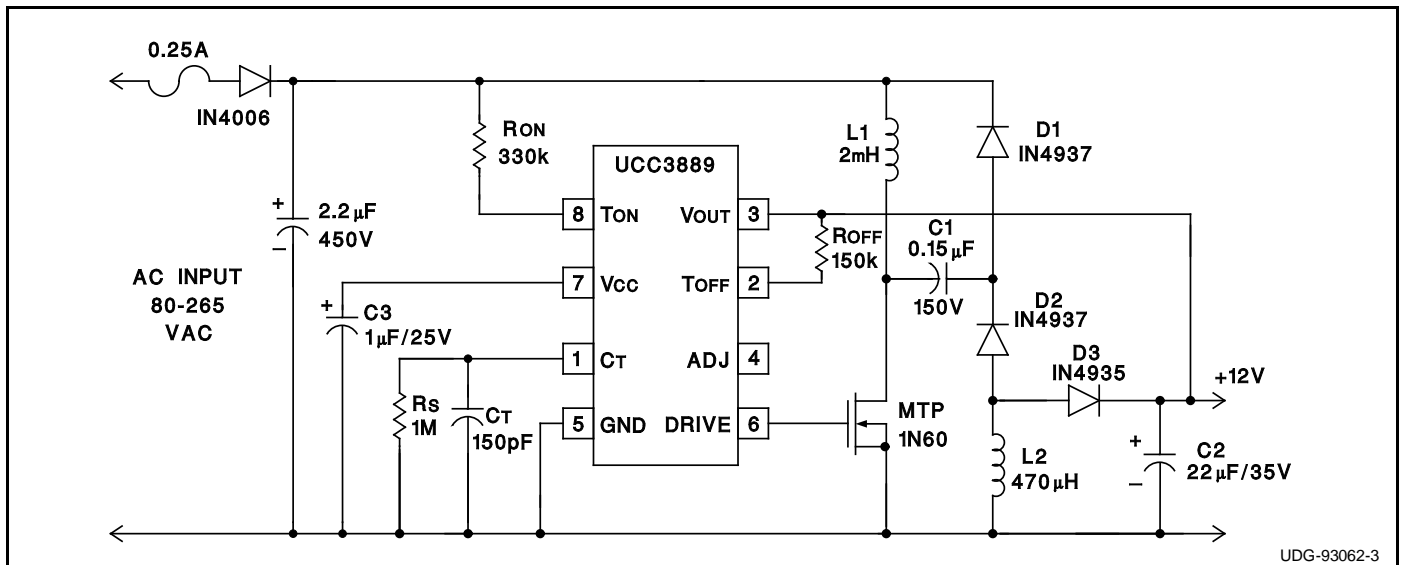
ABSOLUTE MAXIMUM RATINGS

Icc 5mA
Current into T_{ON} Pin 1.5mA
Voltage on V_{OUT} Pin 20V
Current into T_{OFF} Pin 250µA
Storage Temperature . . . . -65°C to +150°C

Note: Unless otherwise indicated, voltages are referenced to
ground and currents are positive into, negative out of, the speci-
fied terminals.

CONNECTION DIAGRAM

DIL-8, SOIC-8 (Top View)
N or J, D Package

```
        CT  | 1        8 |  TON
      TOFF  | 2        7 |  VCC
      VOUT  | 3        6 |  DRIVE
       ADJ  | 4        5 |  GND
```

ELECTRICAL CHARACTERISTICS
Unless otherwise stated, these specifications hold for $T_A = 0°C$ to 70°C for the UCC3889, -40°C to +85°C for the UCC2889, and -55°C to +125°C for the UCC1889. No load at DRIVE pin ($C_{LOAD}=0$).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
General					
V_{CC} Zener Voltage	$I_{CC} < 1.5mA$	8.6	9.0	9.3	V
Startup Current	$V_{OUT} = 0$		150	250	µA
Operating Current $I(V_{OUT})$	$V_{OUT} = 11V, F = 150kHz$		1.2	2.5	mA
Under-Voltage-Lockout					
Start Threshold	$V_{OUT} = 0$	8.0	8.4	8.8	V
Minimum Operating Voltage after Start	$V_{OUT} = 0$	6.0	6.3	6.6	V
Hysteresis	$V_{OUT} = 0$	1.8			V
Oscillator					
Amplitude	$V_{CC} = 9V$	3.5	3.7	3.9	V
C_T to DRIVE high Propagation Delay	Overdrive = 0.2V		100	200	ns
C_T to DRIVE low Propagation Delay	Overdrive = 0.2V		50	100	ns
Driver					
VOL	$I = 20mA, V_{CC} = 9V$		0.15	0.4	V
	$I = 100mA, V_{CC} = 9V$		0.7	1.8	V
VOH	$I = -20mA, V_{CC} = 9V$	8.5	8.8		V
	$I = -100mA, V_{CC} = 9V$	6.1	7.8		V
Rise Time	$C_{LOAD} = 1nF$		35	70	ns
Fall Time	$C_{LOAD} = 1nF$		30	60	ns
Line Voltage Detection					
Charge Coefficient: $I_{CHG} / I(T_{ON})$	$V_{CT} = 3V$, DRIVE = High, $I(T_{ON}) = 1mA$	0.73	0.79	0.85	
Minimum Line Voltage for Fault	$R_{ON} = 330k$	60	80	100	V
Minimum Current $I(T_{ON})$ for Fault	$R_{ON} = 330k$		220		µA
On Time During Fault	$C_T = 150pF, V_{LINE} = Min - 1V$		2		µs
Oscillator Restart Delay after Fault			0.5		ms
V_{OUT} Error Amp					
V_{OUT} Regulated 12V (ADJ Open)	$V_{CC} = 9V, I_{DCHG} = I(T_{OFF})/2$	11.2	11.9	12.8	V
V_{OUT} Regulated 18V (ADJ = 0V)	$V_{CC} = 9V, I_{DCHG} = I(T_{OFF})/2$	16.5	17.5	19.5	V
Discharge Ratio: $I_{DCHG} / I(T_{OFF})$	$I(T_{OFF}) = 50µA$	0.93	1.00	1.07	
Voltage at T_{OFF}	$I(T_{OFF}) = 50µA$	0.6	0.95	1.3	V
Regulation gm (Note 1)	Max $I_{DCHG} = 50µA$		1.0		mA/V
	Max $I_{DCHG} = 125µA$	0.8	1.7	2.9	mA/V

Note 1: gm is defined as $\dfrac{\Delta I_{DCHG}}{\Delta V_{OUT}}$ for the values of V_{OUT} when V_{OUT} is in regulation. The two points used to calculate gm are for I_{DCHG} at 65% and 35% of its maximum value.

PIN DESCRIPTIONS

ADJ: The ADJ pin is used to provide a 12V or an 18V regulated supply without additional external components. To select the 12V option, ADJ pin is left open. To select the 18V option, ADJ pin must be grounded. For other output voltages less than 18V, a resistor divider between V_{OUT}, ADJ and GND is needed. Note, however, that for output voltages less than V_{CC}, the device needs additional bootstrapping to V_{CC} from an external source such as the line voltage. If so, precautions must be taken to ensure that total I_{CC} does not exceed 5mA.

CT (timing capacitor): The signal voltage across C_T has a peak-to-peak swing of 3.7V for 9V V_{CC}. As the voltage on C_T crosses the oscillator upper threshold, DRIVE goes low. As the voltage on C_T crosses the oscillator lower threshold, DRIVE goes high.

DRIVE: This output is a CMOS stage capable of sinking 200mA peak and sourcing 150mA peak. The output voltage swing is 0 to V_{CC}.

GND (chip ground): All voltages are measured with respect to GND.

TOFF (regulated output control): T_{OFF} sets the discharge current of the timing capacitor through an external resistor connected between V_{OUT} and T_{OFF}.

TON (line voltage control): T_{ON} serves three functions. When C_T is discharging (off time), the current through T_{ON} is routed to V_{CC}. When C_T is charging (on time), the current through T_{ON} is split 80% to set the C_T charge time and 20% to sense minimum line voltage which occurs for a T_{ON} current of 220µA. For a minimum line voltage of 80V, R_{ON} is 330kΩ.

The C_T voltage slightly affects the value of the charge current during the on time. During this time, the voltage at the T_{ON} pin increases from approximately 2.5V to 6.5V.

Vcc (chip supply voltage): The supply voltage of the device at pin V_{CC} is internally clamped at 9V. Normally, V_{CC} is not directly powered from an external voltage source such as the line voltage. In the event that V_{CC} is directly connected to a voltage source for additional bootstrapping, precautions must be taken to ensure that total I_{CC} does not exceed 5mA.

VOUT (regulated output): The V_{OUT} pin is directly connected to the power supply output voltage. When V_{OUT} is greater than V_{CC}, V_{OUT} bootstraps V_{CC}.

BLOCK DIAGRAM
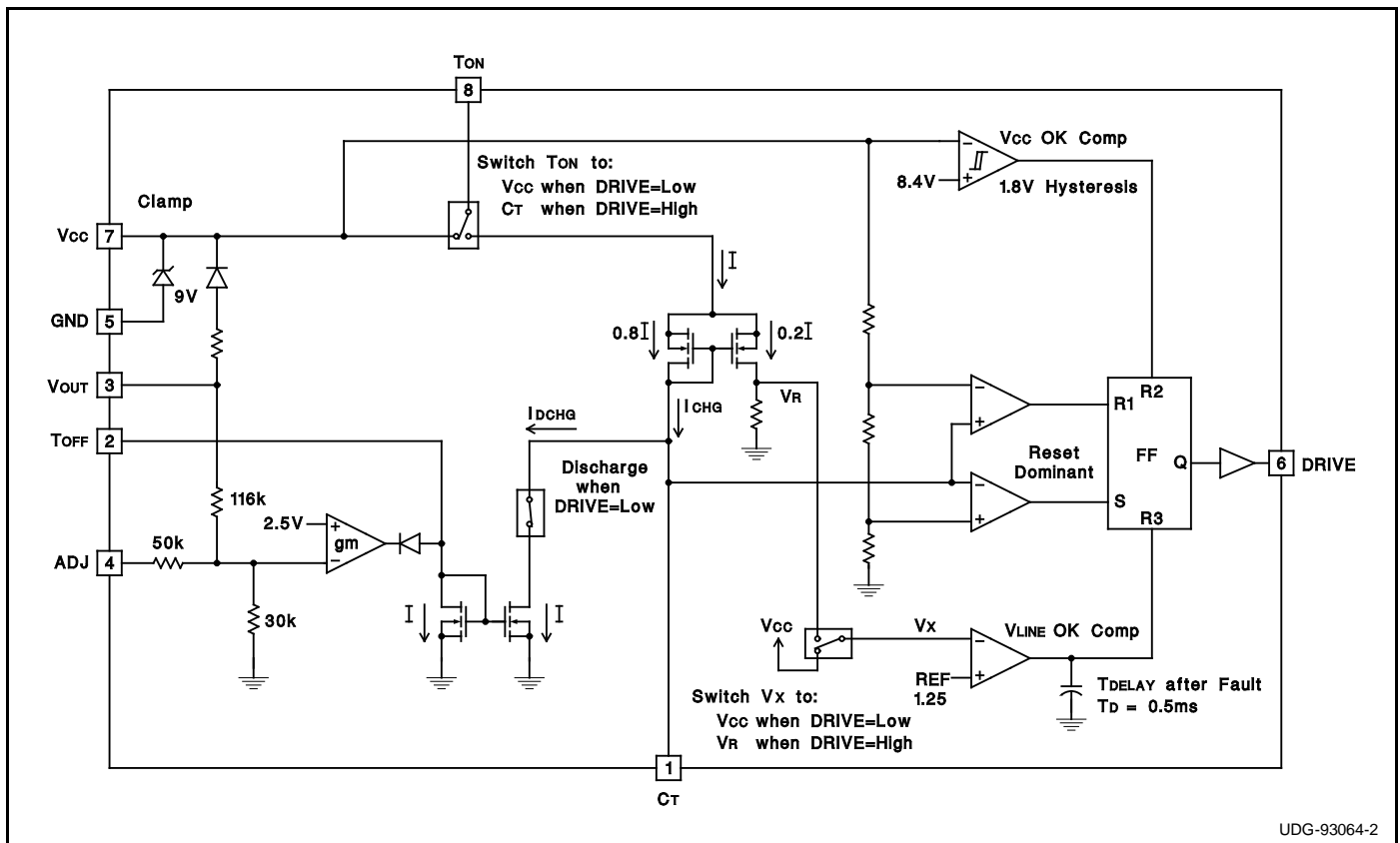
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TYPICAL WAVEFORMS

I$_{CHG}$ vs Line Voltage, R$_{ON}$=330k, V$_{CT}$=3V

I$_{CHG}$ vs V$_{CT}$, R$_{ON}$=330K

I$_{DCHG}$ vs V$_{OUT}$, ADJ Open, R$_{OFF}$=82K

I$_{DCHG}$ vs V$_{OUT}$, ADJ Open, R$_{OFF}$=82K
(Expanded V$_{OUT}$ Axis)

ERROR AMP gm vs MAXIMUM I$_{DCHG}$

ERROR AMP gm vs TEMPERATURE

6
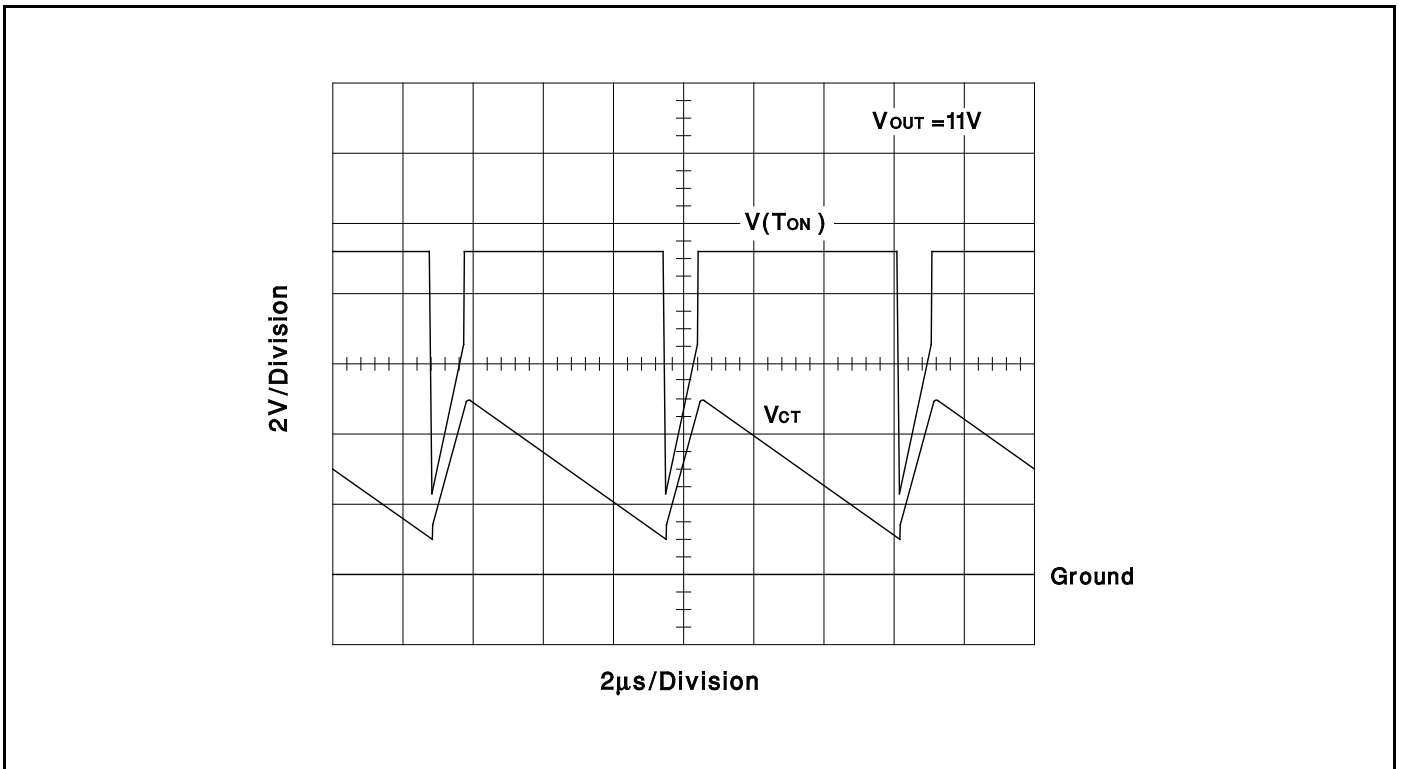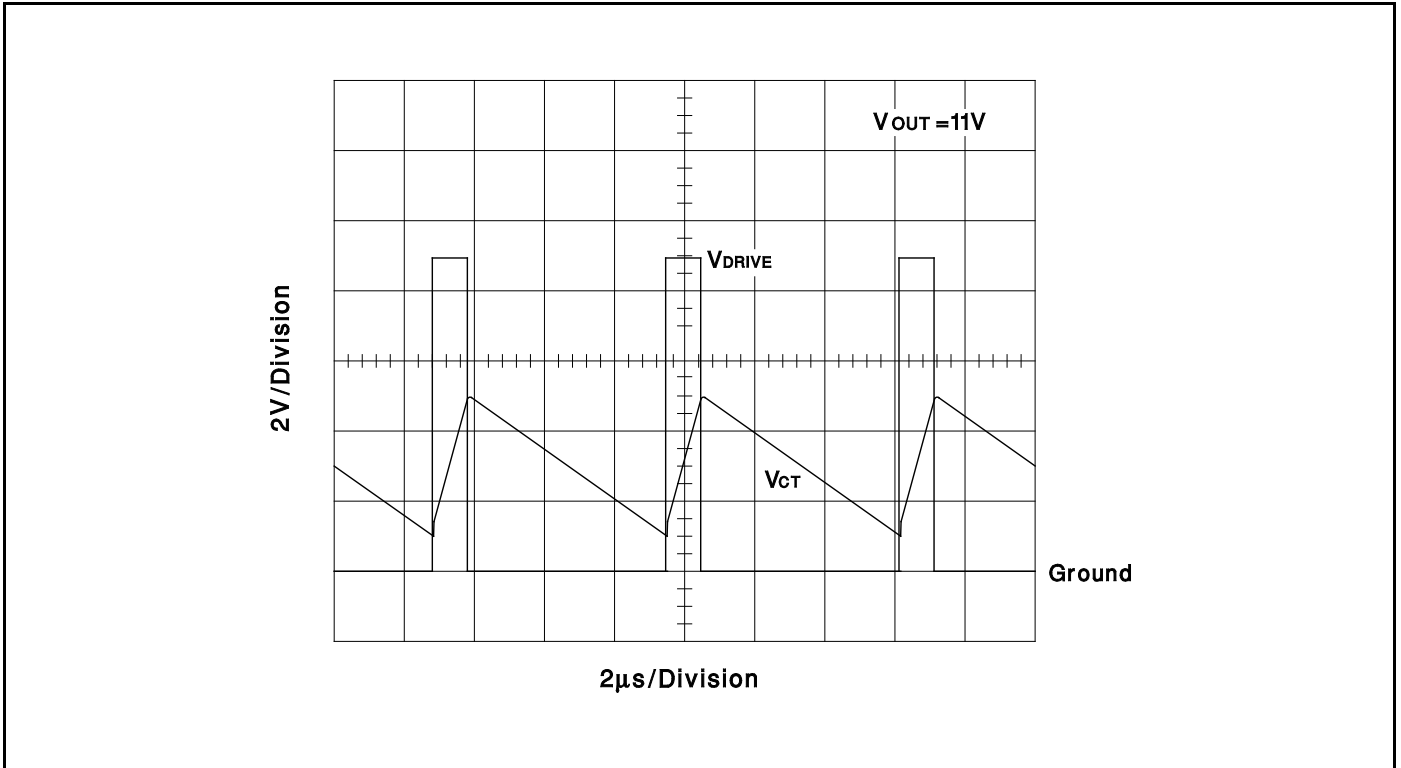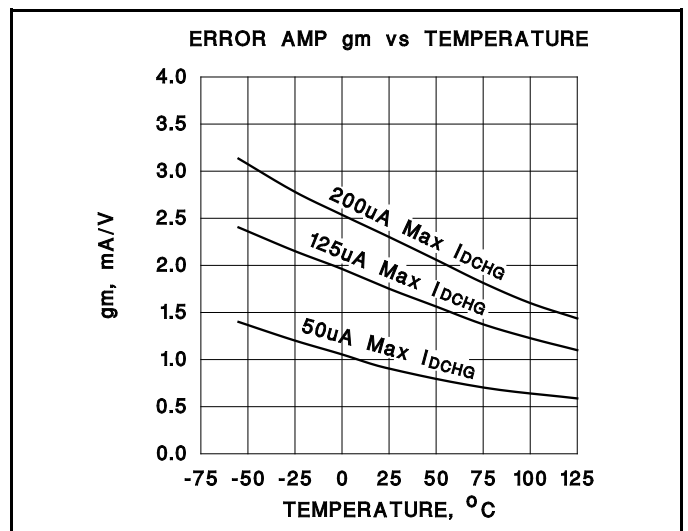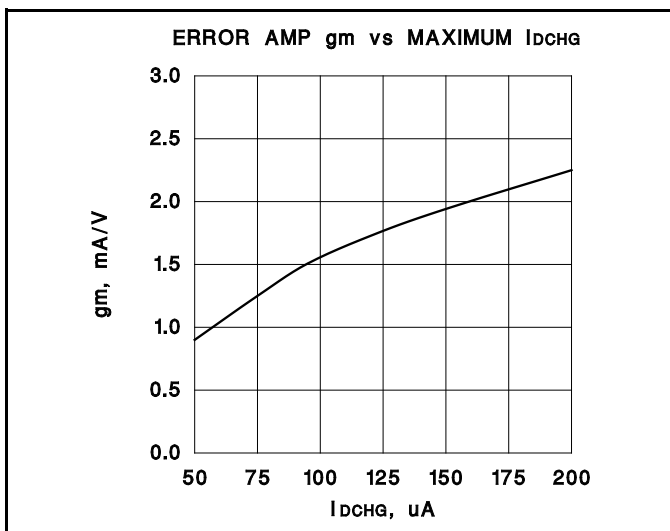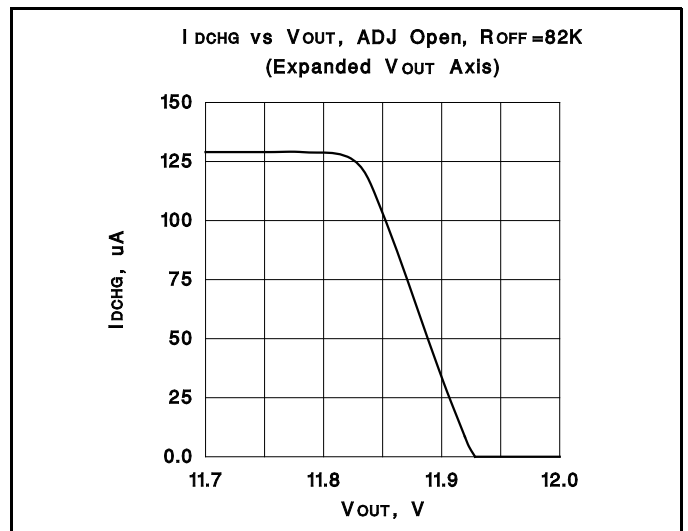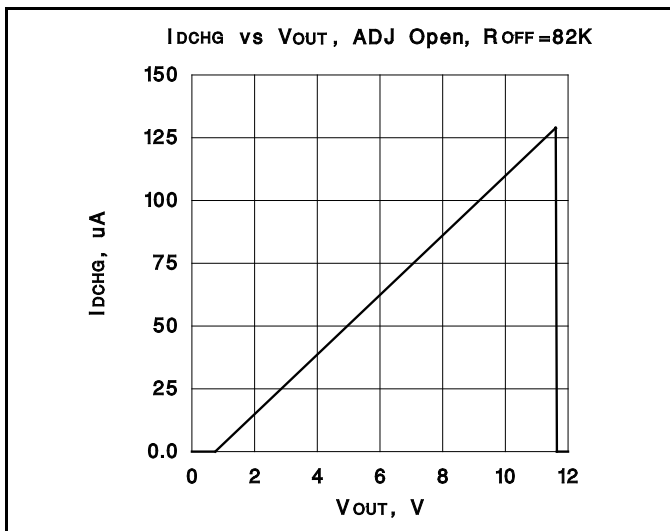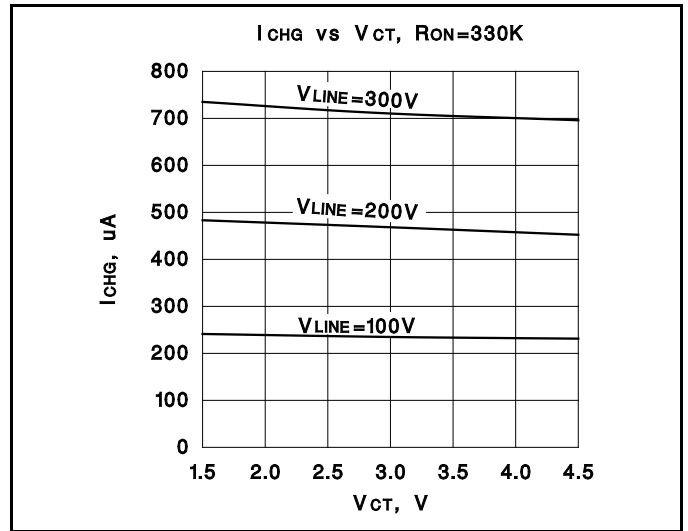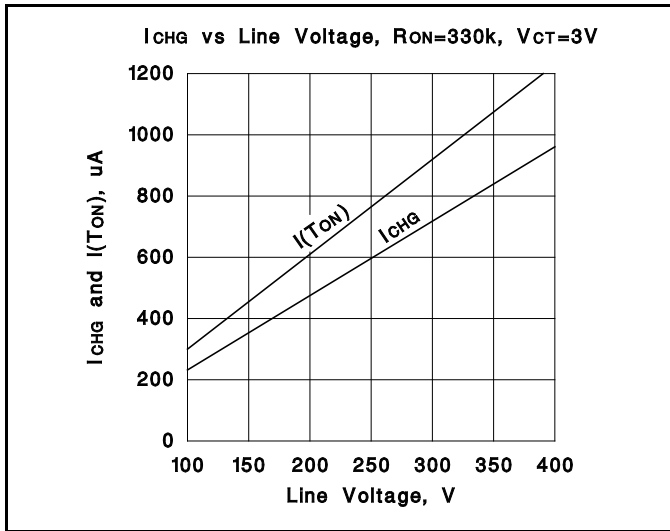
PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC2889D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UCC2889	Samples
UCC2889DTR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UCC2889	Samples
UCC2889DTRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UCC2889	Samples
UCC2889N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	UCC2889N	Samples
UCC3889D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC3889	Samples
UCC3889DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC3889	Samples
UCC3889DTR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC3889	Samples
UCC3889N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UCC3889N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TEXAS INSTRUMENTS

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

Reel Diameter

Reel Width (W1)

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

Sprocket Holes

User Direction of Feed

Pocket Quadrants

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC2889DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC3889DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC2889DTR	SOIC	D	8	2500	367.0	367.0	35.0
UCC3889DTR	SOIC	D	8	2500	367.0	367.0	35.0

D (R−PDSO−G8)   PLASTIC SMALL OUTLINE

0.197 (5,00)
0.189 (4,80)
⟂C⟂

8   5

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80) ⟂D⟂

Pin 1
Index Area

1   4

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ | 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

Gauge Plane

0.004 (0,10)

Seating Plane

0.010 (0,25)

0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−3/M   06/11

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
              not exceed 0.006 (0,15) each side.
         D.   Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
         E.   Reference JEDEC MS−012 variation AA.

TEXAS INSTRUMENTS
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D (R−PDSO−G8)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

Stencil Openings
(Note D)

6x1,27

8x0,55

6x1,27

8x1,50

5,40

5,40

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

0,60

1,55

Example
Solder Mask Opening
(See Note E)

0,07

All Around

4211283−2/E 08/12

NOTES: A. All linear dimensions are in millimeters.
         B. This drawing is subject to change without notice.
         C. Publication IPC−7351 is recommended for alternate designs.
         D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
             contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
         E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

P (R−PDIP−T8)   PLASTIC DUAL−IN−LINE PACKAGE

0.400 (10,16)
0.355 (9,02)

8   5

0.260 (6,60)
0.240 (6,10)

1   4

0.070 (1,78)
0.045 (1,14)

0.045 (1,14)
0.030 (0,76)

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92)
MAX

4040082/E 04/2010

NOTES: A. All linear dimensions are in inches (millimeters).
          B. This drawing is subject to change without notice.
          C. Falls within JEDEC MS−001 variation BA.

IMPORTANT NOTICE